A Quasi-Square-Wave Modular Multilevel Resonant DC/DC Converter With ZCS and Current-Shaping Capacity for High Step-Ratio Application

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***Abstract*—High step-ratio dc/dc converter is one of the key equipments for dc grids to satisfy the requirement of interconnecting low voltage dc and medium voltage dc buses. This article proposes a high step-ratio modular multilevel resonant dc/dc converter, where two full bridges are connected in parallel at LV side, and two submodules (SMs) strings are connected in series at MV side. Due to the series connection of two SM strings, the number of SMs and the size of the passive filter at MV terminal can be significantly reduced. Moreover, with the quasi-square-wave (QSW) modulation, the proposed converter can achieve flexible current-shaping capability. On this basis, through an internal phase-shifted angle of QSW modulation, the output voltage can be regulated with a fixed switching frequency, simplifying the design procedure of magnetic components. And zero current switching turn-OFF of full-bridge switches at LV side can be realized in forward and backward mode. In addition, based on the analysis of the operation principle with the time-domain method, the basic control strategy and parameter design procedure are introduced in detail. Finally, the feasibility of the proposed converter is validated by a 100 V/1 kV/4 kW prototype.**

***Index Terms*—Dc/dc converter, modular multilevel converter (MMC), quasi-square-wave (QSW) modulation, resonant converter, soft switching.**

NOMENCLATURE

MVDC	Medium voltage dc.
MV	Medium voltage.
SM	Submodule.
MMDC	Modular multilevel dc/dc converter.
TMMDC	Three-phase modular multilevel dc/dc converter.
LVDC	Low voltage dc.
MDCT	Modular multilevel high-frequency link dc transformer.
QSW	Quasi-square-wave.
MFT	Medium frequency transformer.
DAB	Dual-active-bridge.
SMMDCT	Sharing-branch modular multilevel dc transformer.
ZVS	Zero voltage switching.
ZCS	Zero current switching.
RMMC	Resonant modular multilevel dc/dc converter.
MMR	Modular multilevel resonant.
MMC	Modular multilevel converter.
DCM	Discontinuous conduction mode.
RMS	Root mean square.
ESR	Equivalent series resistance.

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I. INTRODUCTION

WITH the increasing penetration of renewable energy resources and dc loads, dc grid technology has attracted great concern and is also considered as a promising solution for efficient, reliable and flexible collection and transmission of the large-scale offshore wind farm and the solar power station [1], [2], [3]. In such dc grid applications, a dc/dc converter is essential for interconnecting dc buses with different voltage levels, which needs to meet several requirements, including bidirectional power conversion capability, high power rating, high step-ratio, high power density, and high efficiency [4], [5], [6].

Numerous topologies of high-power dc/dc converters have been proposed in recent years, including both nonisolated and isolated types. The isolated dc/dc converter is preferred in high step-ratio applications with internal transformers, achieving better device utilization than the nonisolated type [6], [7], [8]. Conventional isolated dc/dc converter is challenging to use in medium voltage dc (MVDC) applications due to the voltage stress limitation of the available power switches. One way to overcome this issue is to form a front-to-front dc/dc converter with the modular multilevel structure on the medium voltage (MV) side [9], [10], [11]. The series-connected submodules (SMs) of the modular multilevel dc/dc converter (MMDC) can reduce device voltage stress, improve reliability and add additional control flexibility. Several existing MMDC topologies are summarized in Table I. In [12], a three-phase modular multilevel dc/dc converter (TMMDC) has been proposed to achieve the low

TABLE I
SUMMARY OF THE MMDC TOPOLOGIES

Topology	Type	Number of SMs	Number of transformers	MV terminal concentrated capacitor	Blocking capacitor	Bidirectional power transmission	Soft switching	Control Strategy
TMMDC [12]	DAB	$6N$	1	No	No	Yes	Good	Phase-shifted control
MDCT [13]	DAB	$4N$	≥1	No	No	Yes	General	Phase-shifted control
SMMDCT [18]	DAB	$2N$	1	No	Yes	Yes	Good	Phase-shifted control
RMMC [26]	Resonant	N	1	Yes	No	Yes	Good	Variable-frequency control
MMR [27]	Resonant	$2N$	1	Yes	No	No	General	Variable-frequency control

voltage dc (LVDC) to MVDC conversion. In [13], a full-bridge-type modular multilevel high-frequency link dc transformer (MDCT) with multiple parallel-connected LV-side full-bridge modules is proposed to decrease the power capacity of each transformer. Besides, series-connected SMs can be modulated with the quasi-square-wave (QSW) method to mitigate *dv*/*dt* stress on medium frequency transformers (MFTs) [14], [15]. With the QSW modulation, the MMDC can work as a conventional dual-active-bridge (DAB) converter with phase-shifted control, which can achieve soft switching of power devices [16], [17]. In [18], A DAB-type sharing-branch modular multilevel dc transformer (SMMDCT) is proposed with the parallel SM string to reduce the number of SMs while eliminating the concentrated capacitor at the MV terminal. However, for the DAB-type converter, the power devices are turned OFF with a high current, leading to increased switching loss [19], [20]. This problem will become more severe for LV-side devices that withstand the high current. Moreover, the trapezoidal ac link current with large harmonic contents increases the transformer loss [5], [21].

Compared with the DAB structure, the resonant structure is more desirable for achieving high efficiency because of the quasi-sinusoidal current and the ability to achieve zero voltage switching (ZVS) and/or zero current switching (ZCS) [22], [23], [24], [25]. A resonant modular multilevel dc/dc converter (RMMC) is proposed in [26], where SMs and transformer are connected in series at MV terminal. The RMMC inherits the benefits of soft switching operation from the resonant converter. But the high current stress on MV side limits its applications. In [27], a modular multilevel resonant (MMR) dc/dc converter is proposed by employing a half-bridge-type modular multilevel converter (MMC) on MV side and a diode rectifier circuit on LV side. Half of the primary side switches and the secondary rectifier diodes can realize soft switching over the whole operating range. The output voltage is regulated by variable-frequency control, and bidirectional power conversion can be achieved by replacing the diodes with active power devices. In [28], the control optimization based on modulation index and variable-frequency control is proposed for MMR to adjust the output voltage, achieving a narrower frequency variation range. However, a variable-frequency control poses a substantial challenge to the design of magnetic components.

This article proposes a modular multilevel resonant dc/dc converter with ZCS and current-shaping capacity for high-power and high step-ratio applications. The fixed frequency operation and low switching loss can be achieved by combining MMC and resonant dc/dc converter. The proposed converter adopts two full bridges connected in parallel at LV side to increase the current capacity and two half-bridge SM strings connected in series to withstand the MV terminal voltage. With the two SM strings series configuration, the number of SMs can be reduced, the MV-side concentrated capacitor can be eliminated, and the size of filter inductor can be minimized. The output voltage can be regulated with an internal phase-shifted angle of QSW modulation with a fixed switching frequency. With the QSW modulation, the resonant current is shaped as a quasi-sinusoidal wave to achieve ZCS-OFF for LV-side full-bridge switches and ZVS-ON ZCS-OFF for partial switches on MV-side SM strings under forward and backward mode.

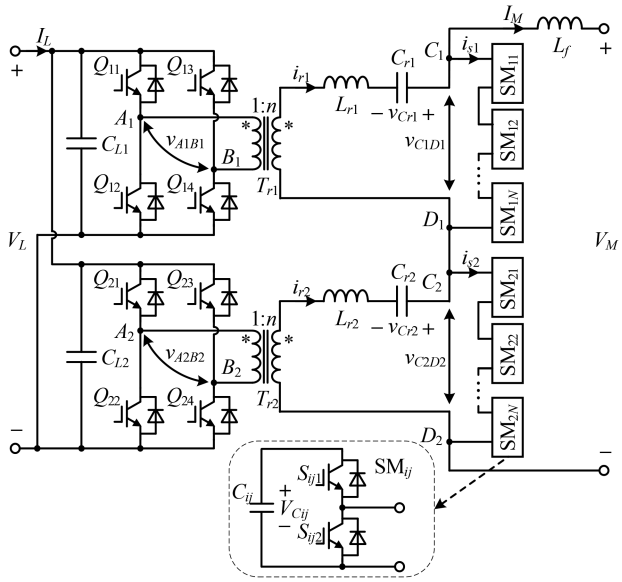

Fig. 1. Topology of the proposed modular multilevel resonant dc/dc converter.

The rest of this article is organized as follows. In Section II, the circuit configuration and operating principle of the proposed converter are introduced. Section III analyzes the steady-state characteristics of the proposed converter and presents the control strategy. In Section IV, the parameters design procedure is demonstrated clearly. In Section V, a comparison with different dc/dc converters is provided. Section VI gives the experimental verification. Finally, Section VII concludes this article.

II. OPERATING PRINCIPLE

A. Circuit Configuration

The topology of the proposed modular multilevel resonant dc/dc converter is shown in Fig. 1. The converter consists of two phases and a filter inductor L_f at MV terminal. Each phase consists of an LV-side full bridge $Q_{i1}-Q_{i4}$ ($i = 1, 2$), a medium

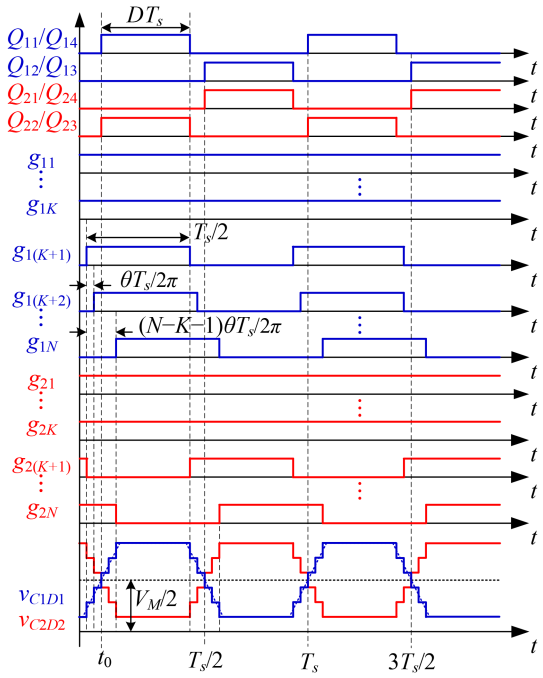

Fig. 2. Modulation scheme.

frequency transformer T_{ri}, a resonant inductor L_{ri}, a resonant capacitor C_{ri} and a half-bridge SM string. LV-side full bridges of two phases are connected in parallel to increase the current capacity. Two half-bridge SM strings are connected with the filter inductor L_f in series sequentially to interface with MV terminal. The turns ratio of T_{r1} and T_{r2} are 1:n.

B. Operating Principle

The proposed converter operates in resonant current discontinuous conduction mode (DCM) to achieve low switching loss. And the output voltage regulation can be achieved by the internal phase-shifted angle of QSW modulation under a fixed switching frequency. The modulation scheme is shown in Fig. 2. The LV-side full bridges employ the basic PWM control strategy with duty cycle D. The driving signals of two full bridges are phase-shifted by π. For each SM, the driving signals of upper and lower switches are complementary with enough dead time. The driving signal of the upper switch is denoted as g_{ij} ($j = 1, 2, \ldots, N$). The QSW modulation is employed for each half-bridge SM string [14], [18]. K SMs are constantly inserted, while $N-K$ SMs work with 50% duty cycles. Moreover, there is an internal phase-shifted angle θ between any two adjacent driving signals, which is employed to regulate the ac link voltage. Therefore, the proposed converter can regulate the terminal voltage in both forward and backward modes by changing the internal phase-shifted angle.

As shown in Fig. 2, assuming that the SM capacitor voltage V_{Cij} is well balanced, the output voltage of each string v_{C1D1} and v_{C2D2} are staircase waveforms with $N-K+1$ steps. The maximum value of v_{C1D1} and v_{C2D2} is NV_C, and the minimum value is KV_C, where V_C is the SM capacitor voltage. With the phase-shifted angle π between two strings, there are $N+K$ SMs inserted to withstand the MV terminal voltage. And the MV terminal voltage V_M can be expressed as (1) summed by v_{C1D1} and v_{C2D2}.

$$V_M = v_{C1D1} + v_{C2D2} = (N+K)\,V_C. \tag{1}$$

According to (1), the SM capacitor voltage can be expressed as follows:

$$V_C = \frac{V_M}{N+K}. \tag{2}$$

Based on Fig. 2 and (2), the dc bias component of v_{C1D1} and v_{C2D2}, which are denoted as V_{d1} and V_{d2}, respectively, can be calculated as follows:

$$V_{d1} = V_{d2} = \frac{1}{2}\left(KV_C + NV_C\right) = \frac{V_M}{2}. \tag{3}$$

Then, the amplitude of ac components in v_{C1D1} and v_{C2D2} can be expressed as follows:

$$V_{C1D1} = V_{C2D2} = \frac{N-K}{2\,(N+K)}V_M. \tag{4}$$

As shown in Fig. 1, the dc bias component of v_{C1D1} and v_{C2D2} are eliminated by C_{r1} and C_{r2}, respectively, and the average voltage of V_{Cr1} and V_{Cr2} are $V_M/2$. With the configuration of two series-connected SM strings and the aforementioned modulation scheme, the total MV terminal voltage is guaranteed to be a stable dc voltage, which is given by the sum of the two string voltages v_{C1D1} and v_{C2D2}. Hence, additional MV terminal passive filters are eliminated to reduce the size and cost of the converter.

According to Fig. 1, the string current i_{s1} and i_{s2} can be expressed as (5), where i_{r1} and i_{r2} are the resonant currents of each phase and I_M is the MV terminal current.

$$\begin{cases} i_{s1} = i_{r1} - I_M \\ i_{s2} = i_{r2} - I_M \end{cases}. \tag{5}$$

Due to a large number of SMs, the staircase voltage during rising and falling processes of v_{C1D1} and v_{C2D2} are simplified into oblique lines to simplify the analysis and calculation, and the following assumptions are made.

1) All the components are ideal.
2) The terminal voltages V_L and V_M remain stable.
3) Resonant parameters of the two phases are the same, namely $L_{r1} = L_{r2} = L_r$ and $C_{r1} = C_{r2} = C_r$.
4) Two phases operate symmetrically, and string output voltage v_{C1D1} and v_{C2D2} have the same duty cycle during rising and falling processes, namely $d_{N1} = d_{N2} = d_N$.

Resonant frequency f_r and characteristic impedance Z_r of the resonant tank are defined as follows:

$$f_r = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}} = \frac{1}{2\pi\sqrt{L_{r2}C_{r2}}} = \frac{1}{2\pi\sqrt{L_rC_r}} \tag{6}$$

$$Z_r = \sqrt{\frac{L_{r1}}{C_{r1}}} = \sqrt{\frac{L_{r2}}{C_{r2}}} = \sqrt{\frac{L_r}{C_r}}. \tag{7}$$

The operation waveforms of the proposed converter in forward and backward modes are shown in Fig. 3. Since the

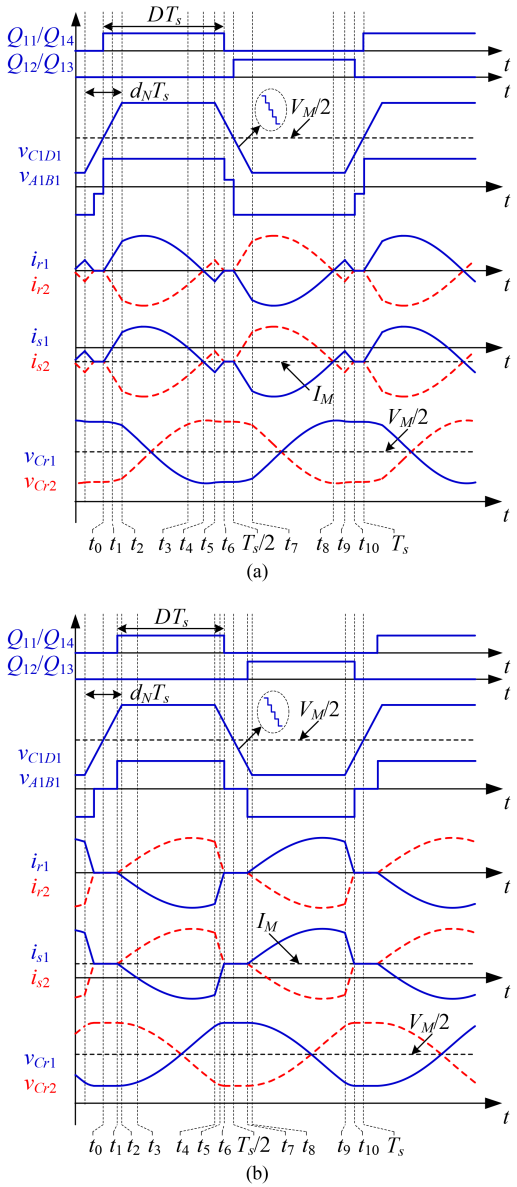

Fig. 3. Key waveforms of the proposed converter. (a) Forward mode. (b) Backward mode.

operation principle of the two phases is identical, only one phase ($i = 1$) is described as an example in detail.

1). Forward Mode: Referring to Fig. 3(a), the proposed converter has eight operating modes during one switching period when the power is transferred from the LV terminal to the MV terminal (forward mode). And the respective equivalent circuits of each mode are presented in Fig. 4. The MV-side half-bridge string SMs has two operating states, including inserted and bypassed state. As shown in Fig. 4, the black SMs means being inserted, while the grey SMs means being bypassed.

Mode 1 [t_0, t_2] [see Fig. 4(a)]: At t_0, Q_{11} and Q_{14} are turned ON. $(N+K)/2$ SMs are inserted into the circuit. And the string voltage v_{C1D1} is $V_M/2$. The resonant current i_{r1} is zero, and the string current i_{s1} is I_M. The resonance between L_{r1} and C_{r1} begins. During [t_0, t_2], the SMs are inserted one by one, and v_{C1D1} gradually increases to $N/(N+K)V_M$. At t_1, i_{s1} rises over zero. Hence, the lower switches S_{1j2} of SMs inserted during [t_0, t_1] can be turned OFF with ZCS, while the upper switches S_{1j1} of SMs inserted during [t_1, t_2] can be turned ON with ZVS. In this mode, the state equation of the circuit can be written as follows:

$$\begin{cases} L_{r1}\frac{di_{r1}(t)}{dt} = v_{Cr1}(t) - \frac{(N-K)V_M}{(N+K)d_N T_s}(t-t_0) + nV_L - \frac{V_M}{2} \\ C_{r1}\frac{dv_{Cr1}(t)}{dt} = -i_{r1}(t) \end{cases}. \tag{8}$$

Mode 2 [t_2, t_5] [see Fig. 4(b)]: At t_2, all the SMs are inserted into the circuit. The string voltage v_{C1D1} keeps $N/(N+K)V_M$ during [t_2, t_5]. After i_{s1} falls below zero at t_3, the current of S_{1j1} shifts from the anti-paralleled diodes to the switches. As i_{r1} falls below zero at t_4, the transmission power of resonant tank reverses, and the current flow through the parallel diodes of Q_{11} and Q_{14}. In this mode, the state equation of the circuit can be expressed as follows:

$$\begin{cases} L_{r1}\frac{di_{r1}(t)}{dt} = v_{Cr1}(t) - \frac{NV_M}{N+K} + nV_L \\ C_{r1}\frac{dv_{Cr1}(t)}{dt} = -i_{r1}(t) \end{cases}. \tag{9}$$

Mode 3 [t_5, t_6] [see Fig. 4(c)]: At t_5, SMs begin to be bypassed. And the string voltage v_{C1D1} gradually decreases to $V_M/2$ during this mode. i_{r1} and i_{s1} increase rapidly until $i_{r1} = 0$ and $i_{s1} = I_M$. Since $i_{s1}<0$ during [t_5, t_6], the lower switches S_{1j2} of bypassed SMs can be turned ON with ZVS. During [t_5, t_6], the state equation of the circuit can be expressed as follows:

$$\begin{cases} L_{r1}\frac{di_{r1}(t)}{dt} = v_{Cr1}(t) + nV_L - \frac{NV_M}{N+K} + \frac{(N-K)V_M}{(N+K)d_N T_s}(t-t_5) \\ C_{r1}\frac{dv_{Cr1}(t)}{dt} = -i_{r1}(t) \end{cases}. \tag{10}$$

Mode 4 [t_6, $T_s/2$] [see Fig. 4(d)]: At t_6, Q_{11} and Q_{14} are turned OFF with ZCS. During [t_6, $T_s/2$], i_{r1} and i_{s1} are clamped at 0 and I_M, respectively, until this mode ends at $T_s/2$. And the lower switches S_{1j2} of bypassed SMs can achieve ZVS-ON because of the negative i_{s1} in this mode.

Mode 5 [$T_s/2$, t_7] [see Fig. 4(e)]: When $t = T_s/2$, Q_{12} and Q_{13} are turned ON. The string voltage v_{C1D1} is $V_M/2$. The resonant current i_{r1} and string current i_{s1} are zero and I_M, respectively. The resonance between L_{r1} and C_{r1} begins. During [$T_s/2$, t_7], SMs are bypassed gradually, and v_{C1D1} changes from $V_M/2$ to $KV_M/(N+K)$. The lower switches S_{1j2} of bypassed SMs can be turned ON with ZVS with negative i_{s1}.

Mode 6 [t_7, t_9] [see Fig. 4(f)]: At t_7, $(N-K)$ SMs are bypassed, while K SMs are inserted into the circuit. The string voltage v_{C1D1} keeps $KV_M/(N+K)$ during [t_7, t_9]. When i_{r1} rises above zero at t_8, the transmission power of the resonant tank reverses, and the current shifts to the parallel diodes of Q_{12} and Q_{13}.

Mode 7 [t_9, t_{10}] [see Fig. 4(g)]: During [t_9, t_{10}], v_{C1D1} decreases gradually as SMs are inserted. In addition, i_{r1} and i_{s1} decrease until $i_{r1} = 0$ and $i_{s1} = I_M$. As $i_{s1}<0$ during [t_9, t_{10}], the lower switches S_{1j2} of inserted SMs can achieve ZCS-OFF.

Mode 8 [t_{10}, T_s] [see Fig. 4(h)]: At t_{10}, Q_{12} and Q_{13} are turned OFF with ZCS. During [t_{10}, T_s], the SMs are inserted one by one, and v_{C1D1} gradually decreases to $K/(N+K)V_M$. i_{r1} and i_{s1} remain unchanged until this mode ends at T_s. Because of

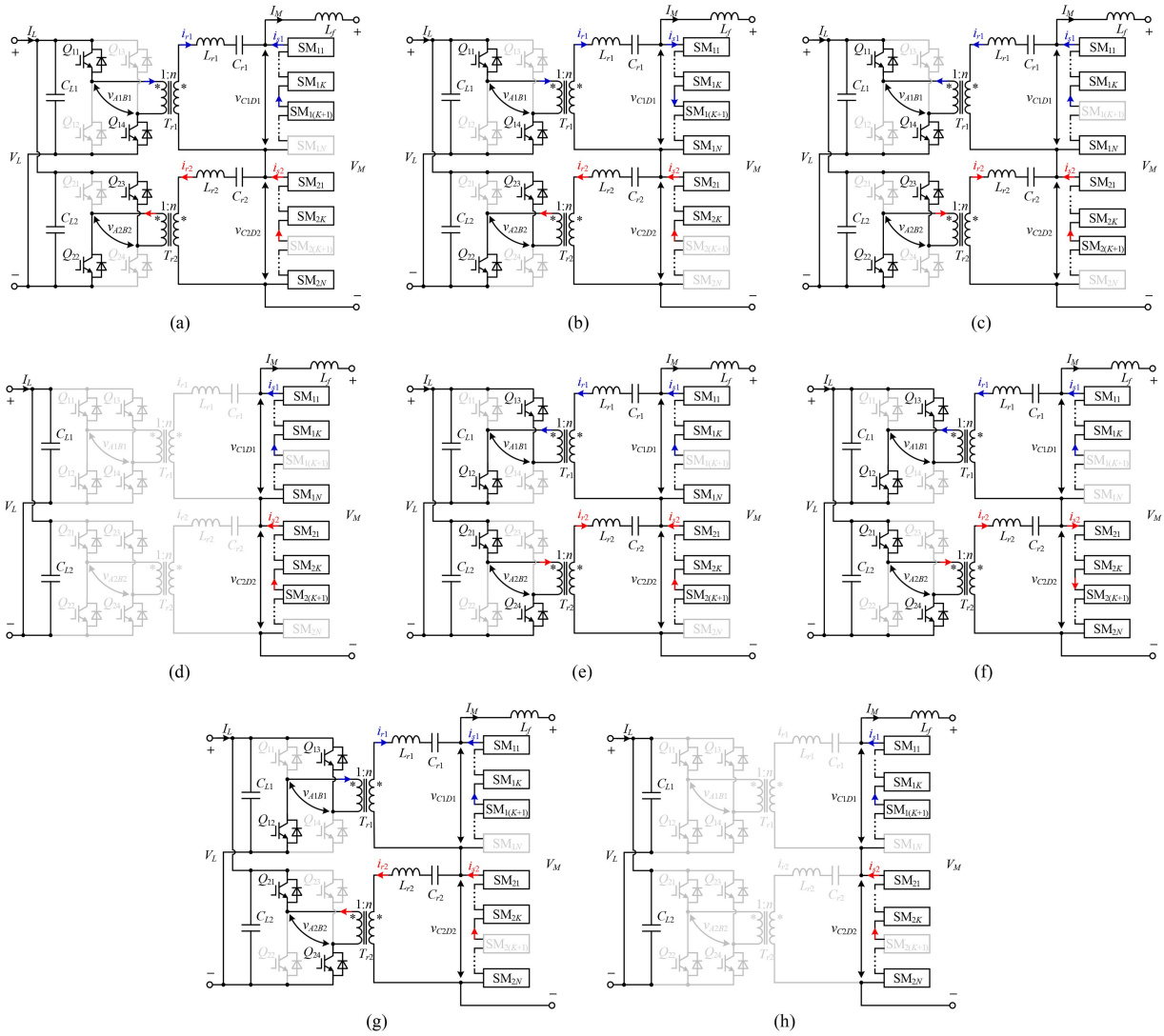

Fig. 4. Operation modes of the proposed converter in forward mode. (a) [t_0, t_2]. (b) [t_2, t_5]. (c) [t_5, t_6]. (d) [t_6, T_s/2]. (e) [T_s/2, t_7]. (f) [t_7, t_9]. (g) [t_9, t_{10}]. (h) [t_{10}, T_s].

i_{s1}<0 in this mode, the lower switches S_{1j2} of inserted SMs can be turned OFF with ZCS.

According to (8)−(10), the expression of i_{r1} and v_{Cr1} in half switching period can be obtained as (A1) and (A2) in Appendix, respectively, where ω_r is the resonant angular frequency, $\omega_r = 2\pi f_r$. Besides, the waveforms of i_{r1} and v_{Cr1} in [t_0, T_s/2] are symmetrical with those in [T_s/2, T_s]. The operation modes of the next period are the same as those described previously.

2). Backward Mode: According to Fig. 3(b), the proposed converter can be divided into ten operating modes over one switching period in backward mode. The equivalent circuits are presented in Fig. 5.

Mode 1 [t_0, t_1] [see Fig. 5(a)]: At t_0, the string voltage v_{C1D1} is V_M/2. And the SMs are gradually inserted. The resonant current i_{r1} keeps zero, and the string current i_{s1} keeps I_M until (v_{C1D1}−V_M/2)>nV_L at t_1. The upper switches S_{1j1} of inserted SMs in this mode can achieve ZVS-ON with positive i_{s1}.

Mode 2 [t_1, t_2] [see Fig. 5(b)]: At t_1, Q_{11} and Q_{14} are turned ON, and the resonance between L_{r1} and C_{r1} begins. As the number of inserted SMs increases, v_{C1D1} gradually rises to N/(N+K)V_M during [t_1, t_2]. Since i_{s1}>0 in this mode, the upper switches S_{1j1} of inserted SMs can be turned ON with ZVS. The state equation of the circuit during [t_1, t_2] can be written as follows:

$$\begin{cases} L_{r1}\frac{di_{r1}(t)}{dt} = v_{Cr1}(t) - \frac{(N-K)V_M}{(N+K)d_N T_s}(t-t_1) - \frac{V_M}{2} \\ C_{r1}\frac{dv_{Cr1}(t)}{dt} = -i_{r1}(t) \end{cases}. \tag{11}$$

Mode 3 [t_2, t_4] [see Fig. 5(c)]: At t_2 all the SMs are inserted into the circuit. The string voltage v_{C1D1} is N/(N+K)V_M during [t_2, t_4]. When i_{s1} falls below zero at t_3, the current shifts from the parallel diodes to the switches. The state equation of the circuit can be expressed as (12) in this mode.

$$\begin{cases} L_{r1}\frac{di_{r1}(t)}{dt} = v_{Cr1}(t) - \frac{NV_M}{N+K} + nV_L \\ C_{r1}\frac{dv_{Cr1}(t)}{dt} = -i_{r1}(t) \end{cases}. \tag{12}$$

Mode 4 [t_4, t_6] [see Fig. 5(d)]: At t_4, SMs begin to be bypassed gradually. And the string voltage v_{C1D1} decreases from N/(N+K)V_M. Since i_{s1}<0 during [t_4, t_5], the lower switches

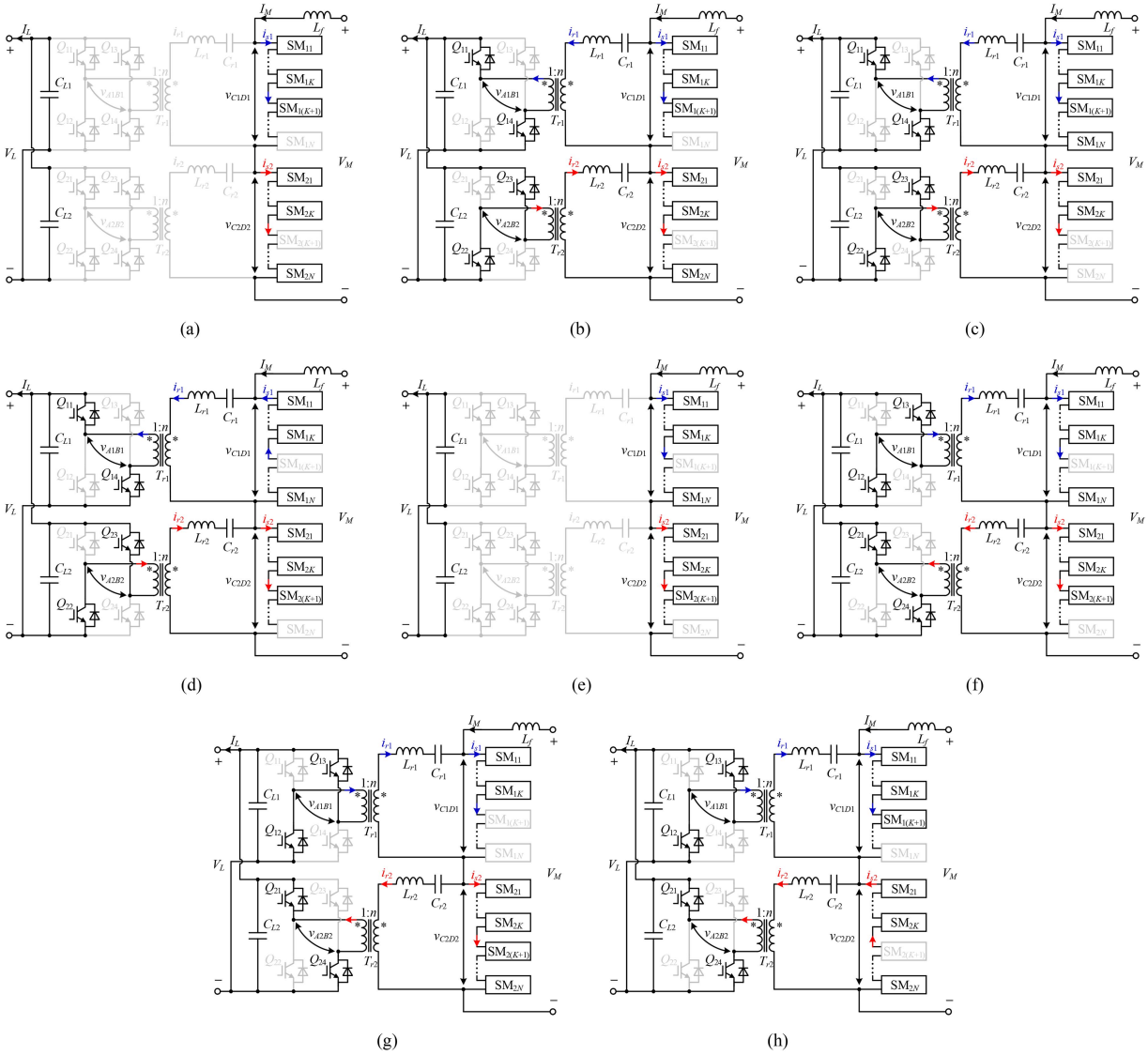

Fig. 5. Operation modes of the proposed converter in backward mode. (a) $[t_0, t_1]$ and $[t_{10}, T_s]$. (b) $[t_1, t_2]$. (c) $[t_2, t_4]$. (d) $[t_4, t_6]$. (e) $[t_6, T_s/2]$ and $[T_s/2, t_7]$. (f) $[t_7, t_8]$. (g) $[t_8, t_9]$. (h) $[t_9, t_{10}]$.

S_{1j2} of bypassed SMs can be turned ON with ZVS. After i_{s1} rises over 0 at t_5, the upper switches S_{1j1} of other SMs inserted during $[t_5, t_6]$ can be turned OFF with ZCS. i_{r1} and i_{s1} increase rapidly until $i_{r1} = 0$ and $i_{s1} = I_M$ at t_6. The state equation of the circuit during $[t_4, t_6]$ can be expressed as follows:

$$\begin{cases} L_{r1}\dfrac{di_{r1}(t)}{dt} = v_{Cr1}(t) + \dfrac{(N-K)V_M}{(N+K)d_N T_s}(t-t_4) + nV_L - \dfrac{NV_M}{N+K} \\ C_{r1}\dfrac{dv_{Cr1}(t)}{dt} = -i_{r1}(t) \end{cases}. \tag{13}$$

Mode 5 $[t_6, T_s/2]$ [see Fig. 5(e)]: At t_6, Q_{11} and Q_{14} are turned OFF with ZCS when i_{r1} is zero. The SMs are bypassed gradually, and the string voltage v_{C1D1} decreases until $V_M/2$ in this mode. The upper switches S_{1j1} of SMs can achieve ZCS-OFF with positive i_{s1}. In addition, both i_{r1} and i_{s1} keep unchanged until this mode ends at $T_s/2$.

Mode 6 $[T_s/2, t_7]$ [see Fig. 5(e)]: When $t = T_s/2$, the string voltage v_{C1D1} is $V_M/2$. The resonant current i_{r1} and the string current i_{s1} are zero and I_M, respectively. The SMs are bypassed gradually, and v_{C1D1} decreases from $V_M/2$. The upper switches S_{1j1} of bypassed SMs can be turned OFF with ZCS because of the positive i_{s1} in this mode.

Mode 7 $[t_7, t_8]$ [see Fig. 5(f)]: At t_7, the resonance begins, and Q_{12} and Q_{13} are turned ON. As the SMs are bypassed, v_{C1D1} gradually decreases to $KV_M/(N+K)$ during $[t_7, t_8]$. In this mode, the upper switches S_{1j1} of bypassed SMs can realize ZCS-OFF because of the positive i_{s1}.

Mode 8 $[t_8, t_9]$ [see Fig. 5(g)]: During $[t_8, t_9]$, only K SMs are inserted into the circuit. And the string voltage v_{C1D1} is $KV_M/(N+K)$.

Mode 9 $[t_9, t_{10}]$ [see Fig. 5(h)]: During $[t_9, T_s]$, SMs begin to be inserted, and the string voltage v_{C1D1} increases gradually. Since $i_{s1}>0$ in this mode, the upper switches S_{1j1} of inserted SMs can be turned ON with ZVS. Moreover, i_{r1} and i_{s1} decrease rapidly until $i_{r1} = 0$ and $i_{s1} = I_M$.

Mode 10 [t_{10}, T_s] [see Fig. 5(a)]: At t_{10}, Q_{12} and Q_{13} are turned OFF with ZCS. As the SMs inserted gradually, the string voltage v_{C1D1} gradually changes to $V_M/2$. i_{r1} and i_{s1} remain unchanged until this mode ends at T_s. The upper switches S_{1j1} of inserted SMs can achieve ZVS-ON because of positive i_{s1} in this mode.

Based on (11)−(13), the expression of i_{r1} and v_{Cr1} in half switching period under backward mode can be solved as (A3) and (A4) in Appendix. And the expressions of waveforms in [$T_s/2$, T_s] are symmetry with the waveforms in [t_0, $T_s/2$].

According to the above-mentioned analysis, the proposed converter can achieve ZCS-OFF for all LV-side full-bridge switches and ZVS-ON and ZCS-OFF for switches of partial MV-side SM when the converter works in forward and backward modes.

III. Steady-State Analysis of the Proposed Converter

A. Transmission Power

For the proposed converter with QSW modulation, d_N is used to regulate the transmission power in both forward and backward modes. To obtain the relationship between the control variables d_N and the transmission power, the transmission power characteristic is presented in this part with the time-domain analysis method.

According to (A1) and (A2), the transmission power P_1 in forward mode can be expressed as (A5) in Appendix, where k is defined as $(T_s/2-t_6)/(d_NT_s/2)$. Besides, referring to Fig. 3(a), the following initial and final conditions of i_{r1} and v_{Cr1} must be satisfied, where the initial resonant current $i_{r1}(t_0)$ is zero. And the transmission power P_1 should equal the reference power P_t.

$$\begin{cases} i_{r1}(t_0) = i_{r1}\left(\frac{T_s}{2}\right) = i_{r1}(T_s) = 0 \\ v_{Cr1}(t_0) = V_M - v_{Cr1}\left(\frac{T_s}{2}\right) = v_{Cr1}(T_s). \\ P_1 = P_t \end{cases} \tag{14}$$

According to (14), (A1), (A2), and (A5), the initial resonant capacitor voltage $v_{Cr1}(t_0)$, k and d_N can be solved in forward mode. Then, numerical solutions can be found for P_1, M and d_N, where M is the voltage gain, $M = V_M/(2nV_L)$. The curves of the duty cycle of string voltage rising and falling process d_N versus nominalized transmission power P_1/P_N and voltage gain M are illustrated in Fig. 6(a), where P_N is the rated power. According to Fig. 6(a), M and P_1/P_N increase with d_N when in forward mode. And the regulation of transmission power in the full-load range is achieved by a small variation range of d_N.

When the power is transferred from the MV terminal to the LV terminal, based on (A3) and (A4), the transmission power P_2 can be expressed as (A6) in Appendix, where $k_e = (t_1-t_0)/(d_NT_s/2) = 2nV_L(N+K)/(V_M(N-K))$. As shown in Fig. 6(b), the numerical solutions of P_2, M and d_N are solved. According to Fig. 6(b), P_2/P_N changes from 0 to −1 with the decrement of d_N. Besides, M increase with d_N for the same P_2/P_N in backward mode.

In addition, the number of constantly inserted SMs K can be used together with d_N to regulate the transmission power when terminal voltage varies over a wide range [18].

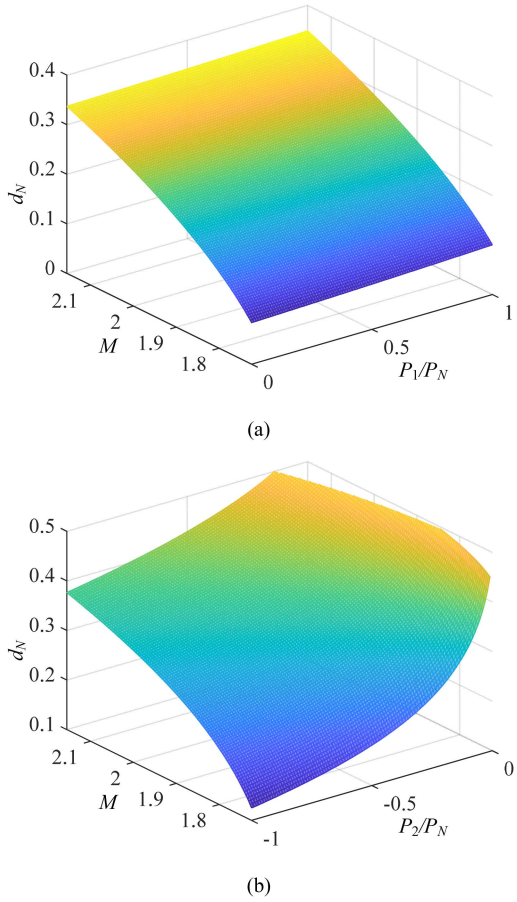

Fig. 6. Duty cycle of string voltage rising and falling process d_N versus nominalized transmission power and voltage gain M. (a) Forward mode. (b) Backward mode.

B. Soft Switching

All the switches of LV-side full bridges for the proposed converter can achieve ZCS-OFF with the aforementioned modulation scheme and appropriate parameters design. While the switches of MV-side half-bridge SM strings have different soft switching characteristics due to the dc circulating current.

1). Soft Switching for LV-Side Full Bridges: According to Fig. 3(a), to ensure the ZCS-OFF of LV-side full-bridge switches in forward mode, the resonant current i_{r1} should fall below zero before t_5 and rise to zero before $T_s/2$. Hence, the ZCS-OFF condition can be written as follows:

$$i_{r1}(t_5) \le 0 \tag{15}$$

$$0 \le \frac{T_s}{2} - t_6 \le \frac{d_NT_s}{2}. \tag{16}$$

In backward mode, i_{r1} must decrease to zero before the resonant current increases in the next half switching period to ensure the ZCS-OFF of LV-side full-bridge switches. Besides, on account of the tolerance of parameters and the finite commutation speed in practical application, it is acceptable to control i_{r1} down to zero before $T_s/2$. Hence, (17) should be satisfied.

$$\frac{T_s}{2} - t_6 \ge 0. \tag{17}$$

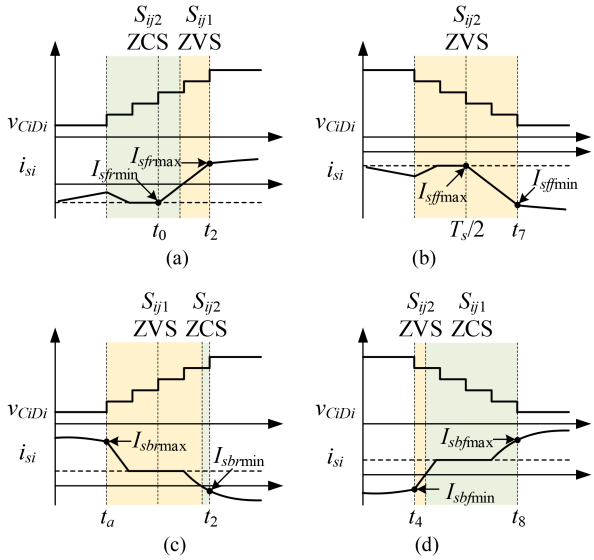

Fig. 7. Soft switching characteristics of SMs. (a) String voltage rising stage in forward mode. (b) String voltage falling stage in forward mode. (c) String voltage rising stage in backward mode. (d) String voltage falling stage in backward mode.

2). Soft Switching for MV-Side Half-Bridge SMs: The soft switching characteristics of MV-side half-bridge SMs are determined by the string current i_{si} and the transition process of string voltage v_{CiDi}, as shown in Fig. 7. The soft switching characteristics also change under different load conditions. Fig. 8 illustrates the nominalized string current versus transmission power and voltage gain M during the string voltage transition process, where $I_{MN} = P_N/V_M$.

For the forward mode, string current i_{si} has a negative bias. As shown in Fig. 7(a), during the string voltage rising stage, i_{si} changes from negative to positive. The maximum value of i_{si} denoted as $I_{sfr\max}$ reaches at $t = t_2$, while the minimum value of i_{si} denoted as $I_{sfr\min}$ arrives at $t = t_0$. According to Fig. 8(a), $I_{sfr\max}$ is greater than 0, and $I_{sfr\min}$ is less than 0 in the full-load range. Therefore, there are always some SMs where S_{ij1} realize ZVS-ON and other SMs where S_{ij2} are turned OFF with ZCS. As shown in Fig. 7(b), the maximum value of i_{si} ($I_{sff\max}$) is $i_{si}(T_s/2)$, and the minimum value of i_{si} ($I_{sff\min}$) is $i_{si}(t_7)$ during the string voltage falling stage. According to Fig. 8(b) $I_{sff\max}$ and $I_{sff\min}$ are negative, which ensures that the S_{ij2} realize ZVS-ON in the full-load range.

For the backward mode, string current i_{si} has a positive bias. As shown in Fig. 7(c), during the string voltage rising stage, i_{si} changes from positive to negative. $I_{sbr\max}$, the maximum value of i_{si} reaches at $t = t_a$. And $I_{sbr\min}$, the minimum value of i_{si} arrives at $t = t_2$. According to Fig. 8(c), $I_{sbr\max}$ is positive in the full-load range. However, as transmission power increases and M decreases, $I_{sbr\min}$ changes from negative to positive. Therefore, the soft switching characteristics of lagging inserted SMs will change from ZCS-OFF of S_{ij2} to ZVS-ON of S_{ji1}. As shown in Fig. 7(d), during the string voltage falling stage, the maximum and minimum values of i_{si} are $i_{si}(t_8)$ and $i_{si}(t_4)$, respectively. The

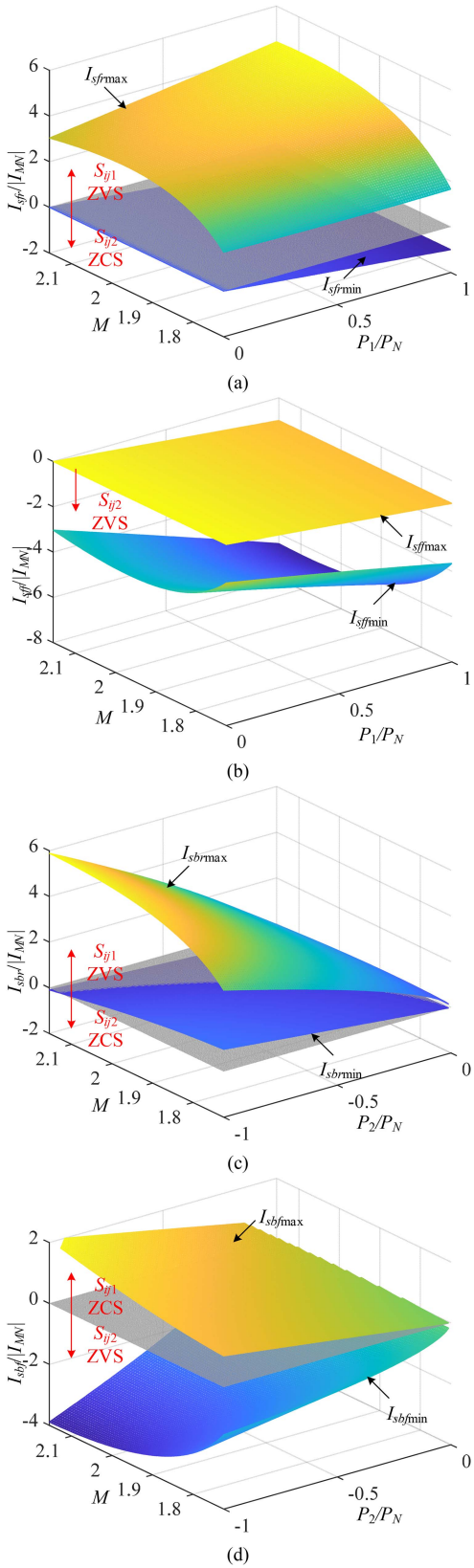

Fig. 8. Nominalized string current versus nominalized transmission power and voltage gain M. (a) String voltage rising stage in forward mode. (b) String voltage falling stage in forward mode. (c) String voltage rising stage in backward mode. (d) String voltage falling stage in backward mode.

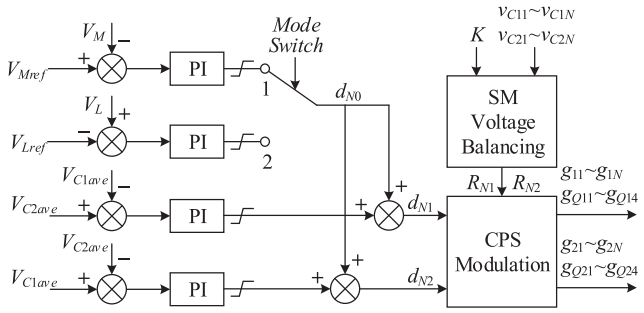

Fig. 9. Block diagram of the output voltage strategy.

soft switching characteristic of SMs is unchanged in the full-load range since $I_{sbf\max}<0$ and $I_{sbf\min}>0$, according to Fig. 8(d).

C. Control Strategy

According to the above-mentioned analysis, the basic output voltage control strategy for the proposed converter is shown in Fig. 9. In the forward mode, the MV terminal voltage V_M is sampled and fed back to generate the basic d_{N0} (*Mode Switch* $= 1$). In the backward mode, the basic d_{N0} is generated with the LV terminal voltage V_L (*Mode Switch* $= 2$). The average SM capacitor voltages of each string $V_{C1\,ave}$ and $V_{C2\,ave}$ are compared with $V_{C2\,ave}$ and $V_{C1\,ave}$ separately to obtain the respective compensation for d_{N0}, achieving voltage balancing between two half-bridge SM strings. In this article, an open loop rotation modulation scheme is adopted to achieve SM voltage balancing [17], [29]. With N and K, N-dimensional rotational SM voltage balance sequences $\boldsymbol{R}_{N1}$ and $\boldsymbol{R}_{N2}$ can be obtained, which indicate the switching patterns of SMs in NT_s. Then, based on $\boldsymbol{R}_{N1}$, $\boldsymbol{R}_{N2}$, d_{N1}, and d_{N2}, the driving signals for MV-side SMs and LV-side full-bridge are configured with CPS modulation strategy.

IV. Parameters Design

This section presents the design procedure for the key parameters of the proposed converter, including the total number of SMs, resonant inductor, resonant capacitor, SM capacitor, and filter inductor.

A. Number of SMs

Based on the modulation scheme of the proposed converter, totally $N+K$ SMs are inserted to withstand the MV terminal voltage. The number of SMs can be determined by the device voltage stress and the number of constantly inserted SMs. According to (1), the total number of MV-side SMs N_{total} can be expressed as follows:

$$N_{total} = 2N = \frac{2V_M}{V_C} - 2K. \tag{18}$$

According to (18), N_{total} decreases with the increment of V_C and K. Therefore, N_{total} can be reduced by increasing K, and the minimum value of N_{total} is V_M/V_C+1 when $K=N-1$. However, V_{CiDi} decreases as K increases according to (4), which leads to high current stress of MV-side devices.

B. Resonant Inductor and Capacitor

The parameters of resonant inductor L_r and capacitor C_r can be designed to meet the requirements of soft switching for LV-side full-bridge and low resonant current. Since the operation principle of forward and backward modes are unsymmetrical, both forward and backward are considered to design the resonant parameters.

The turns ratio n can be designed with rated terminal voltages V_M and V_L as well as N and K. And $2nV_L/V_M < (N-K)/(N+K)$ must be satisfied to ensure the proper operation of the converter in forward and backward modes.

Then, based on (14), (A1) and the ZCS-OFF constraint in forward and backward modes shown in (15)−(17), the maximum value of i_{ri} (I_{rpeak}) in forward or backward mode can be calculated by numerical method with a specific combination of L_r and C_r. By comparing the I_{reapk} under different combinations of L_r and C_r, the optimum resonant parameters corresponding to bottom I_{rpeak} can be obtained.

C. SM Capacitor

The value of SM capacitance can be designed according to the ripple tolerance requirement. The SM capacitor is charged with positive i_{si} and discharged with negative i_{si} when S_{ij1} is ON, which decides the voltage fluctuation of SM capacitor. And the voltage fluctuation of SM capacitor is zero when S_{ij1} is OFF. Besides, the voltage fluctuations are different for SMs working with 50% duty cycle and constantly inserted.

For the constantly inserted SM, S_{ij1} is turned ON over one switching period, and the voltage fluctuation of SM capacitor can be expressed as (19), where $d_K = -(N-K-1)/(2(N-K))d_N$.

$$\Delta V_K(t) = \tfrac{1}{C_{ij}} \int_{t_0+d_K T_s}^{t_0+d_K T_s+t} i_{si}(t)\,dt, \quad 0 \le t < T_s. \tag{19}$$

For the SM working with a 50% duty cycle, the voltage fluctuation of SM capacitor diverges due to the same duty cycle but the different internal phase-shifted angle of each SMs under QSM. The voltage fluctuation of SM capacitor for the lth inserted SM working with 50% duty cycle within each switching period can be expressed as (20), where $l = 1, 2, \ldots, N-K$, and d_l is the internal phase-shifted duty cycle of lth SM working with 50% duty cycle, $d_l = ((l-1/2)/(N-K)-1/2)d_N$.

$$\Delta V_N(t, d_l) = \begin{cases} \frac{1}{C_{ij}} \int_{t_0+d_l T_s}^{t_0+d_l T_s+t} i_{si}(t)\,dt, & 0 \le t < \frac{T_s}{2} \\ \frac{1}{C_{ij}} \int_{t_0+d_l T_s}^{t_0+d_l T_s+T_s/2} i_{si}(t)\,dt, & \frac{T_s}{2} \le t < T_s \end{cases}. \tag{20}$$

According to the rotation modulation SM voltage balancing scheme, the driving signals of a specific SM are circulated in the rotational SM voltage balance sequence $\boldsymbol{R}_N = [d_K, \ldots, d_K, d_1, \ldots, d_{N-K}]$. And the voltage fluctuation of each SM capacitor varies periodically within the rotational SM voltage balance period NT_s. Therefore, the maximum SM capacitor voltage fluctuation can be found over NT_s. Combing (19) and (20), the voltage fluctuation of a specific SM capacitor in mth switching periods ($m \le N$) under sequence $\boldsymbol{R}_N$ can be expressed

as follows:

$$\Delta V_m(t) = \begin{cases} \Delta V_K(t), & R_N[m] = d_K \\ \Delta V_N(t, S_N[m]), & R_N[m] \neq d_K \end{cases}. \quad (21)$$

According to (21), the voltage fluctuation of SM capacitor during NT_s can be obtained as follows:

$$\Delta V_{RN}(t) = \begin{cases} \Delta V_1(t), & 0 \le t < T_s \\ \Delta V_2(t-T_s) + \Delta V_1(T_s), & T_s \le t < 2T_s \\ \vdots & \\ \Delta V_N(t-(N-1)T_s) & \\ + \sum_{p=1}^{N-1} \Delta V_p(T_s), & (N-1)T_s \le t < NT_s \end{cases}. \quad (22)$$

According to (22), the peak-to-peak SM capacitor voltage ΔV_{Cpp} can be obtained as follows:

$$\Delta V_{Cpp} = \max\{\Delta V_{RN}(t)\} - \min\{\Delta V_{RN}(t)\}. \quad (23)$$

Therefore, based on (19)–(23), the value of C_{ij} can be determined under the rated power P_N to limit the voltage ripple of SM capacitor within the maximum tolerance range.

D. Filter Inductor

With the configuration of two SM strings connected in series and the complementary string output voltages, the sum of two string voltages is constantly equal to V_M. Therefore, L_f can be minimized due to the tiny voltage fluctuation and current ripple. On the other hand, the short-circuit fault situation should also be considered in the design of the filter inductor. When a fault occurs on the MV terminal, the filter inductor is responsible for limiting the fault current. Assuming that the SM capacitor voltage V_{Cij} is unchanged when a fault occurs on MV terminal, the fault current rise rate can be expressed as follows:

$$\frac{di_M}{dt} = \frac{(N+K)V_C}{L_f} = \frac{V_M}{L_f}. \quad (24)$$

According to (24), the filter inductor can be determined by di_M/dt depending on the current rating of power devices and the controller delay.

E. Design Example

A dc/dc converter with the following specifications is taken as an example to illustrate the design procedure.

1) LV terminal voltage $V_L = 100$ V.
2) MV terminal voltage $V_M = 1$ kV.
3) Rated power $P_N = 4$ kW.
4) Switching frequency $f_s = 10$ kHz.

Depending on the given V_M, V_C is set as 200 V. Since a large K can reduce N_{total}, but leads to high current stress of MV-side devices, $K = 1$ is chosen in this design example. $N_{total} = 2N = 8$ can be calculated by (18) when $V_M = 1$ kV, $V_C = 200$ V and $K = 1$. After determining N and K, the turns ratio n can be set as 2.9 here.

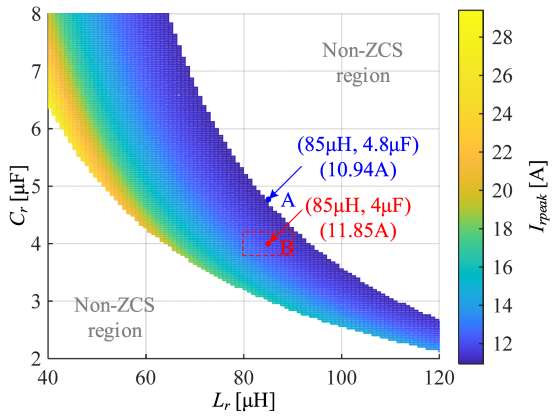

Fig. 10. Maximum value of i_{ri} versus C_r and L_r.

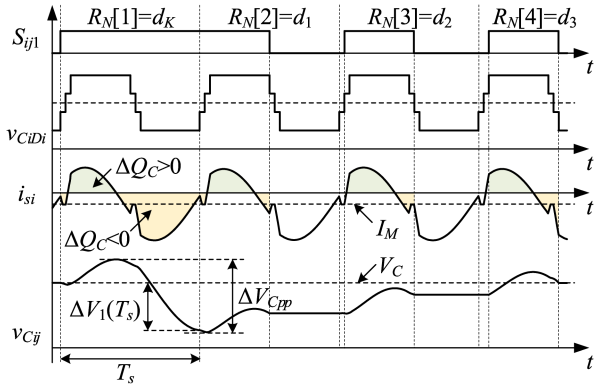

Fig. 11. SM capacitor voltage fluctuation when $N = 4$ and $K = 1$.

The resonant parameters L_r and C_r can be designed to meet the requirements of soft switching of LV-side full bridge switches as well as low resonant current. According to (14)–(17), and (A1), I_{rpeak} in forward mode for different resonant parameters can be calculated, and the results are shown in Fig. 10, where L_r varies from 40 to 120 μH, and C_r ranges from 2 to 8 μF. According to Fig. 10, I_{rpeak} decrease with the increase of L_r and C_r. The minimum $I_{rpeak} = 10.94$ A is obtained at point A where $L_r = 85$ μH, $C_r = 4.8$ μF. On account of the tolerance of passive components set as $\pm 5\%$, point B is selected as the design point to reduce I_{rpeak} on the basis of guaranteeing the soft switching of LV-side full-bridge switches.

The value of C_{ij} can be determined according to its voltage fluctuation. Take the forward mode as an example. The voltage fluctuation of SM capacitor when $N = 4$ and $K = 1$ is shown in Fig. 11 following the rotational SM voltage balance sequence $\boldsymbol{R}_N = [d_K, d_1, d_2, d_3]$. The largest SM capacitor voltage fluctuation occurs during the first switching period when the SM is constantly inserted into the circuit. According to (19)–(23), the SM capacitor C_{ij} is selected to be 150 μF to limit the maximum SM capacitor voltage ripple below 4.5 V.

Finally, accounting for the controller delays and current rating of power devices, the fault current rise rate di_M/dt should be less than 0.5 A/μs. Hence, the filter inductor L_f should be larger than

TABLE II
MAIN DESIGN PARAMETERS OF THREE DC/DC CONVERTERS SCHEMES

Items	RMMC [26]	MMR [27]	Proposal
LV terminal voltage /V		750	
MV terminal voltage /kV		10	
Rated power /kW		500	
AC link frequency /kHz		5	
Number of SM	10	20	20
SM capacitor/μF	800	150	100
Resonant inductor /μH	12	1000	270
Resonant capacitor /μF	/	2	5
Turns ratio of transformer 1:n	0.7	6.7	6.6
Magnetizing inductor /mH	0.18	3.5	/
Filter inductor /mH	/	/	7.5
LV terminal capacitor /mF	5	5	2.5
MV terminal capacitor /mF	1	0.12	/

TABLE III
COMPARISON RESULTS OF THREE DC/DC CONVERTER SCHEMES

Parameter	RMMC [26]	MMR [27]	Proposal
Number of switches on LV side	4	4	8
Voltage stress of switches on LV side /V	750	750	750
Current stress of switches on LV side /A	1126.7/1086.0	1141.9	484.7
Number of switches on MV side	20	40	40
Voltage stress of switches on MV side /V	1170	1000	1000
Current stress of switches on MV side /A	$1621.8^{U}/1620.4^{L}$	$115.5^{U}/144.6^{L}$	$84.1^{U}/123.2^{L}$
Number of transformers	1	1	2
Number of inductors	1	2	3
Number of capacitors	12	24	24
Devices cost /k$	93.42	16.10	12.49
Efficiency /%	95.88	97.76	97.74

Note:
^{U}- Current stress of upper switch in half-bridge SM.
^{L}- Current stress of lower switch in half-bridge SM.

2 mH based on (24). And L_f is set as 2.5 mH in this design example.

V. COMPARISON WITH DIFFERENT DC/DC CONVERTERS

In this section, a thorough comparison is conducted among RMMC, MMR, and the proposed converter. The comparison is performed in terms of the number of components, voltage and current stress of switches, cost, and efficiency.

The main design parameters of three dc/dc converter schemes are shown in Table II, where 750 V/10 kV/500 kW is selected as a specific case study. Considering the performance and cost of existing commercial devices, 1200 and 1700 V semiconductor switches are chosen as the power switches for LV-side full bridges and MV-side half-bridge SMs of three dc/dc converters, respectively. Therefore, the rated voltage of MV-side switches and capacitors is designed to be around 1 kV. Then, the number of SMs is 10, 20, and 20 for the RMMC, MMR, and the proposed converter with the basic modulation scheme. The ac link frequency is set as 5 kHz. In addition, the voltage ripple of the LV and MV terminal capacitors is designed as 1% of the rated value. For MMR and the proposed converter, the voltage ripple of SM capacitor is set as 2% of the rated value. And for RMMC, the voltage ripple of SM capacitor is set at 20% since the SM capacitor also operates as the resonant capacitor. And detailed comparison results are summarized in Table III.

A. Semiconductor Switches

The semiconductor switches are selected from *Infineon Technology* [30], of which the withstand voltage and current are set as 1.5−2 of the rated values in Table II. The prices of devices are obtained from *Mouser Electronics* [31]. The FF1200R12IE5 IGBTs (1200 V/1200 A) are employed on LV side for RMMC and MMR, whereas the FF600R12IP4 IGBTs (1200 V/600 A) are selected as the LV-side full-bridge switches for the proposed converter. For the MV-side SMs, the FF150R17KE4 IGBTs (1700 V/150 A) are selected for MMR and the proposed converter, whereas the FF1800R17IP5 IGBTs (1700 V/1800 A) are adopted for RMMC. Besides, the dual-driver core 2SC0435T is employed to drive IGBTs. Therefore, the costs of switches and drivers can be calculated and illustrated in Fig. 12(a). The costs of proposed converter converters are the lowest, followed by MMR. For RMMC, its total costs are high due to the high unit price of high current rating IGBTs, even though the number of IGBTs and drivers is much lower than the other two schemes.

The power loss of switches is estimated by the PLECS. The junction temperature of all switches is set around 85°C. The switching frequency of RMMC is 500 Hz that is 1/10 of the ac link frequency, while the switching frequency of MMR and the proposed converter is 5 kHz. The results are shown in Fig. 12(b). The RMMC has the lowest switching loss among the three schemes. And the conduction loss of the proposed converter and MMR are significantly reduced due to the low ac link current at MV side compared with RMMC.

B. Magnetic Components

Based on Table II, the magnetic components for three dc/dc converter schemes are designed, and the loss is analyzed. The design principle is set as minimizing the volume of magnetic components, which are defined as the cubical space occupied by the magnetic components [20]. The U-U-Type Mn-Zn ferrite (TPW33) is selected as the core. And the air gap between two half of U-U cores is introduced for the transformers of RMMC and MMR and all inductors. For the transformer and the resonant inductor, the operating flux density is set as 0.2 T. And for the filter inductor, which only flows through dc current, the operating flux density is set as 0.3 T. The litz wire is adopted to reduce the ac winding loss with a current density of 3 A/mm^2. The 35 kV insulation is compulsorily guaranteed between MV and LV windings and between MV winding and core.

The power loss results of magnetic components are calculated and presented in Fig. 12(b). According to Fig. 12(b), the total loss of the magnetic components in the three dc/dc converter schemes are approximately the same under the same design. It should be noted that the price of customized magnetic components is not provided here. Considering the fault limit inductor connected in

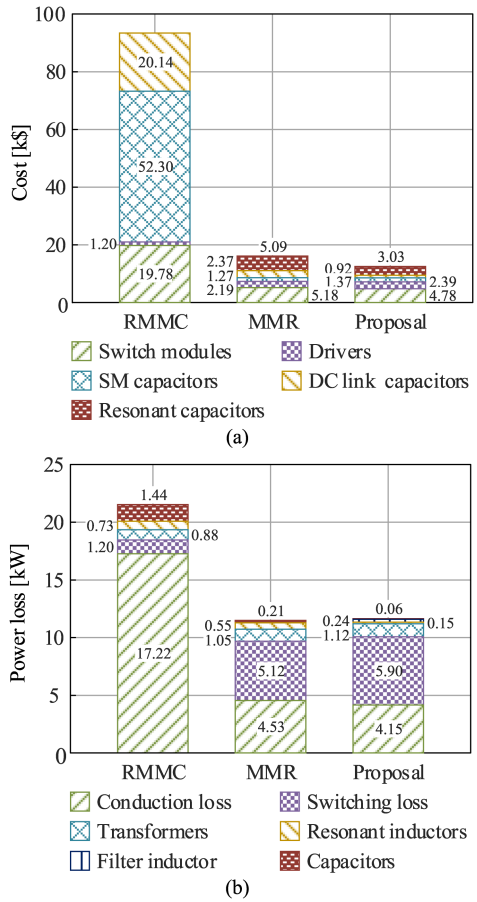

Fig. 12. Cost and power loss breakdown of three dc/dc converter schemes. (a) Cost. (b) Power loss.

the MV terminal, three kinds of magnetic components are used in different schemes with the same total power rating. Therefore, their price is approximately close, which is related to the power ratings of magnetic components.

C. Capacitors

The capacitors in three dc/dc converters schemes include the SM capacitors, filter capacitors, resonant inductors as well as MV and LV terminal dc link capacitors. The capacitors are selected from *KEMET Electronics* [32]. The prices of the devices are from *Mouser Electronics*.

To meet the voltage and current stress requirements, eighty paralleled C44ASGP5100ZA0J (1500 V_{dc}/32 A/10 μF) are selected as the SM capacitor for RMMC. And for MMR and the proposed converter, C44USGT6165M83K (1500 V_{dc}/40 A /165 μF) and C44USGT6120M81K (1500 V_{dc}/41 A/120 μF) are adopted as the SM capacitors. Moreover, Four C44UQGT7140M54K (1100 V_{dc}/100 A/1.4 mF) are chosen as the LV terminal dc link capacitor for three dc/dc converter schemes. Ninety-one C44UVGT6550M54K (1800 V_{dc}/89 A/550 μF, seven in series and thirteen in parallel) are used to construct the MV terminal dc link capacitor for RMMC. As for MMR, four C44USGT6550M53K (1500 V_{dc}/91 A/550 μF) are connected in series as the MV terminal dc link capacitor. In addition, thirty C44BXFP4150ZA0J (2400 V_{dc}/18 A/1.5 μF, three in series and ten in parallel) and C44BXFP3100ZA0J (2400 V_{dc}/5 A/0.1 μF, two in series and forty in parallel) are used as the resonant capacitor for the proposed converter and MMR, respectively. And the cost and total power loss of capacitors are shown in Fig. 12.

TABLE IV
EXPERIMENTAL PARAMETERS

Parameters	Value
LV terminal voltage V_L/V	100
MV terminal voltage V_M/kV	1
Rated power P_N/kW	4
Switching frequency f_s/kHz	10
Number of SMs per string N	4
SM capacitor C_{ij}/μF	150
Filter inductor L_f/mH	2.5
Resonant inductor L_{ri}/μH	85
Resonant capacitor C_{ri}/μF	4
Transformer turns ratio 1:n	1:2.9
LV-side capacitor C_{Li}/μF	940

The proposed converter has no MV terminal dc link capacitor. And the currents through SM capacitors and resonant capacitors are reduced. Therefore, the total capacitor loss of the proposed converter can be significantly reduced compared with RMMC and MMR. In addition, the total cost of capacitors is also lower than the other two dc/dc converter schemes.

D. Overall Analysis

According to Fig. 12(a), the cost of the proposed converter is the lowest among the three schemes, followed by MMR and RMMC. As shown in Fig. 12(b), the power loss of the proposed converter and MMR are close and significantly lower than RMMC. And the proposed converter can achieve an efficiency of 97.74%. Actually, the RMMC is preferred to be used in the application with the high input voltage but low transmission power.

VI. EXPERIMENTAL VERIFICATION

A. Experimental Prototype Setup

A 100 V/1 kV/4 kW prototype is established to verify the feasibility of the proposed converter. Fig. 13 shows the circuit configuration and photograph of the prototype, and detailed experimental parameters are listed in Table IV. Each half-bridge string includes four SMs with 200 V nominal voltage. Both LV-side full-bridge switches and MV-side half-bridge SM switches employ IKW40N65ET7 IGBT. The transformer cores adopt ONL-100 × 50 × 25 nanocrystalline core. The EE55/55/21 ferrite core is chosen to manufacture two resonant inductors, and TPW33 is selected as the core material. Two stacked 77620 A cores are used as the filter inductor core. The primary winding of the transformer uses 0.1 mm × 1200 strands litz wire. Litz wire of 0.1 mm × 350 strands is used for the transformer secondary winding and inductor winding.

And litz wire of 0.1 mm × 250 strands is chosen for filter inductor winding. Besides, DMJ-PS 450 V_{dc} 150 μF and

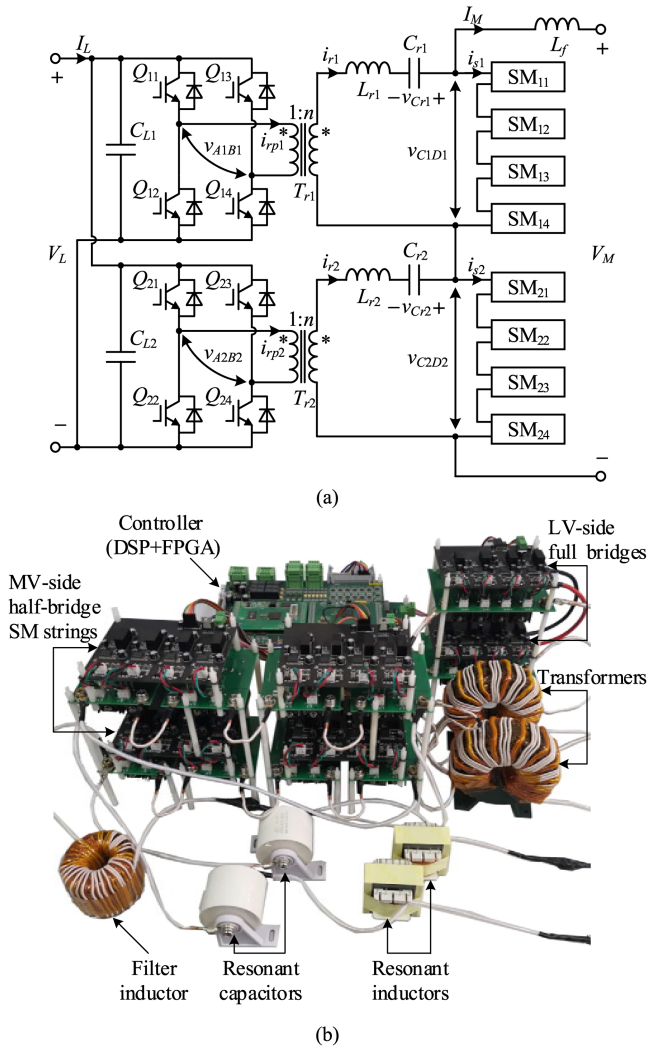

Fig. 13. Experimental prototype. (a) Configuration of the experimental circuit. (b) Photograph of the prototype.

ELH2WM471R50KT are selected as SM capacitors and LV terminal dc link capacitors, respectively. The resonant capacitors employ two RMJ-MT 1200 V_{dc} 4 μF. In addition, the control schemes are implemented by a TMS320F28346 DSP and a C6SLX16-2FTG256I FPGA. And the dead time is set as 2 μs.

B. Experimental Results

The experimental waveforms are shown in Figs. 14–17. Fig. 14 shows the steady-state experimental waveforms when in forward mode. Fig. 14(a) shows the waveforms of v_{A1B1}, v_{C1D1}, i_{r1} and i_{r2} in the full-load condition ($P_t = 4$ kW). The string voltage v_{C1D1} is a 3-step staircase waveform with one constantly inserted SM that takes a minimum value of 200 V and a maximum value of 800 V. The resonant current i_{r1} and i_{r2} are phase-shifted by π with a peak value of 18.1 A, which is larger than the corresponding analysis result in Section IV owning to the saturation voltage of power switches. It should be noted that the positive and negative periods of i_{r1} and i_{r2} are not strictly symmetrical due to the dead time of power devices. d_{N1}

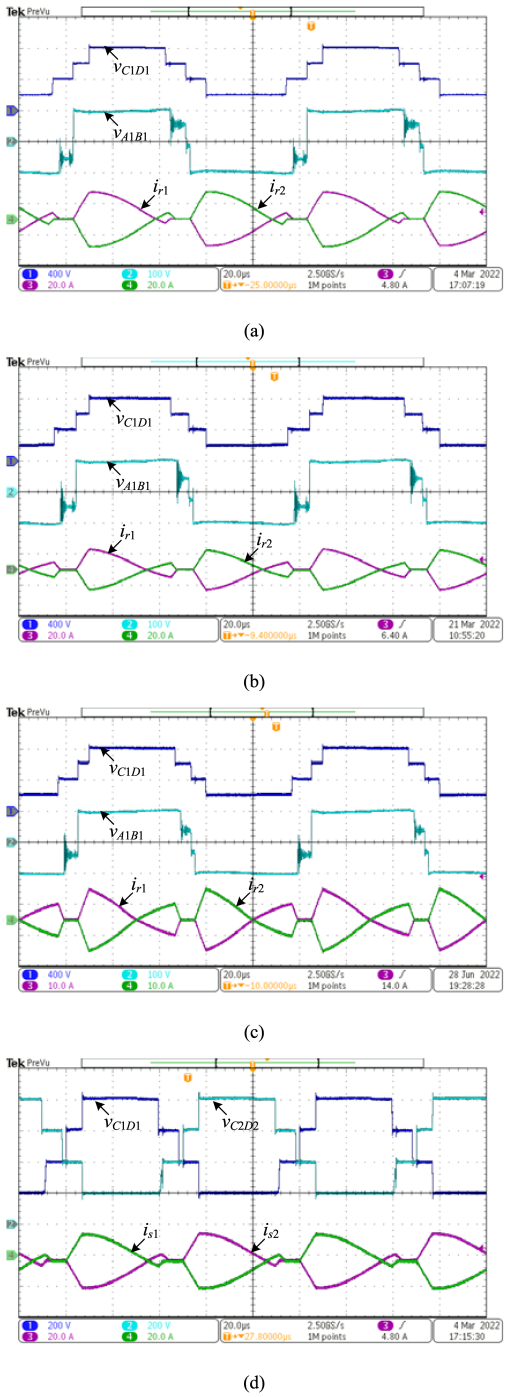

Fig. 14. Steady-state experimental waveforms in forward mode. (a) v_{C1D1}, v_{A1B1}, i_{r1} and i_{r2} under full-load condition ($P_t = 4$ kW). (b) v_{C1D1}, v_{A1B1}, i_{r1} and i_{r2} under half-load condition ($P_t = 2$ kW). (c) v_{C1D1}, v_{A1B1}, i_{r1} and i_{r2} under light-load condition ($P_t = 0.8$ kW). (d) v_{C1D1}, v_{C2D2}, i_{s1} and i_{s2} under full-load condition ($P_t = 4$ kW).

is about 0.18 in this condition. Fig. 14(b) presents the operation waveforms under the half-load condition ($P_t = 2$ kW). Both i_{r1} and i_{r2} have a peak value of 13.6 A, and d_{N1} is approximately 0.16. The operation waveforms under the light-load condition are shown in Fig. 14(c) ($P_t = 0.8$ kW). The peak value of i_{r1} and i_{r2} are 9.9 A, and d_{N1} is approximately 0.14. Besides, as

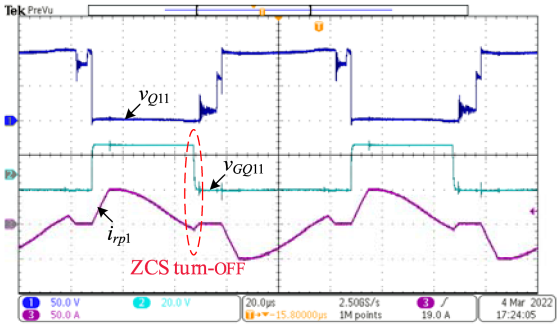

Fig. 15. Steady-state experimental waveforms of v_{Q11} v_{GQ11} and i_{rp1} in forward mode under full-load condition ($P_t = 4$ kW).

shown in Fig. 14(d), the string voltage v_{C1D1} and v_{C2D2} are phase-shifted by π, and the string current i_{s1} and i_{s2} have a -4 A dc bias. It can be seen that i_{s1} and i_{s2} change from negative to positive during the corresponding string voltage rise, indicating that lower switches of some SMs can achieve ZCS-OFF while the upper switches of other SMs can achieve ZVS-ON. In the string voltage falling process, i_{s1} and i_{s2} are negative, indicating that all the SM lower switches can achieve ZVS-ON.

Fig. 15 shows the steady-state experimental waveforms of voltage and driving signal of Q_{11}, denoted as v_{Q11} and v_{GQ11}, as well as the primary current of transformer i_{rp1}. After Q_{11} is turned ON, i_{rp1} increases from zero to the peak value of 52 A, then descend below zero and rises to zero before the next half switching period. Hence, the ZCS-OFF of LV-side full-bridge switches can be achieved.

Fig. 16 shows the steady-state experimental waveforms in backward mode. As shown in Fig. 16(a), the peak value of i_{r1} and i_{r2} are 10.8 A and $d_{N1} = 0.05$ under the full-load condition ($P_t = -4$ kW). When operating in half-load condition ($P_t = -2$ kW), the peak value of i_{r1} and i_{r2} are 6.1 A, and d_{N1} is 0.08, as shown in Fig. 16(b). The operation waveforms under the light-load condition ($P_t = -0.8$ kW) are shown in Fig. 16(c). The peak value of i_{r1} and i_{r2} are 2.6 A, and d_{N1} is approximately 0.14. Besides, the LV-side full-bridge switches are turned OFF with ZCS in backward mode. Fig. 16(d) shows the waveforms of v_{C1D1}, v_{C2D2}, i_{s1} and i_{s2} under the full-load condition ($P_t = -4$ kW). It can be seen that i_{s1} and i_{s2} have a 4 A dc bias. Therefore, i_{s1} and i_{s2} are positive during the corresponding string voltage rise, which ensures ZVS-ON for all SM upper switches. During the string voltage falling process, i_{s1} and i_{s2} are positive due to the dead time effect, indicating that all the SM upper switches can achieve ZCS-OFF.

Fig. 17 shows the voltage waveforms of SM capacitors. As shown in Fig. 17(a), the SM capacitor voltages are well balanced at about 200 V. According to Fig. 17(b), the maximum voltage fluctuation of SM capacitor is 3.9 V, which appears in the switching period when SM is constantly inserted under the rotational SM voltage balance sequence $\boldsymbol{R}_N = [d_K, d_1, d_2, d_3]$. The results are consistent with the theoretical analysis.

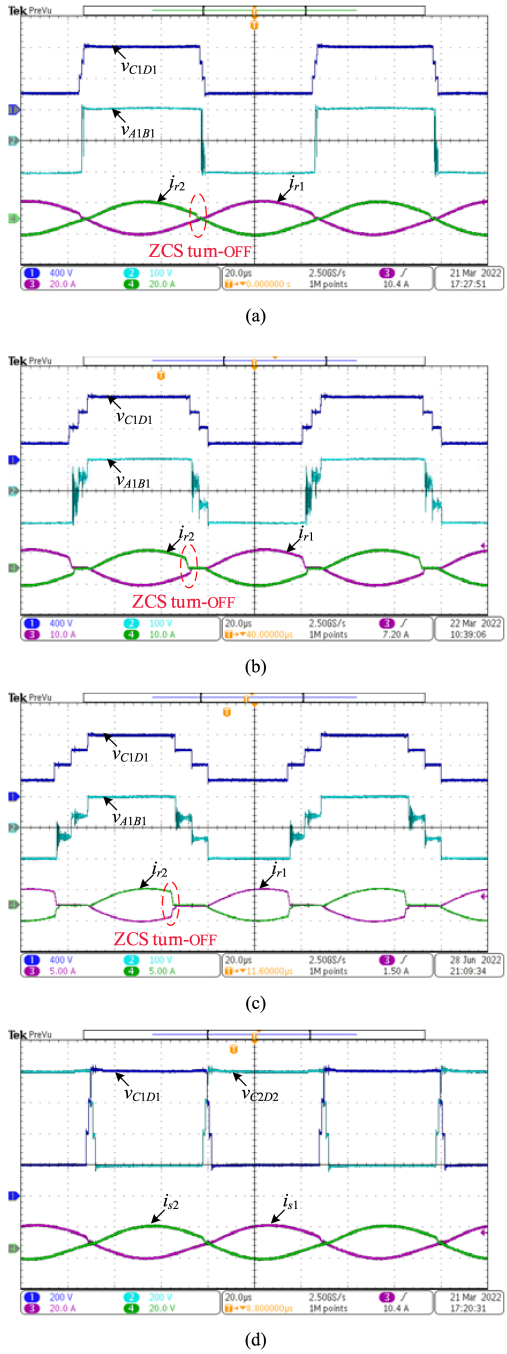

Fig. 16. Steady-state experimental waveforms in backward mode. (a) v_{C1D1}, v_{A1B1}, i_{r1} and i_{r2} under full-load condition ($P_t = -4$ kW). (b) v_{C1D1}, v_{A1B1}, i_{r1} and i_{r2} under half-load condition ($P_t = -2$ kW). (c) v_{C1D1}, v_{A1B1}, i_{r1} and i_{r2} under light-load condition ($P_t = -0.8$ kW). (d) v_{C1D1}, v_{C2D2}, i_{s1} and i_{s2} under full-load condition.

C. Efficiency and Power Loss

Fig. 18 presents the measured efficiency curves for both forward and backward modes. The peak efficiency is 92.9% in forward mode and 94.2% in backward mode. Besides, the efficiency in forward mode is slightly lower than backward mode due to the reactive power of the converter in forward mode. The results illustrate that the proposed converter can achieve high

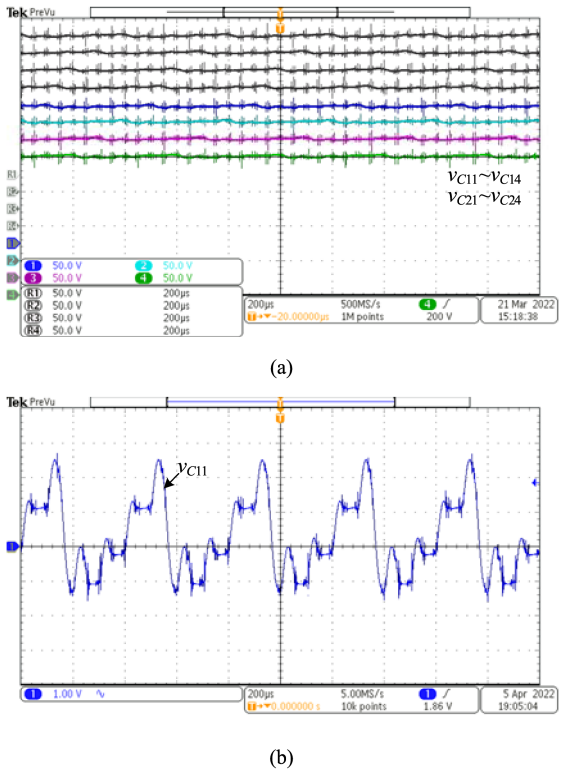

Fig. 17. Voltage waveforms of SM capacitors. (a) $v_{C11}-v_{C14}$ and $v_{C21}-v_{C24}$. (b) v_{C11}.

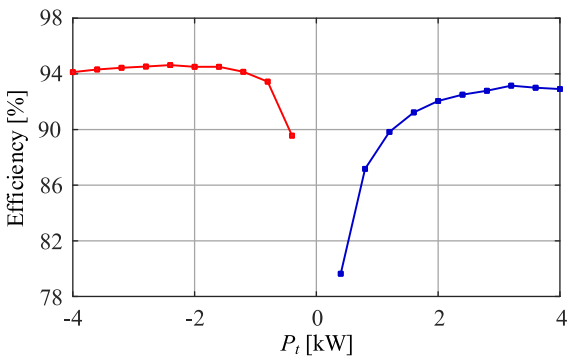

Fig. 18. Measured efficiency versus transmission power.

efficiency in forward and backward modes. In addition, the loss analysis for the prototype is carried out.

1). Power Loss of Switches: Assuming both the on-state voltage $V_{\rm CE}$ across the IGBTs and the forward voltage drop V_F across the anti-paralleled diodes are constants. And the difference between $V_{\rm CE}$ and V_F is not noticeable, $V_F = V_{\rm CE} = V_{\rm drop}$. The conducting loss $P_{\rm cond}$ in the IGBTs and diodes can be calculated as follows [33]:

$$P_{\rm cond}=\frac{2V_{\rm drop}}{T_s}\left(N\int_{t_0}^{t_0+T_s}|i_{s1}(t)|\,dt+2\int_{t_0}^{t_0+T_s}n\,|i_{r1}(t)|\,dt\right). \tag{25}$$

The switching loss calculation depends on the switching mode (hard switching or soft switching). The switching loss is low when soft switching is achieved, which can be neglected. In hard switching mode, assuming the current flowing through the switch linearly changes during the switch state transition [34]. For the LV-side full-bridge switches, the turn-OFF loss is negligible due to the realization of the ZCS-OFF. And the turn-ON current of LV-side full-bridge switches is zero. Hence, the turn-ON loss can also be neglected. For each MV-side half-bridge string, taking forward mode as an example, $N_{\rm ZCS}$ lower switches S_{ij2} can achieve ZCS-OFF, and $N_{\rm ZVS}$ upper switch S_{ij1} can realize ZVS-ON during string voltage rising stage, $N_{\rm ZCS}+N_{\rm ZVS} = N-K$. And $N-K$ lower switches S_{ij2} can realize ZVS-ON during the string voltage falling stage. Then, the turn-ON and turn-OFF loss in switches can be calculated as (26) and (27), where $t_{\rm on}$ and $t_{\rm off}$ are the switching time of turn-ON and turn-OFF states, respectively.

$$P_{\rm swon}=2\left(\frac{t_{\rm on}}{2T_s}V_C\sum_{l=1}^{N_{\rm ZCS}}|i_{s1}(t_0+d_l)|\right) \tag{26}$$

$$P_{\rm swoff}=2\left(\frac{t_{\rm off}}{2T_s}V_C\left(\sum_{l=N_{\rm ZCS}+1}^{N-K}|i_{s1}(t_0+d_l)|+\sum_{l=1}^{N-K}\left|i_{s1}\left(t_0+\frac{T_s}{2}+d_l\right)\right|\right)\right). \tag{27}$$

Then, the switching loss $P_{\rm sw}$ in the IGBTs and diodes can be calculated as follows:

$$P_{\rm sw}=P_{\rm swon}+P_{\rm swoff}. \tag{28}$$

2). Power Loss of Magnetic Components: The power loss of magnetic components contains core loss and copper loss. The total copper loss of transformers, resonant inductors, and filter inductor are given as (29), in which $I_{r1\rm RMS}$ and $I_{rp1\rm RMS}$ are the root mean square (RMS) value of i_{r1} and i_{rp1}, respectively. R_{Trp}, R_{Trs}, R_{Lr}, and R_{Lf} are the equivalent resistances of the primary and secondary winding of transformer, the winding of resonant inductor, and the winding of filter inductor, respectively.

$$P_{\rm copp}=2\left(R_{Trp}I_{rp1\rm RMS}^2+(R_{Trs}+R_{Lr})\,I_{r1\rm RMS}^2\right)+R_{Lf}I_M^2. \tag{29}$$

Since the current flow through the filter inductor is a dc current, the core loss of the filter inductor can be ignored. Therefore, the total core loss of transformers and resonant inductors are given as (30), where V_{eTr} and V_{eLr} are the volume of transformer and resonant inductor cores, P_{VTr} and P_{VLr} represent the core loss per unit volume of transformer and resonant inductor cores.

$$P_{\rm core}=2\left(P_{VTr}V_{eTr}+P_{VLr}V_{eLr}\right). \tag{30}$$

3). Power Loss of Capacitors: The power loss of capacitors can be calculated as (31). Where $I_{CL\rm RMS}$ and $I_{C\rm RMS}$ are the RMS current of LV terminal capacitor C_{Li} and half-bridge SM capacitor C_{ij}, respectively. $R_{CL\rm ESR}$, $R_{C\rm ESR}$ and $R_{Lr\rm ESR}$ are the equivalent series resistances (ESRs) of the LV terminal capacitor C_{Li} and half-bridge SM capacitor C_{ij} and resonant capacitor C_{ri}, respectively.

$$P_{\rm cap}=2\left(I_{CL\rm RMS}^2R_{CL\rm ESR}+NI_{C\rm RMS}^2R_{C\rm ESR}+I_{r1\rm RMS}^2R_{Lr\rm ESR}\right). \tag{31}$$

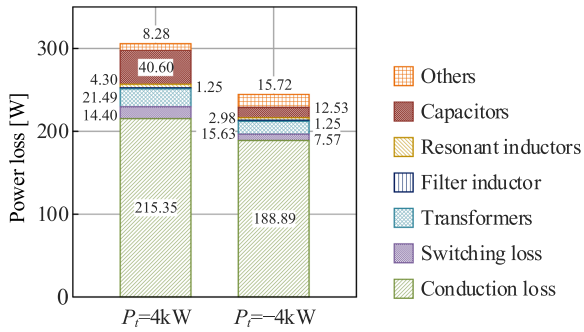

Fig. 19. Power loss breakdown of the experimental prototype.

4). Overall Analysis: According to the aforementioned analysis, the power loss breakdown of the experimental prototype is shown in Fig. 19. According to Fig. 19, the conduction loss is the main part of the total loss. And the total power loss in forward mode ($P_t = 4$ kW) is 305.67 W, which is slightly higher than 244.57 W in backward mode ($P_t = -4$ kW).

VII. Conclusion

This article presents a novel modular multilevel resonant dc/dc converter with QSW modulation to achieve ZCS for the interconnection between LVDC and MVDC buses. With the QSW modulation, the proposed converter operates in DCM mode with a quasi-sinusoidal current wave to achieve low switching loss in forward and backward modes. The output voltage can be regulated with an internal phase-shifted angle of QSW modulation, and ZCS-OFF for LV-side full-bride switches and ZVS-ON ZCS-OFF for switches on the part of MV-side SMs can be realized over the whole power range. Besides, the MV-side concentrated capacitor can be eliminated, and the size of filter inductor can be minimized with the two SM strings series configuration. The operation principle and soft switching characteristic are analyzed in detail with the time-domain method. And experimental results verify the operation principle and the control strategy of the converter.

Appendix

According to (8)−(10), the expression of i_{r1} and v_{Cr1} can be obtained as (A1) and (A2) shown at the bottom of this page, respectively, where ω_r is the resonant angular frequency, $\omega_r = 2\pi f_r$.

Based on (11)−(13), the expression of i_{r1} and v_{Cr1} in half switching period under backward mode can be solved as (A3) shown at the bottom of this page and (A4) shown at the top of next page.

According to (A1) and (A2), the transmission power P_1 in forward mode can be expressed as (A5), where k is defined as $(T_s/2-t_6)/(d_N T_s/2)$.

$$i_{r1}(t) = \begin{cases} \left(i_{r1}(t_0) + C_r\frac{(N-K)V_M}{(N+K)d_N T_s}\right)\cos(\omega_r(t-t_0)) \\ +\left(v_{Cr}(t_0) + nV_L - \frac{V_M}{2}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_0)) - C_r\frac{(N-K)V_M}{(N+K)d_N T_s}, & t_0 \le t < t_2 \\ i_{r1}(t_2)\cos(\omega_r(t-t_2)) + \left(v_{Cr}(t_2) + nV_L - \frac{NV_M}{N+K}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_2)), & t_2 \le t < t_5 \\ \left(i_{r1}(t_5) - C_r\frac{(N-K)V_M}{(N+K)d_N T_s}\right)\cos(\omega_r(t-t_5)) \\ +\left(v_{Cr}(t_5) + nV_L - \frac{NV_M}{N+K}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_5)) + C_r\frac{(N-K)V_M}{(N+K)d_N T_s}, & t_5 \le t < t_6 \\ i_{r1}(t_6), & t_6 \le t < \frac{T_s}{2} \end{cases} \tag{A1}$$

$$v_{Cr1}(t) = \begin{cases} -\left(i_{r1}(t_0) + C_r\frac{(N-K)V_M}{(N+K)d_N T_s}\right)Z_r\sin(\omega_r(t-t_0)) + \left(v_{Cr1}(t_0) + nV_L - \frac{V_M}{2}\right)\cos(\omega_r(t-t_0)) \\ +\frac{(N-K)V_M}{(N+K)d_N T_s}(t-t_0) - nV_L + \frac{V_M}{2}, & t_0 \le t < t_2 \\ -i_{r1}(t_2)Z_r\sin(\omega_r(t-t_2)) + \left(v_{Cr}(t_2) + nV_L - \frac{NV_M}{N+K}\right)\cos(\omega_r(t-t_2)) - nV_L + \frac{NV_M}{N+K}, & t_2 \le t < t_5 \\ -\left(i_{r1}(t_5) - C_r\frac{(N-K)V_M}{(N+K)d_N T_s}\right)Z_r\sin(\omega_r(t-t_5)) + \left(v_{Cr}(t_5) + nV_L - \frac{NV_M}{N+K}\right)\cos(\omega_r(t-t_5)) \\ -\frac{(N-K)V_M}{(N+K)d_N T_s}(t-t_5) - nV_L + \frac{NV_M}{N+K}, & t_5 \le t < t_6 \\ v_{Cr1}(t_6), & t_6 \le t < \frac{T_s}{2} \end{cases} \tag{A2}$$

$$i_{r1}(t) = \begin{cases} i_{r1}(t_0), & t_0 \le t < t_1 \\ \left(i_{r1}(t_1) + C_r\frac{(N-K)V_M}{(N+K)d_N T_s}\right)\cos(\omega_r(t-t_1)) \\ +\left(v_{Cr1}(t_1) - \frac{V_M}{2}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_1)) - C_r\frac{(N-K)V_M}{(N+K)d_N T_s}, & t_1 \le t < t_2 \\ i_{r1}(t_2)\cos(\omega_r(t-t_2)) + \left(v_{Cr1}(t_2) + nV_L - \frac{NV_M}{N+K}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_2)), & t_2 \le t < t_4 \\ \left(i_{r1}(t_4) - C_r\frac{(N-K)V_M}{(N+K)d_N T_s}\right)\cos(\omega_r(t-t_4)) \\ +\left(v_{Cr1}(t_4) + nV_L - \frac{NV_M}{N+K}\right)\frac{1}{Z_r}\sin(\omega_r(t-t_4)) + C_r\frac{(N-K)V_M}{(N+K)d_N T_s}, & t_4 \le t < t_6 \\ i_{r1}(t_6), & t_6 \le t < \frac{T_s}{2} \end{cases} \tag{A3}$$

$$v_{Cr1}(t)=\begin{cases} v_{Cr1}(t_0), & t_0\le t<t_1\\ -\left(i_{r1}(t_1)+C_r\frac{(N-K)V_M}{(N+K)d_NT_s}\right)Z_r\sin(\omega_r(t-t_1))\\ +\left(v_{Cr1}(t_1)-\frac{V_M}{2}\right)\cos(\omega_r(t-t_1))+\frac{(N-K)V_M}{(N+K)d_NT_s}(t-t_1)+\frac{V_M}{2}, & t_1\le t<t_2\\ -i_{r1}(t_2)Z_r\sin(\omega_r(t-t_2))+\left(v_{Cr1}(t_2)+nV_L-\frac{NV_M}{N+K}\right)\cos(\omega_r(t-t_2))-nV_L+\frac{NV_M}{N+K}, & t_2\le t<t_4\\ -\left(i_{r1}(t_4)-C_r\frac{(N-K)V_M}{(N+K)d_NT_s}\right)Z_r\sin(\omega_r(t-t_4))\\ +\left(v_{Cr1}(t_4)+nV_L-\frac{NV_M}{N+K}\right)\cos(\omega_r(t-t_4))-\frac{(N-K)V_M}{(N+K)d_NT_s}(t-t_4)-nV_L+\frac{NV_M}{N+K}, & t_4\le t<t_6\\ v_{Cr1}(t_6), & t_6\le t<\frac{T_s}{2}\end{cases} \tag{A4}$$

$$P_1=\frac{4}{T_s}\int_{t_0}^{t_0+T_s/2}nV_Li_{r1}(t)\,dt$$

$$=\frac{2nV_Lf_s}{Z_rd_N\omega_r(N+K)}\begin{pmatrix}(N+K)(2v_{Cr}(t_0)-V_M+2nV_L)d_N\left(1-\cos\left(\frac{\omega_r}{2f_s}(d_Nk-1)\right)\right)\\ +2(N-K)V_M\frac{f_s}{\omega_r}\left(\sin\left(\frac{\omega_r}{2f_s}(d_N+d_Nk-1)\right)+\sin\left(\frac{\omega_r}{2f_s}(d_Nk-d_N)\right)\right.\\ \left.-\sin\left(\frac{\omega_r}{2f_s}(d_Nk-1)\right)\right)-(N-K)V_Md_Nk\end{pmatrix} \tag{A5}$$

$$P_2=\frac{4}{T_s}\int_{t_0}^{t_0+T_s/2}nV_Li_{r1}(t)\,dt$$

$$=\frac{2nV_Lf_s}{Z_rd_N\omega_r(N+K)}\begin{pmatrix}(N+K)d_N\left((V_M-2v_{Cr}(t_0))\left(\cos\left(\frac{\omega_r}{2f_s}(d_Nk+d_Nk_e-1)\right)-1\right)\right.\\ \left.-2nV_L\left(\cos\left(\frac{\omega_r}{2f_s}(d_N+d_Nk-1)\right)-1\right)\right)\\ -(N-K)V_M\begin{pmatrix}d_Nk-d_Nk_e\cos\left(\frac{\omega_r}{2f_s}(d_N+d_Nk-1)\right)\\ +\frac{2f_s}{\omega_r}\left(\sin\left(\frac{\omega_r}{2f_s}(d_Nk+d_Nk_e-1)\right)-\sin\left(\frac{\omega_r}{2f_s}(d_Nk-d_N)\right)\right.\\ \left.-\sin\left(\frac{\omega_r}{2f_s}(d_N+d_Nk-1)\right)\right)\end{pmatrix}\end{pmatrix}. \tag{A6}$$

When in backward mode, based on (A3) and (A4), the transmission power P_2 can be expressed as in (A6), where $k_e=(t_1-t_0)/(d_NT_s/2)=2nV_L(N+K)/(V_M(N-K))$.

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