Letters

A Novel Interleaved Parallel Cascaded Three-Level PFC With Low Inductance Volt-Second and Low Common-Mode Noise

Junjie Zhang, Yuanbin He, *Member, IEEE*, and Lijun Hang, *Senior Member, IEEE*

***Abstract*—Interleaved parallel cascaded multilevel technology is an attractive approach for converters to achieve high efficiency, high-power density, and high modularity. In this letter, a novel single-phase interleaved parallel cascaded three-level (IPC-TL) power factor correction (PFC) converter is proposed. It is formed by cascading two interleaved parallel totem-pole PFC cells. The proposed topology exhibits the merits of lower inductance volt-second and inductor current ripples, lower common-mode noise, and lower control cost, compared with the traditional IPC-TL topology. A laboratory-scale experimental prototype is developed to verify the effectiveness of the proposed topology.**

***Index Terms*—Common mode (CM), inductor current ripple, interleaved parallel cascaded three-level (IPC-TL) power factor correction (PFC).**

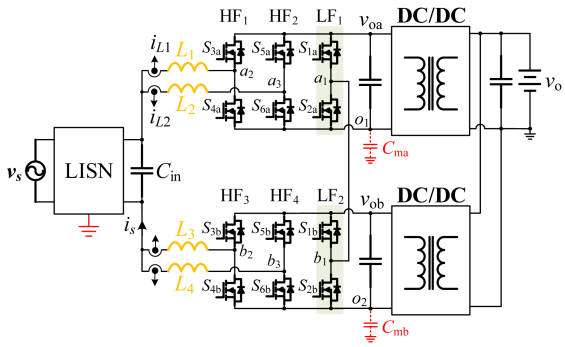

Fig. 1. Traditional IPC-TL PFC with LISN and dc–dc converters.

I. Introduction

TO MEET the demand of ac–dc power converters for high efficiency and high power density, multilevel technology is becoming popular in recent years due to its low switch voltage stress and small passive component size [1], [2], [3]. Recently, with the implementation of flying capacitor multilevel topology and cascaded multilevel topology, the power density of the power factor correction (PFC) stage has been increased to 1000 W/in^3, while achieving a peak efficiency of more than 99% [2], [3]. Among them, cascaded multilevel topology is favored for its higher modularity and scalability.

With the increasing power demand, multilevel technology combing with interleaved parallel technology can handle high current and increase system redundancy. Interleaved operation is known for reducing input and output ripples due to the ripple cancellation effect [4], [5], [6], [7]. For now, the research work on interleaved parallel multilevel converters mainly focuses on clamping multilevel topologies [8], [9], [10] and flying capacitor multilevel topologies [11], [12], [13]. In addition, some literature reported dual three-phase inverters-based open-winding multilevel converters, either powered by a single dc bus or separated dc sources [14], [15], [16], [17]. Due to the particularity of the open-winding configuration, such converter might be difficult to use in other application scenarios. To authors' knowledge, very little attention is paid to the interleaved parallel cascaded (IPC) multilevel converters with higher modularity and scalability.

For IPC multilevel converters, although interleaving operation can greatly reduce overall input and output current ripples, the inductor current ripple will become much larger because of the circulating current between interleaved parallel phases [18]. Recently, Viatkin et al. [19] applied the IPC multilevel technique to the modular multilevel converter (MMC), and employ a hybrid modulation scheme to ensure normal operation of MMC. The hybrid modulation consists of level-shift pulsewidth modulation (PWM) for series connected bridges and phase-shift PWM for parallel bridges, but whether it contributes to the inductor current ripple is not mentioned. Lu et al. [20] discussed the current ripples under different phase-shift modulation strategies for the interleaved parallel cascaded three-level (IPC-TL) dc–dc converter, and employ inverse-coupled inductors to reduce inductor current ripples. Yet, it cannot eliminate the circulating current because of mutual coupling between the interleaved parallel bridges.

By the same token, Fig. 1 presents the traditional IPC-TL PFC, together with line impedance stabilization network (LISN) and dc–dc converters, in which the input series output parallel architecture is common in two-stage ac–dc conversion

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The authors are with the Department of Electrical Engineering and Automation, Hangzhou Dianzi University, Hangzhou 310018, China (e-mail: 947041633@qq.com; yuanbinhe@hdu.edu.cn; lijunhang.hhy@aliyun.com).

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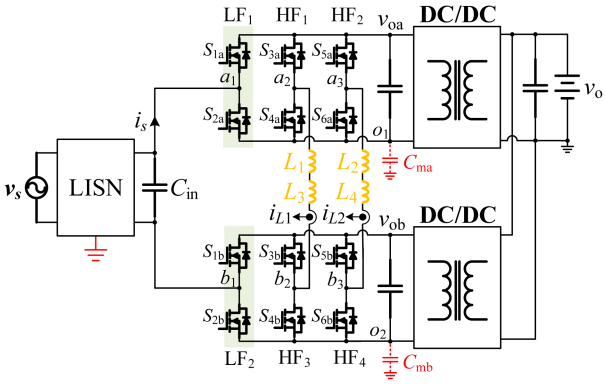

Fig. 2. Proposed IPC-TL PFC with LISN and dc–dc converters.

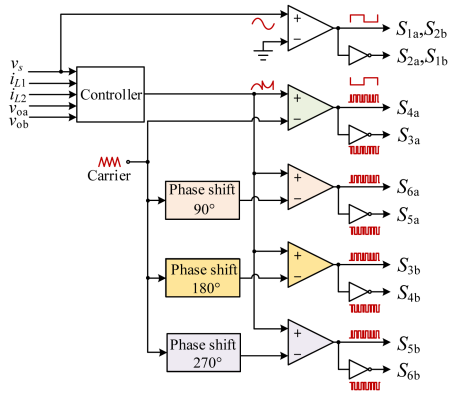

Fig. 3. Phase shift modulation strategy of the proposed PFC.

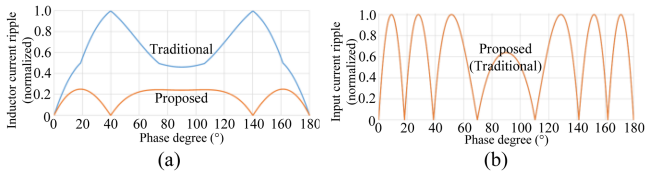

Fig. 4. Current ripples in positive half line-cycle (normalized). (a) Inductor current ripples (normalized). (b) Input current ripples (normalized).

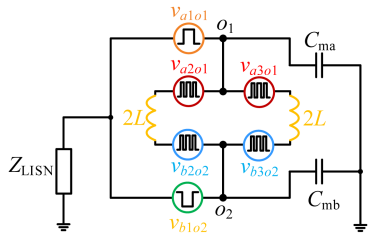

Fig. 5. CM equivalent circuit of the proposed PFC.

systems [21]. The unfolding half bridges LF_1 and LF_2 operate at power frequency, and the input and output current ripples are reduced by performing 90° phase-shift modulation between high-frequency half bridges HF_1–HF_4. However, the traditional IPC-TL PFC has the following main issues.

1) The circulating current occurs between interleaved parallel bridges, resulting in an increase of the inductor volt-second and inductor current ripples [8], [20].
2) High frequency *dv/dt* of interleaved parallel bridges will cause serious common mode (CM) noise [22].

In order to solve the abovementioned problems, this letter will propose a novel IPC-TL PFC. Compared with the traditional topology, it has the following advantages.

1) There is no circulating current between interleaved parallel bridges. Thus, small inductor volt-second and small inductor current ripples are achieved.
2) CM noise sources change at line frequency and will not cause CM noise problems theoretically.
3) The parallel branches are halved. Thus, only two current sensors are used to perform current sharing control.

II. Proposed Solution

A. System Configuration and Operating Principle

Fig. 2 shows the circuit structure of the proposed IPC-TL PFC, together with LISN and dc–dc converters, which is formed by cascading two interleaved parallel totem-pole PFC cells. In Fig. 2, the midpoints of two unfolding half bridges are directly connected to both ends of the ac source, and the midpoints of the high-frequency half bridges in two cells are cascaded with each other through the inductors.

The new topology performs 180° and 90° phase shift modulation for cascaded bridges and parallel bridges, respectively, which is also reported in the traditional IPC-TL dc–dc topology [20]. The specific modulation strategy is shown in Fig. 3. Then, the voltage across the inductor L_1 can be expressed as

$$v_{L_1} = \frac{v_{a_2a_1}}{2} - \frac{v_{b_2b_1}}{2} + \frac{v_s}{2}. \tag{1}$$

Likely, by taking the positive half line-cycle as an example, the voltage across the inductor L_1 in traditional IPC-TL PFC can be written as

$$v_{L_1} = \frac{\sum_{i=2,3} v_{b_io_1} - \sum_{i=2,3} v_{a_io_1}}{4} - \frac{v_{a_2o_1} - v_{a_3o_1}}{2} + \frac{v_s}{2}. \tag{2}$$

It can be seen from (2) that the voltage across one inductor in the traditional topology is related to the voltage mismatch between two phases (i.e., $v_{a_2o_1} - v_{a_3o_1}$), forming the circulating current between phases [20]. In contrast, there is no voltage mismatch between two phases in (1). By substituting (1) and (2) into the corresponding formulas in [20], the comparative inductor current ripples and input current ripples under different topologies are drawn in Fig. 4. It can be seen that the maximal inductor current ripple of the proposed IPC-TL PFC is reduced to nearly one fourth that of the traditional case. In addition, due to the interleaved modulation between two phases, both topologies have the same overall input current ripple, as shown in Fig. 4(b).

B. Common-Mode Analysis

Based on Fig. 2, the CM equivalent circuit is derived, as shown in Fig. 5, wherein C_{ma} and C_{mb} are the dc side parasitic capacitances of two cells, respectively, $L_1 - -L_4$ are equal to L, Z_{LISN} is the equivalent impedance of LISN, and the six pulsating noise sources of v_{a1o1}, v_{b1o2}, v_{a2o1}, v_{a3o1}, v_{b2o2}, and

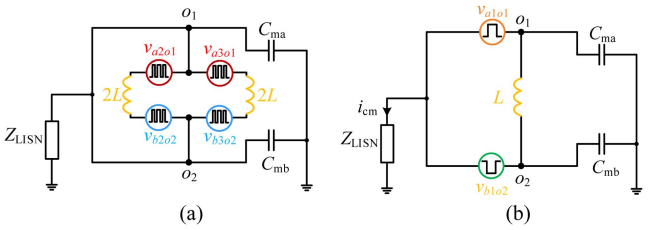

Fig. 6. CM subcircuits of the proposed PFC. (a) Subcircuit I. (b) Subcircuit II.

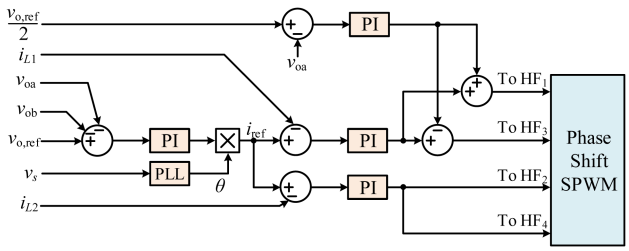

Fig. 7. Control diagram of the proposed PFC.

v_{b3o2} are sequentially generated by two unfolding half bridges LF_1 and LF_2, and four high-frequency bridges HF_1–HF_4. Using the superposition theorem, this equivalent circuit is further decomposed into two CM subcircuits, as shown in Fig. 6. Since the voltages across o_1 and o_2 are clamped to zero in the subcircuit, as shown in Fig. 6(a), high-frequency noise sources do not generate CM currents through the LISN. According to the Kirchhoff's voltage law and Kirchhoff's current law, it deduces that the CM current flowing through the LISN in the subcircuit presented in Fig. 6(b) is

$$i_{\text{cm}} = \frac{s(C_{\text{ma}} \cdot v_{\text{a1o1}} + C_{\text{mb}} \cdot v_{b1o2})}{Z_{\text{LISN}} \cdot s(C_{\text{ma}} + C_{\text{mb}}) + 1}. \tag{3}$$

Since v_{a1o1} and v_{b1o2} are complementary line-frequency signals, $i_{\text{cm}} = 0$ in the above formula when $C_{\text{ma}} = C_{\text{mb}}$. Even with $C_{\text{ma}} \neq C_{\text{mb}}$, the CM current caused by line-frequency signals v_{a1o1} and v_{b1o2} is minor. Therefore, the proposed topology can achieve nearly zero CM current without relying on impedance balance.

C. Control Strategy

The control strategy of the proposed IPC-TL PFC is given in Fig. 7, where the outer voltage loop employs PI controller to regulate the total dc bus voltage, and the output signal of the controller is multiplied by ac voltage phase information obtained through the phase-locked loop to obtain the reference command of the inner current loop. The inner current loop takes charge of balancing two inductor currents. The corresponding modulation indexes are assigned to four high-frequency bridges, respectively. The balancing control of two dc bus voltage is performed by one set of cascaded bridges. The corresponding control principle in the above can refer to [23].

Compared with the traditional IPC-TL PFC, the proposed topology only has two parallel branches, two power inductors, and hereby only needs two current sensors to realize current sharing control. In view of this point, the proposed topology has lower control cost.

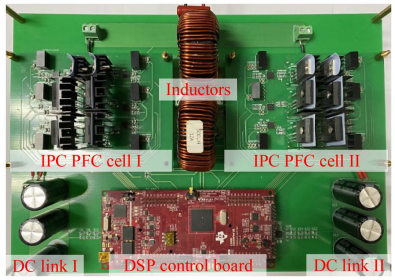

Fig. 8. Experimental prototype photo of the proposed IPC-TL PFC.

TABLE I
SYSTEM PARAMETERS

Parameter	Value
Power inductance	$L_1 = L_2 = L_3 = L_4 = 0.3$ mH
Dc capacitor	$C_{dc} = 680$ uF
Output load	$R = 100\ \Omega$
Switching frequency	50 kHz
Input Ac voltage	220V rms/50 Hz
Output Dc voltage	200 V
Parasitic capacitance	$C_{ma} = 0.5$ nF, $C_{mb} = 0.5$ nF

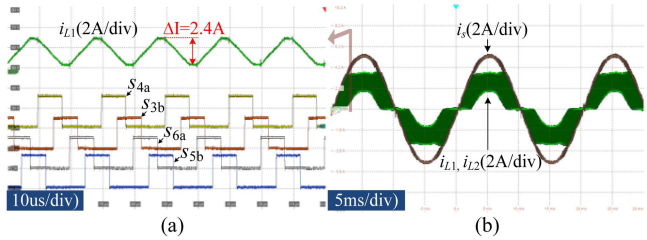

Fig. 9. Waveforms of the traditional topology. (a) Measured inductor current and switching sequences. (b) Measured input current and inductor current.

III. Experimental Results and Discussion

Two lab-scale IPC-TL PFC converters are built in order to demonstrate comparative results. The lab-prototype photo of the proposed topology is given in Fig. 8. The key parameters are tabulated in Table I. For a fair comparison, the same inductance value is chosen based on the input current ripple requirement (i.e., <10% of the rated current) for both topologies. The input side of the converter is connected with the grid, and a resistive load is connected to its output side.

For the traditional IPC-TL topology, in order to ensure that the inductor current ripples in two phases are the same, 180° phase shift modulation for parallel bridges and 90° phase shift modulation for cascaded bridges are employed. The specific switching sequence of four switches and the corresponding intracycle information of the inductor current are presented in Fig. 9(a). As shown in Fig. 9(b), by adopting reasonable control strategies, the inductor current sharing is achieved. Although the input current ripple is very small due to the ripple cancellation effect, the inductor current ripple is still very large. That is because the circulating current between two phases increases the inductor volt-second product.

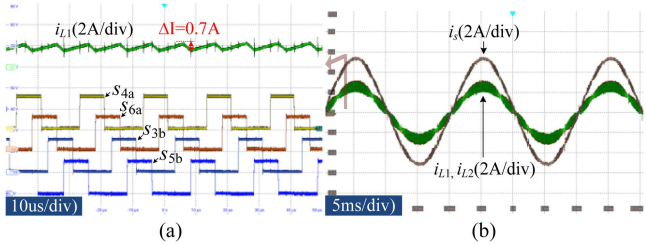

Fig. 10. Waveforms of the proposed topology. (a) Measured inductor current and switching sequences. (b) Measured grid current and inductor current.

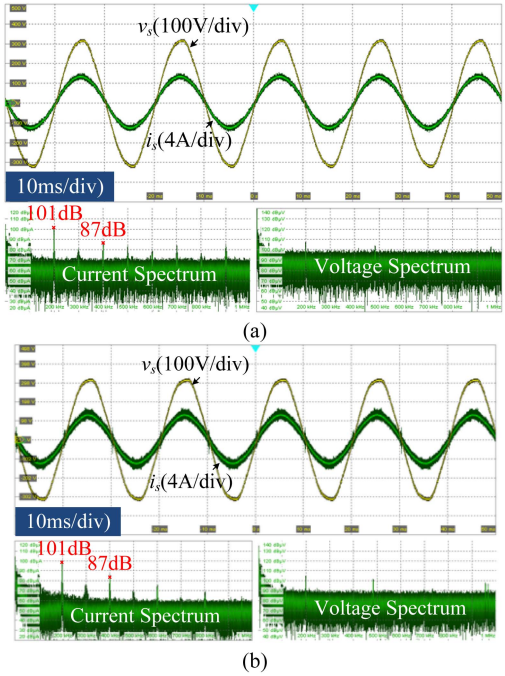

Fig. 11. Spectrum of the input current and voltage. (a) Traditional topology. (b) Proposed topology.

For the proposed IPC-TL topology, by employing the phase shift modulation strategy, as shown in Fig. 3, the switching sequence of four switches and the corresponding intracycle information of the inductor current are presented in Fig. 10(a). Because the interleaved parallel bridges are decoupled, the inductor current ripple is only determined by the cascaded bridges. Therefore, both small input current ripple and small inductor current ripple are achieved, as presented in Fig. 10(b).

Fig. 11 presents the spectrum of the overall input current and the voltage across C_{in} for both topologies. It can be seen that the amplitude of main current ripple at 200 kHz and 400 kHz is the same, which matches with the theoretical analysis in Fig. 4(b).

CM noise measurement has been conducted using LISN equipment without CM filter and the spectrum results are shown in Fig. 12. Two capacitors with capacitance of 500 pF are placed between each dc bus and ground to simulate parasitic capacitances in the latter dc–dc converters. Compared with traditional IPC-TL topology, the proposed topology reduces CM noise amplitude by up to 45 dBμV. Thus, the proposed topology will require smaller value and size of CM filters. Since the design of CM filters is beyond the scope of this brief, no experimental

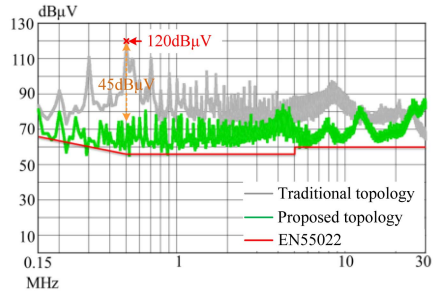

Fig. 12. Measured noise spectrum comparison of traditional and proposed IPC-TL topology without CM filters.

results regarding the CM noise suppression with CM filters are given in this section.

IV. Conclusion

A new IPC-TL topology to reduce the inductance volt-second and inductor current ripples, CM noise, and system cost is presented. Unlike conventional IPC-TL PFC topology that causes serious CM noise and circulating current between interleaved parallel phases, the proposed IPC-TL PFC topology cascades two interleaved parallel totem-pole PFC cells and decouples the interleaved parallel bridges. The decoupled parallel bridges significantly reduce inductor current ripples by eliminating the circulating current. Two cascaded totem-pole structures suppress CM noise without replying the impedance balance. The number of parallel branches and inductors are halved. Measurement results from an experimental PFC converter demonstrated the effects of the proposed IPC-TL topology.

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