A Modulation Scheme With Full Range ZVS and Natural Power Factor Correction for Bridgeless Single-Stage Isolated AC–DC Converter

Yun Zhang, *Senior Member, IEEE*, Gen Yang, Jing Li, *Member, IEEE*,
Zhiguo Kong, and Xinshan Zhu, *Member, IEEE*

***Abstract*—The ac side structure of a bridgeless single-stage isolated ac–dc converter reduces the number of components by sharing power switches between the bridgeless rectifier and the dual-active-bridge (DAB) dc–dc converter. However, it also makes it more difficult to achieve zero-voltage switching (ZVS) for the ac side switches. Therefore, a modulation scheme is proposed to achieve ZVS for all switches over the full ranges of the grid voltage and load. A quasi-fixed switching frequency control method is also applied, in which the switching frequency is constant during a half-cycle of the grid voltage. By adjusting the switching frequency, the grid side inductor can operate in critical conduction mode without a zero-current-detection circuit, which facilitates the ZVS realization of the ac side switches. In addition, a natural power factor correction can be realized without the grid-side current sensors. Finally, a 500 W prototype was built to validate the theoretical analysis and the effectiveness of the proposed modulation scheme.**

***Index Terms*—AC–DC converter, dual active bridge (DAB), power factor correction (PFC), zero-voltage switching (ZVS).**

I. Introduction

AC–DC converters with the power factor correction (PFC) are widely used in many applications, such as data-center power supplies, chargers for electric vehicles, energy storage systems, and dc distribution systems. When galvanic isolation and/or high voltage conversion ratio are required, the conventional approach is a two-stage solution with a PFC rectifier and a subsequent isolated dc–dc converter [1], [2]. However, the efficiency of the conventional solution is limited due to the two-stage power conversion. A large number of components and the complex control loops increase the complexity and cost of the system. The large-capacity electrolytic capacitor generally used as a dc-link capacitor to buffer energy between the two stages affects the system reliability and the power density [3].

Several single-stage isolated ac–dc converter topologies have been proposed to overcome the aforementioned drawbacks. A quasi-single-stage isolated ac–dc converter consisting of a diode bridge or synchronous rectifier followed by an isolated dc–dc converter with a wide voltage gain range was proposed in [4]–[7]. The rectified voltage is directly fed to the input of the dc–dc converter, which can reduce the number of high-frequency (HF) switches and, thus, reduce the switching loss. However, the conduction loss on the rectifier bridge still limits the efficiency. If the synchronous rectifier is integrated into the primary side of the dc–dc converter by employing bidirectional switches, a real single-stage power conversion can be realized [8], [9]. However, the number of switches and gate drivers is not reduced. The synchronous rectifier switches cannot be replaced with regular Si MOSFETS, because each switch operates with a high frequency in a certain half-period of the grid voltage. The converter proposed in [10]–[13] adopts a bridgeless structure on the ac side. Thus, the conduction loss and the number of switches is reduced due to the absence of the rectifier bridge.

The aforementioned single-stage isolated ac–dc converters reduce the number of switches and power conversion stages, which improve the efficiency and the power density. The power fluctuation at double line frequency is buffered by the large output capacitor at the dc side (if the load on the dc side is a battery, the power fluctuation is absorbed by the battery, which is named as sinusoidal charging in [14]), instead of the dc-link capacitor. Then, the dc-link capacitor can be replaced by a film capacitor with a small capacitance, across which the voltage is usually with a sine wave or a rectified sine wave. This causes the single-stage converters to operate usually over an extremely wide voltage gain range. Thus, research on the single-stage isolated ac–dc converters mainly has been focusing on improved modulation schemes, which increase the converter efficiency over the whole range of voltage and load conditions.

The modulation schemes have been widely studied in dual-active-bridge (DAB) dc–dc converters [15] and are further

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Yun Zhang, Gen Yang, and Xinshan Zhu are with the School of Electrical and Information Engineering, and also with the National Industry-Education Platform of Energy Storage, Tianjin University, Tianjin 300072, China (e-mail: zhangy@tju.edu.cn; yanggen@tju.edu.cn; xszhu@tju.edu.cn).

Jing Li is with the Key Laboratory of More Electric Aircraft Technology of Zhejiang Province, University of Nottingham Ningbo China, Ningbo 315100, China (e-mail: jing.li@nottingham.edu.cn).

Zhiguo Kong is with the China Automotive Technology and Research Center Company, Ltd., Tianjin 300300, China (e-mail: kongzhiguo@catarc.ac.cn).

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improved in single-stage ac–dc converters to accommodate the ultrawide voltage-gain range. The high-voltage conversion ratio generally occurs around the zero crossing of the grid voltage. To maintain zero-voltage switching (ZVS) and reduce the current stress in this region, the variable frequency control can be used [5], [8]. But the calculation of the switching frequency and the phase shift angle are coupled with each other, which makes the control laws complex or even without analytical solutions. Sometimes a lookup table is needed to implement the complex modulation scheme, which can be complicated to realize in practice. In [16], a fixed-switching-frequency triple-phase-shift (TPS) control is used at the light load (around the zero crossing of the grid voltage) condition to reduce complexity, however, the transformer peak current and the rms current are increased. Besides, the step change of the phase shift angle between the TPS and dual-phase-shift control may cause an oscillatory transient in the grid current [17]. The modulation scheme proposed in [18] has only one operating mode, so no transitions between multiple operating modes are required, and the calculation of the control variables is relatively simple, but the dc side switches may lose ZVS as the load increases.

Typically, to achieve PFC, the grid-side current needs to be sampled for the current control. However, the nonlinear relationship between the control variables and the grid-side current makes the current controller design complicated and may cause high total harmonic distortion (THD). In [11] and [12], the phase-shift angle is directly output by the PI controller, without considering the nonlinear relationship between the phase shift angle and the grid current. To obtain a better control performance, a variable frequency control can be adopted to convert the nonlinearity of the phase shift angle into a linear function [19], but a PI controller and a grid-side current sensor are still required. It has been found that DAB-based single-stage ac–dc converters can realize natural PFC without the grid-side current loop and the current sensor [9], [20], [21], which simplifies the controller design and reduces the cost of the system. The natural PFC control usually requires closed-form solutions of all control variables, which limits the use of complex modulation schemes employed in DAB. A modulation scheme based on the inner mode has a linear power relationship inherently but results in a high transformer peak current [9]. In [20], continuous conduction mode mode is used to reduce the current stress. However, the converter operates in discontinuous conduction mode (DCM) when the grid voltage is low or under light load conditions, where the phase drift phenomenon is prone to cause hard switching [22]. The modulation scheme in [21] combines the inner and outer modes, optimizes the transformer current stress, and obtains a wider ZVS range.

For the bridgeless topology, the ac side switch current is the sum of two inductor currents, so the realization of ZVS is more difficult. A minimum average current modulation scheme is proposed in [10] to reduce the conduction loss. But the modulation scheme is not suitable for HF applications, because the soft-switching conditions are not considered. The control variables are step changed at the boundaries of adjacent operating regions, which will cause output voltage oscillation (ac-to-dc operation). The soft switching condition for the bridgeless topology is studied in [11]. The tradeoff between the switching and conduction loss is considered when designing the grid-side inductors.

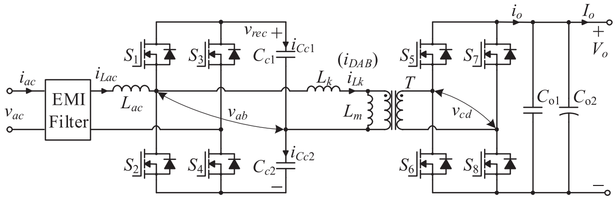


Fig. 1. Topology of the single-stage ac–dc converter.

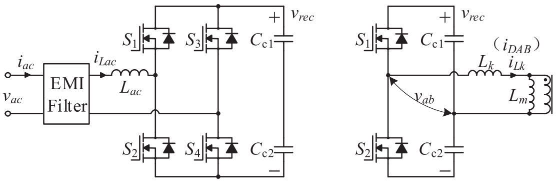
In summary, it is difficult to maintain ZVS and optimize the transformer current over the whole range of grid voltage, especially when a bridgeless structure is used on the ac side. Moreover, the natural PFC control and real-time calculation requirements limit the use of complex modulation schemes. To solve these problems, a modulation scheme for a bridgeless single-stage isolated ac–dc converter is proposed to achieve ZVS over the full ranges of the grid voltage and the load. Two operating modes and three control variables including the dc side duty cycle D_2, the outer phase-shift ratio φ, and the switching frequency f_s are used in the modulation scheme. All control variables have closed-form solutions, so real-time calculation and natural PFC control can be realized. The trajectories of all control variables are continuous without step changes, so a seamless transition between the two operating modes can be achieved. By adjusting the switching frequency, the grid side inductor can operate in critical conduction mode (CRM) without a zero-current-detection (ZCD) circuit. The switching frequency is constant during a half-cycle of the grid voltage (namely a quasi-fixed switching frequency control). The reactive power consumed by C_{c1} and C_{c2} is compensated to improve the power factor of the converter.

This article is further organized as follows. In Section II, the topology and operating principle of the bridgeless single-stage ac–dc converter are explained. In Section III, the proposed modulation scheme is clarified in detail, including the ZVS conditions analysis and the implementation of the natural PFC control. Section IV shows the experimental results and analysis. Special attention is paid to the ZVS realization at different moments in the grid voltage under different load conditions. Finally, Section V concludes this article.

II. TOPOLOGY AND OPERATION PRINCIPLE

A. Topology

The topology of the single-stage ac–dc converter is illustrated in Fig. 1. The dc side of the converter is a full-bridge. The filter capacitor C_{o1} bypasses the HF components of i_o. An electrolytic capacitor C_{o2} is placed at the dc side to filter the double line frequency power component due to the absence of the dc-link capacitor. The ac side of the converter can be decomposed into the following two parts: a full-bridge rectifier shown in Fig. 2(a) and a half-bridge shown in Fig. 2(b). They share switches S_1 and S_2 to reduce the count of the power devices. v_{ac} and i_{ac} are the grid voltage and current, respectively. S_1 and S_2 operate at the



(a) (b)

Fig. 2. Topology breakdown of the ac side. (a) Full-bridge rectifier. (b) Half-bridge, the primary side of the DAB converter.

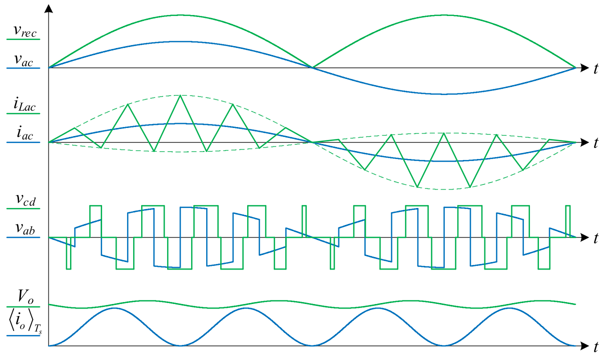


Fig. 3. Typical operating waveforms.

high frequency, while S_3 and S_4 just operate at the line frequency for the synchronous rectification. L_{ac} is the grid-side inductor with a relatively small inductance. Thus, an electromagnetic interference (EMI) filter is essential for eliminating the HF components in i_{Lac}. C_{c1} and C_{c2} are clamping capacitors with low capacitance and low parasitic resistance, which are not used for energy storage. The half-bridge shown in Fig. 2(b) constructs a DAB converter with the full-bridge on the dc side. The ac and the dc sides are connected by an HF transformer *T*, whose turns ratio is *n*:1. The transformer magnetizing inductance and the leakage inductance are denoted by L_k and L_m, respectively. i_{Lk} is the transformer leakage inductance current, and its average value in a half-switching cycle is i_{DAB}.

B. Operation Principle

Fig. 3 shows the typical operating waveforms of the converter. On the ac side, S_1 and S_2 are switched complementarily at high frequency with a fixed 50% duty ratio. S_3 and S_4 operate at the line frequency. When v_{ac} is positive, S_4 is turned ON and S_3 is turned OFF. Conversely, when v_{ac} is negative, S_3 is turned ON and S_4 is turned OFF. As a result, the grid voltage can be rectified into a dc voltage v_{rec} pulsating at twice the ac line frequency. The amplitude of v_{ac} and i_{ac} are V_{ac} and I_{ac}, respectively. Due to the 50% duty ratios of S_1 and S_2, the amplitude of v_{rec} is $2V_{\text{ac}}$. S_1 and S_2 also yield an HF two-level square wave v_{ab} with a 50% duty ratio, whose amplitude is V_{ac}. L_{ac} operates in CRM to achieve the ZVS of S_1 and S_2. Note that the ZCD circuit is not required for the CRM operation, but only to control the switching frequency (will be further clarified in Section III). On the dc side, the cross-connected switch pairs of the full-bridge are operated with an inner phase-shift ratio. Then, the output ac voltage of the full-bridge is a three-level waveform v_{cd}. If the reactive (capacitive) power consumed by C_{c1} and C_{c2} is ignored, i_{ac} is equal to i_{DAB}. Therefore, the grid current can be controlled directly by controlling i_{DAB}, which means that the PFC can be realized by the DAB converter.

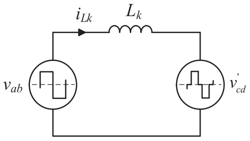


Fig. 4. Simplified (lossless), primary-side referred equivalent circuit.

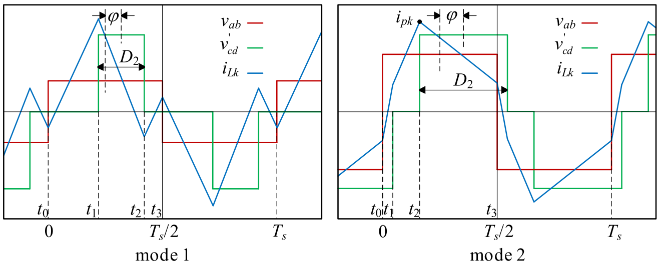


Fig. 5. Operating modes.

The converter is based on the DAB converter. Under the assumption of ideal components, a simplified electrical representation of the DAB is shown in Fig. 4. The primary side referred voltage v'_{cd} is given by $v'_{\text{cd}} = nv_{\text{cd}}$. The transformer magnetizing inductance L_m is assumed to be much larger than the leakage inductance L_k and is neglected in the following.

III. Proposed Modulation Scheme With Full Range ZVS and Natural PFC

A. Operating Modes

The voltage conversion ratio *m* is defined in (1). It will be limited when the grid voltage is close to zero

$$m = \frac{2nV_o}{v_{\text{rec}}} = \frac{nV_o}{|v_{\text{ac}}|}. \tag{1}$$

Since v_{ab} is a two-level waveform, the modulation scheme is based on extended-phase-shift modulation, and the inner phase-shift ratio can only be added to the dc side H-bridge [23]. The converter must operate under the condition $m > 1$ to achieve full-load range ZVS, so only two operating modes shown in Fig. 5 are selected, where D_2 represents the duty cycle of v_{cd}, and φ represents the outer phase-shift ratio. Mode 1 is suitable for large *m* or low-power conditions. As the power increases or *m* decreases, mode 1 will transition to mode 2 seamlessly.

The current is normalized to obtain generalized characteristics. The base value of the current is given by the following equation:

$$I_{\text{base}} = \frac{V_o T_s}{4L_k}. \tag{2}$$

The normalized inductor current at different moments in mode 1 is shown in the following equation:

$$\begin{cases} i^*_{\mathrm{Lk}}(t_0) = \frac{mD_2-1}{m} \\ i^*_{\mathrm{Lk}}(t_1) = \frac{(m-1)D_2+2\varphi}{m} \\ i^*_{\mathrm{Lk}}(t_2) = \frac{(1-m)D_2+2\varphi}{m} \\ i^*_{\mathrm{Lk}}(t_3) = -i^*_{\mathrm{Lk}}(t_0) \end{cases}. \tag{3}$$

Then, the normalized average inductor current over a half-switching cycle on the ac side, i^*_{DAB}, can be calculated by the following equation:

$$i^*_{\mathrm{DAB}} = \frac{2}{T_s}\int_{t_0}^{t_3} i^*_{L_k}(t)dt = 2D_2\varphi. \tag{4}$$

Similarly, for mode 2, the normalized inductor current at different moments and the average inductor current i^*_{DAB} can also be obtained as follows:

$$\begin{cases} i^*_{\mathrm{Lk}}(t_0) = \frac{m(1-2\varphi)-1}{m} \\ i^*_{\mathrm{Lk}}(t_1) = \frac{(m+1)D_2+2\varphi-2}{m} \\ i^*_{\mathrm{Lk}}(t_2) = \frac{(m-1)D_2+2\varphi}{m} \\ i^*_{\mathrm{Lk}}(t_3) = -i^*_{\mathrm{Lk}}(t_0) \end{cases} \tag{5}$$

$$i^*_{\mathrm{DAB}} = \frac{2}{T_s}\int_{t_0}^{t_3} i^*_{L_k}(t)dt = -\frac{D_2^2}{2} + D_2 - 2\left(\varphi - \frac{1}{2}\right)^2. \tag{6}$$

It can be seen from (4) and (6) that i^*_{DAB} can be controlled by D_2 and φ, which is the basis of the natural PFC control.

B. ZVS Analysis of S_1 and S_2

To realize ZVS, the inductor currents have to be large enough to charge/discharge the drain–source capacitances of the power switches in a bridge leg. The required minimum current I_{ZVS} can be calculated roughly as

$$I_{\mathrm{ZVS}} \geq V\sqrt{\frac{2C_{\mathrm{oss.eq}}}{L}} \tag{7}$$

where V is the voltage stress across the power switch, $C_{\mathrm{oss.eq}}$ is the equivalent drain–source capacitance, and L is the inductance involved in commutation [24]. If the parasitic capacitance of switches can only be partly charged/discharged before turning ON, only a quasi-ZVS can be achieved, which is still much better than fully hard switching. Assuming $L = 150\ \mu$H, the relationship between I_{ZVS} and V can be calculated and plotted in Fig. 6. The relationship between $C_{\mathrm{oss.eq}}$ and V is obtained from the MOSFET datasheet [25]. It can be seen from Fig. 6 that I_{ZVS} is approximately proportional to the voltage stress.

For the bridgeless topology, the ac side switch current is the sum of the two inductor currents, so the ZVS realization of S_1 and S_2 is more difficult. The ZVS conditions of S_1 and S_2 are analyzed only in the positive half-cycle of v_{ac}, and the analysis in the negative half-cycle is similar.

Fig. 7 shows the waveforms of $i_{L\mathrm{ac}}$, i_{Lk}, and the currents in S_1 and S_2 (i_{S1} and i_{S2}) during the positive half-cycle of v_{ac}. The current $i_{L\mathrm{ac}}$ at different moments is shown in the following equation:

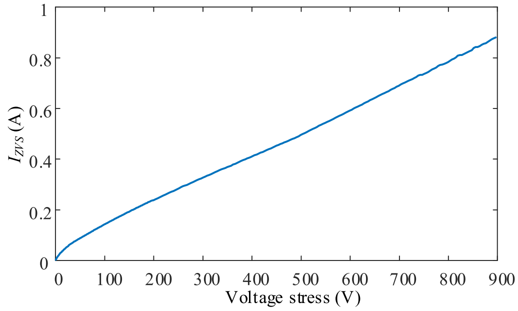


Fig. 6. I_{ZVS} versus the voltage stress of the MOSFETS.

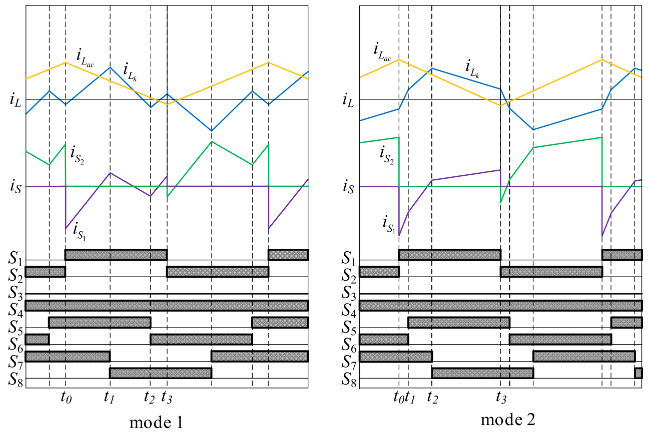


Fig. 7. Key waveforms to illustrate the ZVS characteristic during the positive half-cycle of v_{ac}.

$$\begin{cases} i_{L\mathrm{ac}}(t_0) = i_{\mathrm{ac}} + \frac{v_{\mathrm{ac}}T_s}{4L_{\mathrm{ac}}} \\ i_{L\mathrm{ac}}(t_3) = i_{\mathrm{ac}} - \frac{v_{\mathrm{ac}}T_s}{4L_{\mathrm{ac}}} \end{cases}. \tag{8}$$

The ZVS constraints of S_1 and S_2 are shown in (9). Note that $i_{\mathrm{Lk}}\ (t_0) = \ -i_{\mathrm{Lk}}(t_3)$, then $i_{S1}(t_0) - i_{S2}\ (t_3) = -[i_{L\mathrm{ac}}(t_0) + i_{L\mathrm{ac}}(t_3)] < 0$, so only the second constraint in (9) needs to be satisfied, which means if S_2 can achieve ZVS, then S_1 can also achieve ZVS

$$\begin{cases} i_{S_1}(t_0) = i_{\mathrm{Lk}}(t_0) - i_{L\mathrm{ac}}(t_0) < -i_{\mathrm{ZVS1}} \\ i_{S_2}(t_3) = i_{L\mathrm{ac}}(t_3) - i_{\mathrm{Lk}}(t_3) < -i_{\mathrm{ZVS1}} \end{cases}$$
$$\text{for mode 1 and mode 2.} \tag{9}$$

It can be seen from (9) that both $i_{L\mathrm{ac}}$ and i_{Lk} can provide the commutation current required by S_1 and S_2. If both $i_{L\mathrm{ac}}$ and i_{Lk} are considered, the expressions of φ and D_2 will be complicated. To simplify the analysis, the required commutation currents of S_1 and S_2 are all provided by $i_{L\mathrm{ac}}$. Then, the second constraint in (9) can be transformed into the following equation:

$$\begin{cases} i_{\mathrm{Lk}}(t_3) = 0 \\ i_{L\mathrm{ac}}(t_3) < -i_{\mathrm{ZVS1}} \end{cases} \tag{10}$$

$i_{L\mathrm{ac}}(t_3) < -i_{\mathrm{ZVS1}}$ is fulfilled by controlling the switching frequency f_s, which will be clarified in detail later. Now, for mode 1, φ, and D_2 can be solved by two equations in the following equation:

$$\begin{cases} i^*_{\mathrm{Lk}}(t_3) = 0 \\ i^*_{\mathrm{DAB}} = i^*_{\mathrm{ref}} \end{cases}. \tag{11}$$

The corresponding solutions are shown as follows:

$$\begin{cases} \varphi = \frac{m i^*_{\mathrm{ref}}}{2} \\ D_2 = \frac{1}{m} \end{cases}. \tag{12}$$

For mode 2, if the constraint $i_{\mathrm{Lk}}\ (t_3) = \ 0$ is still applied, there will be a large inductor peak current, and in some cases, there are no solutions of φ and D_2. Therefore, a minimum inductor peak current modulation scheme is adopted in mode 2, which not only satisfies the second constraint in (9), but also optimizes the inductor peak current. Since $m > 1$ is always satisfied, the peak current in mode 2 always appears at t_2. Then, D_2 and φ can be obtained by solving the optimization problem as shown in the following equation:

$$\begin{cases} \min\ \ i^*_{\mathrm{Lk}}(t_2) \\ \text{s.t.}\ \ i^*_{\mathrm{DAB}} = i^*_{\mathrm{ref}} \end{cases}. \tag{13}$$

The corresponding solutions can be shown as follows:

$$\begin{cases} \varphi = \frac{1}{2} - \frac{\sqrt{\frac{-2i^*_{\mathrm{ref}}+1}{m^2-2m+2}}}{2} \\ D_2 = 1 - \sqrt{-4\varphi^2 + 4\varphi - 2i^*_{\mathrm{ref}}} \end{cases}. \tag{14}$$

From Fig. 5, the transition between two modes occurs when $D_2 = \ 1 - \varphi$. Substituting it into (12) or (14), the same mode transition condition can be obtained as shown in the following equation:

$$i^*_{\mathrm{ref}} = \frac{m-1}{m^2}. \tag{15}$$

By substituting (14) into (5), the expression of $i_{\mathrm{Lk}}(t_3)$ can be obtained as follows:

$$i^*_{\mathrm{Lk}}(t_3) = \frac{1}{m} - \sqrt{\frac{1-2i^*_{\mathrm{ref}}}{m^2-2m+2}}. \tag{16}$$

Since $(m-1)/m^2 < i^*_{\mathrm{ref}} < 0$, and $m > 1$ in mode 2, it can be proved that $i^*_{\mathrm{Lk}}(t_3) > 0$, indicating that i_{Lk} can also provide commutation current in mode 2. If $i_{L\mathrm{ac}}$ has provided enough commutation current ($i_{L\mathrm{ac}}(t_3) < -i_{\mathrm{ZVS1}}$), then the second constraint in (9) is satisfied.

The second constraint in (10), $i_{L\mathrm{ac}}(t_3) < -i_{\mathrm{ZVS1}}$, is realized by controlling the switching frequency f_s to make L_{ac} work in CRM. Since the voltage stress across S_1 and S_2 is v_{rec}, whose waveform is a rectified sine wave, so the minimum commutation current required for the ZVS of S_1 and S_2 also varies. Assuming that i_{ZVS1} is the minimum commutation current required by S_1 and S_2, then i_{ZVS1} is approximately proportional to v_{rec} and can be written as (17), where I_{ZVS1} is the required minimum commutation current when v_{rec} reaches its peak (when $\omega t = \pi/2$)

$$i_{\mathrm{ZVS1}} = I_{\mathrm{ZVS1}}\,|\sin(\omega t)|\,. \tag{17}$$

Meanwhile, the expression of $i_{L\mathrm{ac}}(t_3)$ in (8) can be written as:

$$i_{L\mathrm{ac}}(t_3) = i_{\mathrm{ac}} - \frac{v_{\mathrm{ac}}T_s}{4L_{\mathrm{ac}}} = \left(I_{\mathrm{ac}} - \frac{V_{\mathrm{ac}}T_s}{4L_{\mathrm{ac}}}\right)|\sin(\omega t)|\,. \tag{18}$$

Let $i_{L\mathrm{ac}}\ (t_3) = \ -i_{\mathrm{ZVS1}}$, (19) can be obtained as follows:

$$I_{\mathrm{ac}} - \frac{V_{\mathrm{ac}}T_s}{4L_{\mathrm{ac}}} = -I_{\mathrm{ZVS1}}. \tag{19}$$

From (19), to satisfy the ZVS condition in the entire half-cycle of v_{ac}, it is only necessary to satisfy the ZVS condition at the moment $\omega t = \pi/2$. If V_{ac} and I_{ac} have fixed values, then T_s can be controlled to satisfy (19), while T_s is constant in half a cycle.

In summary, the modulation scheme adopted in mode 1 and mode 2 can realize ZVS of S_2. If S_2 can achieve ZVS, then S_1 can also achieve ZVS.

C. ZVS Analysis of S_5–S_8

The ZVS analysis of S_5–S_8 is the same as that in DAB topology. The following analysis will prove that the solutions in (12) and (14) can at least realize the quasi-ZVS of S_5–S_8.

The ZVS constraints of S_5–S_8 are shown in (20), where I_{ZVS2} is the minimum commutation current of the secondary side switches to achieve ZVS

$$\begin{cases} i_{\mathrm{Lk}}(t_1) > I_{\mathrm{ZVS2}} \\ -i_{\mathrm{Lk}}(t_2) > I_{\mathrm{ZVS2}} \end{cases} \text{for mode 1,}$$

$$\begin{cases} i_{\mathrm{Lk}}(t_1) > I_{\mathrm{ZVS2}} \\ i_{\mathrm{Lk}}(t_2) > I_{\mathrm{ZVS2}} \end{cases} \text{for mode 2.} \tag{20}$$

For mode 1, substituting (12) into (3), (21) can be obtained as follows:

$$\begin{cases} i^*_{\mathrm{Lk}}(t_1) = \frac{m^2 i^*_{\mathrm{ref}}+m-1}{m^2} \\ -i^*_{\mathrm{Lk}}(t_2) = \frac{-m^2 i^*_{\mathrm{ref}}+m-1}{m^2} \end{cases}. \tag{21}$$

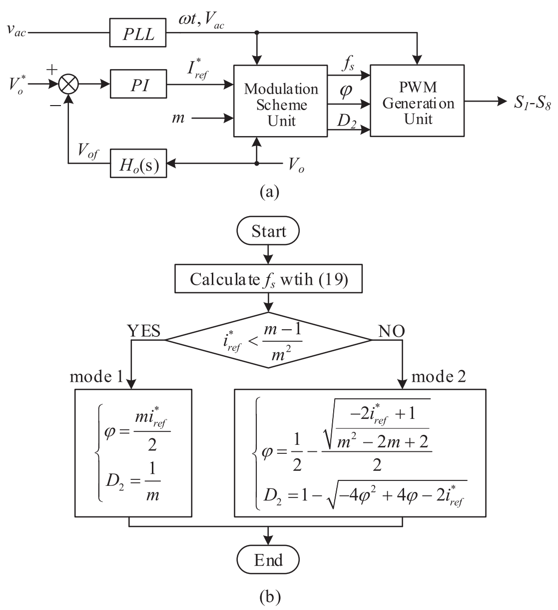
It can be proved that when $0 < i^*_{\mathrm{ref}} < (m-1)/m^2$ and $m > 1$, then $i^*_{\mathrm{Lk}}(t_1) > -i^*_{\mathrm{Lk}}(t_2) > 0$, indicating that S_5–S_8 can at least achieve quasi-ZVS, and if S_5 can achieve ZVS, then S_6–S_8 can also achieve ZVS in mode 1.

For mode 2, substituting (14) into (5), (22) can be obtained as follows:

$$\begin{cases} i^*_{\mathrm{Lk}}(t_1) = 1 - m\sqrt{\frac{1-2i^*_{\mathrm{ref}}}{m^2-2m+2}} \\ i^*_{\mathrm{Lk}}(t_2) = 1 - \frac{m^2-2m+2}{m}\sqrt{\frac{1-2i^*_{\mathrm{ref}}}{m^2-2m+2}} \end{cases}. \tag{22}$$

It can be proved that when $(m-1)/m^2 < i^*_{\mathrm{ref}} < 0.5$ and $m > 1$, then $i^*_{\mathrm{Lk}}(t_2) > i^*_{\mathrm{Lk}}(t_1) > 0$, indicating that the modulation scheme used in mode 2 can obtain at least quasi-ZVS of S_5–S_8. Meanwhile, if S_5 can achieve ZVS, then S_6–S_8 can also guarantee ZVS in mode 2.

In summary, the modulation scheme adopted in mode 1 and mode 2 can at least realize quasi-ZVS of S_5–S_8. If S_5 can achieve ZVS, then S_6–S_8 can also obtain ZVS. Note that the quasi-ZVS only occurs near the zero crossing of the grid voltage and a very small interval near the mode transition point, which has little effect on the efficiency.



(a)

(b)

Fig. 8. Control block diagram of the converter. (a) Closed-loop control diagram. (b) Flow chart of the modulation scheme unit.

D. Natural PFC Realization

In Section II-A, the closed-form solutions of D_2 and φ have been obtained. D_2 and φ are obtained by calculation instead of the output of the voltage loop. The output of the voltage loop does not vary with the phase angle of v_{ac}. Therefore, the natural PFC can be realized.

Fig. 8 shows the control block diagram and the flow chart of the modulation scheme unit. Assuming that a unit power factor is achieved and the reactive (capacitive) power consumed by C_{c1} and C_{c2} is ignored, the current reference i_{ref}^* can be expressed as (23), where I_{ref}^* is the amplitude of the grid current obtained from the output of the voltage loop

$$i_{\mathrm{ref}}^* = I_{\mathrm{ref}}^* \left|\sin(\omega t)\right| . \tag{23}$$

T_s is calculated with (19). After that, φ and D_2 are calculated according to (12) and (14), then the DAB can be controlled as a current source to realize PFC. H_o(s) is a notch filter to reduce ripples of the double line frequency in the output voltage feedback path. Fig. 9 shows the curves of φ, D_2, the voltage conversion ratio m, and the current reference i_{ref}^* in a half-grid period. There are no step changes in the curves, so a seamless transition between the two operating modes can be achieved.

According to (19), the relationship between f_s and the amplitude of i_{ac} can be obtained, as shown in Fig. 10(a). When I_{ac} decreases, the switching frequency f_s will increase. When i_{ac} is small, continuing to increase f_s will reduce the current ripple of $i_{L\mathrm{ac}}$ and thereby the conduction loss and core loss, but the switching loss will become large. As a tradeoff, the upper limit of f_s is set to 100 kHz in this article. It can be seen from Fig. 10(b) that the switching frequency f_s is fixed within a half-grid period but varies with the amplitude of i_{ac}.

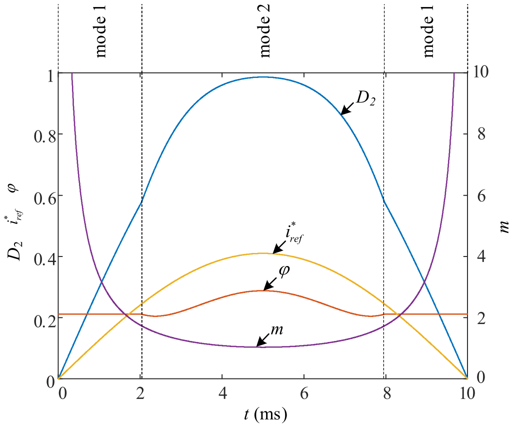
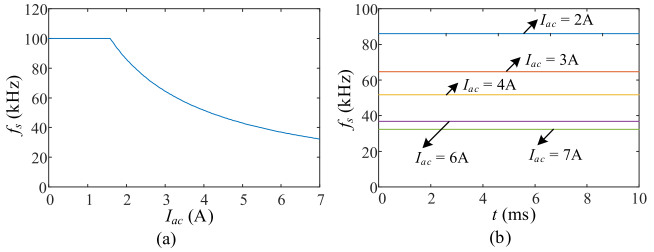


Fig. 9. Control variables over a half-cycle of v_{ac}.



(a)

(b)

Fig. 10. Switching frequency curves, $V_{\mathrm{ac}} = 155$ V, $L_{\mathrm{ac}} = 150$ μH, and $I_{\mathrm{ZVS1}} = 1$ A. (a) Relationship between f_s and I_{ac}. (b) Switching frequency curves in a half-cycle of v_{ac}.

E. Reactive Power Compensation Method

C_{c1} and C_{c2} will draw a small reactive current from the grid because the voltages on them are rectified sine waves. Therefore, the power factor of the converter will be reduced especially at light load. In order to meet the PFC requirement, this part of reactive power needs to be compensated.

If the loss of the converter and the energy stored in L_{ac} and the EMI filter (which can be neglected compared to the energy stored in C_{c1} and C_{c2}) are ignored, the power on the ac side of the converter satisfies the following relationship according to the power conservation principle as follows:

$$P_{\mathrm{ac}} = P_{Cc1} + P_{Cc2} + P_{\mathrm{DAB}} \tag{24}$$

where P_{ac} is the input power, P_{DAB} is the power transferred to the secondary side through the transformer, P_{Cc1} and P_{Cc2} are the reactive power consumed by C_{c1} and C_{c2}. They can be described as follows:

$$\begin{cases} P_{\mathrm{ac}} = v_{\mathrm{ac}} i_{\mathrm{ac}} \\ P_{\mathrm{DAB}} = \frac{v_{\mathrm{rec}}}{2} i_{\mathrm{DAB}} \\ P_{Cc1} + P_{Cc2} = v_{Cc1} i_{Cc1} + v_{Cc2} i_{Cc2} \end{cases} . \tag{25}$$

Since $v_{Cc1} = v_{Cc2} = v_{\mathrm{rec}} / 2 = v_{\mathrm{ac}}$, the power relationship in (24) can be converted to the current form as follows:

$$i_{\mathrm{DAB}} = i_{\mathrm{ac}} - (i_{Cc1} + i_{Cc2}) \tag{26}$$

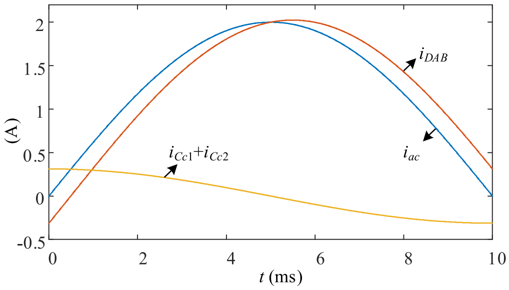


Fig. 11. Waveforms of $i_{Cc1} + i_{Cc2}$, i_{DAB} and i_{ac} in the positive half-cycle of v_{ac}, $I_{\mathrm{ac}} = 2$ A, $v_{\mathrm{ac}} = 110$ $\mathrm{V_{rms}}$, and $C_{c1} = C_{c2} = 3.2$ μF.

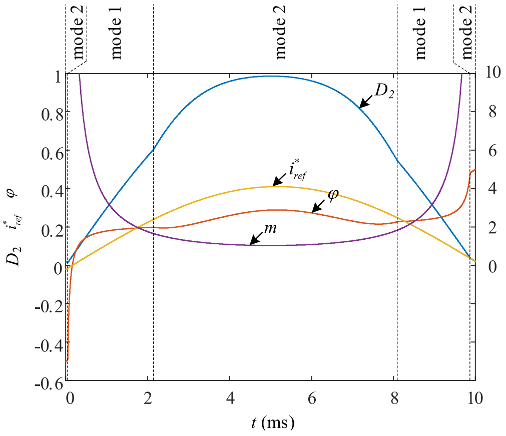


Fig. 12. Control variables over a half-cycle of v_{ac} after using the reactive power compensation method.

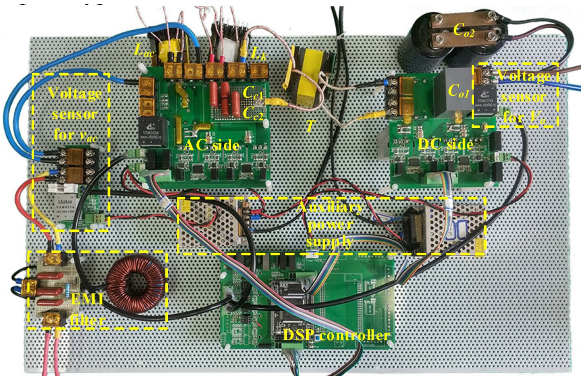
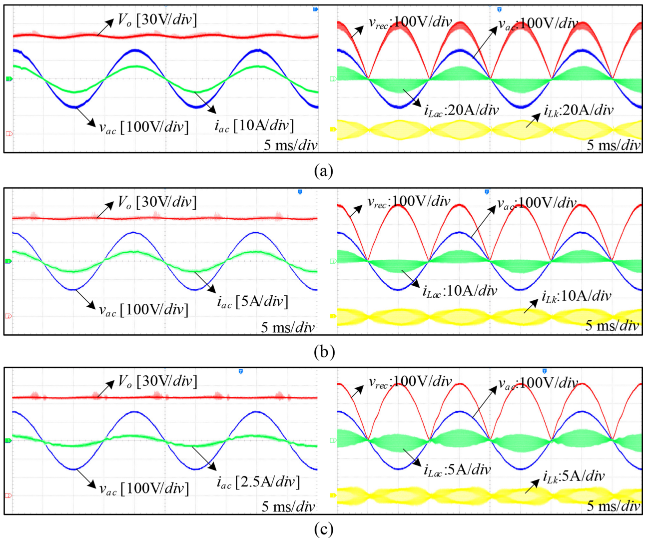


Fig. 13. Photograph of the hardware prototype.

where $i_{Cc1} + i_{Cc2}$ can be calculated with

$$i_{Cc1} + i_{Cc2} = \frac{dv_{Cc1}}{dt} + \frac{dv_{Cc2}}{dt} = (C_{c1} + C_{c2})\,\omega V_{\mathrm{ac}} \cos(\omega t). \tag{27}$$

The reactive power compensation can be realized by controlling i_{DAB} to satisfy (26). Fig. 11 shows the waveforms of i_{Cc1} + i_{Cc2}, i_{DAB} and i_{ac} in the positive half-cycle of v_{ac}. In order to compensate the reactive power consumed by C_{c1} and C_{c2}, i_{DAB} is no longer symmetrical in a half-cycle of v_{ac}, and there is a step change at the zero-crossing point of the grid voltage. Fig. 12 shows the curves of the control variables in a half-grid period after using the reactive power compensation method. Compared with Fig. 9, the trajectory of φ also becomes asymmetric and has a step change at the zero-crossing point of v_{ac}. Since the voltage at the zero-crossing point of v_{ac} is low, this step change of φ will not cause an obvious oscillation of i_{Lk}.



(a)

(b)

(c)

Fig. 14. Steady-state waveforms under 110 V_{ac} input voltage and 160 V_{dc} output voltage. (a) $P_o = 500$ W. (b) $P_o = 200$ W. (c) $P_o = 50$ W.

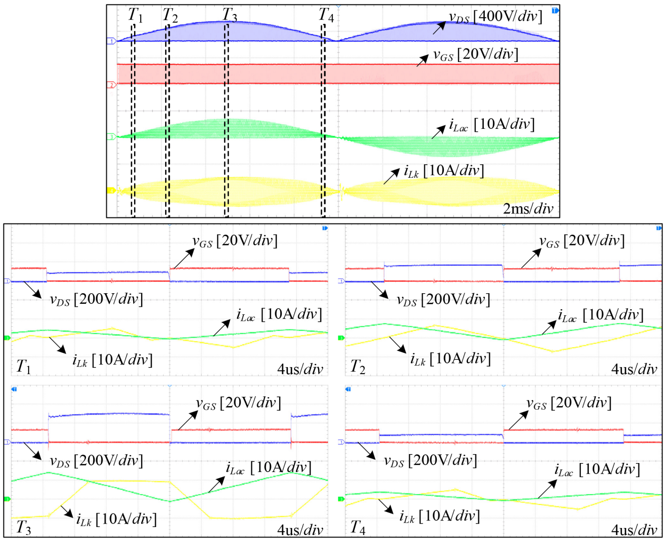


Fig. 15. ZVS waveforms for S_2 during the positive half-cycle, $P_o = 500$ W.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

A 500 W prototype shown in Fig. 13 was built to validate the theoretical analysis and evaluate the performance. The CRM operation of L_{ac} needs to ensure that the valley value of i_{Lac} is below zero, so the parameter design of L_{ac} will be highlighted. According to (19), the switching frequency decreases as the output power of the converter increases. In this article, the

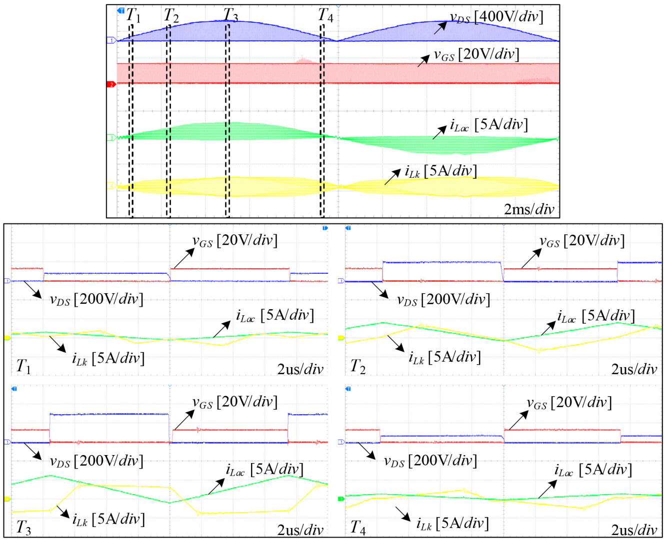


Fig. 16. ZVS waveforms for S_2 during the positive half-cycle, $P_o = 200$ W.

TABLE I
SYSTEM SPECIFICATIONS

Symbol	Description	Value
v_{ac}	Input voltage	110 Vrms, 50 Hz
V_o	Output voltage	160 V
f_s	Switching frequency	30 kHz–100 kHz
P_o(rated)	Rated power	500 W
L_{ac}	AC side inductor	150 μH
$n : 1$	Transformer turns ratio	1:1
L_k	Transformer leakage inductance	80 μH
L_m	Transformer magnetizing inductance	3.85 mH
C_{C1}, C_{C2}	AC side capacitor	3.2 μF
C_{o1}	HF DC side capacitor	50 μF
C_{o2}	LF DC side capacitor	2200 μF

minimum switching frequency is set to 30 kHz, which is based on general considerations, rather than on in-depth system optimization. Considering a 10% overload capacity, the switching frequency at the rated power is set to 33 kHz. Then, according to (19), L_{ac} can be calculated as follows:

$$L_{\text{ac}} = \frac{V_{\text{ac}} T_s}{4(I_{\text{ac}} + I_{\text{ZVS1}})} = 149.2(\mu\text{H}) \tag{28}$$

where I_{ZVS1} is set to 1 A. I_{ac} at the rated power is set to 6.9 A due to the consideration of the converter loss. The specification of the prototype is shown in Table I.

The steady-state waveforms under the full load, 40% load, and 10% load are shown in Fig. 14. When the output power is 500 W, the power factor is 0.998 and the THD of the grid current is 1.6%. When the output power is 200 W, the power factor is 0.992 and the THD of the grid current is 2.2%. When the output power is 50 W, the power factor is 0.934 and the THD of the grid current is 6.9%. The THD is low even without sampling the grid side current.

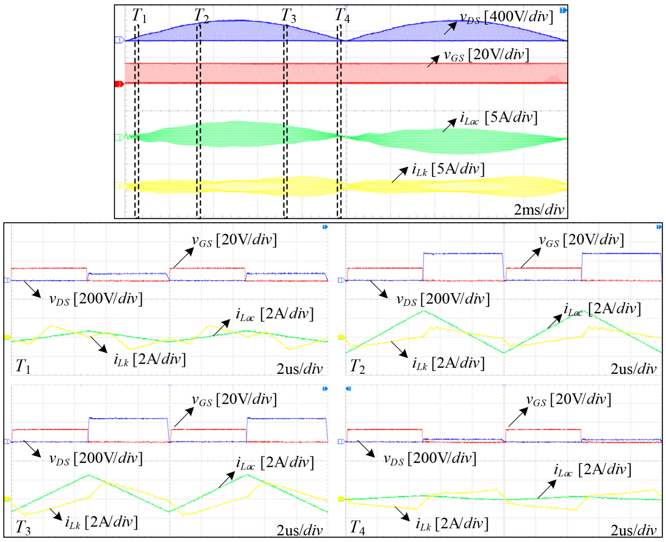


Fig. 17. ZVS waveforms for S_2 during the positive half-cycle, $P_o = 50$ W.

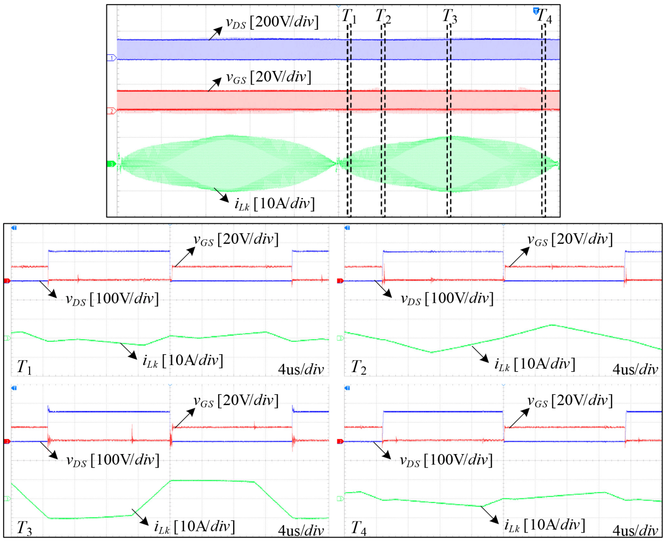


Fig. 18. ZVS waveforms for S_5 during a certain half-cycle, $P_o = 500$ W.

From the waveform of i_{Lac}, it is obvious that L_{ac} can operate in CRM under different load conditions with the quasi-fixed frequency control. When the output power is 50 W, the switching frequency is limited to 100 kHz according to Fig. 10, which makes the valley value of i_{Lac} lower than -1 A. In Fig. 14(a), the measured f_s is about 32.8 kHz. Meanwhile, the amplitude of the grid current I_{ac} is 6.95 A, and f_s calculated with (19) is 32.6 kHz. In Fig. 14(b), the measured f_s is about 66.7 kHz. Meanwhile, the amplitude of the grid current I_{ac} is 2.81 A, and the calculated f_s is 68.1 kHz. In Fig. 14(c), the switching frequency is limited to 100 kHz to limit the switching loss. The measured value agrees well with its calculated one.

As explained in Section III, during the positive half-cycle of v_{ac}, if S_2 can achieve ZVS, S_1 can also achieve ZVS. Therefore, only the ZVS realization of S_2 during the positive half-cycle of v_{ac} needs to be verified. For S_5–S_8, if S_5 can achieve ZVS, S_6–S_8 can also achieve ZVS. Therefore, only the ZVS realization of S_5 in a certain half-cycle of v_{ac} needs to be verified. The ZVS realization of S_2 and S_5 during the positive half-cycle of v_{ac} is verified under different load conditions. Four different time

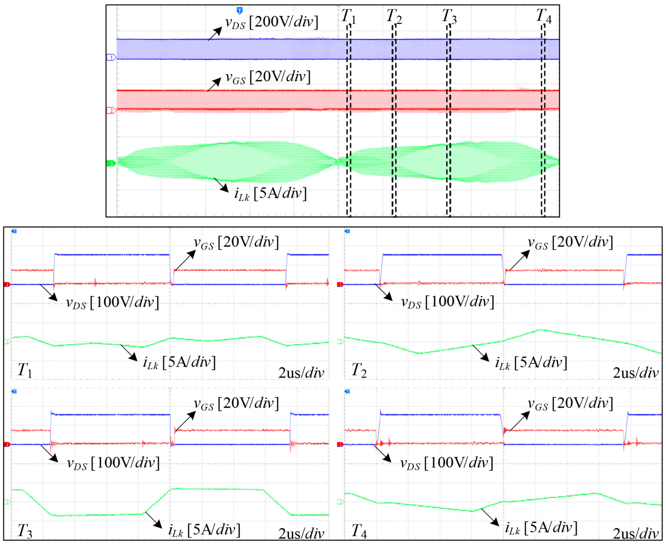


Fig. 19. ZVS waveforms for S_5 during a certain half-cycle, $P_o = 200$ W.

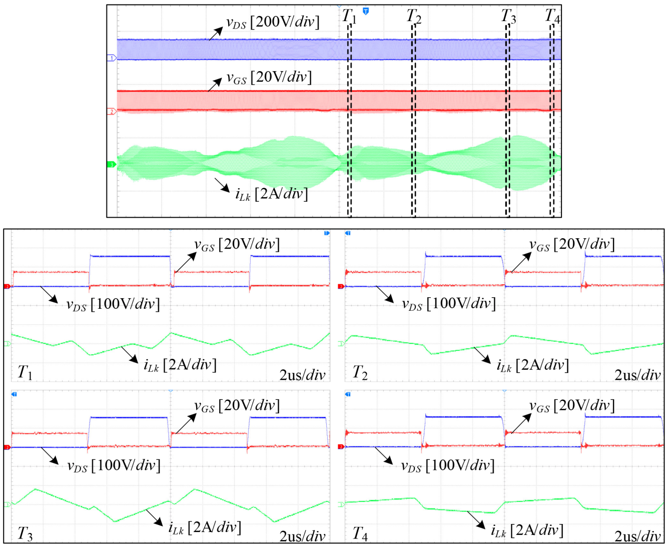
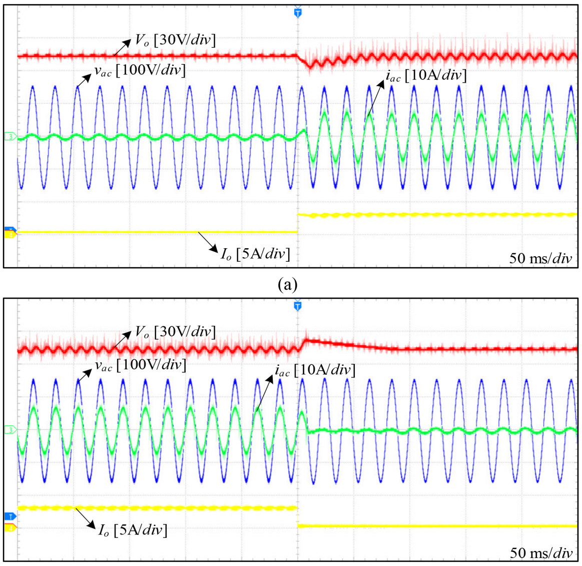


Fig. 20. ZVS waveforms for S_5 during a certain half-cycle, $P_o = 50$ W.

intervals T_1–T_4 are selected for each case to verify the ZVS realization. The mode transition from mode 1 to mode 2 occurs in T_2.

The switching waveforms of S_2 in the positive half-cycle of $v_{\rm ac}$ under different load conditions are illustrated in Figs. 15–17. $L_{\rm ac}$ operates in CRM, and $i_{L{\rm ac}}$ can provide enough commutation current for S_2. S_2 can realize ZVS over the full range of $v_{\rm ac}$ under different load conditions. The switching frequency remains constant within a half-cycle of $v_{\rm ac}$ under the same load condition.

The switching waveforms of S_5 in a half-cycle of $v_{\rm ac}$ under different load conditions are shown in Figs. 18–20. Except for the quasi-ZVS near the zero crossing of v_{ac} and the mode transition, S_5 can achieve ZVS over almost the full range of the grid voltage.



(a)

(b)

Fig. 21. Experimental results for load step change. (a) Load step-up from 50 to 500 W. (b) Load step-down from 500 to 50 W.

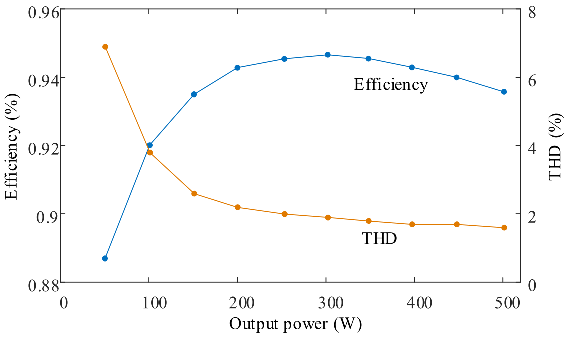


Fig. 22. Measured efficiency and THD of the converter.

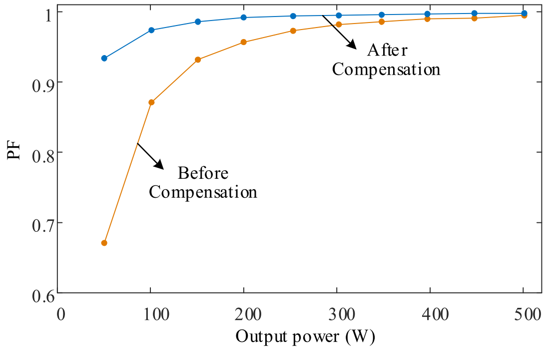


Fig. 23. Measured power factor of the converter before and after the reactive power compensation.

Fig. 21 shows the dynamic response to the load step-up and step-down. As seen, during the load change, the output voltage fluctuates slightly, and the transition of the grid current is smooth and fast. Fig. 22 shows the measured efficiency and THD of the converter with the proposed modulation scheme. The prototype achieves an efficiency of 93.6% at the full load. The peak efficiency of 94.6% is achieved at 300 W. The THD is low even without sampling the grid-side current. Fig. 23 shows the power factor measurement results before and after the reactive power compensation. After adopting the power factor compensation method, the power factor of the converter at light load has been significantly improved.

V. CONCLUSION

In this article, a modulation scheme for a bridgeless single-stage isolated ac–dc converter is proposed. With the proposed modulation scheme, all HF power switches can achieve ZVS over the full ranges of the grid voltage and the load. The grid side inductor can operate in CRM without a ZCD circuit by applying the quasi-fixed switching frequency control. Since the switching frequency is fixed within a half-cycle of the grid voltage and independent of the other two control variables, the modulation scheme is simple and easy to implement. The natural PFC control can be realized without sampling the grid current. The reactive power consumed by C_{c1} and C_{c2} is compensated to improve the power factor of the converter, especially at light loads. The experimental results obtained from a 500 W prototype verify the ZVS analysis. By employing the proposed modulation scheme, the converter achieves a peak efficiency of 94.6% and a minimum THD of 1.6%.

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Yun Zhang (Senior Member, IEEE) was born in Jiangsu, China, in 1980. He received the B.S. and M.S. degrees from the Harbin University of Science and Technology, Harbin, China, in 2003 and 2006, respectively, and the Ph.D. degree from the Harbin Institute of Technology, Harbin, China, in 2010, all in electrical engineering.

Subsequently, he joined the Tianjin University, Tianjin, China, as a Lecturer with the School of Electrical and Information Engineering, where he is currently a Professor of Power Electronics. From December 2016 to December 2017, he was an Academic Visitor with the Power Electronics, Machines and Control (PEMC) Group, University of Nottingham, Nottingham, U.K. His current research interests include topologies, modulation, and control strategies of power converters for electric vehicles and microgrids.

Dr. Zhang is an Associate Editor of the *Journal of Power Electronics*.

Gen Yang was born in Tianjin, China, in 1997. He received the B.S. degree in electrical engineering in 2019 from the School of Electrical and Information Engineering, Tianjin University, Tianjin, China, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include topology and control of ac–dc converters and dc–dc converters.

Jing Li (Member, IEEE) received the B.Eng. and M.Sc. degrees (Hons.) from the Beijing Institute of Technology, Beijing, China, in 1999 and 2002, respectively, and the Ph.D. degree from the University of Nottingham, Nottingham, U.K., in 2010, all in electrical and electronic engineering.

She was a Research Fellow after graduation with the Power Electronic, Machine and Control Group, University of Nottingham. In 2016, she joined the University of Nottingham Ningbo China, Ningbo, China, as an Assistant Professor, where she is currently an Associate Professor with the Department of Electrical and Electronic Engineering. Her research interests include condition monitoring for motor drive systems and power distribution systems, advanced control, and design of motor drive systems.

Zhiguo Kong was born in Jiangsu, China in 1977. He received the master’s and doctor’s degrees in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2003 and 2007, respectively.

He is currently a professional-level Senior Engineer with China Automotive Technology and Research Center Company, Ltd, Tianjin, China. He has almost 20 years of development experience in hybrid powertrains and motor driving system. His research interests also include EDS test technology, control strategy of hybrid electric vehicle, wireless power transmission, and power electronics.

Xinshan Zhu (Member, IEEE) received the B.E. and the M.E. degrees in automation control from the Harbin Institute of Technology, Harbin, China, in 2000 and 2002, respectively, and the Ph.D. degree in pattern recognition and intelligent systems from the Institute of Automation, Chinese Academy of Sciences, Beijing, China, in 2005.

He is currently an Associate Professor with the School of Electrical and Information Engineering, Tianjin University, Tianjin, China. His research interests include artificial intelligence, image processing, signal processing, and control for electric vehicles.