Letters

A Family of High Step-Up Magnetically Coupled Impedance Source Inverters With Clamped DC-Link Voltage and Low Shoot-Through Current

Ali Nikbahar and Mohammad Monfared, *Senior Member, IEEE*

***Abstract*—The use of coupled inductors in impedance source inverters improves the voltage gain performance at the expense of high dc-link voltage spikes and shoot-through (ST) currents. The result is an increase in voltage and current stresses on semiconductors, as well as reactive element capacity and overall losses. Thus, to overcome these problems, this letter proposes a new family of magnetically coupled impedance source inverters with a smooth dc-link voltage, a low ST current, and a higher voltage gain that are confirmed through experimental tests.**

***Index Terms*—Leakage inductance, magnetically coupled impedance source (MCIS) inverter, shoot-through (ST) current, voltage spike.**

I. Introduction

THE magnetically coupled impedance source (MCIS) inverters offer single-stage buck-boost conversion [1]. The turn ratio, as extra design flexibility, allows improving some important characteristics, such as the boost factor B. It is defined in (1), where V_{in} and V_{PN} are the input and the dc-link voltages, respectively. Also, D is the (ST) duty ratio and δ is a function of the turn ratio.

$$B = \frac{V_{PN}}{V_{\text{in}}} = \frac{1}{1-\delta D}. \tag{1}$$

As evident from (1), the proper choice of δ offers high boost factors with even small values of D. It is regarded as the main advantage of the MCIS networks. On the other hand, the leakage inductance causes voltage spikes when the inverter switches from ST to the nonshoot-through (NST) state. It demands bulky and lossy snubbers or some other active voltage clamping techniques. Some approaches have been already proposed in [2] and [3] by adding one more diode to the basic MCIS circuit. Although the peak of the voltage spike is limited by these clamp circuits, it is not fully mitigated and still deteriorates the voltage stresses of semiconductors. In another approach, the Δ-source impedance network is proposed to minimize the leakage inductance at the price of a more complicated magnetic circuit [4], [5]. Some recent circuits are proven more successful in mitigating the voltage spikes by recovering the energy stored in the leakage inductance [6], [7], [8], [9], [10]. However, both the spiky and the smooth dc-link voltage groups suffer from a huge ST current. The common problem is that the ST current peak is δ times the input current peak. It means that an increase of δ to obtain higher voltage gains proportionally increases the ST current. The higher ST current means more losses, higher semiconductor ratings, larger reactive components, and lower efficiency and power density. Although some MCIS inverters have been introduced based on the switched boost inverter [11] to reduce the ST current [12], [13], they suffer from voltage spikes, either in dc-link or active switch in their impedance networks. Moreover, the ST current is still high.

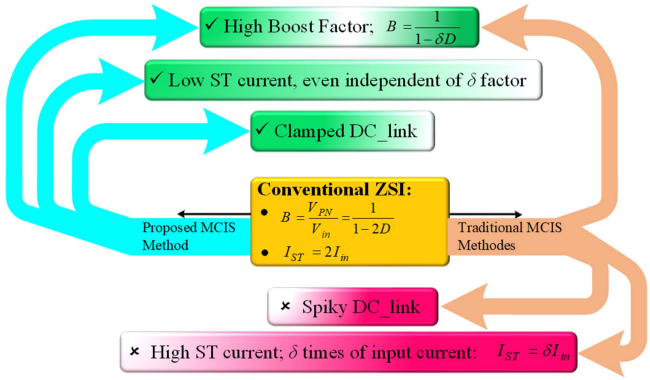

Fig. 1. Evolution of the MCIS inverters.

To mitigate the abovementioned problems while incorporating the coupled inductor, this letter proposes a family of 12 MCIS inverters. The development and circuit configuration of the proposed topologies are depicted in Figs. 1 and 2, respectively. They prominently feature clamped dc-link voltage and low ST current. Furthermore, each proposed topology inherits all individual advantages of the basic spiky structure which is derived from that. By the proposed techniques, the energy of the leakage inductance of the coupled inductor is recovered and the dc-link is efficiently clamped. Furthermore, not only

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Ali Nikbahar is with the Department of Electrical Engineering, Faculty of Engineering, Ferdowsi University of Mashhad, Mashhad 9177948974, Iran (e-mail: ali_nikbahar@mail.um.ac.ir).

Mohammad Monfared is with the Swansea University, Swansea SA1 8EN, U.K., and also with the Ferdowsi University of Mashhad, Mashhad 9177948974, Iran (e-mail: m.monfared@um.ac.ir).

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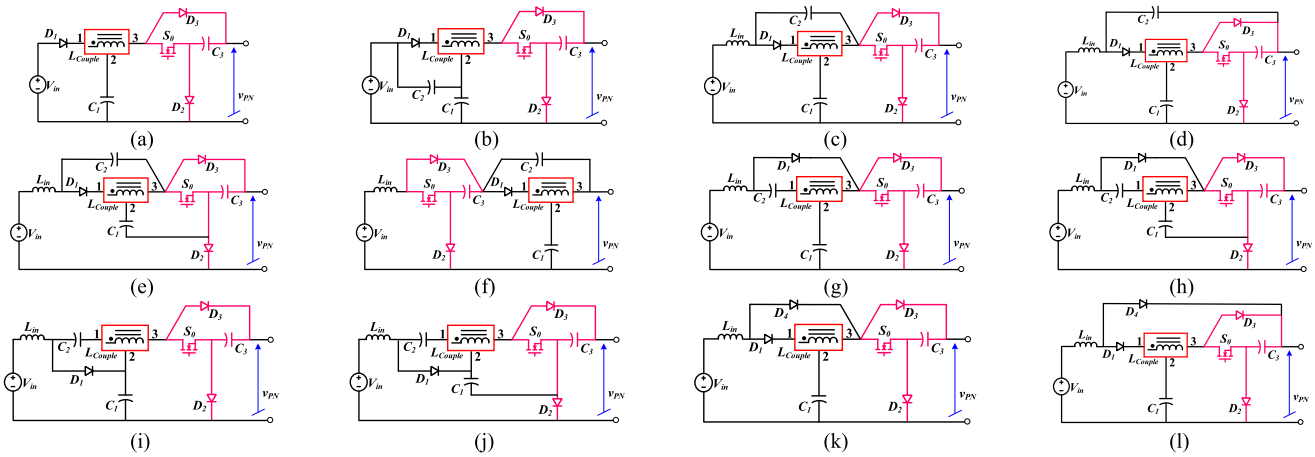

Fig. 2. Proposed MCIS inverters: (a) topology 1, (b) 2, (c) 3, (d) 4, (e) 5, (f) 6, (g) 7, (h) 8, (i) 9, (j) 10, (k) 11, and (l) 12.

the ST current is remarkably reduced in terms of its duration and magnitude, its dependency on the δ factor is eliminated. Thus, the proposed converters offer high efficiency and power density. The validity of the theoretical achievements is confirmed through experimental results obtained from a laboratory prototype converter.

II. Proposed Topologies

Fig. 2 illustrates the 12 converters that make up the proposed family of MCIS inverters. The part that eliminates the voltage spike and reduces the ST current is highlighted in pink. The remaining elements drawn in black are existing MCIS inverters. The block L_{couple} denotes the coupled inductor. Any of the Y[14], Δ[4], T[15], Γ[16], or flipped Γ[17]-shaped coupled inductors can be placed in this block. Depending on the application, one of these 12 circuits may be used. For example, the first topology has fewer components. However, the input current is discontinuous, which is not desirable in some applications, such as photovoltaic systems. The second topology has an additional capacitor to smooth the input current. The rest have an inductor at the input, thus the continuity of the input current can be guaranteed. Also, topologies 7 and 8 require the minimum magnetic core volume, since their windings are connected in series with the capacitors, the dc part of the magnetizing current is blocked. The two last topologies can be named diode-assisted MCIS inverters due to the one more diode utilization in their circuits. To avoid unnecessary repetition and somehow similar operation principles, only the performance principles of the topology 5 are studied in detail while the final expressions of all proposed converters are summarized in Table I.

III. Operation Principles

The single-phase highly efficient quasi-YSI (HE-qYSI) is depicted in Fig. 3. It is one possible realization of topology 5. The equivalent circuits and key waveforms are shown in Figs. 4 and 5, respectively. For the sake of simplicity, the inverter bridge and the load are replaced by a switch in parallel with a current

TABLE I
Boost Factors and ST Current of the Proposed Inverters

Topology	*B*	*δ factor*	*Norm. ST current, I_{ST}/ I_{in}*
1	$1/(1-2KD)$	$2K$	0.5δ
2	$1/(1-2KD)$	$2K$	0.5δ
3	$1/(1-2(K+1)D)$	$2(K+1)$	0.5δ
4	$1/(1-(2K+1)D)$	$2K+1$	$0.5\delta+0.5$
5	$1/(1-(K+2)D)$	$K+2$	1
6	$1/(1-(K+2)D+KD^2)$	$K+2-KD$	$\delta-1$
7 [18]	$1/(1-2(K+1)D)$	$2(K+1)$	0.5δ
8	$1/(1-(K+2)D)$	$K+2$	1
9	$1/(1-2(K+2)D)$	$2(K+2)$	0.5δ
10	$1/(1-(K+3)D)$	$K+3$	1
11	$1/(1-2(K+1)D+2KD^2)$	$2(K+1)-2KD$	0.5δ
12	$1/(1-(2K+1)D+2KD^2)$	$2K+1-2KD$	$0.5\delta+0.5$

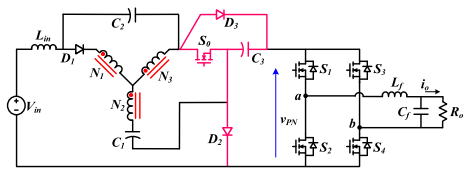

Fig. 3. Proposed HE-qYSI.

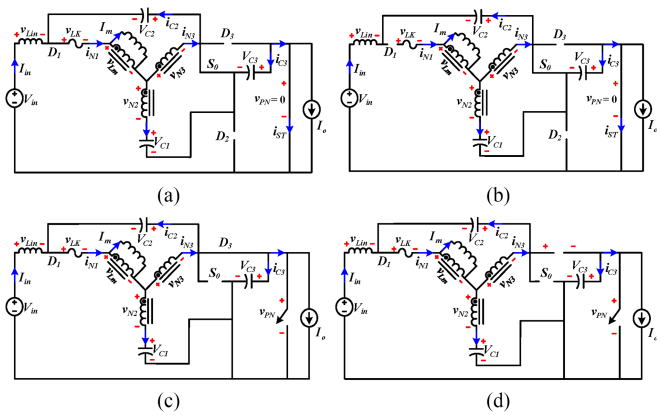

Fig. 4. Operation modes of the HE-YSI- topology 5: (a) ST state $[t_0, t_1]$, (b) ST state $[t_1, t_2]$, (c) NST state $[t_2, t_3]$, and (d) NST state $[t_3, T_s]$.

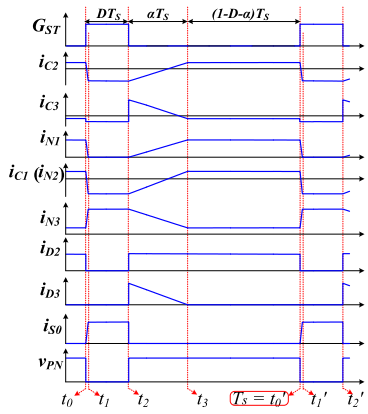

Fig. 5. Key waveforms of the fifth proposed inverter.

source I_o, denoting the average of inverter current during one switching period T_s. The three windings coupled inductor is modeled with the leakage L_k, and the magnetizing L_m elements and its turn ratio is N_1: N_2: N_3. The capacitors C_1 to C_3 and the inductors L_{in} and L_m are assumed to be large enough, such that the voltages across the capacitors and the currents through the inductors are almost constant within a switching period. The low value of L_k results in significant fluctuations in the current through it. The proposed converter, such as other Z-source inverters (ZSIs), operates in either ST or NST states, as described in the following.

ST [t_0, t_1]: The switch S_0 starts conducting from zero current at t_0 while the dc-link voltage v_{PN} becomes zero. The capacitors C_1 and C_2 are in transition from discharge to charge mode. On the contrary, from the beginning of the ST state, C_3 immediately enters charge mode. Because of the voltage polarity of C_3, both D_2 and D_3 are reverse-biased. In addition, the current through D_1 decays to zero at a rapid rate, until the energy of L_k reaches zero while L_{in} and L_m are being charged from capacitors and the input voltage source V_{in}. During this very short state, the energy of all reactive components, which are large enough, can be assumed unchanged except for the leakage inductor. The voltage expressions of the inductors can be derived as

$$v_{L\text{in}}^{I} = V_{\text{in}} + V_{C2} + V_{C3} \tag{2}$$

$$v_{Lm}^{I} = \frac{N_1}{N_3 - N_2} V_{C1} \tag{3}$$

$$v_{Lk}^{I} = -(KV_{C1} + V_{C2}) \tag{4}$$

where

$$K = \frac{N_1 + N_3}{N_3 - N_2}. \tag{5}$$

ST [t_1, t_2]: As shown in Figs. 4(b) and 5 D_2, and D_3 remain reverse-biased. As L_k is fully discharged, the current through D_1 is zero and it blocks while S_0 continues to conduct. This interval can be safely considered as the ST state duration DT_s. The voltage across L_{in} and L_m are still as (2) and (3), respectively. Also, by applying KCL and considering Ampere's law, i.e., $N_1 i_1 + N_1 i_1 + N_1 i_1 = N_1 i_m$, the discharge current of capacitors can be obtained from the following:

$$i_{C1}^{II} = -\frac{N_1}{N_3 - N_2} I_m \tag{6}$$

$$i_{C2}^{II} = -I_{\text{in}} \tag{7}$$

$$i_{C3}^{II} = -I_{\text{in}}. \tag{8}$$

NST [t_2, t_3]: In this state, S_0 is turned OFF by setting its gate pulse to zero. All diodes start to conduct and the currents of the coupled inductor windings vary linearly without any abrupt changes as depicted in Fig. 5. During this mode, the conduction of D_2 provides a clamping path across the dc-link via C_3. Also, the voltages across three windings of the coupled inductor are clamped by C_1 to C_3. Therefore, voltage spikes at the ST to NST state transition, unlike the traditional circuit, are effectively prevented. By applying Kirchhoff's voltage law to Fig. 4(c), one can write

$$v_{L\text{in}}^{III} = V_{\text{in}} + V_{C2} - V_{C3} \tag{9}$$

$$v_{Lm}^{III} = -\frac{N_1}{N_3 - N_2}(V_{C3} - V_{C1}) \tag{10}$$

$$v_{Lk}^{III} = -V_{C2} + K(V_{C3} - V_{C1}). \tag{11}$$

As can be seen from Fig. 5, the current of the capacitors linearly changes during this state. Thus, with two points, the linear equations can be obtained to estimate the currents of the capacitors in this interval. As the voltages of the windings are clamped by the capacitors, their currents also vary continuously with time. Their initial values at the beginning of the third interval ($t_2{}^+$) are the final values at the end of the second interval ($t_2{}^-$). Therefore, the capacitor currents at the start of this state can be derived as

$$i_{C1}(t_2^+) = -\frac{N_1}{N_3 - N_2} I_m \tag{12}$$

$$i_{C2}(t_2^+) = -I_{\text{in}} \tag{13}$$

$$i_{C3}(t_2^+) = I_{\text{in}} - I_o + \frac{N_1}{N_3 - N_2} I_m. \tag{14}$$

NST [t_3, T_s]: At t_3, the current through D_3 reaches zero. However, D_1 and D_2 still conduct. Hence, the voltages across the windings and the dc-link are still clamped. Therefore,

$$v_{L\text{in}}^{IV} = V_{\text{in}} + \left(1 - \frac{\beta}{K}\right) V_{C2} - V_{C1} \tag{15}$$

$$v_{Lm}^{IV} = -\frac{\beta N_1}{N_1 + N_3} V_{C2} \tag{16}$$

$$v_{Lk}^{IV} = -(1 - \beta) V_{C2} \tag{17}$$

$$i_{C1}^{IV} = I_{\text{in}} \tag{18}$$

$$i_{C2}^{IV} = \frac{N_1}{N_1 + N_3} I_m - \frac{(K-1)}{K} I_{\text{in}} \tag{19}$$

$$i_{C3}^{IV} = -I_o \tag{20}$$

where β is the series voltage divider ratio between $(1+N_3^2/N_1^2)L_m$and L_k. By assuming a small L_k, thus, $\beta \approx 1$. Besides, by applying the volt–second balance law to the input and magnetizing inductors, along with the amp–second balance law to the capacitors, the voltages across the capacitors, the ST current, and the time interval ratio of the third mode can be derived as

$$\begin{cases} V_{C1} = (1-D)BV_{\text{in}} \\ V_{C2} = KDBV_{\text{in}} \\ V_{C3} = BV_{\text{in}} \end{cases} \tag{21}$$

$$I_{\text{ST}} = I_{\text{in}} \tag{22}$$

$$\alpha = 2\,\frac{1-(K+1)D}{K+1} \tag{23}$$

where B is the voltage boost factor of the proposed converter

$$B = \frac{1}{1-(K+2)D} = \frac{1}{1-\delta D}. \tag{24}$$

As can be seen, the proposed topology 5 can successfully clamp the dc-link voltage while the ST current does not depend on the δ factor anymore. For completeness, the boost factor δ and the ST current of the proposed smooth dc-link MCIS inverters are listed in Table I, while the Y-coupled inductors are assumed in all circuits. It should be noted that, although only the ST current of the topologies 5, 8 and 10 do not depend on the δ factor, this parameter for the other proposed topologies is lowered, in comparison to the original MCSI inverters.

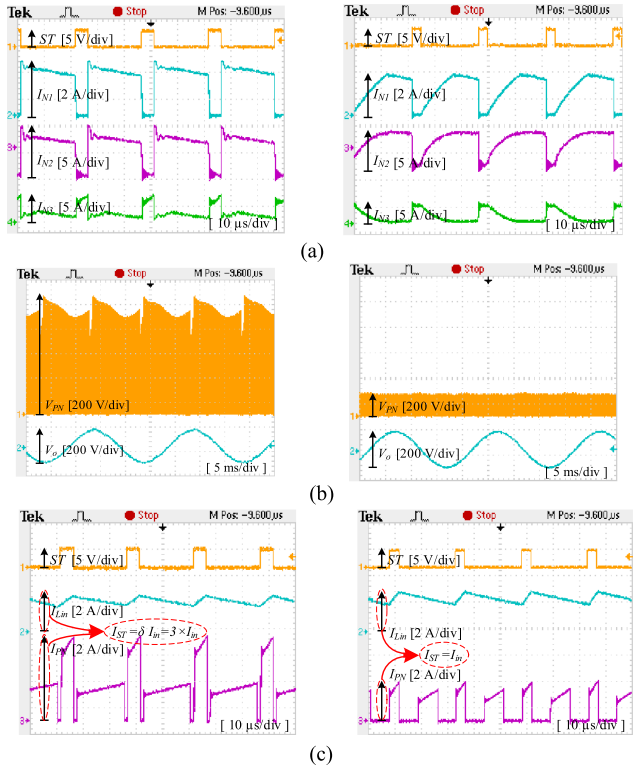

Fig. 6. Experimental waveforms of qYSI (left-hand side) and HE-qYSI (right-hand side): (a) ST signal and coupled inductor windings' currents, (b) dc-link and output voltages, and (c) ST signal and input and dc-link currents.

IV. Practical Evaluation

The performance of the proposed HE-qYSI is validated using a 200 W prototype setup. To emphasize the mitigation capability of voltage spikes, the Y-shaped coupled inductor is deliberately wound loosely on the toroid magnetic core 0077615A7. It results in the leakage inductances of $L_{K1} = 0.6$ μH, $L_{K2} = 1.23$ μH, and $L_{K3} = 13.6$ μH. Also, $L_{\text{m}} = 432$ μH. The dc input and the peak output voltages are 80 V and 180 V peak, respectively. The simple boost modulation with the carrier frequency of 20 kHz is implemented where the modulation index M is supposed to be $1-D$.

To have a comprehensive comparison in the experiment, the proposed converter and qYSI [1] are tested on the same test rig. The ST duty cycles are set to be 0.1394 and 0.1954 for these inverters, respectively. The lower ST requirement of the proposed inverter reflects its improved voltage gain when compared with the qYSI converter with a similar turn ratio. The boost factor for qYSI is $1/(1-(K+1)D)$, and when compared with (24), clearly, for the same voltage gain, it requires a bigger D. The experimental results are shown in Fig. 6. First, to show the voltage spike elimination capability of the proposed converter, the ST signal and current waveforms of the coupled inductor windings of both inverters are shown in Fig. 6(a). Also, their dc-link and output voltages are presented in Fig. 6(b). As already discussed, the currents of windings of qYSI, when it enters NST mode, change abruptly. Thus, large spikes in the dc-link voltage appear as the peak reaches around 900 V. On the contrary, when the proposed modification is applied to this MCIS converter, no voltage spikes are observed as the current waveforms change smoothly from ST to NST. Consequently, the ac output waveforms are highly sinusoidal, whereas the high-frequency dc link is stabilized at v_{pn} (≈180 V). Next, the ST signal, the input, and the dc-link currents of both converters are plotted in Fig. 6(c). In the proposed converter, the ST current is a minimum of equal to the input current, whereas in the traditional MCIS it is δ ($=3$) times the input current. The large magnitude of the current and the high-duty cycle of ST mode result in high power losses and large active elements. High efficiency and power density can, therefore, be considered the salient features of the proposed MCIS inverter.

Eventually, Fig. 7(a) compares the efficiencies of HE-qYSI and qYSI for the same experimental conditions. All tests are conducted at 110 Vrms by adjusting D and M. Obviously, although the proposed technique makes the dc-link smooth and significantly reduces the ST current, the power losses associated with extra elements avoid efficiency improvement at light load. In the other words, by raising the output power, its effect on the power loss reduction is revealed. At this time, the power loss originating from the large ST current causes a dramatic efficiency decrease of the spiky qYSI. Therefore, the proposed converter offers higher efficiency. To investigate this issue, the power loss distribution among the components of the converters is also calculated at 250 W output power, and the results are

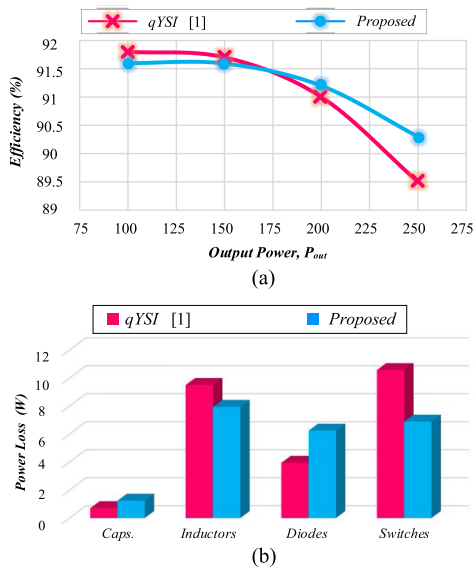

Fig. 7. (a) Efficiency comparison and (b) loss distribution at 250 W output power between qYSI and HE-qYSI.

depicted in Fig. 7(b). As already discussed, the basic qYSI suffers from a high ST current, which is three times the proposed one. Moreover, to boost the dc input voltage, basic qYSI requires a higher ST duty cycle. Thus, as shown in Fig. 7(b), the power loss of the active switches of the proposed converter is decreased by almost 57% in comparison to the spiky qYSI. In addition, the low ST current of the proposed inverter leads to a reduction in the losses of the inductors too. Although the power losses of the diodes and capacitors of the proposed converter are higher than the qYSI, the loss reduction of the other part is dominant and they improve the efficiency.

V. Conclusion

By proposing a family of highly efficient MCIS inverters, this letter overcomes the challenges of coupled inductor utilization. They provide regeneration of the trapped energy in the leakage inductances and clamping of the voltages across the coupled inductor windings, resulting in a smooth dc-link voltage and efficient operation. A remarkable reduction of the ST current, which is not even dependent on δ, is also achieved, which leads to a lower rating of semiconductors, the capacity of the reactive elements, and power losses. Overall, the proposed converters inherit all the benefits of traditional MCIS inverters with higher efficiency and no voltage spikes. The validation of the aforementioned properties of the proposed converters was done by performing extensive experiments on a 200 W laboratory prototype.

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