A Design of Wireless Power Receiver With Gate Charge Recycled Dual-Mode Active Rectifier and Step-Down Converter With 88.2% System Efficiency for Power Management IC

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***Abstract*—This article presents a power management integrated circuit for a wireless power receiver unit. A dual-mode high-efficiency active rectifier design is based on alliance for wireless power (A4WP) and wireless power consortium (WPC) standards. A gate charge recycling technique is proposed in the dual-mode active rectifier so that the current generated by the switching of the high side gate driver can be recycled to the rectifier output voltage in order to enhance efficiency. A step-down dc–dc converter with a proposed bootstrap circuit and dynamic pull-up resistor gate driver circuit is designed. The chip is implemented in a 0.18-μm bipolar-CMOS double-diffused metal-oxide-semiconductor process. The total die area, including the pad, is 2.64 mm $\times$ 2.6 mm. The measurement results show that the active rectifier achieves peak power conversion efficiency (PCE) of 94.7% and generates an output voltage of 7.68 V in WPC mode and 9.1 V with 93.4% efficiency in A4WPC mode. The input voltage varies from 10 $V_{P\text{-}P}$–12 $V_{P\text{-}P}$. Similarly, the step-down dc–dc converter obtains a peak PCE of 93.2% at a load current of 500 mA while producing an output voltage of 5 V. The overall system efficiency at A4WP and WPC mode are 86.7% and 88.2%, respectively.**

***Index Terms*—Alliance for wireless power (A4WP), dual-mode, dynamic pull-up resistor, gate charge recycle, inductive coupling, magnetic resonance, power conversion efficiency (PCE), reverse leakage current, wireless power consortium (WPC).**

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I. Introduction

WIRELESS power transfer (WPT) has emerged as one of the most promising new technologies. Many useful techniques for wireless power charging systems have been developed. The WPT system employs inductive coupling and magnetic resonance methods. The magnetic resonance approach is used alliance for wireless power (A4WP) standard, whereas the inductive coupling method is used for the wireless power consortium (WPC) [1]. In a WPT system, the frequency of the WPC standard is adjusted from 87–357 kHz to enhance efficiency [2]. The A4WP standard, on the other hand, is based on the magnetic resonance approach, which is capable of transferring power across a few centimeters more than inductive coupling. A4WP operates at a frequency of 6.78 MHz, which is much higher than that of WPC.

Wireless charging systems need first to be rectified and regulated. Wireless charging technology is increasingly applied to a wide range of devices and the Internet of Things (IoT). The IoT has become a big phenomenon in portable electronics in recent years. As a result, power consumption has risen in order to provide high-performance tasks. However, battery life and charging technologies have not kept up with the IoT's needs. The power source, battery life, and size all play a part in a good power management system. The efficiency of the WPT is reduced,

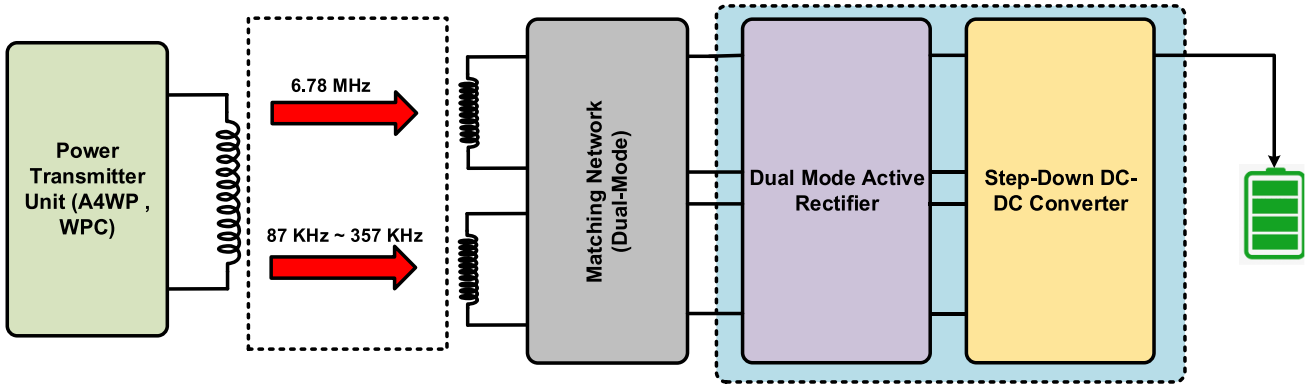


Fig. 1. Block diagram of dual-mode WPT system.

due to multistage power processing [3]. Various topologies have been explored recently to improve the efficiency of WPT systems [4], [5], [6]. To achieve high efficiency is the main goal of WPT research [7], [8], [9]. The study being conducted to enhance efficient power management strategies is gradually growing due to system demand and the need to fix the power requirement. As a result, increased battery life and decreased size are critical requirements to boost the user's flexibility [10]. In power management integrated circuits (PMICs), an active rectifier is used in the first step to convert ac to dc. A dc–dc converter is used in the second step, and battery charging is done in the third stage. The high-efficiency active rectifier [11], [12], [13] and dc–dc converters [14], [15], [16], [17] are used to improve the efficiency of the respective phase but the system efficiency reduces due to multiple stages of power processing. PMIC is not a new concept when it comes to its function in extending battery life, reducing power consumption, and providing a dedicated power supply to the system. A major module of PMICs, along with other switching and linear regulators, is the power conversion circuit, or in colloquial terms, the circuit that takes power from a battery source and provides a steady and stable power source to a system. The dc–dc converters and rectifiers are regarded as the most important in PMICs for wireless power receivers (WPRs) due to their ability to achieve high efficiency [18]. Different types of rectifiers and dc–dc converters are used depending on the needs of the users, but the primary goal is to achieve high efficiency, small size, and low power consumption. Different types of control schemes are used for various conditions and applications. To save space, the building blocks for each mode of the active rectifier should be shared. The rectifier, on the other hand, faces the following challenges when it comes to sharing the circuit. First, correct synchronous rectifier functioning is difficult to accomplish because the frequencies of the transmitted signals vary for each standard. Second, depending on whether the communication and control techniques have inductive coupling or magnetic resonant, each standard has a different communication and control technique.

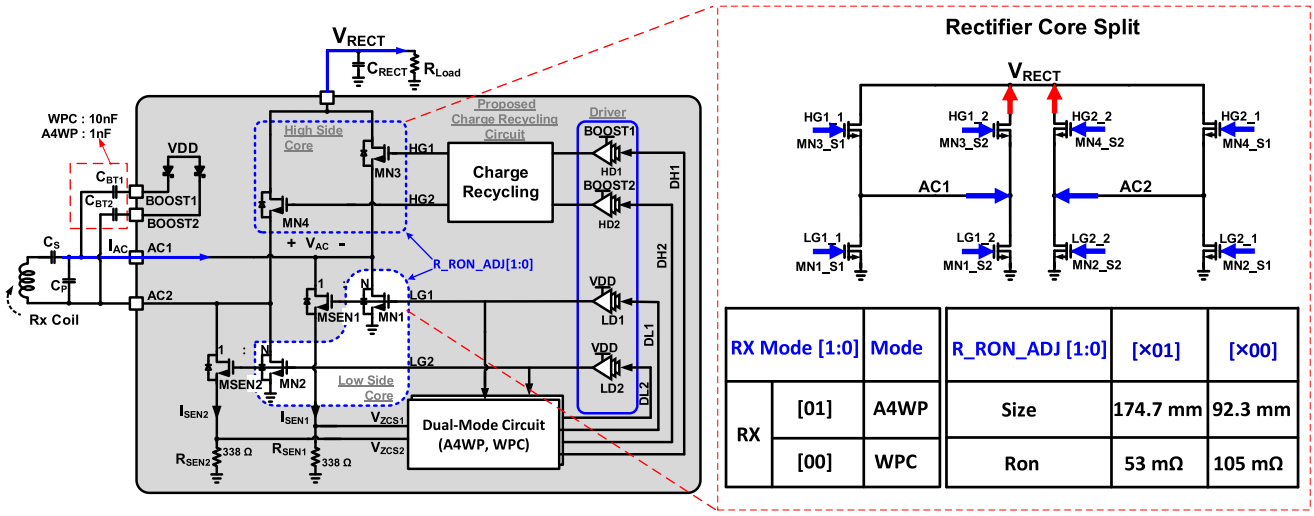
In addition, the WPT receiver's output power level should be enhanced to effectively shorten charging time. Therefore, a dual-mode active rectifier that supports dual-mode having different control block but sharing the single-core block with charge recycled technique for high efficiency and smaller area is proposed in this article. Fig. 1 shows the block diagram of the dual-mode WPT system.

In the A4WP standard mode, the analog delay-locked loop structure was previously employed [5]. As a result of the capacitors and other components, the circuit area increased, and its current consumption increased as the circuit was used more frequently. The efficiency of the system deteriorated as current consumption increased. Because the digital phase detector (DPD) structure was adopted, this design was able to reduce the area as compared to previous studies. The current consumption is also decreased because after the optimum delay locking, the circuit is turned OFF and efficiency improves as a result of lower current consumption.

Zero current sensing (ZCS) circuit is used in WPC mode [1]. There may be an effect on the glitch if the sensor value (V_{ZCS1}) and the reference value (V_{REFC}) are considerably different. In this article, a blanking circuit (BC) is used to eliminate the glitch problem. The SR-Latch circuit creates ZCS set/reset signals, which are used to ensure that the gate signal is timed correctly.

The efficiency of the rectifier is determined by two major factors: conduction loss and switching losses. Conduction loss is the dominating factor in WPC mode, the core should be as large as feasible to reduce on-resistance; however, when switching loss is the dominant factor in A4WP mode, the core can be smaller than in WPC mode. Both these losses affect rectifier efficiency. To increase the rectifier power conversion efficiency (PCE), the proposed charge recycling technique is utilized subsequently at high side gate drivers. This allows the current generated by the gate driver's switching to be recycled and applied to the rectifier output voltage (V_{RECT}).

The output power level of the WPTR dc–dc converter has recently been enhanced to shorten charging time. If the output power level is increased while the power efficiency is maintained, the heat generated by the circuit will become more significant. So, a dynamic pull-up resistor gate driver circuit is implemented in our proposed step-down dc–dc converter, which offers a dynamic pull-up resistor to drive the high side switch and suppress the gate to a source voltage spike.



RX Mode [1:0]	Mode	R_RON_ADJ [1:0]	[×01]	[×00]
[01]	A4WP	Size	174.7 mm	92.3 mm
[00]	WPC	Ron	53 mΩ	105 mΩ

Fig. 2. Block diagram of dual-mode active rectifier.

The rest of this article is organized as follows. Section II describes the proposed dual-mode active rectifier. Section III shows the building blocks of the proposed rectifier, whereas Section IV presents the dc–dc converter. Experimental results are presented in Section V. Finally, Section VI concludes this article.

II. Proposed Dual-Mode Active Rectifier

A dual-mode active rectifier for the wireless power-receiving unit with high efficiency based on the A4WP and WPC standards with gate charge recycled technique is proposed in this article. Fig. 2 shows the block diagram of the dual-mode active rectifier. The core of the rectifier is composed of four power N-channel metal-oxide semiconductor (NMOS) transistors and each transistor has two core cells, MN1 (MN1_S1, MN1_S2) and MN2 (MN2_S1, MN2_S2) for the low side, and MN3 (MN3_S1, MN3_S2) and MN4 (MN4_S1, MN4_S2) for the high side, one driver cell for per one core cell. In this design, LDMOSFET was used. The core of the rectifier can be divided in accordance with Rx mode (WPC/A4WP). To get the optimum sizes for the power devices, a proper core size test has been performed on the power devices to determine the device with minimum conduction losses and switching losses. In WPC, conduction loss is the dominant factor, the core should be as large as possible to reduce on-resistance and in A4WPC mode, switching loss is the dominant factor, and the core can be reduced compared to the core size of WPC mode. The size of the core can be controlled by the control bit R_RON_ADJ<1:0> and it is automatically selected depending on the mode (A4WP and WPC). It is challenging to attain high PCE for the rectification of the received ac power input due to the high power level and resonance frequency. To improve the efficiency of the rectifier, the proposed charge recycling approach is used after the high side gate driver so that the current produced by the gate driver switching can be recycled and applied to the rectifier output voltage (V_{RECT}) to improve the rectifier's PCE.

The rectifier converts the ac voltages (AC1 and AC2) into dc voltage (V_{RECT}). In rectifier, P-channel metal-oxide semiconductor (PMOS) cross-coupled structures can also be employed to minimize the switching loss in high-side core implementations because they are part of the *LC* resonant tuning capacitor that does not dissipate power [19], [20], [21]. However, because PMOS has a lower mobility than NMOS, the size of the PMOS transistor should be as large as possible to reduce the PMOS V_{DS} voltage drop [22]. Because of the reasons stated earlier, NMOS transistors are used at the high-side core in order to reduce core size while maintaining a low V_{DS} voltage drop. Furthermore, the proposed dual-mode rectifier output voltage (V_{RECT}) is greater than 5 V, allowing the WPR buck converter to provide a constant output voltage of 5 V. As a result, high-voltage lateral double-diffused metal-oxide-semiconductor (LDMOS) core transistors are used in the dual-mode active rectifier to ensure device stability. Boosting voltages (BOOST1, BOOST2) are produced and used to drive high-side NMOS (MN3, MN4) and to ensure MN3 and MN4 have a 5-V V_{GS} voltage. The switching frequency of the A4WP is 6.78 MHz, which is exceptionally high compared to the WPC standard. Therefore, parasitic capacitance and internal circuit delay are the primary switching power losses in A4WP. Even though the exact power transmitter generates switching signals (LG1, LG2, HG1, HG2), which are delayed due to the delays from the drivers (HD1, HD2, LD1, LD2) of power NMOS transistors, results in reverse leakage current flowing through the power NMOS transistors, lowers overall efficiency [5].

In order to minimize the reverse leakage current, two control blocks are used. Open-loop delay circuit (OLDC) for the A4WP mode ZCS circuit is used in the WPC mode rectifier. By using different operating frequencies for A4WP and WPC mode rectifiers, these techniques compensate for the delay and minimize the reverse leakage current. To control the two different modes of a rectifier in the proposed architecture, the analog 2×1 multiplexer has been used. It has two inputs and one output that it controls from the select line. To select mode A (WPC)

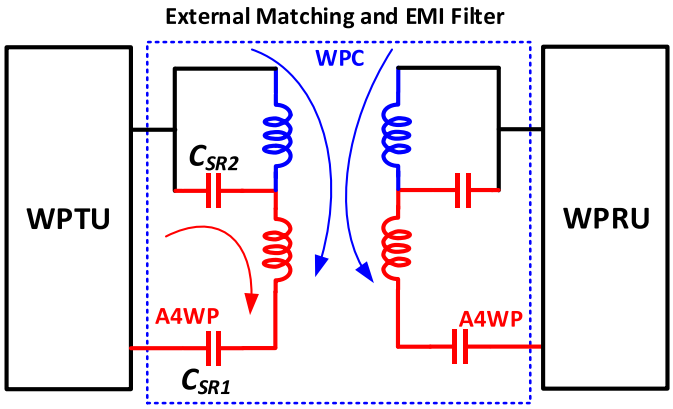


Fig. 3. Block diagram of matching network.

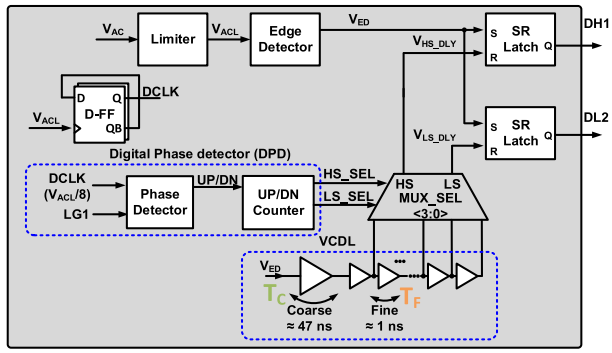


Fig. 4. Block diagram of OLDC.

select line is 0 and to control the B (A4WP) mode, select line is 1. To select a mode in the proposed circuit mux, select line is controlled externally from the graphical user interface. By default, mode A is active.

III. Building Blocks of Proposed Rectifier

A. Matching Network

It is essential to build a matching network that allows power to be transmitted at two different resonant frequencies. To control and operate the system at a resonant state to transfer energy at high efficiency in a WPT system, most research is being focused on the matching network. [23]. In a WPT system, the matching network reduces a large portion of the inductive impedance. The matching network must make sure that a stable function with any load resistance fluctuating from minimum value to an open circuit. C_{SR1} and C_{SR2} are used to implement the matching network for different frequencies, as shown in Fig. 3. Both inductors are enhanced to operate at frequencies ranging from 87 to 357 kHz for WPC and 6.78 MHz for A4WP standards, correspondingly. Two series resonances are provided by the matching network, one at high frequency and the other at low frequency.

B. Open-Loop Delay Circuit

The OLDC block is designed to compensate for reverse leakage current produced by internal circuit delays, such as drivers, and to improve PCE [24]. A block diagram of the proposed OLDC is shown in Fig. 4. An input ac voltage V_{AC} is applied from the external to voltage limiter circuit, which limits the input voltage to 5 V. A voltage limiter (V_{ACL}), an edge detector (V_{ED}), a DPD, a D-flip flop (D-FF) with a divided-by-8 divider (/8 Div.), coarse and fine delay cells, a multiplexer (MUX), and an SR latch make up this circuit. The OLDC in Fig. 4 is used to synchronize the driver's output falling edge LG2, with the zero-crossing point of the ac signal, AC2 so that the MN2 can be turned OFF when AC2 becomes negative and AC1 climbs from negative to positive. In Fig. 5, the falling edges of DCLK and LG2, which are the voltage signal of AC2 and the final gate control signal of MN2, are compared using the DPD. V_{ACL} falling edge is generated as $V_{LS\cdot DLY}$, which is the delayed signal of V_{ED} through the coarse and fine delay cells. In OLDC, coarse delay is used to drive the loop near to the lock state and a fine delay line is used to make minor fine-tuning to the output phase. The input of coarse delay is the output of the edge detector. Ten delayed signals from coarse and fine delay cells are applied to the input of MUX and can be selected from DPD by MUX [3:0], synchronizing LG2 falling edge with that of V_{ACL}. In an OLDC, the coarse delay gives 47-ns delay and the fine delay gives 1 ns shown in the simulation result in Fig. 6. When the functions of DL1 and DL2 are switched after the comparison, the rectifier's internal signals need some time to settle down.

The frequency of V_{ACL} is divided by 8 and used as a DPD clock for the settling time of the rectifier. In DPD, two inputs voltage signals DCLK and LG2 are compared and the result is generated at two outputs UP and DN. The two output of DPD presents the phase difference between DCLK and LG2. Since the DPD does not care about the frequency and only checks the phase difference it selects, the closest edge to be compared even though eight falling edges is located in LG2. In the ideal case, if the UP signal is active, DN will be low and reverse. When DCLK and LG2 are synchronized subsequently, the counter stops counting. When the falling edge of DCLK lags behind that of LG2, the DPD adds 1 to the value of MUX [3:0], allowing the delay to be increased. Otherwise, when the falling edge of DCLK precedes that of LG2, the DPD subtracts 1 from the value of MUX [3:0] to reduce the delay. V_{ED} is utilized as a set signal and $V_{LS\cdot DLY}$ is used as a reset signal through the SR latch, resulting in DL2 being generated and applied to the input of gate driver LD2. The DPD comparison is repeated a certain amount of times and is completed when the falling edges of DCLK and LG2 are synchronized reducing the reverse leakage current in the circuit and improving the PCE.

C. ZCS Circuit

In WPC mode, active rectifier ZCS circuit is used for 150-kHz frequency. The reverse leakage current should be kept to a minimum to enhance the PCE of the active rectifier. The ZCS circuit is used to reduce the amount of reverse leakage current produced when the incorrect input signal is applied to the gates of core MOSFET. A reverse leakage current develops during the ON

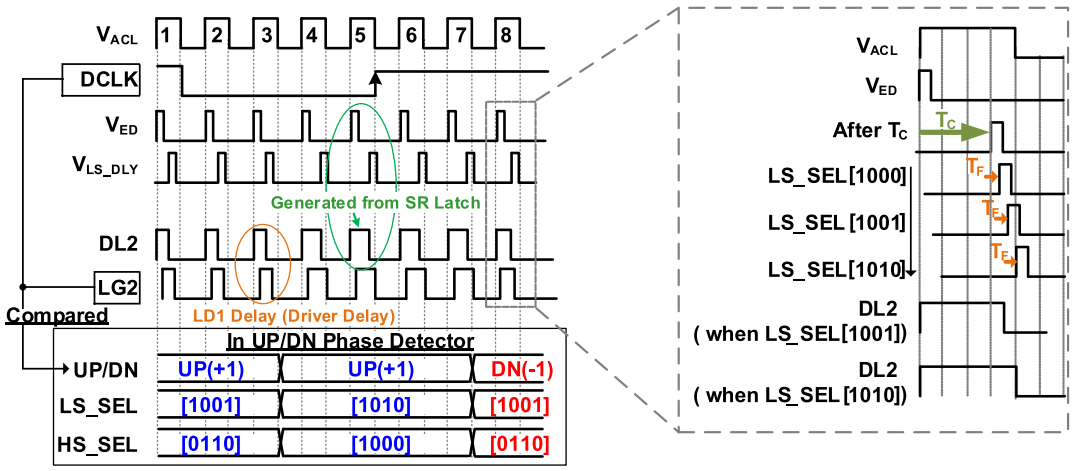


Fig. 5. Timing diagram of OLDC.

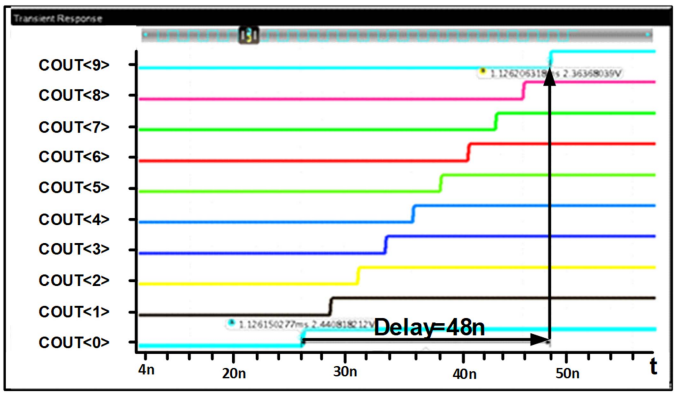
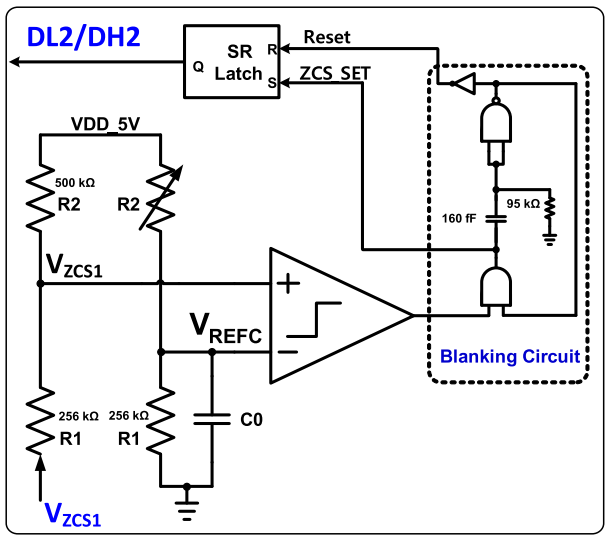
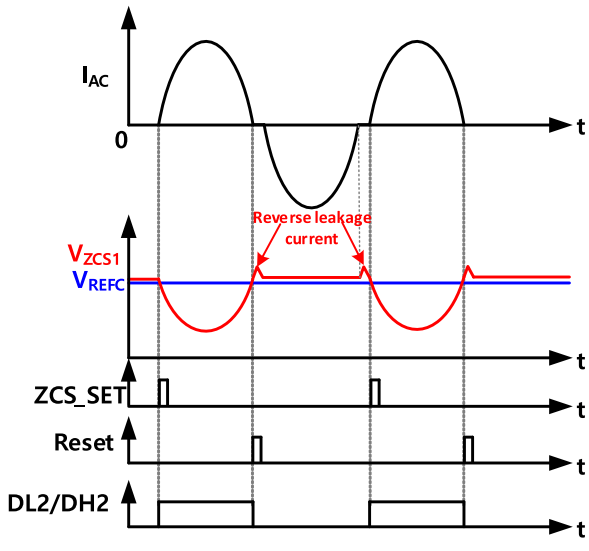


Fig. 6. Simulation result of coarse and fine delay.



(a)



(b)

Fig. 7. (a) ZCS circuit. (b) Timing diagram of ZCS circuit.

operating time, reducing efficiency and causing heat generation. To increase efficiencies, the ZCS circuit is used to detect the current such that the gate signal is switched OFF before the sensed current decreases to a negative value. From Fig. 2, currents I_{SEN1} and I_{SEN2} flow from sensing MOSFETs (MSEN1 and MSEN2) to the dividing resistors, and V_{ZCS1} and V_{ZCS2} flow to the ZCS circuit. Fig. 7(a) shows a block diagram of the ZCS circuit. It is critical to detect the edge and create the gate signal by adding delay to reduce reverse leakage current. The value of V_{ZCS} is determined by the sensed signal V_{ZCS1} and voltage division of R_1 and R_2 in the ZCS circuit, as shown in the following:

$$IN\_V_{\mathrm{ZCS}} = (VDD\_5V - V_{\mathrm{ZCS1}})\frac{R_1}{R_1 + R_2}. \qquad (1)$$

In the ZCS, circuit voltage is distributed between R_1 and R_2, which reduces V_{ZCS1} signal, due to which the difference between V_{REFC} and V_{ZCS} becomes small, and the gate signal is cut OFF due to the glitch phenomenon. A BC is used to eliminate the glitch problem that occurs as a result of noise generated during switching, shown in the simulation result of the ZCS circuit in Fig. 8. Fig. 7(b) shows the timing diagram of the ZCS

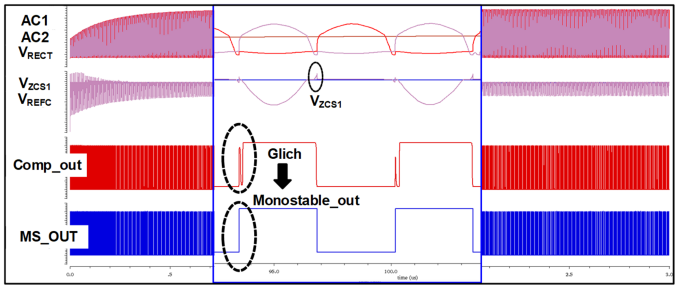


Fig. 8. Simulation result of ZCS circuit.

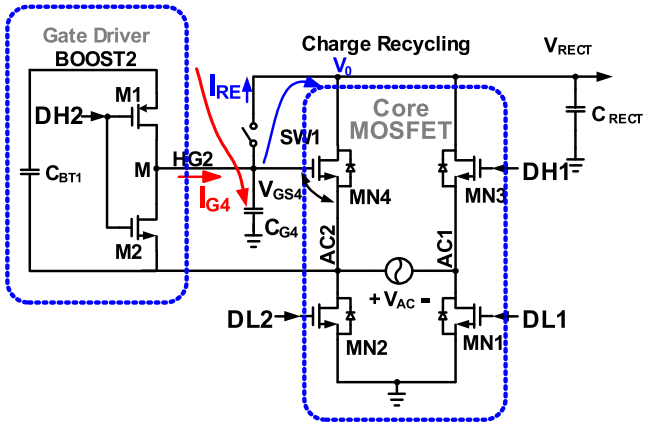
circuit. It compares reference voltage (V_{REFC}) with sensing signal (V_{ZCS}) and generate I_{AC} by removing reverse leakage current. The SR-Latch circuit generates ZCS set/reset signals, which are used to produce the correct timing of the gate signal.

D. Gate Charge Recycling Technique

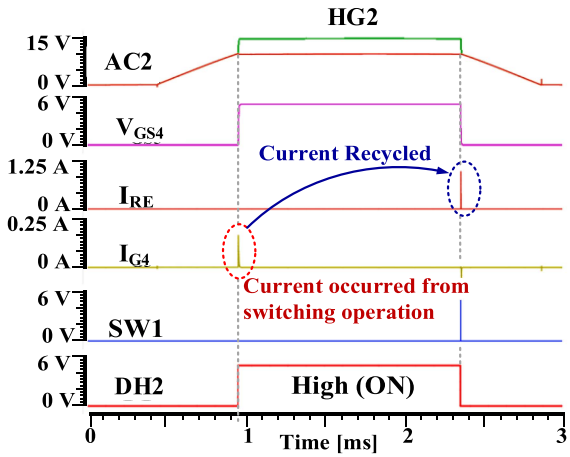
Current charging and discharging gate capacitances, which are primarily utilized to drive the rectifier power switches, cause switching loss. The switching is mostly caused by the switching power consumption of CMOS circuits, which may be represented as

$$P_{SW} = CV^2 f_s \tag{2}$$

where C is the switching capacitance, V is the gate swing voltage, and f_s is the switching frequency. Thus, switching power consumption must be reduced in order to enhance active rectifier efficiency. According to (2), the switching loss can be reduced by minimizing the switching frequency or reducing switching capacitance. Several design methods for decreasing switching loss have been described. To optimize the tradeoff between effective gate capacitance and power transistor on-resistance, a segmented power stage control can be utilized [25]. It can, however, increase switching activity and complexity. In an active rectifier, the gate charge recycling technique is proposed to reuse the current produced by the switching of the high side gate driver of the rectifier and recycled to the rectifier output voltage in order to improve the power efficiency. In every switching cycle, the proposed charge recycling circuit stores the current produced by switching OFF the power transistors M1 and M2 in the capacitor C_{G4} and transfers it to the output. A simplified block diagram of the gate charge recycling technique is shown in Fig. 9(a). The core MOSFET is composed of the four NMOS power transistors MN1, MN2, MN3, and MN4 are driven by the gate driver, and are controlled by the switching signals DH2, DL1, and DH1, DL2. In DH2 and DL1 phase, MN4 and MN1 turn ON and in DH1 and DL2 phase, MN2 and MN3 turn ON. During DH2 and DL1 phase, M1 and M2 of the gate driver turn ON and OFF as the voltage increase from 0 to 5 V. After this, the current of I_{G4} flows from M and charges the gate capacitance of MN4, driving the power switch MN4 and in the next phase DH1 and DL2, the gate capacitance of MN4 discharge, due to the charging and discharging of parasitic gate capacitors, resulting in excessive storage and release of energy. Hence, switching loss occurs. The



(a)



(b)

Fig. 9. (a) Gate charge recycling circuit. (b) Simulation result of charge recycling circuit.

current I_{G4} generate from the gate driver of high-side MOSFET is stored in C_{G4}. When the DH2 and DL1 phase is operated at high, at that time, DH1 and DL2 phase is operated at low and SW1 is OFF. If DH1 and DL2 phase is operated at high, DH2 and DL1 phase becomes low, SW1 is ON for 4.039 ns. Therefore, switching loss is stored in the capacitor. When DH1 and DL2 become low, SW1 is closed for a period of time 4.061 ns, allowing the stored charge in C_{G4} to be transmitted to V_0 node and added to V_{RECT} as a discharge starts. The same charge recycling process occurs in the MN3 power transistor when DH2 and DL1 phase becomes low.

The charge capacitor size and switch are the most important factors in gate charge recycling. The switch (SW1) has 35-mΩ on-resistance is made using the high voltage component given by the process because V_{RECT} and BOOST2 are both high voltages. Furthermore, the capacitor is quite huge, and the size of the capacitor was chosen by considering the area on the layout. The standard specification value of the switching capacitance of 190 pF is determined based on the simulation results. The simulation result of the proposed charge recycling technique conceptual operation is shown in Fig. 9(b). As previously stated,

TABLE I
POWER CONSUMPTION ANALYSIS OF RECTIFIER

Parameters	WPC Mode	A4WP Mode
Conduction losses	4.5%	3.6%
Switching losses	0.17%	1.6%
Gate driver losses	0.07%	0.3%
Internal circuit losses	0.56%	1.1%
Total losses	5.3%	6.6%
Input power	7.5 W	7.5 W
Output Power	7.1 W	7 W
Efficiency	94.7%	93.4%

the current generated by the driver switching operation is stored in capacitor C_{G4} and added to the output voltage V_{RECT}. When AC2 goes high, HG2 becomes higher than the AC2 from the boosting circuit BOOST2. When the DH2 and DL1 transition occurs from 0 to 5 V, current I_{G4} generate from the gate driver. I_{G4} is stored in the C_{G4} until the SW1 is turned ON. When DH2 and DL1 phase becomes OFF and the transition occurs, SW1 is turned ON for a set period to allow the charge stored in capacitor C_{G4} to flow through I_{RE}. As can be seen from the simulation results, the current I_{G4} is recycled to I_{RE} to improve overall efficiency.

The overall power consumption of the dual-mode active rectifier is summarized in Table I. The breakdown of power usage for each state has been presented, which consists of conduction, switching, gate driver, and internal circuit losses, as well as total losses, which are the parameters evaluated while analyzing power losses.

IV. DC–DC CONVERTER

The step-down dc–dc converter uses two N-type high-voltage LDMOS in the power stage, as shown in Fig. 10. NMOS transistors are used at the high side instead of PMOS in order to reduce the area and PMOS has limited voltage rating as compared to NMOS. The input of the step-down dc–dc converter is connected with the output voltage (V_{RECT}) of the active rectifier. In the WPT system, ripples frequency in V_{RECT} is double the frequency of V_{AC}. Due to ripples in V_{RECT}, the dc–dc converters' functioning has to be more stable. The pulsewidth modulation (PWM) technique is used in the dc–dc converter that has been designed. In this technique, the control voltage is proportional to the duty cycle of gate driver signals that control the power switches (MH and ML).

Two enhancement mode power switches of step-down dc–dc converter MH and ML are employed at the high side and low side. Due to fast *di/dt* in the switch, a voltage spike occurs. It produces radiated electromagnetic interference and is conducted in the system [26]. Voltage spike drains out the battery energy and reduces the efficiency. When the voltage spike is very high, it consumes a large portion of harvested power, thus lowering the total efficiency of the dc–dc converter. To make the power

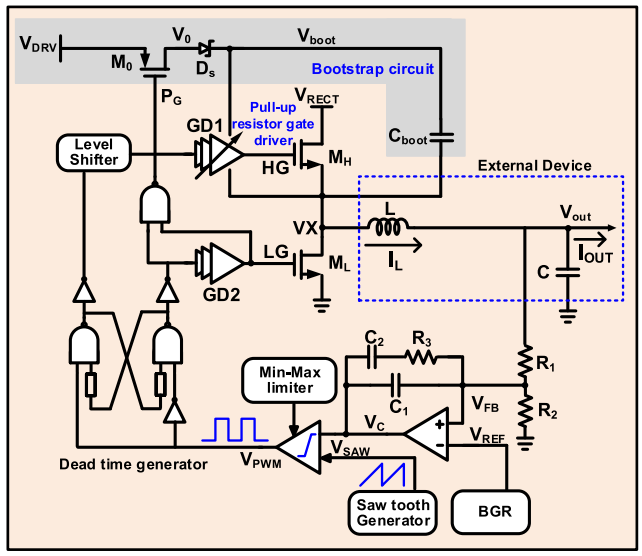


Fig. 10. Step down dc–dc converter.

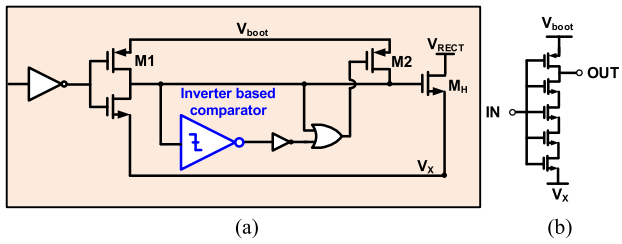


Fig. 11. (a) Dynamic pull-up resistor gate driver. (b) Multiple series inverter.

device safe from voltage spikes, a resistor is placed between GD1 and HG to limit the driving current. Using a resistor, on the other hand, will slow down the transition time, resulting in a large switching loss. So, a dynamic pull-up resistor gate driver circuit is implemented in this step-down dc–dc converter, which offers a dynamic pull-up resistor to drive MH and suppress the gate to a source voltage spike. Fig. 11(a) shows the dynamic pull-up resistor gate drivers circuit and Fig. 11(b) is a multiple series inverter. M1 is operated by a duty signal, whereas M2 is controlled by a duty signal as well as a feedback loop. When the input signal becomes high, M1 and M2 both turn ON, driving M_H at the same time. When V_{gs} of M_H approach V_{boot}, M2 shuts OFF, which is detected by the comparator and prevents voltage spikes. The maximum driving current I_{Max} is calculated as follows:

$$I_{\text{Max}} = \frac{V_{\text{boot}} - V_x}{R_{\text{on},M1} // R_{\text{on},M2}}. \tag{3}$$

$R_{\text{on, M1,}}$ and $R_{\text{on, M2}}$ are the ON resistors of M1 and M2, respectively.

A comparator detects M_H gate-to-source voltage. A multiple series inverter is used rather than a continuous-time comparator because a continuous-time comparator has a considerably higher

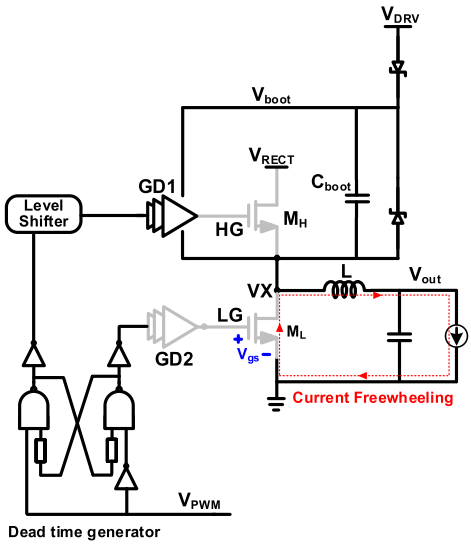


Fig. 12. Inductor current path during dead time.

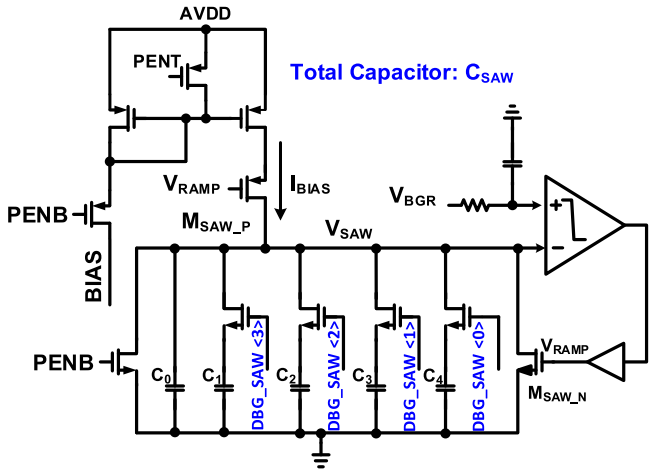


Fig. 13. Circuit diagram of saw-tooth generator.

quiescent current and propagation delay than Schmitt trigger inverter and its transition voltage is also high.

Using the standard bootstrap circuit during dead time has a critical flaw. Because of the body diode, inductor current flows through ML in Fig. 12. We can observe that the ML operates in the saturation area, with Vx dropping to –3 V. V_{DRV} will charge the $\mathrm{C_{boot}}$ voltage up to 8 V, resulting in the breakdown of V_{gs} of $\mathrm{M_H}$ and high side driver. In practice, $\mathrm{C_{boot}}$ cross voltage is clamped at the Zener diode breakdown voltage by adding a Zener diode parallel to it. This method will result in an increase in power consumption. Another method is to connect the Schottky diode in parallel with the low-side power switch ($\mathrm{M_L}$). During current wheeling, a Schottky diode clamps the switching node voltage Vx to 0.2 V. $\mathrm{C_{boot}}$ will not overcharge however, adding an additional diode increases the parasitic capacitor at Vx, resulting in higher switching loss. So, the proposed bootstrap circuit is used that avoids V_{DRV} charging $\mathrm{C_{boot}}$, during the dead time and during high-side turns ON time. The proposed bootstrap circuit basic concept is to avoid V_{DRV} charging $\mathrm{C_{boot}}$ during the dead time and high side turns ON periods and allows the buck converter to continue operation at input rectifier voltage. The bootstrap rail voltage is 4.8 V. The proposed bootstrap circuit is shown in Fig. 10. The switch $\mathrm{M_0}$ controls the charging route of the bootstrap circuit. Sensing the input and output signals of the low side gate driver generates $\mathrm{P_G}$ control signal. During dead time, the $\mathrm{P_G}$ goes high, and the high side switches ON. The on-resistance (0.147 Ω) of $\mathrm{M_0}$ is properly designed in order to operate at high switching frequencies. During $\mathrm{M_H}$ turns ON time, $\mathrm{D_S}$ is utilized to prevent the high voltage of V_{boot}, the body diode of $\mathrm{M_0}$ clamp V_0 below $V_{\mathrm{DRV}} + V_{\mathrm{D}}$, that is why the high voltage will be applied across $\mathrm{D_S}$, whose die size is 0.377 $\mathrm{cm^2}$ rather than $\mathrm{M_0}$ $\mathrm{V_D}$ is the forward diode voltage. Because of $\mathrm{D_S}$, $\mathrm{M_0}$ may be performed using a low-voltage device, eliminating the requirement for a level shifter.

The step-down dc–dc converter consists of a bandgap reference, which generates the internal reference voltage (V_{REF}).

TABLE II
PERFORMANCE PARAMETERS OF DC–DC CONVERTER

Process	0.18 μm
Input Voltage (V_{IN})	7 ~ 10 V
Output Voltage (V_{OUT})	5 V
High side turn on / off propagation delay	4.076 ns / 4.095 ns
Low side turn on / off propagation delay	5.302 ns/ 3.431 ns
Switching Frequency (F_{SW})	2 MHz
Load Current Range (I_{LOAD})	0 ~ 1.2 A
Inductor (L)	2.2 μH
Output capacitor	100 μF
Effective Series Resistance (R_{ESR})	2 μm
Peak Power Efficiency	93.2% @ 0.5 A

The voltage difference between the feedback voltage (V_{FB}) and reference voltage (V_{REF}) is control voltage (V_{C}). In Fig. 10, L and C are the output capacitor and dc–dc converter inductance, respectively. A 2-nF bootstrap capacitor is fully on-chip to reduce the gate loop parasitic inductor. The compensating feedback loop is made up of R_1, R_2, R_3, C_1, and C_2. V_{C} is the output of the error amplifier that is fed to the comparator. The comparator compares the saw-tooth voltage (V_{SAW}) with V_{C} and provides a pulse signal. The frequency of the dc–dc converter was produced using a saw-tooth generator illustrated in Fig. 13. The switching frequency of the dc–dc converter is 2 MHz. Table II shows the specifications of the proposed dc–dc converter. In order to achieve stability, the switching frequency should be kept high [27]. The min–max duty generator is utilized in the dc–dc converter to prevent unwanted feedback voltage. If the output V_{C} of the error amplifier is higher than the amplitude of V_{SAW}, the output of V_{PWM} becomes ground. Therefore, the closed-loop does not operate the same as the linear regulator.

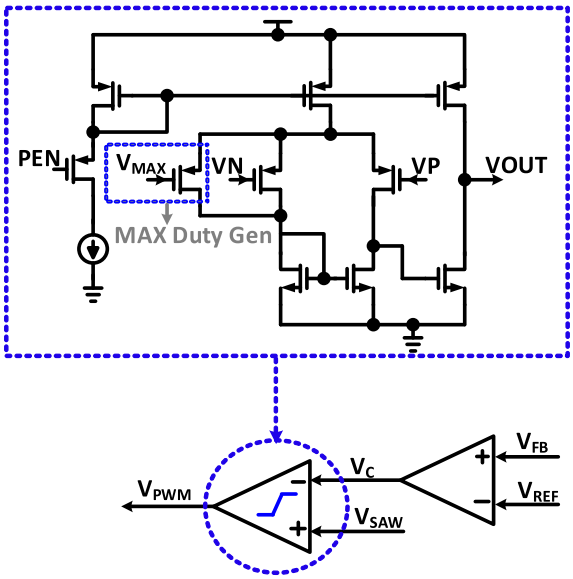


Fig. 14. Circuit diagram of max generator.

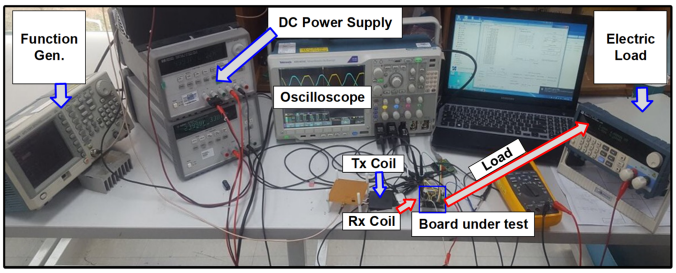


Fig. 15. Measurement setup for PMIC.

Various methods are used to prevent this phenomenon, but it can be constructed by simply adding the same MOSFET as the input MOSFET, as shown in Fig. 14. The gate voltage of additional MOS, which is for MAX Duty Gen., is higher than the voltage that the duty of V_{PWM} can be maximum, and lower than the amplitude of V_{SAW}. Without the max generator, if the V_{C} voltage is higher than V_{SAW}, V_{PWM} will be set to 0 and the dc–dc buck converter will not operate.

The pulse signal (V_{PWM}) is fed to the dead time generator (nonoverlap circuit) that generates two driver control signals for the high-side ($\mathrm{M_H}$) and low-side ($\mathrm{M_L}$) switch, to avoid $\mathrm{M_H}$ and $\mathrm{M_L}$ turning ON at the same time. Turn-ON delay generators are applied in an adaptive dead time control circuit [28], [29], [31]. To optimize the dead time, a dead time generator is used for better efficiency.

V. Experiment Results

Fig. 15 illustrates the measurement environment of the PMIC for the WPT system. Magnetic fields are employed in the WPT system to transfer energy from the primary (Tx) coil to the secondary (Rx) coil. A high-frequency alternating current passing through the primary (Tx) coil produces an electromagnetic field. When both coils resonate at the same frequency, maximum

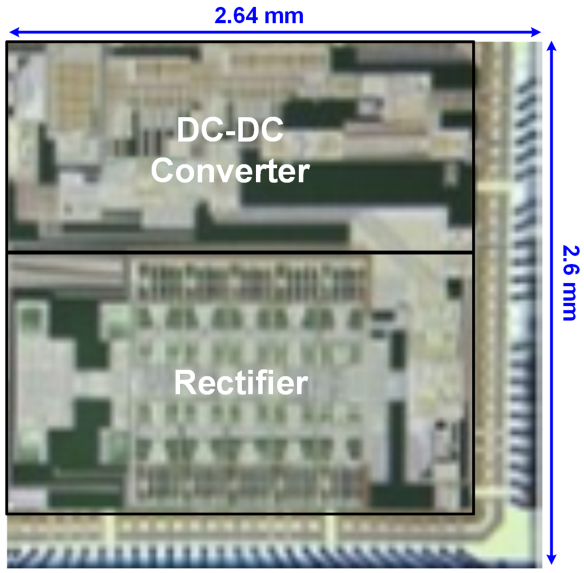


Fig. 16. Microphotograph of the proposed chip.

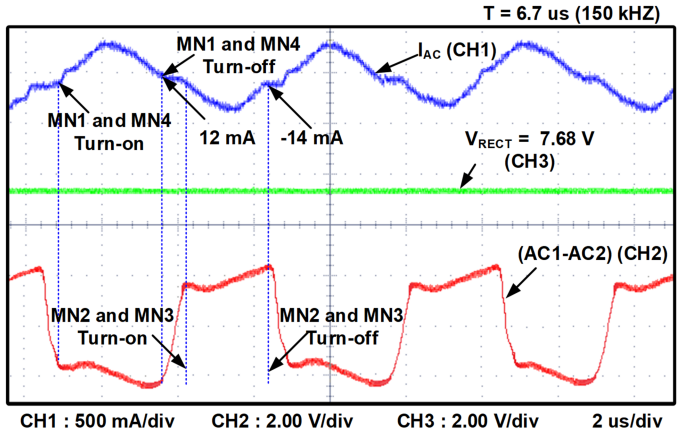


Fig. 17. Measurement result of WPC mode active rectifier.

power is transferred. The Rx coil is located under the Tx coil and the measurement setup consists of the serial peripheral interface control, an oscilloscope, a power supply, an electronic load, a function generator, and the test board. Fig. 16 shows the microphotograph of the chip. The active die area of the power management IC is 2.64 mm $\times$ 2.6 mm, including electrostatic discharge designed with IP6M 0.18-μm CMOS.

The measurement result of the WPC mode active rectifier is shown in Fig. 17. The ZCS circuit senses the current (I_{SEN1} and I_{SEN2}). When I_{AC} is 12 mA, MN2 and MN3 are turned OFF. When I_{AC} current is –14 mA, MN1 and MN4 are turned OFF. Therefore, it minimizes the reverse leakage current. Fig. 18 shows measurement results of the active rectifier in the A4WP mode application. The measured V_{RECT} of the active rectifier is 9.1 V with 93.4% efficiency and the output voltage of the dc–dc converter is 5 V. Fig. 19 shows the WPC and A4WP mode active rectifier efficiency with and without charge recycling technique in relation to the load current. The maximum efficiencies of the

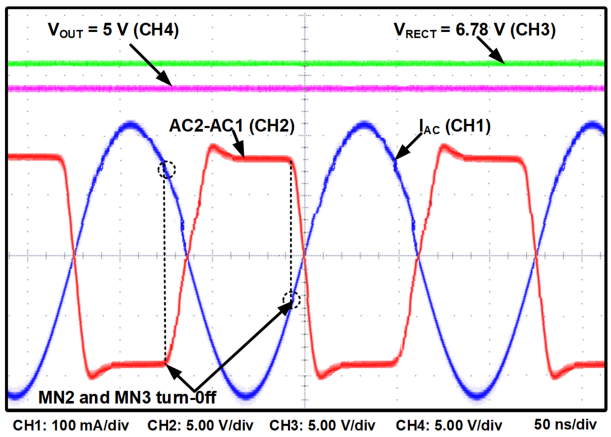


Fig. 18. Measurement result of A4WP mode active rectifier.

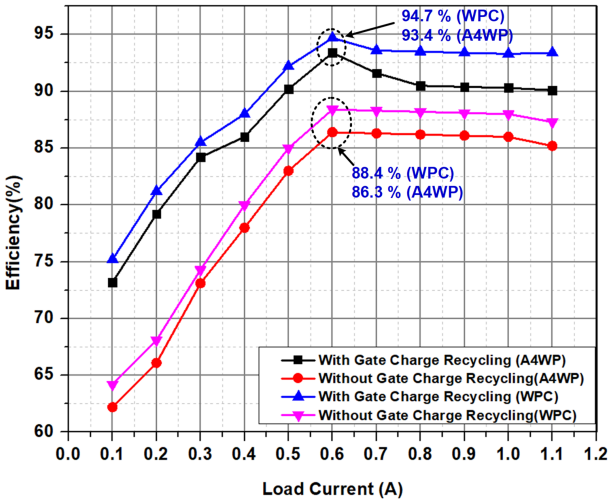


Fig. 19. Measured PCE of WPC and A4WP mode active rectifier with and without gate charge recycled technique.

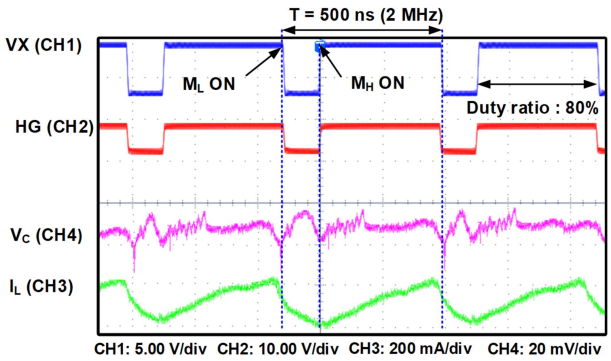


Fig. 20. Measured result of the dc–dc converter.

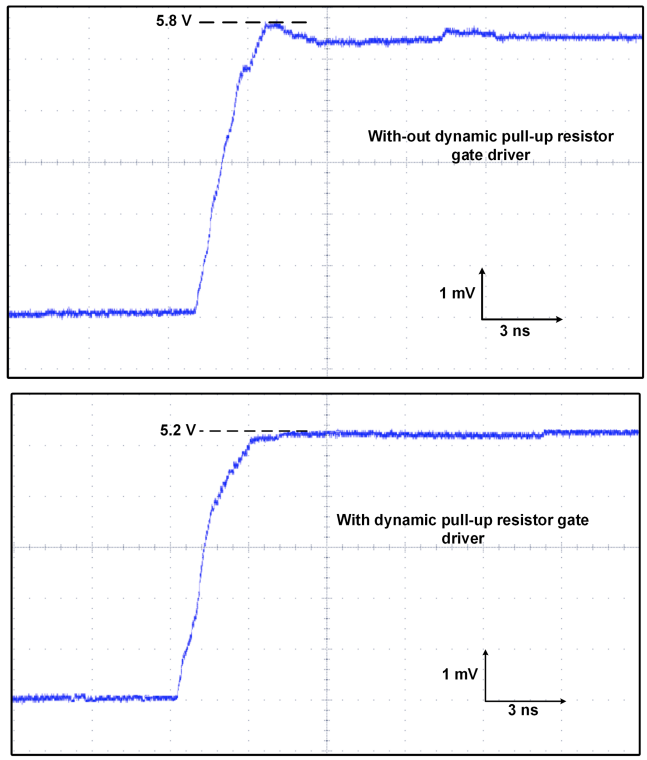


Fig. 21. Measurement result of dynamic pull-up resistor gate driver.

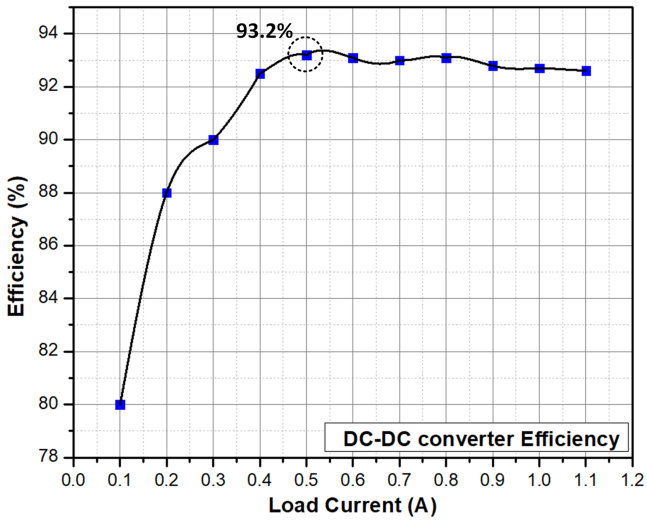


Fig. 22. Measured power efficiency of dc–dc converter.

active rectifier in WPC mode with and without charge recycling technique are 94.7% and 88.4% and 93.4% and 86.3% of A4WP at 600-mA load currents, respectively.

Measurement results of the dc–dc converter are shown in Fig. 20when the load current is 500 mA, the duty ratio is 80%, and the switching frequency is 2 MHz. Fig. 21 shows the measurement result of the dynamic pull-up resistor gate driver. The dynamic pull-up resistor gate driver suppresses a 600-mV voltage spike. PCE of the dc–dc converter is shown in Fig. 22 with respect to the load current. The measured maximum PCE is 93.2% at 500-mA load current. Table III shows the comparison of this research work with recent reference papers [1], [7], [9], [23], [25]. In this article, the PCE of the dual-mode active rectifier and dc–dc converter is higher than the prior works, and system efficiency is also higher than prior works.

TABLE III
COMPARISON TABLE WITH PRIOR WORKS

Parameters	[1]	[5]	[11]	[21]	[24]	**This Work**
Technology	0.18 µm	0.18 µm	0.35 µm	0.35 µm	0.18 µm	**0.18 µm BCD**
Standards	A4WP,WPC and PMA	A4WP	----	A4WP	A4WP	**A4WP and WPC**
Applied Frequency	6.78 MHz / 85-500 KHz	6.78 MHz	13.56 MHz	3.23MH/ 6.78 MHz	6.78 MHz	**6.78 MHz / 87-357 KHz**
Rectifier load value	0.6 A	0.8 A	500 Ω	----	0.1 A	**0.6 A**
Rectifier Efficiency	91.7% @6.78 MHz 92.7% @150 KHz	91.5%	91.4%	81% @3.23 MHz 74% @6.78 MHz	82.14%	**93.4% @6.78 MHz 94.7% @150 KHz**
DC-DC load value	0.5 A	0.3 mA ~ 1.2 A	----	----	----	**0.5 A**
DC-DC converter Efficiency	92.3%	92.7%	Rectifier only	92.5%	Rectifier only	**93.2%**
System Efficiency	84.5% @6.78 MHz 85.5% @ 150 KHz	80.86%	----	75%	-----	**86.7% @ 6.78 MHz 88.2%@150 KHz**

VI. CONCLUSION

This article presents the design of PMIC for WPRs in dual-mode applications. An active rectifier with high efficiency is designed using A4WP and WPC applications with charge recycling approach is applied after the high side gate drive so that the current produced by the gate driver switching can be reused and recycled to the rectifier output voltage (V_{RECT}) to improve the rectifier PCE. The proposed bootstrap circuit in the step-down dc–dc converter is used to avoid V_{DRV} charging C_{boot} during the dead time and high side turns ON periods. Moreover, it also prevents overcharge issues. A dynamic pull-up resistor gate driver suppresses the gate to a source voltage spike. A dead time generator is used to generate the high-side driver and the low-side driver control signal to prevent high-side and low-side power switches from turning ON at the same time. The chip is implemented in a 0.18-μm bipolar-CMOS DMOS process. The WPC mode active rerectifier's highest PCE is 94.7%, and A4WPC mode active rectifier is 93.4%. The dc–dc converter maximum PCE is 93.2%, with a system efficiency at A4WP mode and WPC mode are 86.7% and 88.2%, respectively.

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