Open-Circuit Switching Fault Analysis and Tolerant Strategy for Dual-Active-Bridge DC–DC Converter Considering Parasitic Parameters

Yu Wang, *Member, IEEE*, Yuanpeng Guan, Marta Molinas, *Senior Member, IEEE*, Olav Bjarte Fosso, *Senior Member, IEEE*, Wang Hu, and Yun Zhang

***Abstract*—The dual-active-bridge (DAB) is a typical topology of dc–dc converter for bus connection, voltage conversion, power transmission, and electrical isolation in dc power grids. The open-circuit switching fault (OCSF) may threaten the safe operation of DAB and should be eliminated in time. However, the researches on parasitic parameters mainly focus on traditional dc–dc converters, and there are still few discussions on parasitic parameters in the high-frequency dc–dc converter such as DAB. The power components are usually considered without parasitic parameters in OCSF analysis and tolerant control, leading to deviations in modality analysis and practical control for DAB. To solve this issue, the modality analysis considering parasitic parameters during OCSF in DAB is investigated, and the sneak circuits and electrical characteristics with parasitic parameters are discussed in this article. Besides, to realize fault tolerance for DAB during OCSF considering parasitic parameters, a new fault tolerance control strategy including modeling, topology transformation principle, and practical control architecture are also proposed. Compared with conventional fault tolerance strategy, the proposed strategy will be more efficient, rapid and feasible for DAB during OCSF process. The experimental results in DAB prototype verify correctness and effectiveness of analysis and proposed strategy.**

***Index Terms*—Dual active bridge dc–dc converter, fault tolerance strategy, modality analysis, open-circuit switching fault, parasitic parameters.**

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Yu Wang and Yun Zhang are with the School of Automation, Guangdong University of Technology, Guangzhou 510006, China (e-mail: yuwang@gdut.edu.cn; yun@gdut.edu.cn).

Yuanpeng Guan is with the Energy Electricity Research Center, Jinan University, Zhuhai 519070, China (e-mail: guanyuanpeng@126.com).

Marta Molinas is with the Department of Engineering Cybernetics, Norwegian University of Science and Technology, 7491 Trondheim, Norway (e-mail: marta.molinas@ntnu.no).

Olav Bjarte Fosso is with the Department of Electric Power Engineering, Norwegian University of Science and Technology, 7491 Trondheim, Norway (e-mail: olav.fosso@ntnu.no).

Wang Hu is with the School of Electric Power, South China University of Technology, Guangzhou 510641, China (e-mail: huwang1028@foxmail.com).

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NOMENCLATURE

Ac	Alternating current.
C_P	Capacitance on primary side of DAB.
C_{S}	Capacitance on secondary side of DAB.
c_{p}	Equivalent parasitic capacitance on primary side.
c_{s}	Equivalent parasitic capacitance on secondary side.
DAB	Dual-active-bridge.
DC	Direct current.
DPS	Dual-phase-shift.
d	Phase-shift angle in High-frequency modulation.
f	Operation frequency of DAB.
$G_{\mathrm{DAB\text{-}N}}$	Loop gain of DAB under normal operating.
$G_{\mathrm{DAB\text{-}FT}}$	Loop gain of DAB under proposed strategy.
HFL	High-frequency-link.
I_{P}	Dc current on primary side of DAB.
I_{S}	Dc current secondary side of DAB.
i_{Lp}	HFL current on primary side.
i_{Ls}	HFL current on secondary side.
$i_{\mathrm{L\text{-}max}}$	Maximum value of HFL current.
L_{T}	Equivalent inductance of HFL transformer.
OCSF	Open-circuit switching fault.
P_{DAB}	Transmission power of DAB.
$P_{\mathrm{DAB\text{-}FT}}$	Transmission power of DAB under proposed fault tolerant strategy.
PI	Proportional Integral.
n	Voltage ratio of HFL transformer.
R_{T}	Parasitic resistance of HFL transformer.
SPS	Single-phase-shift.
SVPWM	Space vector pulse width modulation.
TPS	Triple-phase-shift.
t_{f}	Time interval between t_7 and t_8.
U_{P}	Dc voltage on primary side of DAB.
U_{S}	Dc voltage on secondary side of DAB.
U'_{p}	Equivalent ideal dc voltage with ideal switches on primary side of DAB.
U'_{s}	Equivalent ideal dc voltage with ideal switches on secondary side of DAB.
u_{p}	HFL voltage on primary side.
u_{s}	HFL voltage on secondary side.
ZVS	Zero-voltage-switch.
ω_{n}	Natural frequency.
ζ	Damping ratio.

I. Introduction

In RECENT years, with a large consumption of fossil-based energy and the risk of climate change, a global demand of renewable energy is increasing. With the rapid development of renewable power sources, energy storage, and dc equipment, the dc power grids have been significantly attracting global attentions and become important elements for future power systems [1], [2]. In dc power grids, the dc–dc converter plays an important role in buses connection, voltage conversion, power transmission, and electrical isolation. Therefore, the long-time stability and reliability of dc–dc converter are significant to maintain the safe, reliable, and efficient operation of dc power grids [3], [4].

Among various topologies of dc–dc converter, the high- frequency isolated dual-active-bridge (DAB) becomes a typical topology and attracts attentions from researchers and engineers [5], [6]. For the DAB dc–dc converter, the stable operation and reliability are the primary concerns. It is highly required that the DAB maintains operation without any interruption or significant degradation of performance when semiconductors failure. The open-circuit switching fault (OCSF) caused by failures in switches or switch driving circuits is a typical phenomenon, causing a dc bias in HFL current, an overcurrent in semiconductors in faulty full-bridge and even a serious shutdown or damage to converter [7], [8]. Besides, if the OCSF status cannot be solved within a specified time, the operation of DAB may be terminated and the service life of semiconductors may be greatly reduced.

To study the OCSF phenomena and characteristic in DAB, the modality analysis is an effective method. In the existing literature on modality analysis for OCSF, the switches in DAB are usually considered as ideal ones, and parasitic parameters of switch in DAB are always neglected [9], [10]. Besides, the HFL transformer in DAB are usually considered as an ideal inductance in modality analysis during OCSF as well [11], [12]. However, the parasitic parameters of switches and transformer may lead to the unexpected operating modes, resonance, and oscillation in HFL electrical quantities and the deviation and error in modality analysis and controller design, causing the failures of power devices, instability issues of control system, and even the cascaded faults in devices and converters during OCSF process [13]–[15].

Unfortunately, the current research on parasitic parameters mainly focus on conventional dc–dc converters such as buck and boost, and only a few literatures concerned the parasitic parameters in high-frequency dc–dc converter such as DAB [16], [17]. At present, the existing researches on parasitic parameters in DAB mainly contains the stray capacitance of HFL transformer on high-frequency oscillation, the winding capacitance, resistance, and leakage inductance in transformer winding design, the influence of parasitic parameters on the switching characteristics and the precise parasitic parameters identification method [18]–[20]. However, the influence from parasitic parameters on the electrical characteristics, modality analysis, and fault tolerance control of DAB during OCSF have not yet been discussed and studied.

Moreover, based on the modality analysis of OCSF process, the fault tolerance strategies were proposed and investigated to realize the normal operation of DAB during OCSF [21]–[23]. At present, the existing fault tolerance strategies for dc–dc converter mainly include following approaches.

1) *Installing redundant switches*. By implementing the redundancy switch, the OCSF switches can be diagnosed, isolated and replaced for dc–dc converter. However, the fault tolerance strategy by installing redundant switches increases the construction cost and the complicated of topology, leading to difficulty in analysis and control realization [24]–[26].
2) *Reconstruct the converter topology*. By reducing the number of phases or voltage levels when OCSF happens, the fault switches can be isolated. However, the converter operates with a high voltage or current levels in switches under this approach, leading to the additional consumption and the operational risks [27]–[29].
3) *Modifying the SVPWM*. By applying modulated PWM signal out of OCSF switching area, the fault tolerance can be achieved.

However, the SVPWM is difficult to achieve fault tolerance on ac side with symmetrical waveform and low switching cost [30]–[32]. In addition, the existing fault tolerance strategy for DAB mainly on the topology transformation and modulation, and the control loops and parameters evaluation process are complicated, leading to the lack of applied theoretical support and poor practicality. Therefore, a more rapid, efficient and practical fault tolerance strategy for OCSF process in DAB is needed, and further study on control architecture, operation mechanism, and application have the theoretical and practical values [33], [34].

To address the abovementioned issues, a modality analysis considering parasitic parameters for OCSF process in DAB is investigated in this article, and the influence from parasitic parameters on potential sneak circuit, HFL electrical quantities, and operating characteristics in OCSF process are investigated, providing the theoretical and practical references for topology construction, OCSF process analysis and control design for DAB. Besides, a fault tolerance strategy including topology switching principle, practical control architecture, and operating characteristic are proposed. The proposed strategy can eliminate the dc bias, current spike, and oscillation in HFL electrical quantity and maintain stable and efficient operation for DAB during OCSF process. Compared with conventional fault tolerance strategy, the proposed fault tolerance strategy is simple, rapid, efficient, and feasible for DAB during OCSF process, providing a feasible, efficient, and practical fault tolerance scheme for DAB considering parasitic parameter.

II. Modality Analysis of OCSF Process in DAB Considering Parasitic Parameters

The topology configuration of DAB is presented in Fig. 1. The U_{P}, U_{S}, I_{P}, and I_{S} are dc voltages and currents, and C_P and C_{S} are capacitors on primary and secondary sides, respectively.

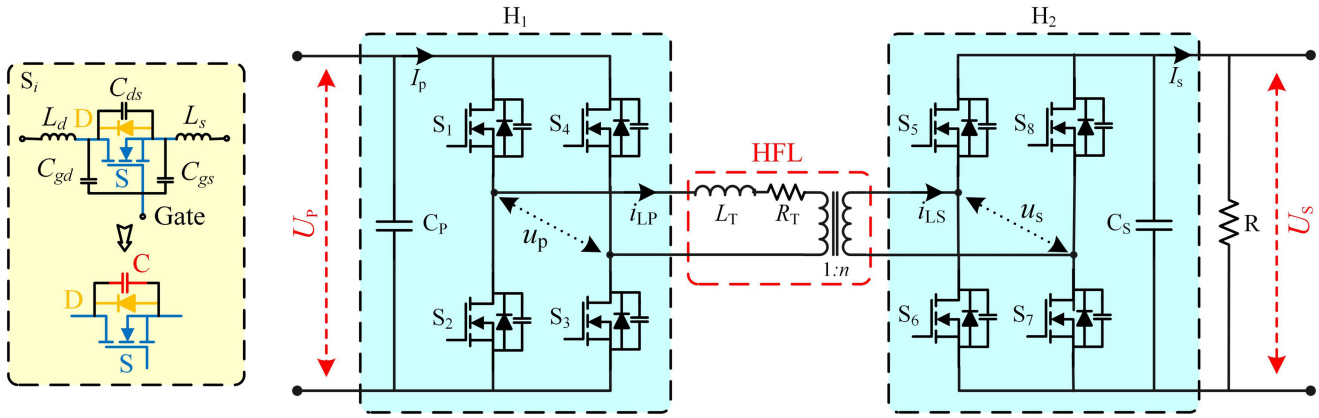


Fig. 1. DAB topology configuration considering parasitic capacitors in switches and parasitic resistance in HFL transformer.

TABLE I
HFL VOLTAGES AND CURRENTS IN SWITCHES DURING OCSF

Switch	Asymmetric duty cycle loss of u_s	Bias of i_{Ls}
S_5	Falling Edge	Positive
S_6	Rising Edge	Negative
S_7	Falling Edge	Positive
S_8	Rising Edge	Negative

L_T is the equivalent inductance and n is voltage ratio of HFL transformer. u_p, u_s, i_{Lp}, and i_{Ls} are HFL voltages and currents in full-bridges on primary and secondary sides, respectively. The power conversion of DAB can be considered as the power exchange between equivalent HFL voltage sources u_p and u_s through equivalent inductor L_T. The HFL currents can be varied by adjusting the phase-shift between HFL voltages u_P and u_S. The $S_1 - S_4$ and $S_5 - S_8$ are switches in full-bridges H_1 and H_2.

Generally, the parasitic parameters are inherent part during operation in practical application. The each switch contains parasitic drain-source capacitor C_{ds}, gate-drain capacitor C_{gd}, gate-source capacitor C_{gs}, drain inductance L_d, and also source inductance L_s and diode D in parallel. These parasitic drain-source, gate-drain, and gate-source capacitors can be integrated as a parasitic capacitance C connected to switch in parallel. Besides, the HFL transformer generally contains the parasitic resistance R_T, and it is usually in milli-ohms level, which is closely related to device package layout.

When the OCSF occurs, the modality operation analysis is essential for DAB to achieve fault tolerance. Due to symmetric topology of DAB, the voltage and current characteristics in switch S_5 and S_7 and switch S_6 and S_8 are both identical, and electrical phenomenon in switch S_5 and S_7 are opposite to those in switches S_6 and S_8, as shown in Table I. Thus, the modality of DAB with faulty switch S_7 in full-bridge H_2 during OCSF process is analyzed in this article, and the operation of other switches and full-bridges can be investigated correspondingly.

Under abovementioned OCSF condition, to present the influence from parasitic parameters on DAB performance, the HFL waveform during OCSF operations in DAB without and with parasitic parameters are presented in Fig. 2. From the HFL waveform during OCSF in DAB without parasitic parameters in Fig. 2(a), the HFL currents operate stably without resonant peak, and the dc bias do not occur. Correspondingly, the HFL waveforms during OCSF in DAB with parasitic parameters are shown in Fig. 2(b). From the figure, the dc bias occur, and

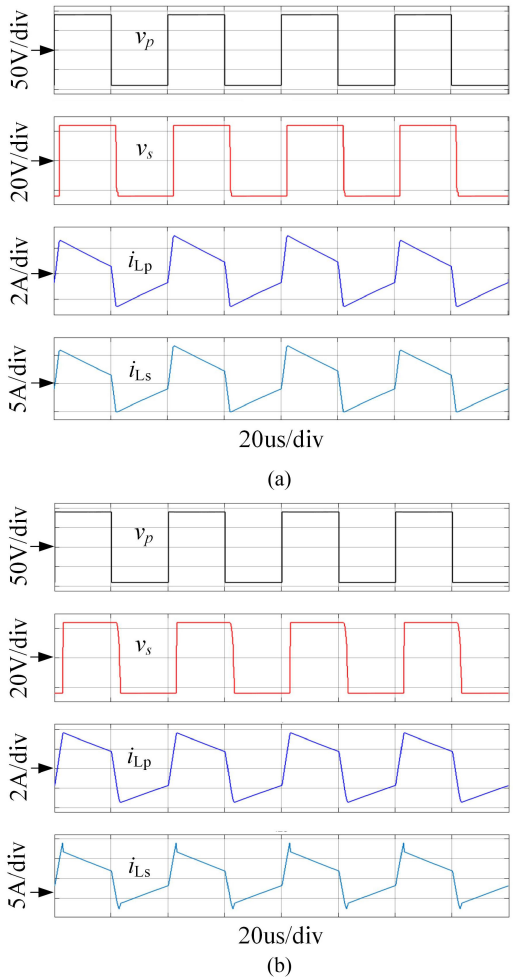


Fig. 2. HFL voltage and current during OCSF with faulty switch S7 in DAB. (a) Without parasitic parameters. (b) With parasitic parameters.

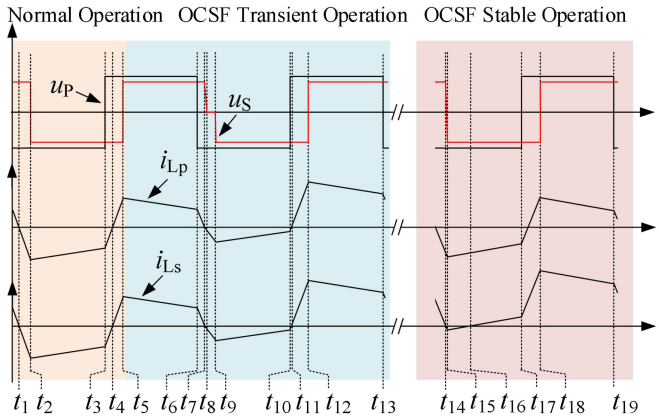


Fig. 3. HFL waveform with parasitic parameter during OCSF in DAB.

the spikes and fluctuation occur in HFL current, and it may lead to heating of transformer and reduced efficiency of DAB. Therefore, the parasitic parameters indeed have influences on DAB operation. Since the parasitic parameters cannot be avoided in practice, the study on parasitic parameters have not only theoretical but also relevant practical values.

To study the modality analysis of OCSF in DAB considering parasitic parameters, the HFL waveform contains OCSF transit, and stable operation are presented in Fig. 3. From the figure, the OCSF with faulty switch S_7 in full-bridge H2 occurs in t_5, then the dc bias in HFL currents and asymmetric duty cycle loss in HFL voltage u_S occur in t_7. Therefore, from Fig. 3, the HFL current in each time interval for DAB can be described as

$$\begin{cases} i_{Ls}(t) = \frac{2nU_P t_f}{\pi L_T} e^{-\frac{R_T}{2L_T}(t-t_7)} \sin\frac{\pi(t-t_7)}{2t_f} & t_7 \sim t_8 \\ i_{Ls}(t) = \frac{-nU_P - R_T i_{Ls}(t_8)}{L_T}(t-t_8) + i_{Ls}(t_8) & t_8 \sim t_9 \\ i_{Ls}(t) = \frac{n(-U_P+nU_S) - R_T i_{Ls}(t_9)}{L_T}(t-t_9) + i_{Ls}(t_9) & t_9 \sim t_{10} \\ i_{Ls}(t) = \frac{n(U_P+nU_S) - R_T i_{Ls}(t_{10})}{L_T}(t-t_{10}) + i_{Ls}(t_{10}) & t_{10} \sim t_{12} \\ i_{Ls}(t) = \frac{n(U_P-nU_S) - R_T i_{Ls}(t_{12})}{L_T}(t-t_{12}) + i_{Ls}(t_{12}) & t_{12} \sim t_{13} \\ i_{Ls}(t) = \frac{n(-U_P-nU_S) - R_T i_{Ls}(t_{13})}{L_T}(t-t_{13}) + i_{Ls}(t_{13}) & t_{13} \sim t_{14} \end{cases} \quad (1)$$

where t_f is the time interval between t_7 and t_8

$$t_f = \frac{2L_T\sqrt{C}}{\sqrt{2n^2L_T - R_T^2 C}}. \quad (2)$$

Besides, compared with the normal operation, the parasitic parameters in switches affect OCSF transient operation. During $t_7 \sim t_8$, the HFL current i_{LS} is lower than zero, and diode D_7 is turn-OFF, and the diode D_8 does not turn on immediately, as presented in Fig. 4(a). The capacitor C_7 is charged and C_8 is discharged, and the HFL voltage u_s is reduced to zero. Besides, the parasitic parameters lead to abnormal freewheeling of D_8 to replace S_7 during $t_8 \sim t_9$, as shown in Fig. 4(b). In addition, during the steady-state of OCSF, a dc bias in HFL current i_{Ls} occurs in $t_{13} - t_{19}$. Therefore, the parasitic parameters change the operating modality and increases dc bias in HFL current, leading to the increased conduction loss, failure of ZVS, and saturation in magnetic component and unexpected protection.

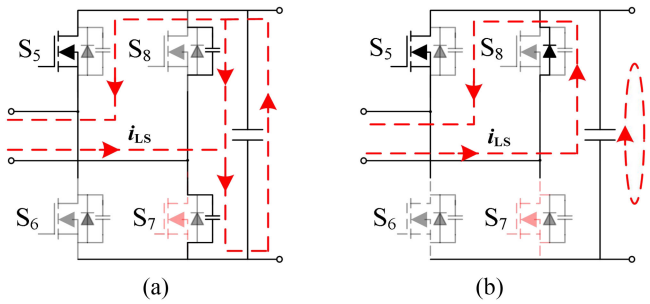


Fig. 4. Circuit paths during OCSF transient operation when S7 is the faulty switch. (a) During time $t_7 \sim t_8$. (b) During time $t_8 \sim t_9$.

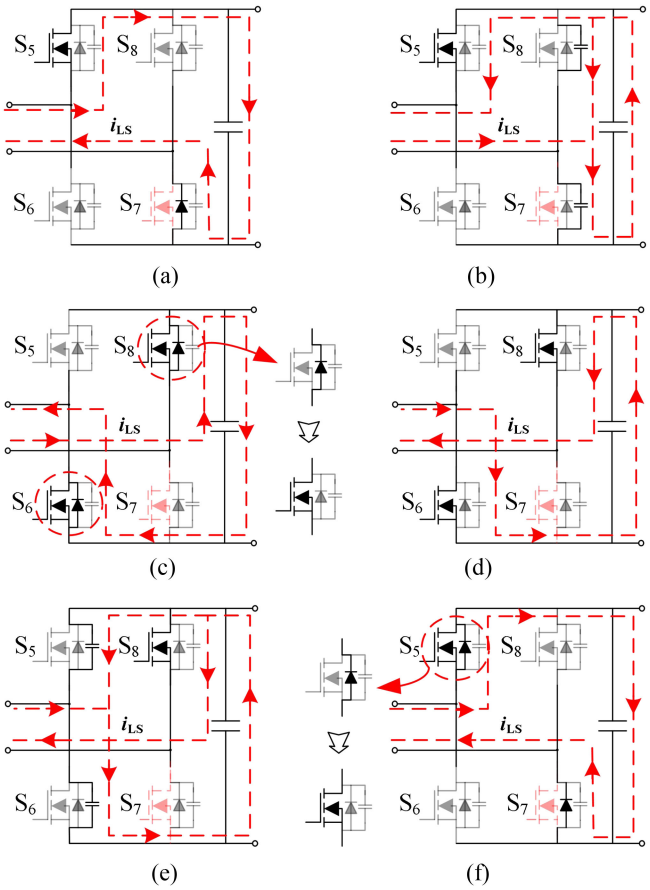


Fig. 5. Circuit paths during OCSF stable operation. (a) During time $t_{13} \sim t_{14}$. (b) During time $t_{14} \sim t_{15}$. (c) During time $t_{15} \sim t_{16}$. (d) During time $t_{16} \sim t_{18}$. (e) Transition of interval. (f) During time $t_{18} \sim t_{19}$.

Moreover, considering the parasitic parameters, the stable operations of OCSF in faulty bridge H_2 during time $t_{13} - t_{19}$ are presented in Fig. 5. According to Fig. 5(a), the DAB operates in $t_{13} \sim t_{14}$, and D_7 is freewheeling. From Fig. 5(b), the DAB operates in $t_{14} \sim t_{15}$, and the discharging C_8 and charging C_7 still operate after freewheeling of D_7. Thus, the HFL current i_{Ls} is not biased above zero completely, and the HFL voltage u_s is approximate to square-wave. Due to resonance of HFL inductor and parasitic capacitor of switches, the resonance, or oscillation of HFL currents may occur. In Fig. 5(c), the DAB operates in $t_{15} \sim t_{16}$. Due to the current direction, D_6 and D_8 are

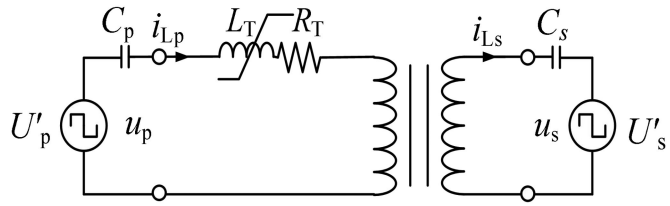


Fig. 6. Equivalent circuit of DAB considering parasitic parameters.

freewheeling, and S_6 and S_8 achieve ZVS at turn-ON instants. In addition, from Fig. 5(d), the DAB operates in $t_{16} - t_{18}$, and the switches maintain operating, as shown in Fig. 5(c). Besides, the Fig. 5(e) presents transition of interval between Fig. 5(d) and (f), where the C_6 is charged and C_5 is discharged. When the DAB operates in $t_{18} \sim t_{19}$, D_7 is turned ON, and switch S_5 achieves ZVS. However, combined with Figs. 2 and 4, the switches cannot achieve the soft-switching at turn-OFF instants.

The equivalent circuit of DAB with parasitic parameters is presented in Fig. 6. The main magnetic flux in HFL transformer of DAB is designed according to redundancy in rated power operation to avoid magnetic saturation and maintain its linear characteristic. During normal operation, it can be regarded as an open circuit in excitation branch for magnetizing inductance and neglected in modeling and derivation. During the fault case, the main magnetic flux can be equivalent as the nonlinear inductance with saturation and the linear part as ideal HFL transformer to simplify the modeling and derivation. From the figure, U'_{p} and U'_{s} are the equivalent ideal voltages with ideal switches, R_{T} is the parasitic resistance of HFL transformer, and c_{p} and c_{s} are the equivalent parasitic capacitors on primary and secondary side, respectively. Thus, considering the parasitic parameters, the HFL current i_{Lp} can be described as

$$L_{\mathrm{T}}\frac{di_{\mathrm{Lp}}}{dt} + R_{\mathrm{T}} i_{\mathrm{Lp}} = u_{\mathrm{P}} - u_{\mathrm{S}}/n. \tag{3}$$

From (3) and Fig. 6, the following equation can be obtained:

$$U'_p - \frac{1}{C_p}\int i_{Lp}dt - L_T\frac{di_{Lp}}{dt} + R_T i_{Lp} = \frac{1}{n}\left(U'_s - \frac{1}{C_s}\int i_{Ls}dt\right). \tag{4}$$

From (4), in s-domain, the transfer function from equivalent voltages to inductor current is shown as

$$i_{Lp}\left(s^2L_T + sR_T + \frac{1}{C_p} + \frac{1}{n^2C_s}\right) = s\left(U'_p - \frac{1}{n}U'_s\right). \tag{5}$$

From (5), the following equation can be obtained:

$$\frac{i_{Lp}}{U'_p - \frac{1}{n}U'_s} = \frac{s}{s^2L_T + sR_T + \frac{1}{C_p} + \frac{1}{n^2C_s}} = \frac{s}{L_T\left[s^2 + s\frac{R_T}{L_T} + \frac{1}{L_T}\left(\frac{1}{C_p} + \frac{1}{n^2C_s}\right)\right]} \tag{6}$$

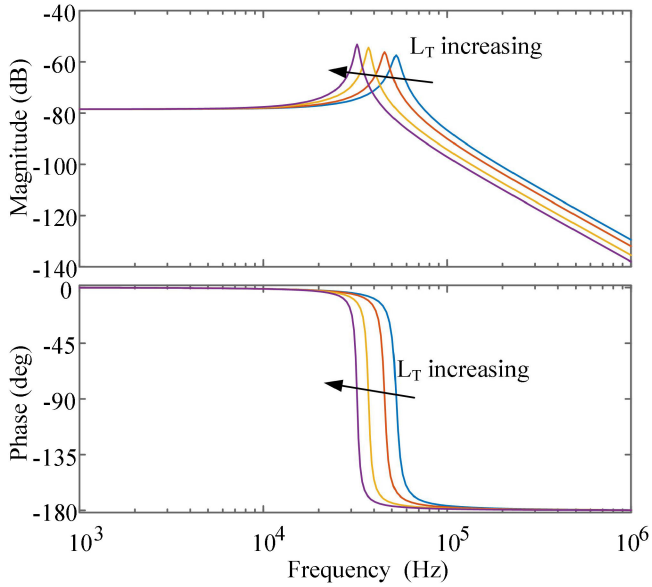


Fig. 7. Bode diagrams of transfer function from inductance current to equivalent voltages.

and the natural frequency ω_{n} and damping ratio ζ are

$$\omega_n = \sqrt{\frac{1}{L_T}\left(\frac{1}{C_p} + \frac{1}{n^2C_s}\right)}, \zeta = \frac{R_T}{2\sqrt{L_T\left(\frac{1}{C_p} + \frac{1}{n^2C_s}\right)}}. \tag{7}$$

According to (6) and (7), the Bode diagrams of transfer function from inductance current to equivalent voltages are presented in Fig. 7. As can be seen from the figure, when the equivalent inductance L_{T} increases, the natural frequency ω_{n}, and damping ratio ζ are decreased. Thus, the implication of large storage inductance may be not an ideal method to reduce the influence of parasitic parameters and suppress current resonance spikes. Besides, the low switching frequency operation may lead to large low frequency harmonics, bringing difficulty in harmonic filtering for system. Thus, low switching frequency operation also may be not an ideal method to reduce the influence of parasitic parameters and suppress the current resonance spikes. Moreover, the high switching frequency operation is one of the significant characteristics and advantage of DAB to achieve large power density and reduced volume of transformer and inductance, and the high switching frequency operation is one of development trends of power converters including DAB.

Besides, from (1)–(5), the HFL current i_{Lp} in each modality can be described as

$$i_{\mathrm{Lp}}(t) = \left(u_{\mathrm{P}}(t) - u_{\mathrm{S}}(t)/n\right) e^{-\frac{R_{\mathrm{T}}}{L_{\mathrm{T}}}t} \Big/ L_{\mathrm{T}} + i_{\mathrm{Lp}}(t_k) \tag{8}$$

where k is 1, 2, 3, …, $t \in [t_k, t_{k+1}]$.

According to (8), due to the damping effect of parasitic resistance R_{T} in HFL inductance L_{T}, a dynamic fluctuation occurs and returns to steady-state in HFL current i_{Lp} during OCSF. This phenomenon is different from HFL current i_{Ls} in faulty full-bridge during OCSF.

Thus, from (2) to (8), the maximum value of HFL current i_{Ls} considering parasitic parameters during OCSF stable operation can be described as

$$\begin{cases} i_{\mathrm{Ls\_max}} = \frac{nU_{\mathrm{P}}+U_{\mathrm{S}}}{n^2fL_{\mathrm{T}}}\left(\frac{d}{2}-ft_{\mathrm{f}}\right) & U_{\mathrm{S}} \geq nU_{\mathrm{P}} \\ i_{\mathrm{Ls\_max}} = \frac{U_{\mathrm{P}}}{nfL_{\mathrm{T}}}\left(d-ft_{\mathrm{f}}-\frac{1}{2}\right)-\frac{U_s}{n^2fL_{\mathrm{T}}}\left(ft_{\mathrm{f}}+\frac{1}{2}\right) & U_{\mathrm{S}}<nU_{\mathrm{P}} \end{cases} \tag{9}$$

From (9), the parasitic capacitance C and parasitic resistance R_{T} affects the HFL currents during OCSF process, causing the unexpected HFL current spikes and bringing a potential harm to DAB safe operation. Moreover, the parasitic capacitance C and parasitic resistance R_{T} have nothing to do with the switching frequency. However, the time interval t_{f} and the maximum value of HFL current are affected by parasitic parameters C and R_{T}, and they both become larger as the parasitic parameters increase, leading to the larger current stress and potential harm to the circuit and operation of DAB.

According to analysis abovementioned, compared with conventional DAB operation without considering parasitic parameters during OCSF process, some new phenomenon occur in DAB operation with parasitic parameters.

1) During OCSF transient operation, the operating modality is varied, and the unexpected operating modes and even sneak circuit emerge.
2) A dc bias occurs in HFL current, leading to failure of ZVS, heating of transformer, and reduced efficiency.
3) Unexpected spikes and fluctuation exist in HFL current, which can lead to the potential harm and unnecessary overcurrent protection.
4) Parasitic parameters have nothing to do with switching frequency, and they do affect the dc bias range and the maximum value of HFL current.

Compared with the conventional modality analysis of DAB in OCSF process, the proposed analysis considering parasitic parameters presents a fundamental operation principle of DAB with parasitic parameters, thus enriching the modality analysis system for DAB. It is beneficial to reveal new operation modes and characteristic of DAB during OCSF considering parasitic parameters, providing theoretical and engineering references on the topology construction, devices selection, and practical control design for DAB.

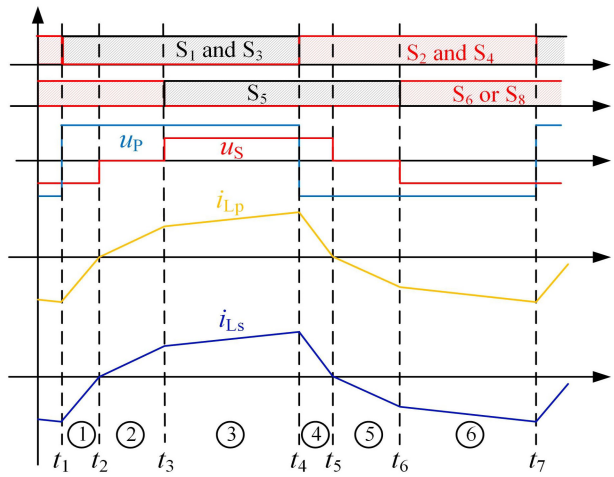


Fig. 8. HFL voltages and currents of semi dual active bridge under proposed fault tolerant method for OCSF.

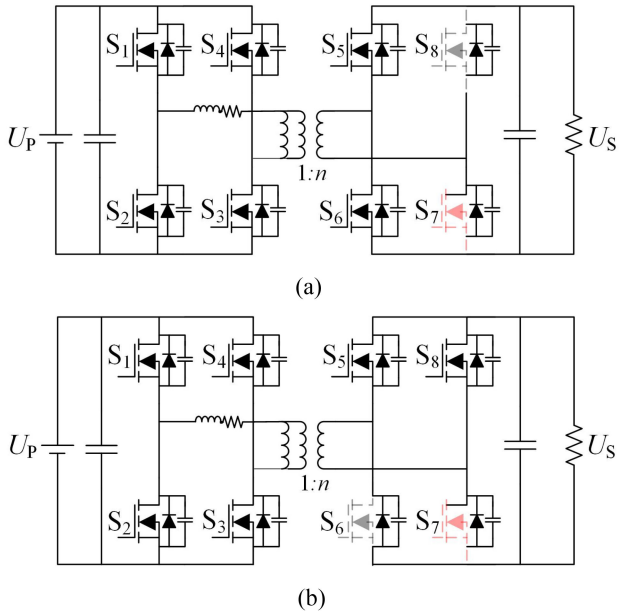


Fig. 9. Symmetrical topology transformation under proposed fault tolerance strategy. (a) Reconstruct the DAB by blocking the vertical adjacent switch. (b) Reconstruct the DAB by blocking the horizontal adjacent switch.

III. Fault-Tolerant Strategy for OCSF

According to the modality analysis of DAB during OCSF process, the asymmetric topology in DAB under OCSF cause asymmetric HFL voltage and current in faulty full-bridge. Thus, a fault tolerance strategy including symmetrical topology transformation and practical control architecture for OCFS in DAB is proposed in this article to achieve a stale output voltage with symmetric HFL voltage and current.

In general, the topology transformation in proposed strategy is to reshape an asymmetric DAB topology during OCSF into a symmetric structure by blocking adjacent switches. There are two topology transformation methods including blocking the switch in fault arm and blocking the switch in fault electric potential. Based on topology transformation, the corresponding practical control architecture is proposed to maintain output voltage and restore current to symmetry.

A. Topology Transformation Under Fault Tolerance Strategy

Since switches in DAB are controllable devices, blocking switches to achieve symmetrical topology transformation is a practical and economic method for a fault tolerance strategy. Under proposed fault tolerant method, the HFL voltages and currents of semi DAB are presented in Fig. 8. According to the symmetrical topology transformation idea, the implementation of proposed fault tolerance strategy is to block the horizontal or vertical adjacent switch in faulty full-bridge, as shown in Fig. 9. From Fig. 9(a), when the OCSF occurs in switch S_7, the drivers of switch S_7 and vertical adjacent switch S_8 are both blocked,

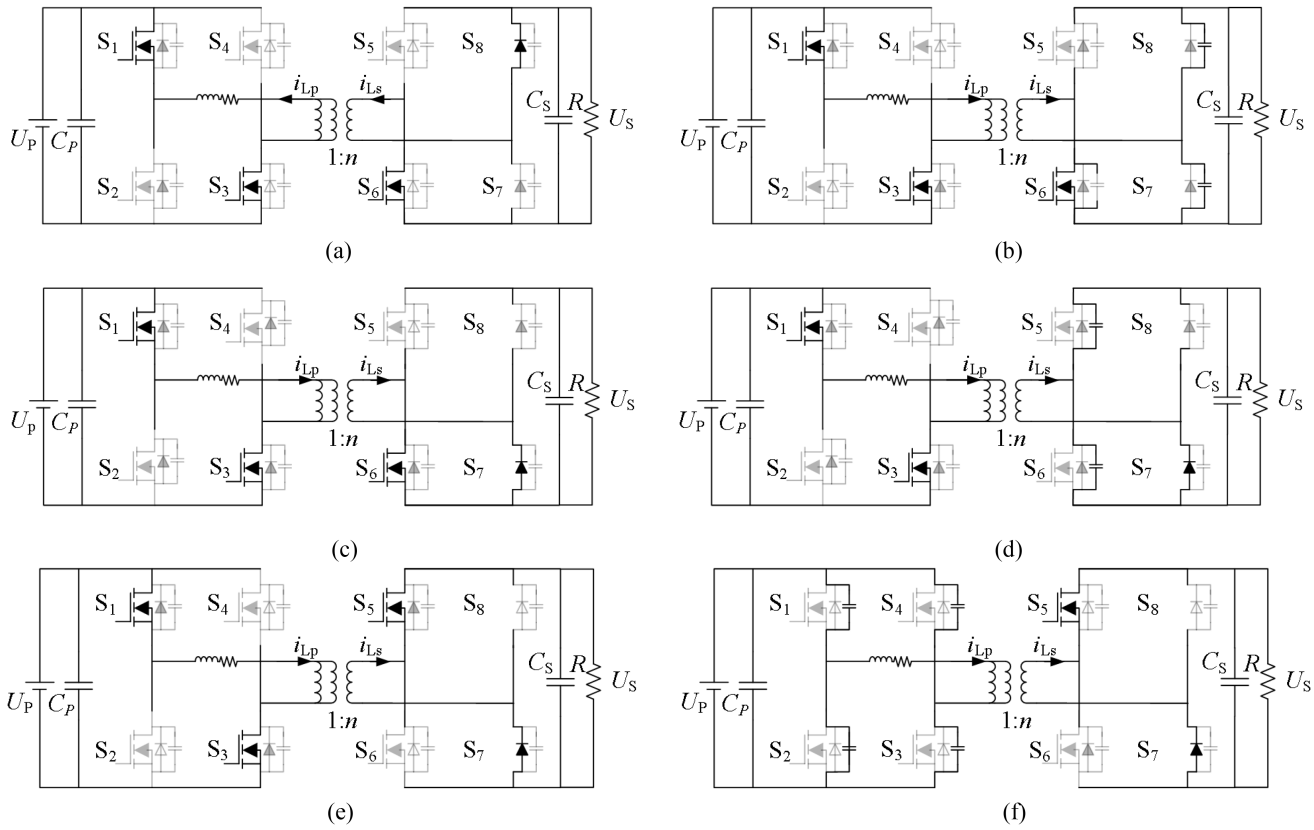


Fig. 10. Corresponding conducting devices and current path of DAB by blocking the vertical adjacent switch proposed fault tolerant strategy. (a) Interval 1. (b) Transition from interval 1 to interval 2. (c) Interval 2. (d) Transition from interval 2 to interval 3. (e) Interval 3. (f) Transition from interval 3 to interval 4.

and the faulty DAB is reshaped to be a semi DAB topology proactively. Similarly, when the OCSF occurs in switch S_7, the drivers of switch S_7, and horizontal adjacent switch S_6 are both blocked, as shown in Fig. 9(b). Under topology transformation, the dc bias can be eliminated and symmetrical HFL current and voltage can be achieved. Thus, the current spike caused by saturated transformer and parasitic parameters are avoided, and DAB is in safe operating range. Besides, the proposed methods realize topology transformation and the fault tolerance for DAB during OCSF, ensuring the feasibility and flexibility of DAB.

Under proposed fault tolerant method, the corresponding modality of DAB by blocking vertical and horizontal adjacent switch are shown in Figs. 10 and 11, respectively. As can be seen from Fig. 8, compared with the HFL waveform in Fig. 3 without proposed fault tolerance strategy, the HFL voltages in DAB become symmetric waveform with duty cycle loss, and HFL currents become stable without bias. During the operation interval 1 in Fig. 8, Figs. 10(a) and 11(a) present the current paths and conducting devices under two fault tolerance methods, respectively. In Fig. 10(a), because the drivers for S_7 and S_8 are blocked, the S_6 turns ON and D_8 is freewheeling to replace S_8. In Fig. 11(a), because the drivers of S_6 and S_7 are blocked, the S_8 turns ON and D_6 is freewheeling to replace S_8. During transition from operation interval 1 to interval 2, the Figs. 10(b) and 11(b) present the current path and conducting devices under two fault tolerance methods. In Fig. 10(b), the HFL current i_{LS} is turned from negative to positive. Because C_7 is being discharged and C_8 is being charged, D_8 is turned OFF and D_7 is not turned ON. In Fig. 11(b), because C_5 is being discharged and C_6 is being charged, D_8 is turned OFF and D_7 is not turned ON. During operation interval 2, the Figs. 10(c) and 11(c) present current paths and conducting devices under two fault tolerance methods, respectively. In Fig. 10(c), the HFL current i_{Ls} is positive, and the discharge of C_7 and the charge of C_8 are completed. Thus, D_7 is turned ON to replace S_7, and a closed circuit is achieved by S_6 and D_7. In Fig. 11(c), because i_{LS} is positive, and the driver of S_5 is not triggered, D_5 and S_8 are turned ON, and a closed circuit is achieved.

During transition from operation interval 2 to interval 3, Figs. 10(d) and 11(d) present current path and conducting devices. In Fig. 10(d), the HFL current i_{LS} is positive, and D_7 is turned ON, and C_5 is being discharged and C_6 is being charged. In Fig. 11(d), D_5 is turned ON, and C_7 is being discharged and C_8 is being charged. During the interval 3, the Figs. 10(e) and 11(e) present the current paths and conducting devices. In Fig. 10(e), the HFL current i_{Ls} is positive, and the discharge and charge of C_5 and C_6 are completed. Thus, S_5 is turned ON with the driver pulse, and a closed circuit is achieved by S_5 and D_7. In Fig. 11(e), S_5 and D_7 are turned ON with the driver pulse, and a closed circuit is achieved. During the transition from operation interval 3 to interval 4, Figs. 10(f) and 11(f) present current paths and conducting devices. In Fig. 10(f), the operations of switches in secondary side is maintained. On primary side, due to the changes of drivers, C_1 and C_3 are being charged, and C_2 and

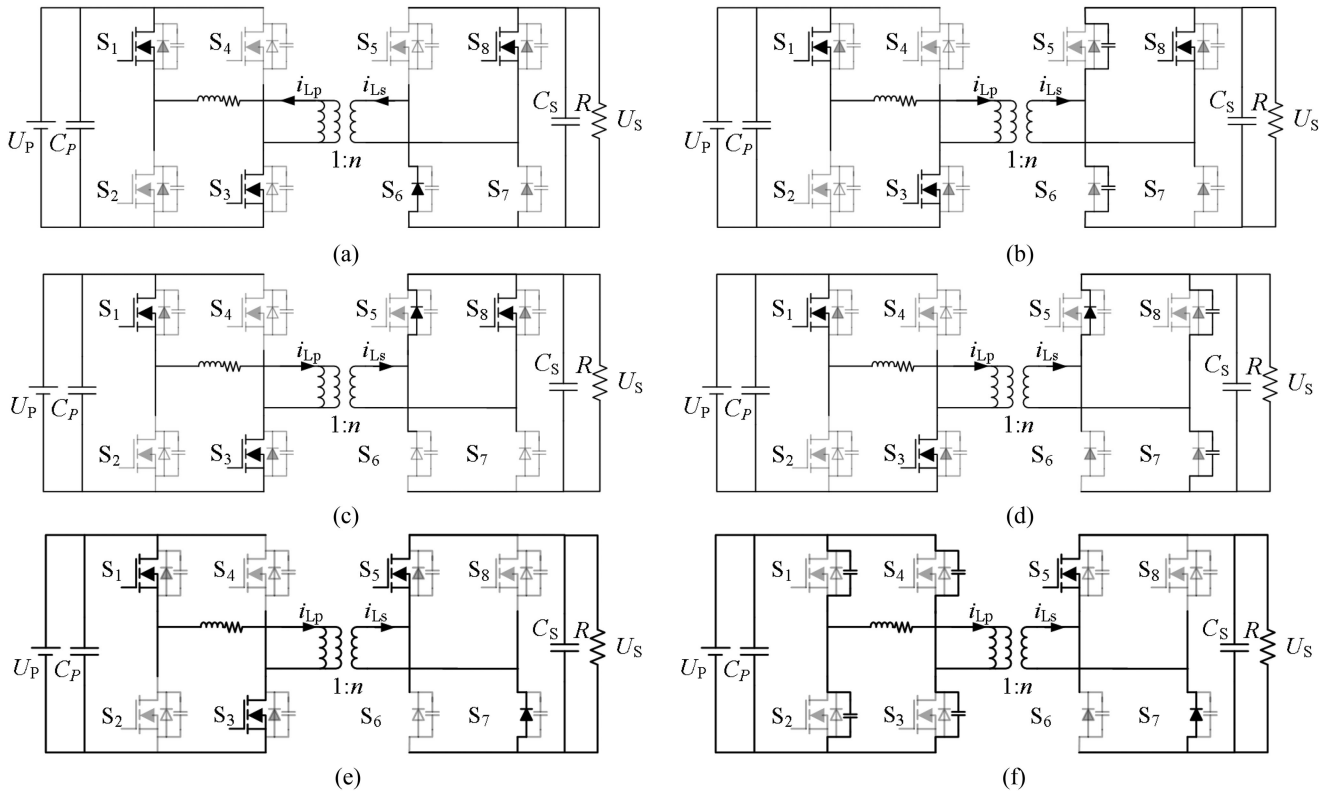


Fig. 11. Corresponding conducting devices and current path of DAB by blocking horizontal adjacent switch proposed fault tolerant strategy. (a) Interval 1. (b) Transition from interval 1 to interval 2. (c) Interval 2. (d) Transition from interval 2 to interval 3. (e) Interval 3. (f) Transition from interval 3 to interval 4.

C_4 are being discharged. Similarly, in Fig. 11(f), operations of switches on secondary side is maintained. On the primary side, due to the changes of drivers, C_1 and C_3 are being charged, and C_2 and C_4 are being discharged. Therefore, from Figs. 10 and 11, the oscillation is likely occurred during the transition in *LC* two order system. However, because of the damping and lighter energy storage of symmetric operation in DAB, the probability of oscillation is decreased compared with that in conventional OCSF operation.

B. Practical Application of Proposed Fault Tolerance Strategy

According to the switching principle and topology analysis previously, the practical control architecture of proposed faulty tolerance strategy is presented in Fig. 12. For DAB, the output voltage feedback and phase-shift HFL modulation are most simplest and typical control method. From the figure, when the DAB operates in normal status, the power rating, and power transmission direction of DAB can be controlled by varying the phase-shift angle *d* under HFL modulation including single-phase-shift (SPS), extended-phase-shift (EPS), dual-phase-shift, and triple-phase-shift. When the OCSF occurs, the DAB switches to fault tolerance control unit. By blocking vertical or horizontal adjacent switch, the fault tolerance can be realized and the DAB maintains operation during OCSF process. The PI controller is retained under both normal operation and OCFS with proposed faulty tolerance strategy.

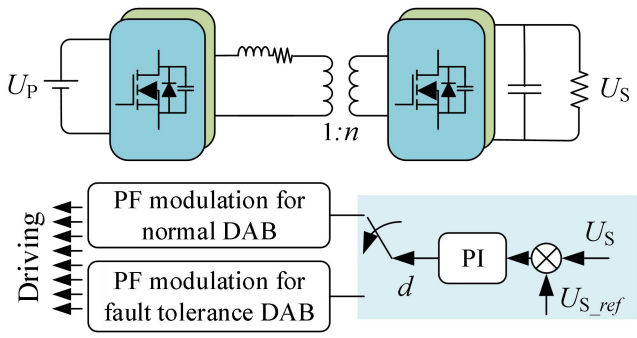


Fig. 12. Practical control architecture of proposed fault tolerance strategy for DAB.

Moreover, when the switch is turned ON and OFF, the driving circuit and main circuit form a path, and a current will flow through the driving resistor, and a short-term pulse current will be generated. Therefore, the driving current can be detected indirectly by detecting the voltage in drive resistor. Combining the timing of rising and falling edges of PWM driving signal and whether the voltage is a normal pulse, it can be judged whether the switch is open-circuit. Thus, the abovementioned method is applied to judge if a switch has an open circuit phenomenon, and the detect and response time is about one switching cycle. For DAB with a switching frequency of 20 kHz, the detection time is about 50 us, and it becomes faster depending on the sampling time. Thus, the OCSF can be detected and the driving signals

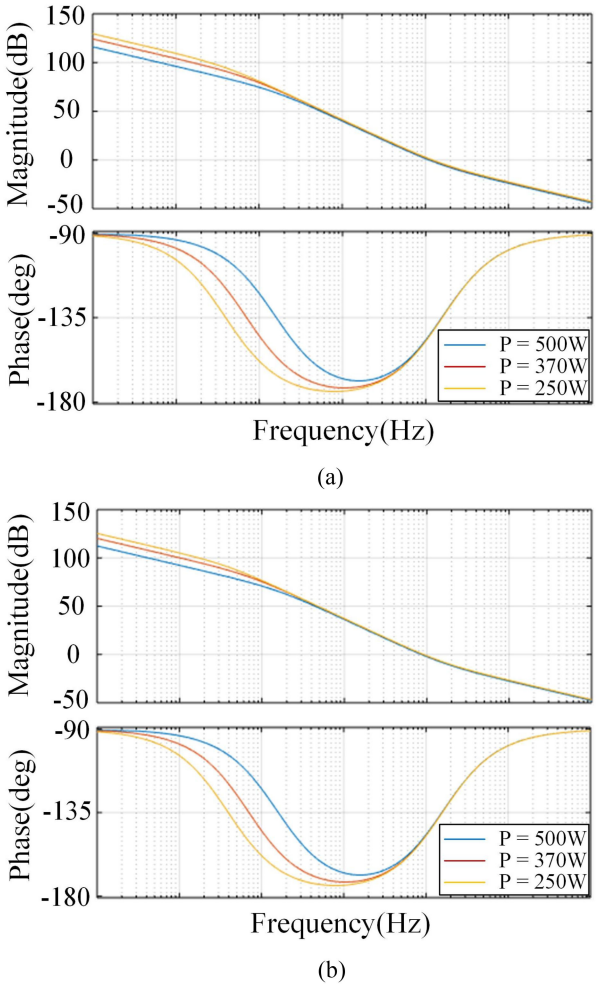


Fig. 13. Comparison of loop gains in DAB between normal operation and under OCFS with proposed faulty tolerance strategy. (a) Normal operation. (b) OCFS process under proposed strategy.

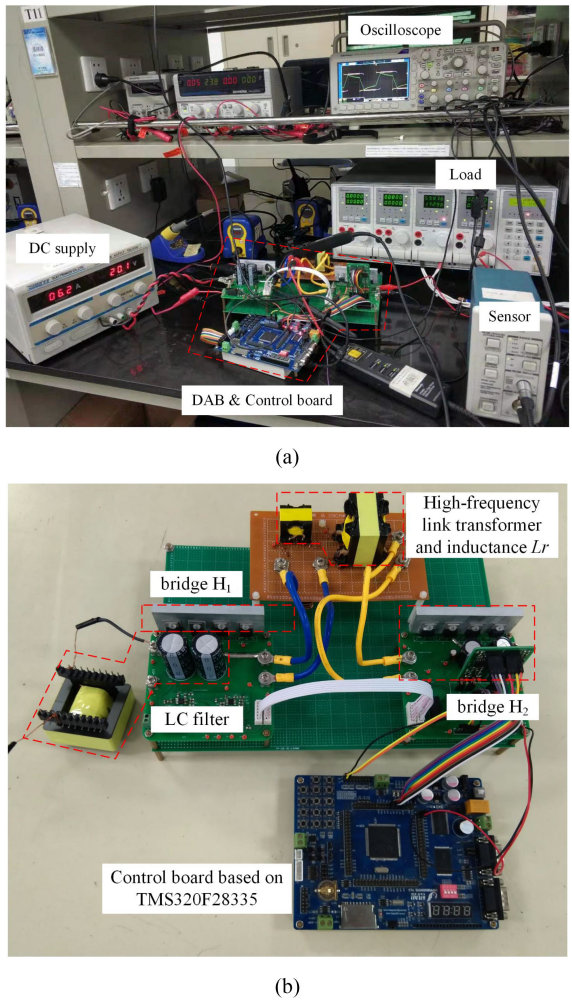


Fig. 14. Experiment setup and DAB prototype. (a) Experiment setup. (b) DAB prototype.

can be adjusted rapidly in DAB, and the proposed fault tolerance strategy is possible in practical application.

C. Operating Characteristic Under Proposed Strategy

The SPS HFL modulation is the typical method for DAB to achieve voltage conversion and power transmission, and the transmit power of DAB under SPS is [4]

$$P_{\mathrm{DAB}} = \frac{U_{\mathrm{P}} U_{\mathrm{S}}}{2nL_{\mathrm{T}}f} d\,(1-d) \tag{10}$$

where d is the phase-shift ratio. From (10), it had been verified that the maximum transmission power of DAB during normal operation can be achieved when $d = 0.5$, and the maximum transmission power of DAB can be described as

$$P_{\mathrm{DAB-Max}} = \frac{U_{\mathrm{P}} U_{\mathrm{S}}}{2nL_{\mathrm{T}}f} \times 0.25. \tag{11}$$

From (3)–(5), under proposed fault tolerant strategy, the transmission power of DAB during OCSF can be described as

$$P_{\mathrm{DAB-FT}} = \frac{U_{\mathrm{P}} U_{\mathrm{S}}}{2n\pi L_{\mathrm{r}}f} \frac{d}{9}\,(6-5d)\,. \tag{12}$$

From (12), when $d = 0.5$, the maximum transmission power of DAB under proposed fault tolerant strategy is

$$P_{\mathrm{DAB-FT-Max}} = \frac{U_{\mathrm{P}} U_{\mathrm{S}}}{2nL_{\mathrm{T}}f} \times 0.2. \tag{13}$$

According to (11) and (13), comparing with the transmission power of DAB in normal operation, the maximum transmission power of DAB under proposed strategy can reach 80% of that during normal operation. Although the proposed strategy can only maintain 80% maximum transmission power of DAB, it can avoid the sudden change in electrical quantity and potential shutdown and damage caused by OCSF to ensure the normal operation of DAB. Therefore, the proposed faulty tolerance strategy is still valuable in practical application.

Besides, according to the control architecture and (1)–(8), the loop gain of DAB under normal operating condition $G_{\mathrm{DAB\text{-}N}}$ and under proposed fault tolerant strategy $G_{\mathrm{DAB\text{-}FT}}$ are

$$G_{\mathrm{DAB-N}} = \frac{nU_{\mathrm{P}}(1-2d)R}{2fL_{\mathrm{T}}(1+sC_S R)} G_{\mathrm{PI}} \tag{14}$$

$$G_{\mathrm{DAB-FT}} = \frac{nU_{\mathrm{P}}(k^2+k+1-(1+2k^2+2k)d)R}{fL_{\mathrm{T}}(2k+1)^2(1+sC_S R)} G_{\mathrm{PI}} \tag{15}$$

TABLE II
COMPARISON AMONG PROPOSED AND EXISTING FAULT TOLERANCE STRATEGIES

	Switching Frequency	Fault Type	DAB Type	Feature & Operation				
				Parasitic Parameters	Fault Analysis	HFL Currents in Transformer	Implementation of FT Control	Fault Tolerance
Proposed Strategy	20 kHz	OCSF	Single Phase	√	√	Both Fault and Normal Sides	√	Symmetric Topology and Duality Principle for FT Topology Transformation
[11]	25 kHz	Frozen Leg	Three Phase	×	√	Fault Side	×	Frozen Leg in Fault Phase
[12]	1 kHz	OCSF	Single Phase	×	√	Fault Side	×	Stop Operation
[14]	1250 Hz	OCSF	Single Phase	×	√	Fault Side	×	Frozen Leg in Fault Phase
[27]	50 kHz	Open-Phase Fault	Three Phase	×	×	None	√	Frozen Leg in Fault Phase
[33]	5 kHz	OCSF	Single Phase	×	×	Fault Side	√	Frozen Leg in Normal Bridge

where $k = U_{\mathrm{P}}/(nU_{\mathrm{S}})$. From (10)–(15), the transmission power and control characteristic of DAB under proposed fault tolerant strategy can be varied with the variation of switching frequency, thus, the proposed strategy can be effectively applied in DAB with low and high switching frequencies.

From (14) and (15), the poles of two transfer functions are the same; however, the open loop gain is slightly different. Thus, the DAB in fault tolerance operation has a high gain, which is similar to that of DAB in normal operation. Besides, when the transferred power through DAB is 500 W, 370 W, and 250 W, the control loop gains of DAB in normal operation and in OCFS under proposed fault tolerance strategy are shown in Fig. 13. From the figures, DAB maintains ideal characteristics in both normal operation and OCFS process under the proposed fault tolerance strategy. Specifically, the phase margin of DAB is about 31° in normal operation, and the phase margin of DAB is about 27° in OCFS process under the proposed strategy. In addition, the amplitude frequency response during OCFS under proposed strategy is slightly lower than that in normal operation, and the cutoff frequencies in both operation status are similar. Therefore, under proposed strategy, the DAB maintains high gain and ideal operation performance during OCSF process.

D. Safe Operating Range Under Proposed Strategy

Generally, the safe operating range of converter is about 1.2 times of peak voltage or current under rated power condition, and the overcurrent protection is triggered over 1.2 times of peak voltage or current. Therefore, the safe operating range of DAB depends on the selection of switching devices according to the peak current value under rated power level. On this base, during OCSF operation in DAB with parasitic parameters, the dc bias range and current spike of HFL current become larger as parasitic parameters increase, reducing the current margin, and safe operating range. Correspondingly, under the proposed fault tolerance strategy, the dc bias range and current spike in HFL current caused by parasitic parameters and transformer saturation can be reduced, and the current margin and safe operating range for DAB can be increased.

TABLE III
PARAMETERS OF DAB PROTOTYPE

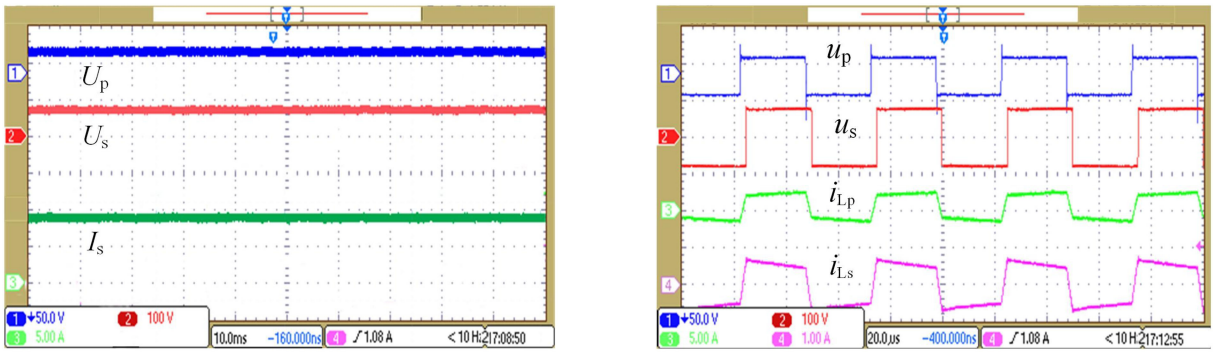
Parameters	values	Parameters	values
C_p	790 μF	Switches 1 – 4	CSD19536KCS
C_s	141 μF	Switches 5 – 8	FDPF12N60NZ
L_{T}, R_{T}	3 μH, 14 mΩ	$C_1 - C_4$	270 pF
n	1:3	$C_5 - C_8$	150 pF
fs	20 kHz	Us	50 – 100 V
P	500 W	U_{p}	20 – 40 V

E. Comparison of the Proposed and Existing Strategies

The comparison among proposed and existing fault tolerance strategies for OCSF is shown in Table II. From the table, the modality analysis considering parasitic parameters in OCSF for DAB can explore the extra operating mode, sneak oscillation mechanism, and influence in HFL voltage and current and operation characteristic during OCSF process. In addition, the proposed fault tolerance strategy is simple and convenient in practical engineering application, and it also has applicability and flexibility suitable to other derived topologies. Besides, during OCSF process, the DAB can only transfer power from one side to other side and lost the bidirectional power transmit capability. The proposed fault tolerance strategy can achieve fault tolerance, avoid potential harm and maintain normal operation for DAB during OCSF, however, it can not change the unidirectional power transmission of DAB during OCSF process, and this becomes one of areas that can be investigated and improved for fault tolerance strategy in further studies.

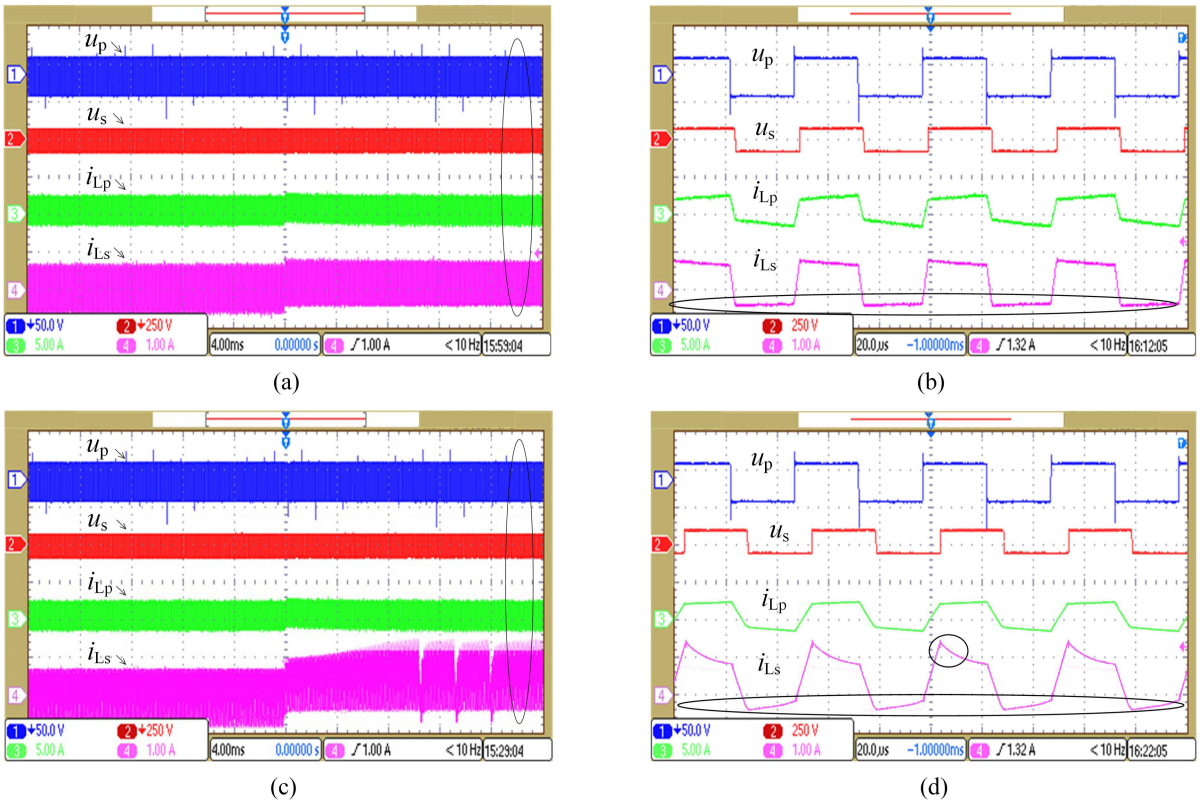
IV. EXPERIMENTAL VERIFICATION

To verify the analysis and proposed fault tolerance strategy for OCSF, a DAB prototype with digital signal processing controller TMS320F28335 DSP is established, as presented in Fig. 14, and main parameters of DAB prototype are presented in Table III. The corresponding experimental setup includes a dc power supply, an electronic load, an oscilloscope based on Tektronix MSO 2024 and several current and voltage sensors. Then, the steady-state HFL voltages and currents waveform in



(a) (b)

Fig. 15. Steady-state waveform in DAB under normal operation. (a) Voltages and currents on both sides. (b) HFL voltages and current.



(a) (b)

(c) (d)

Fig. 16. HFL waveform during OCSF in DAB. (a) DAB with switches FDPF12N60NZ with parasitic capacitance 150 pF, zoom-out view. (b) DAB with switches FDPF12N60NZ with parasitic capacitance 150 pF, zoom-in view. (c) DAB with switches KIA6450A with parasitic capacitance 200 pF, zoom-out view. (d) DAB with switches KIA6450A with parasitic capacitance 200 pF, zoom-in view.

DAB are presented in Fig. 15. From the figure, the dc voltage on primary side U_P is 25 V, and the dc voltage on secondary side U_S is controlled at preset 75 V, as presented in Fig. 15(a). The HFL voltages u_P and u_S are square waveform, and the HFL currents i_{LP} and i_{LS} are stable without oscillation, as presented in Fig. 15(b). The experiment results indicate that, under normal operation condition, the DAB operates normally and realizes voltage conversion and power transmission.

To verify the inherent parasitic parameters of DAB during OCSF process, the HFL voltages, and currents in DAB with varied parasitic parameters are presented in Fig. 16. From the figures, the DAB operates normally with the varied parasitic parameters, and the HFL voltages u_p and u_s are square-waves. When the switch S_7 in full-bridge H2 has malfunction and the OCSF occurs, the dc bias and current spike appear in HFL current on secondary side i_{LS} during OCSF. Specifically, when the applied switches S_5 – S_8 are FDPF12N60NZ with parasitic capacitance 150 pF, the current spike, and oscillation in the HFL current i_{Ls} are not significant during OCSF process, as shown in Fig. 16(a) and (b). When the applied switches S_5 – S_8 are KIA6450A with parasitic capacitance 200 pF, the current spike and oscillation that appear in HFL current i_{Ls} are large during OCSF process, and the dc bias range also becomes larger, as shown in Fig. 16(c) and (d). The experimental results

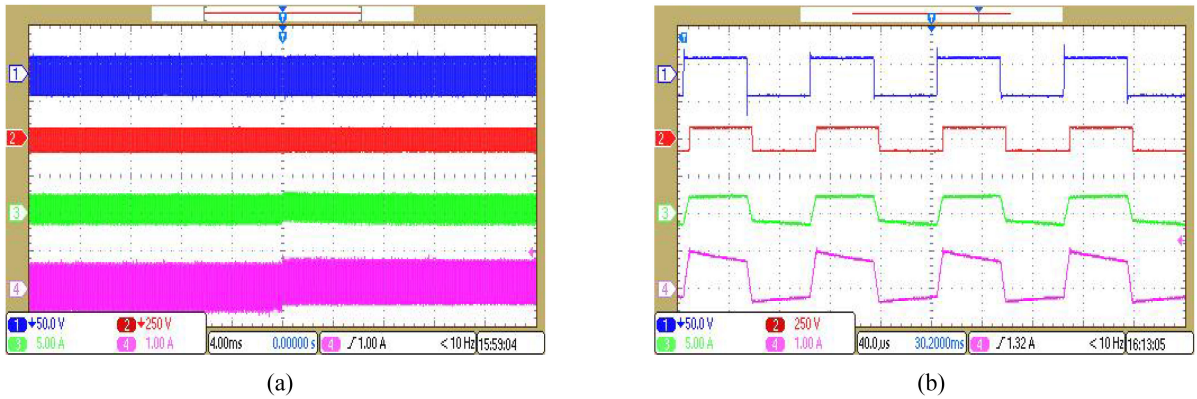


Fig. 17. HFL waveform during OCSF in DAB with parasitic capacitance 150 pF and switching frequency 10 kHz. (a) Zoom-out. (b) Zoom-in view.

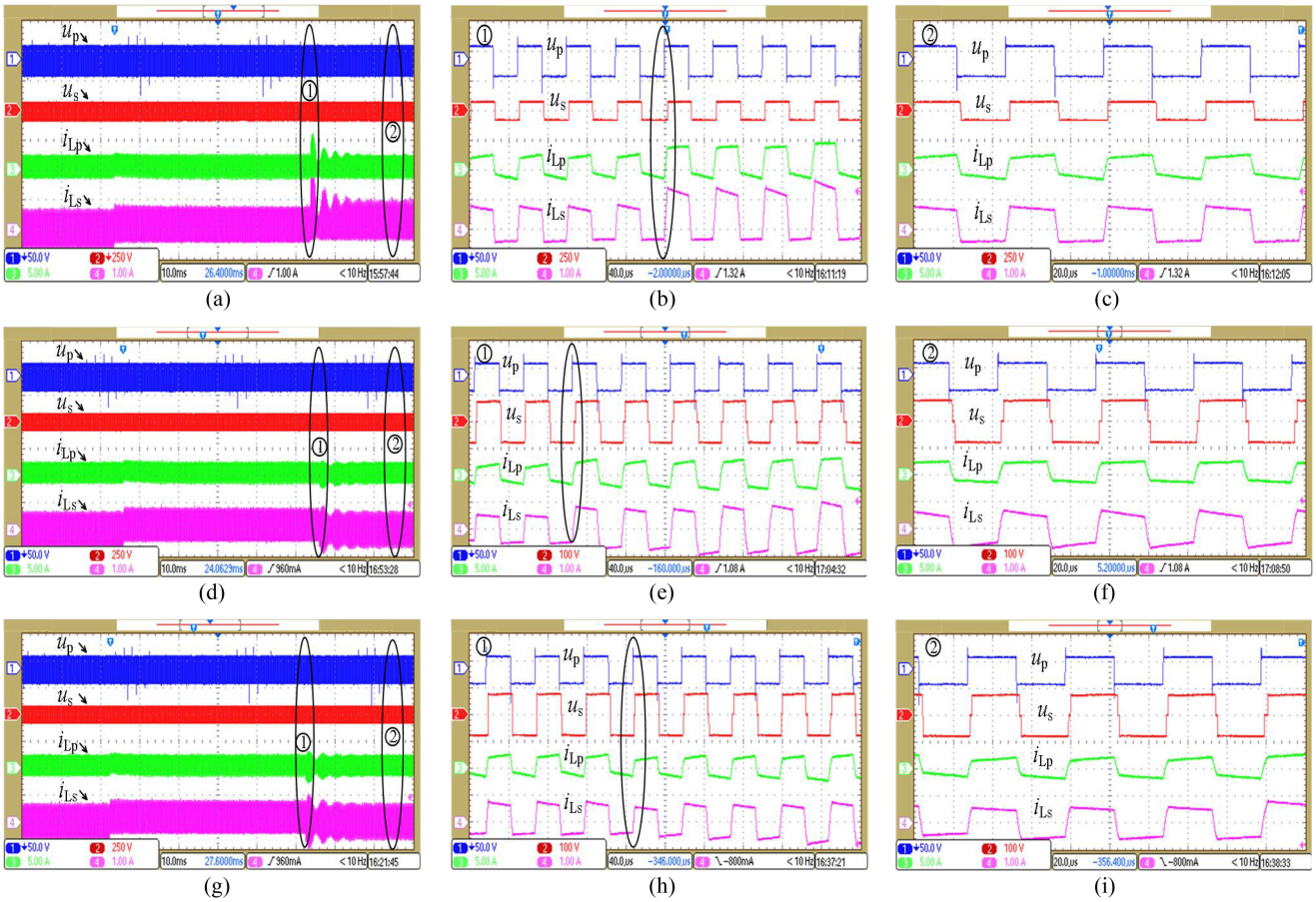


Fig. 18. HFL voltages and currents in DAB without and with proposed faulty tolerance strategy during OCSF. (a)–(c) Without proposed strategy. (d)–(f) With proposed strategy by blocking switches S7 and S8. (g)–(i) With proposed strategy by blocking switches S7 and S6.

verify that parasitic parameters may cause unexpected spikes and oscillation and the larger dc bias range for HFL current during OCSF that leads to failure of ZVS, heating transformer, reduced efficiency, and potential harm for DAB.

To verify the relationship between switching frequency and parasitic parameters, the experiment HFL waveform of DAB applied switches FDPF12N60NZ with parasitic capacitance 150 pF under switching frequency 10 kHz are shown in Fig. 17. Compared with HFL waveform of DAB with same switches and parasitic capacitance under switching frequency 20 kHz shown in Fig. 15(a) and (b), the dc bias range, current spike and oscillation in HFL current do not vary significantly. The experiment results verify that parasitic parameters and their influence are not directly related to switching frequency. When switch S_7 in full-bridge H_2 breaks down and OCSF occurs, the HFL voltages and currents in DAB without and with proposed faulty tolerance strategy are presented in Fig. 18. As can be seen from Fig. 18(a)–(c), without the proposed faulty tolerance strategy,

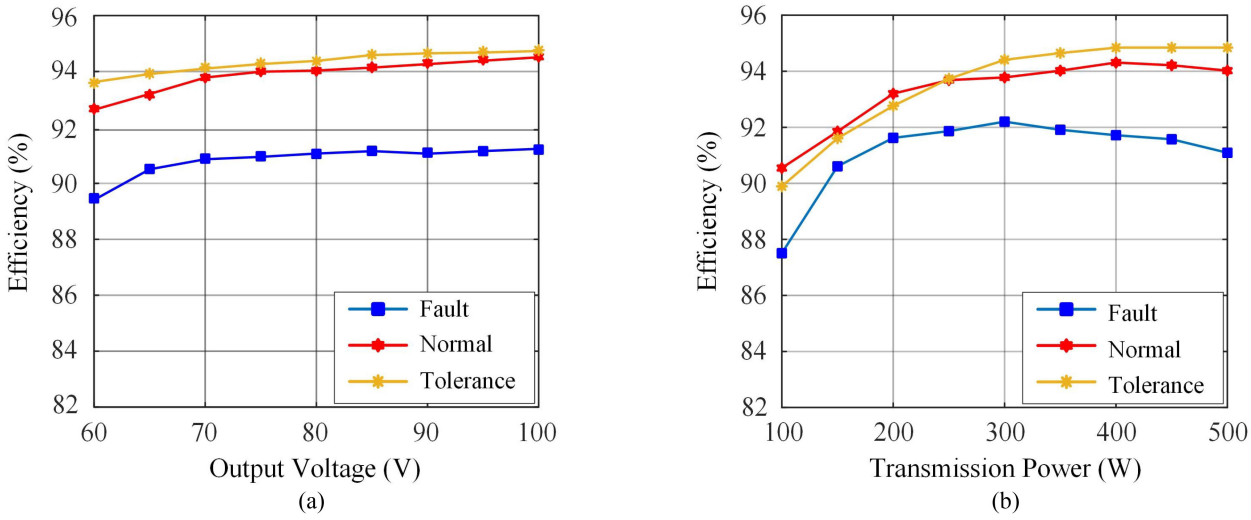


Fig. 19. Efficiency comparison in DAB among normal operation, fault mode, and fault tolerance mode. (a) With varied output voltage. (b) With varied transmission power.

the dc bias, serious current spike and oscillation occur in HFL currents, and the dc bias condition persists during OCSF process. Under the proposed faulty tolerance strategy by blocking the vertical adjacent switch S_8 for DAB during OCSF process, the HFL voltage u_S in faulty full-bridge becomes three-level waveform, and the HFL currents generate transient process and return to steady-state again after several switching periods. Besides, the dc bias, current spike, and oscillation in HFL currents are eliminated, as presented in Fig. 18(d)–(f). Similarly, under the proposed faulty tolerance strategy by blocking the horizontal adjacent switch S_6 for DAB during OCSF, the HFL voltage u_S in faulty full-bridge also becomes three-level waveform. The HFL currents generate transient process and return to steady state again after several switching periods, and the dc bias, current spike, and oscillation in HFL currents are also eliminated, as shown in Fig. 18(g)–(i). Therefore, the experimental results verify that, the proposed faulty tolerance strategy by blocking vertical adjacent switch or horizontal adjacent switch can avoid the dc bias, current spike, and oscillation in HFL voltages and currents, realize the faulty tolerance and maintain the stable operation of DAB during OCSF process, thus improving the efficiency, flexibility, and robustness of DAB.

Moreover, the efficiency comparison in DAB among normal operation, under OCSF process and under the proposed fault tolerance strategy is presented in Fig. 19. As can be seen from Fig. 19(a), when the output voltage varies from 60–100 V with a full-load, the DAB under OCSF process receives the lowest efficiency below 92% compared with that under normal operation and fault tolerance strategy, due to dc bias in HFL currents and the loss of ZVS. Besides, the efficiency of DAB under normal operation and fault tolerance strategy are similar varying from 92–95%, and the DAB under fault tolerance strategy obtains the highest efficiency, because of less switches operation, reduced HFL back flow power and continued ZVS behavior under proposed fault tolerance strategy. In addition, the similar experimental results are obtained for DAB under the varied transmission power, as presented in Fig. 19(b). The experimental results verify that the proposed fault tolerance strategy can realize the fault tolerance and maintain efficient and stable operation of DAB converter during OCSF process, improving the reliability for DAB especially under variable faults and operating conditions.

V. Conclusion

In this article, the modality analysis considering parasitic parameters for OCSF process in DAB dc–dc converter is investigated, and the unexpected operating mode, dc bias, current spike, and fluctuation in HFL voltages and currents caused by parasitic parameters are comparatively discussed, providing theoretical and engineering references on topology construction, devices selection, and practical control design for DAB. Besides, to realize fault tolerance for DAB during OCSF process considering the parasitic parameters, a fault tolerance strategy is proposed, and the topology switching mechanism, practical control architecture, operating characteristic, and safe operating range of DAB is investigated. The proposed strategy can eliminate the dc bias, current spike, and oscillation in HFL electrical quantity and maintain efficient and stable operation for DAB during OCSF process. Compared with conventional fault tolerance strategy, the proposed strategy is more simple, rapid, efficient, and feasible for DAB during OCSF process, thus providing a feasible, efficient, and practical fault tolerance scheme for DAB considering parasitic parameter.

Besides, the limitation of this article needs to be illustrated and the corresponding future work should be considered: 1) Although the influence of parasitic parameters and the fault tolerance strategy for DAB are proposed in this article, the experiment verification is based on DAB with high switching frequency, and the related research in DAB with low switching frequency in high-power application had not been studied in depth. Thus, the theoretical derivation, control characteristics,

and experimental verification in DAB with low switching frequency can be considered in future work; 2) The influence of parasitic parameters and fault tolerance control characteristic of DAB with different switching devices have not been considered in this article, however, the parasitic parameters and control characteristic maybe different for DAB with different switching devices. Thus, the related research in DAB with different switching devices such as MOSFET, IGBT, and even SiC and GaN devices can be studied in future work; 3) The power loss mechanism of DAB using the proposed strategy is still unclear, and the power loss model has not been established yet. Thus, the research on power loss of DAB using proposed strategy should be studied, and an improved control algorithm to realize fault tolerance, reduce power loss and increase efficiency for DAB can be considered in future work.

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Yu Wang (Member IEEE) was born in Guangdong, China, in 1984. He received the B.S. degree in electronic engineering from Nanchang Hangkong University, Nanchang, China, in 2007, the M.S. degree in control engineering from Guangxi University, Nanning, China, in 2010, and the Ph.D. degree in power electronics from South China University of Technology, Guangzhou, China, in 2015.

From 2015 to 2017, he was a Postdoctoral Researcher with the Department of Electrical Engineering, Tsinghua University, Beijing, China. Since 2018, he has been an Associate Professor with the School of Automation, Guangdong University of Technology, Guangzhou, China. From December 2019 to December 2020, he was an ERCIM "Alain Bensoussan" Research Fellow with the Department of Electric Power Engineering, Norwegian University of Science and Technology, Trondheim, Norway. His current research interests include high-frequency power electronic solid-state transformer and flexible dc transmission and distribution systems.

Yuanpeng Guan was born in Hainan, China, in 1992. He received B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2014, the M.S. degree in power electronic from South China University of Technology, Guangzhou, China, in 2017, and the Ph.D. degree in power electronic from South China University of Technology, Guangzhou, China, in 2020.

He is currently an Associate Professor with the Energy Electricity Research Center, Jinan University, Zhuhai, China. His current research interests include grid-connected inverter and dual-active-bridge dc–dc converter.

Marta Molinas (Senior Member, IEEE) received the Diploma degree in electromechanical engineering from the National University of Asuncion, Asuncion, Paraguay, in 1992, the Master of Engineering degree in electrical engineering from Ryukyu University, Nishihara, Japan, in 1997, and the Doctor of Engineering degree in electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2000.

She was a Guest Researcher with the University of Padova, Padova, Italy, in 1998. From 2004 to 2007, she was a Postdoctoral Researcher with the Norwegian University of Science and Technology (NTNU), Trondheim, Norway, and from 2008 to 2014, she was a Professor with the Department of Electric Power Engineering, NTNU. She is currently a Professor with the Department of Engineering Cybernetics, NTNU, Trondheim, Norway. Her research interests include stability of power electronics systems, harmonics, instantaneous frequency, and nonstationary signals from the human and the machine.

Dr. Molinas is an Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, Associate Editor for *IEEE Power Electronics Society* and Editor of the IEEE TRANSACTIONS ON ENERGY CONVERSION. From 2009 to 2011, she was an AdCom Member of the IEEE Power Electronics Society.

Olav Bjarte Fosso (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the Norwegian Institute of Technology, Trondheim, Norway, in 1989.

He is currently a Professor with the Department of Electric Power Engineering, Norwegian University of Science and Technology (NTNU), Trondheim, Norway. He has previously held positions as Scientific Advisor and Senior Research Scientist at SINTEF Energy Research, and the Director of NTNUs Strategic Thematic Area Energy from September 2014–September 2016. From 2008 to 2014, he was a Chairman of CIGRE SC C5 Electricity Markets and Regulation and Member of CIGRE Technical Committee. He was expert evaluator in Horizon2020 and several science foundations, internationally. His research interests include hydro scheduling, market integration of intermittent generation, and signal analysis for study of power system's dynamics and stability.

Wang Hu was born in Hunan, China, in 1992. He received the B.S. degree from the University of South China, Hengyang, China, in 2015, and the M.S. degree in from the Guangdong University of Technology, Guangzhou, China, in 2018, both in electrical engineering. Since 2018, he has been working toward the Ph.D. degree in power electronic with South China University of Technology, Guangzhou, China.

His current research interests include high-power density rectifiers, matrix converters, and nonlinear control strategies.

Yun Zhang received the B.S. and M.S. degrees from the Hunan University, Changsha, China, in 1982 and 1986, respectively, and the Ph.D. degree from the South China University of Technology, Guangzhou, China, in 1998, both in control engineering.

He is currently a Professor with the School of Automation, Guangdong University of Technology, Guangzhou, China. His current research interests include the intelligent control systems, signal processing, and power electronics.