Magnetic Components Reduction in a Three-Phase PFC Converter by Using a Reconfigurable *LCL* Filter

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***Abstract*—Three-phase power factor correction (PFC) converters are the front-end stage of the power conversion that are required to be connected to the grid with a proper filter to meet international standards. A high-order *LCL* filter is a widely used solution to reduce the component size of the filter although it requires six inductors. In this article, a novel reconfigurable *LCL* filter that consists of only three inductors is proposed. The principle of the reconfigurable filter is to fully utilize the converter-side inductors by changing their position from the converter side to the grid side and vice versa. The filter is reconfigured by using three low-frequency (LF) bidirectional switches. The ultimate goal of the proposed topology is to reduce the magnetic components by half and achieve comparable grid current quality as the conventional topology. The proposed PFC topology is verified by a 1-kW experimental prototype. All the experimental results agree with the theoretical concepts and prove that the grid current quality of the proposed topology is comparable with the conventional topology.**

***Index Terms*—Current quality, *LCL* filter, magnetic component, power factor corrector, three-phase converter.**

I. INTRODUCTION

POWER systems are evolving by deploying more distributed generators (DGs), flexible AC transmission (FACTS) devices, and electrical loads in response to environmental and energy crisis. Power electronic converters are the backbone of the evolution since DGs, FACTS devices, and electrical loads are composed of power electronic converters. The recent advances in power electronic converters in terms of topology [1]–[5], control [6], and semiconductor [7], [8] have speeded up the evolution. An example of an electrical load in power systems is a three-phase power factor correction (PFC) converter that interfaces the grid and a load such as electrical vehicles [9] and telecommunication devices [10]. An active PFC aims to provide sinusoidal grid currents and unity power factor at the input. The aim is realized by applying a three-phase two-level rectifier together with necessary control loops. The result is sinusoidal currents at the input although it is contaminated with high-frequency (HF) current ripples. According to international standards such as IEC61000-3-2 [11], HF harmonics are not allowed to be injected into the grid network due to interference with other sensitive loads connected to the grid, transformer or inductor saturation, and extra power losses. Therefore, the active rectifier should be coupled to the grid by a proper filter. The filter topology selection deals with a tradeoff between size, cost, and the grid current quality.

A first-order filter gives the simplest solution [12]. In fact, it is the converter-side inductor without adding extra components. However, it requires a large inductance to reduce the current ripple in compliance with the grid codes. The large inductor is associated with a larger size, higher cost, larger voltage drop across the inductor, and sluggish system dynamic [12]. Therefore, the first-order filter is not suitable for applications above hundreds of kilowatts. To overcome the first-order filter drawbacks, high-order filters have been proposed. The idea is to use additional passive components but smaller in size together with satisfactory harmonic attenuation. The high-order *LCL* filter is widely used in grid-tied converters, shown in Fig. 1(b) [13]. The filter performance highly depends on an optimum design of the filter components. To this end, various design methods based on conceptual approach [14], analytical model [15], and parameter selection of the passive components [16] have been investigated. The trend in high-order filters continues to reduce the filter component size and ensuring high quality grid current. To this end, multiple parallel *LC* branches called Trap filters are added to the conventional *LCL* filter and forms *LTCL* filter as shown in Fig. 2(a) [17], [18]. Trap filters are targeted at the switching frequency and its multiples to attenuate the harmonics. This means that the conventional *LCL* filter needs smaller inductances, and consequently, smaller harmonic attenuation since the Trap filter has already eliminated the switching harmonics. However, resonance issues between parallel branches and a complex design procedure are the main drawbacks of the *LTCL* filter. To reduce the complexity of the *LTCL* filter, the filter capacitor of the *LCL* filter is replaced with a series *LC* branch to create the *LLCL* filter, shown in Fig. 2(b), which has an extra inductor compared to the *LCL* filter [19]. Instead of adding the extra inductor to form the *LLCL* filter, an *LCCL* filter, shown

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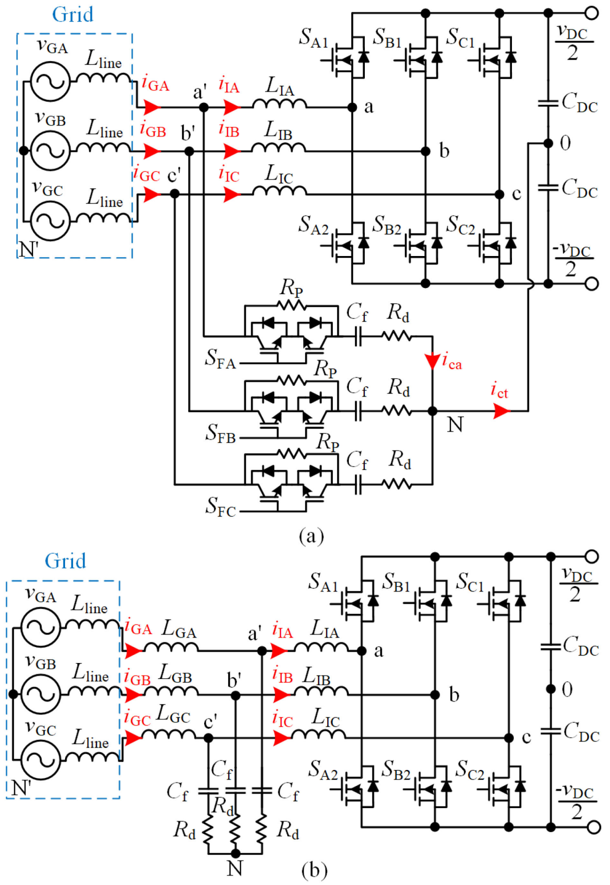


Fig. 1. (a) Proposed PFC topology, (b) Conventional PFC topology with an *LCL* filter.

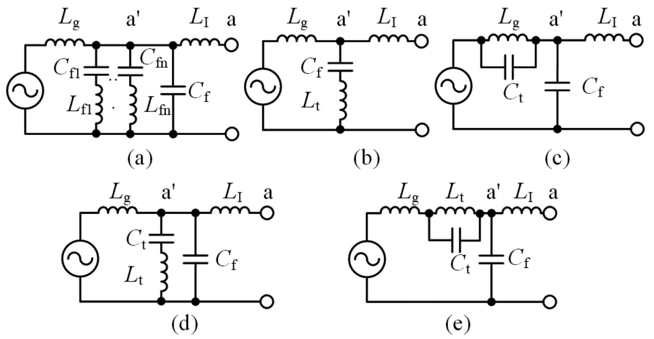


Fig. 2. Single-phase equivalent circuit of (a) *LTCL* filter, (b) *LLCL* filter, (c) *LCCL* filter, (d) modified *LLCL* filter, and (e) modified *LCCL* filter.

in Fig. 2(c), is formed by replacing a parallel *LC* branch with the grid-side inductor of the *LCL* filter to only have an extra capacitor compared to the *LCL* filter [20]. Although the *LLCL* and *LCCL* filters eliminate the switching frequency harmonics, the harmonic attenuation rate decreases from −60 dB/decade to −20 dB/decade in the HF band. To enhance the *LCCL* filter harmonic attenuation rate, one more extra inductor is added in series with the *LCCL* filter, shown in Fig. 2(e) [21]. Moreover, the *LLCL* filter is modified by adding a capacitor in parallel with its *LC* branch to improve the harmonic attenuation rate at high frequencies, shown in Fig. 2(d) [22]–[24]. Efforts in the literature to reduce the size of the *LCL* filter components end up with adding more passive components, which lead to design complexity, resonance issues, and weakening the filter performance.

In this article, a novel reconfigurable *LCL* filter is proposed to reduce the magnetic components by half with no extra passive components and ensuring satisfactory harmonic attenuation in a wide range of harmonic frequencies. The idea is based on the full utilization of the converter-side inductors and changing the filter structure in different operation modes. First, the full utilization of the converter-side inductors needs a special pulse-width modulation (PWM) technique called discontinuous PWM (DPWM) [25]. In three-phase three-wire systems (3p3w), the sum of the phase currents is zero, so if two out of three phase currents are being controlled, the third phase current naturally forms from the controlled phases. This inherent feature of the 3p3w systems can be deployed by applying DPWM techniques to only have two active legs switching at HF and a leg, which is clamped to either positive or negative DC bus, in each 60° interval over a line cycle. Therefore, there is one inductor, which is not used to shape the current. Second, the filter should be reconfigured in each operation mode to place the unused inductor at the grid side to construct the *LCL* filter topology between the grid and the converter. The filter is reconfigured by using low-frequency (LF) bidirectional switches connected in series with filter capacitors, shown in Fig. 1(a). The bidirectional switches act at LF, two times the line frequency, and their power losses are negligible. A criticism may arise regarding the proposed topology that the magnetic component reduction is at the cost of adding more semiconductors and gate drivers. It should be noted that the magnetic components are made up of copper and magnetic materials due to which their prices are increasing. However, semiconductor technology is advancing which results in cheaper products. Moreover, all the bidirectional switches and required gate drivers can be integrated into a small module. Therefore, by considering the future progress in semiconductor technology, the proposed topology gives a promising solution to the current quality issue of the grid-tied converters over the existing solutions.

The proposed topology was initially introduced in [1]. In this article, the proposed topology is elaborated in detail together with other improvements and changes highlighted in the following.

1) Expressing a detailed steady-state characteristic, frequency response, and loss analysis.
2) Improving the third-order harmonic injection and enhancing the grid current quality.
3) Providing design examples.
4) Verifying the proposed topology with extensive experimental results and comparison.

Two topologies are considered for comparison with the proposed topology. They are the conventional two-level topology with an *LCL* filter, shown in Fig. 1(b), and T-type topology with an *LCL* filter [26]–[28]. The former is a comparable candidate, and it is compared in detail with the proposed topology. However, the latter is not comparable due to differences in

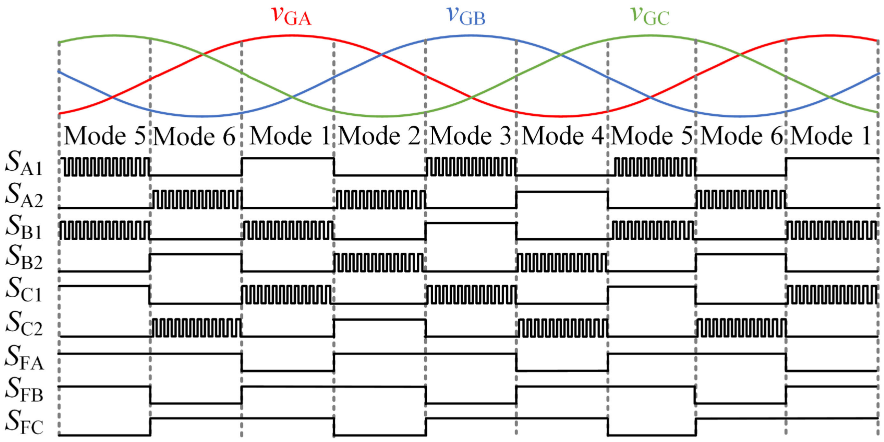


Fig. 3. Switching scheme of the proposed topology.

the principle of the operation, number of gate drivers, and the breakdown voltage of the bidirectional switches. Thus, the differences between the proposed topology and T-type topology are expressed in detail.

The rest of this article is organized as follows. The operation modes of the proposed topology are explained by referring to its equivalent circuits. The components selection of the filter is elaborated by investigating the steady-state characteristic and the frequency response of the proposed topology. Two case studies are designed that include both the conventional *LCL* filter and the proposed *LCL* filter. The case studies are tested and validated by a 1-kW, 208 Vrms-ll (line-to-line)/60-Hz prototype. The experimental results show that the proposed topology achieves grid current quality as good as the conventional topology while it requires three less inductors.

II. PRINCIPLE OF OPERATION

A. Operation Modes of the Proposed Topology

The proposed topology benefits from the inherent feature of the 3p3w systems, i.e., controlling three phase currents by only having two inductors at the converter side. The current under control could be the grid-side current or the converter-side current. The converter-side current is preferred and used in this article since current sensors at the converter side can be used for overcurrent protection of the switches [14]. It should be noted that the sum of the converter-side currents is not zero at high frequencies due to connection of the filter star point to the middle point of DC bus. However, from the fundamental frequency point of view, the sum of the converter-side currents are almost zero, and it agrees with the 3p3w systems. This assumption is based on the total capacitor current (i_{ct}), which contains mainly HF current ripples. The assumption is proved in Appendix and later is supported by an experimental result.

To deploy the feature of the 3p3w systems to reduce magnetic components, there are two prerequisites, i.e., reconfigurable filter structure and DPWM. The reconfigurable filter structure is made up of bidirectional switches working at twice the line frequency. In practice, the bidirectional switches can be made by two IGBTs as back-to-back in series. According to Fig. 1(a), one end of the bidirectional switches is connected to the inductors and the other end is connected to the filter capacitors C_f. Like the conventional *LCL* filter, the damping resistors R_d are placed in series with the filter capacitor. The junction point of the damping resistors is connected to the middle point of DC bus. DPWM is applied to make two converter legs operate at HF and the third leg disable. Therefore, the line cycle is divided into six segments, each segment lasts for 60°. For instance, according to the switching scheme of the proposed topology shown in Fig. 3, the phase voltage v_{GA} has the highest amplitude in Mode 1. Thus, the corresponding leg is disabled by turning $S_{A1} =$ ON and $S_{A2} =$ OFF, and two other legs including S_{B1} and S_{C1} operate at HF to shape the respected phase currents. Two sets of equivalent circuits are shown in Figs. 4 and 5. The equivalent circuits in Fig. 4 show how bidirectional switches form different filter structures in each mode and how the main switches turn to HF or disable modes. Taking Mode 1 in Fig. 4 as an example, S_{FA} is OFF, S_{FB} and S_{FC} couple filter capacitors C_f to the grid-side points of L_{IB} and L_{IC}, respectively. The transition from Mode 1 to Mode 2 is done by making Leg A operate at HF and disabling the switches of Leg C. Moreover, the filter is reconfigured by turning $S_{FA} =$ ON and $S_{FC} =$ OFF. Therefore, the new *LCL* filter is formed in Mode 2. According to the simplified equivalent circuits shown in Fig. 5, the *LCL* filter is constructed between the grid and the converter in all the operation modes by only three inductors. Therefore, the role of the inductors changes from the grid-side inductor to the converter-side inductor or vice versa in different modes. For instance, L_{IB} and L_{IC} are the converter-side inductors and L_{IA} is the grid-side inductor in Mode 1. However, L_{IA} acts as the converter-side inductor and L_{IC} acts as the grid-side inductor in Mode 2.

B. PWM and Third-Order Harmonic Injection

The novelty of the proposed topology is to fully utilize the magnetic components, which leads to overall magnetic components reduction. Full utilization of the magnetic components requires a special PWM technique, which is called DPWM.

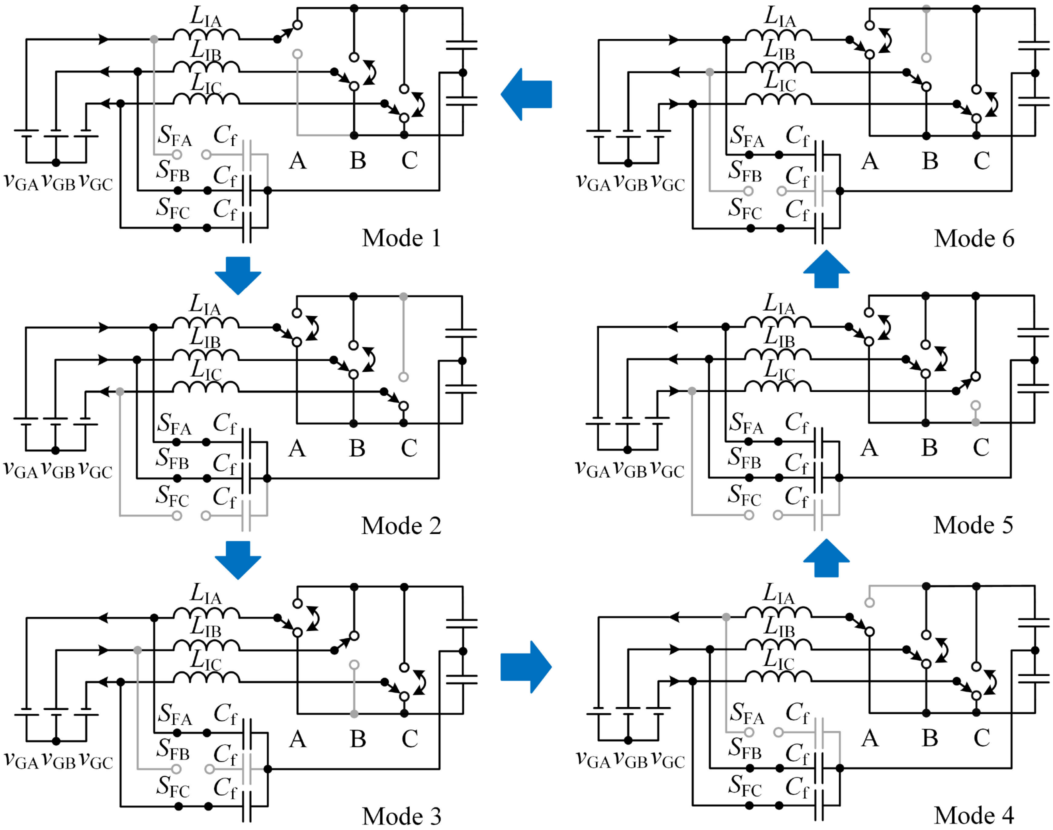


Fig. 4. Equivalent circuits of the proposed topology.

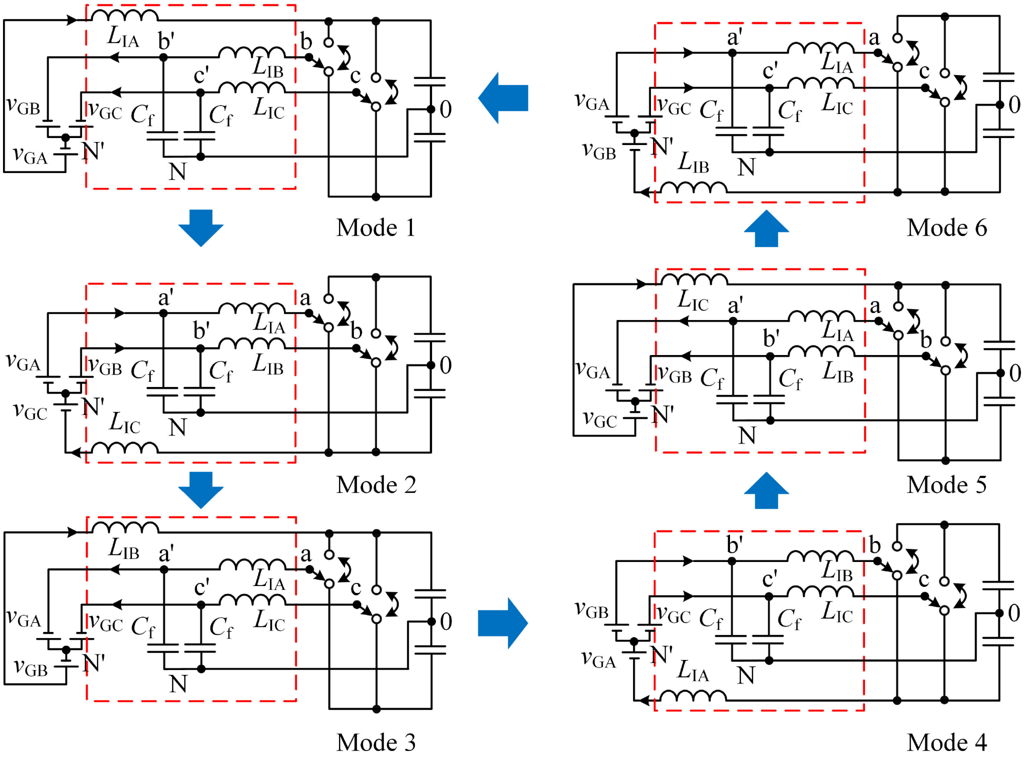
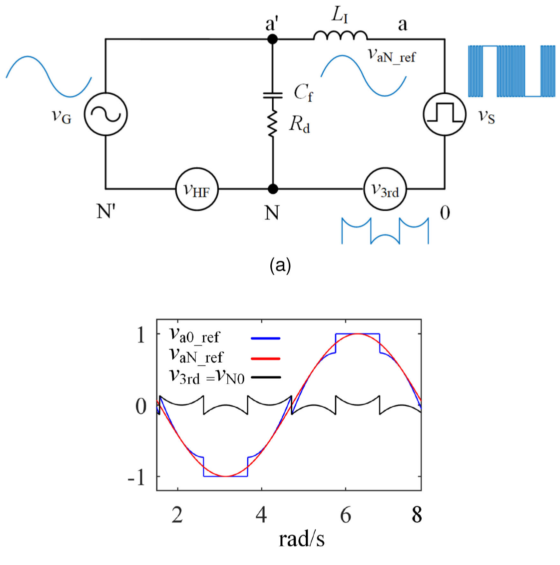


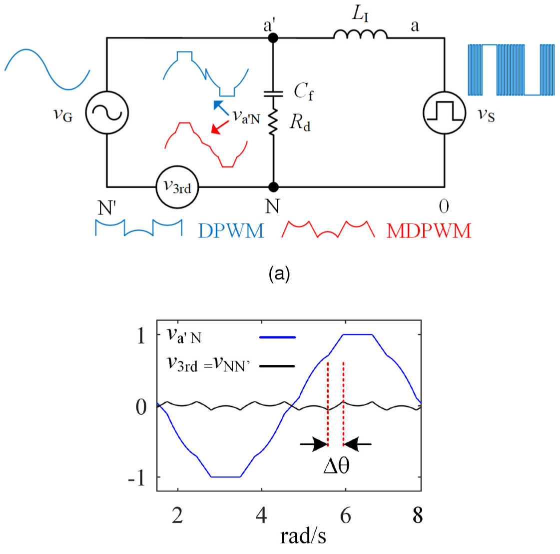
Fig. 5. Simplified equivalent circuits of the proposed topology.



(a)

(b)

Fig. 6. (a) General equivalent circuit of the conventional topology, (b) Key waveforms of the equivalent circuit.



(a)

(b)

Fig. 7. (a) General equivalent circuit of the proposed topology, (b) Key waveforms of the equivalent circuit.

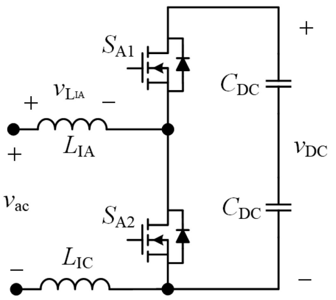


Fig. 8. Switching cell of the proposed topology in Mode 2.

According to the switching scheme in Fig. 3, the PWM signals of the main switches are discontinuous, which means the PWM signals are either zero or one in some operation modes during a line cycle. To investigate the third-order harmonic injection in the conventional topology and the proposed topology, two general equivalent circuits are shown in Figs. 6 and 7, respectively, in which the grid-side inductor is ignored due to its low voltage drop. According to the general equivalent circuit of the conventional topology shown in Fig. 6, the DPWM can be generated by applying space vector PWM (SVPWM), which injects a third-order harmonic to v_{N0} and v_{a0}. The voltages v_{N0} and v_{a0} contain the same third-order harmonic in magnitude but 180° shifted in phase. As a results, when they add up, the reference voltage v_{aN_ref} is generated, and its third-order harmonic is canceled. Moreover, there is HF voltage (v_{HF}) between *N* and *N'* in the conventional topology as shown in Fig. 6(a). The assumption of v_{HF} is ensured by the way the converter is controlled and later is supported by an experimental result. This voltage has a small amplitude, so the capacitor voltage $v_{a'N}$ is almost sinusoidal. However, the capacitor voltage $v_{a'N}$ is not sinusoidal in the proposed topology. According to the general equivalent circuit of the proposed topology shown in Fig. 7(a), the connection between *N* and 0 is shorted. Therefore, the third-order harmonic is injected between *N* and *N'*, and the capacitor voltage $v_{a'N}$ is made up of the grid voltage and the third-order harmonic. As a result, the capacitor voltage has sharp transitions, as shown in Fig. 7, which leads to spikes and ringing on the grid current. A possible solution to damp the ringing and spikes on the grid current is to increase R_d; however, it increases the power loss. Therefore, DPWM used for the conventional topology is not viable for the proposed topology. An effective solution is called modified DPWM (MDPWM) in which the third-order harmonic is modified as shown in Fig. 7(b) [29]. The third-order harmonic injected by MDPWM has a soft transition in the interval of $\Delta\theta$. During $\Delta\theta$, three converter legs operate at HF, all the bidirectional switches are ON, and the filter structure changes from *LCL* to *LC*. Therefore, a large $\Delta\theta$ increases the switching loss, conduction loss in the bidirectional switches, and degrades the filter performance.

III. STEADY-STATE CHARACTERISTIC

A. Converter-Side Inductor Current Ripple

To derive the steady-state characteristic of the proposed topology, the leg A in Mode 2 is considered and shown in Fig. 8. In this mode, S_{A1} is acting at HF, L_{IA} is the converter-side inductor, and the voltage drop on the grid-side inductor L_{IC} is negligible. The inductor voltage v_{LA} can be found as follows:

$$\begin{aligned} &S_{A2} \text{ is ON: } v_{L_{IA}} = v_{ac} \\ &S_{A2} \text{ is OFF: } v_{L_{IA}} = v_{ac} - V_{DC} \end{aligned} \tag{1}$$

where v_{ac} is the line-to-line AC voltage, and V_{DC} is the large signal output DC bus voltage. By applying the volt-second balance rule to the inductor voltage v_{LIA} during a switching

TABLE I
PARAMETERS OF CASE STUDY I

Parameters	Conventional topology	Proposed topology
L_{I}	5.8 mH	5.8 mH
L_{G}	3 mH	N/A
$\Delta I_{\max}$	0.33 A (12%)	0.33 A (12%)
$\Delta\theta$	20°	20°
f_{res}	2.5 kHz	1.8 kHz
f_{sw}	25 kHz	25 kHz
R_{d}	10 Ω	10 Ω
R_{p}	500 kΩ	500 kΩ
r	0.517	N/A
Harmonic attenuation	2.2%	1.1%

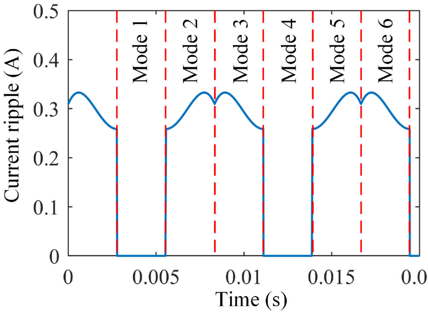


Fig. 9. Time-varying current ripple Δi_{IA}.

cycle, the duty ratio is found as

$$D(t) = 1 - \frac{v_{\mathrm{ac}}(t)}{V_{\mathrm{DC}}}. \tag{2}$$

By using (2), the current ripple in Mode 2 is expressed as

$$\Delta i_{IA}(t) = \frac{v_{\mathrm{ac}}(t)(V_{\mathrm{DC}} - v_{\mathrm{ac}}(t))}{2L_{IA} f_{\mathrm{sw}} V_{\mathrm{DC}}} \tag{3}$$

where f_{sw} is switching frequency. Similarly, the current ripple in other modes can be derived. The detailed derivations of (2) and (3) are explained in Appendix.

The time-varying current ripple of L_{IA} for the parameters listed in Table I is shown in Fig. 9. To plot Fig. 9, $\Delta i_{IA}(t)$ in all modes is required. Therefore, $\Delta i_{IA}(t)$ in (3) is used for Mode 2, and $\Delta i_{IA}(t)$ for other modes can be derived similar to (3). Moreover, it is assumed that Δi_{IA} is zero in Mode 1 and Mode 4 in which L_{IA} acts as the grid-side inductor.

B. Converter-Side Inductor Selection

The inductor value should limit the maximum inductor current ripple Δi_{IA} to a certain value. So, the maximum inductor current ripple $\Delta i_{\mathrm{IA,max}}$ is obtained by applying (4) to (3). Finally, the inductor value is selected as follows:

$$\frac{d(\Delta i_{IA}(t))}{dt} = 0 \tag{4}$$

$$\Delta i_{IA,\max} = \frac{V_{\mathrm{DC}}}{8L_{IA} f_{\mathrm{sw}}} \tag{5}$$

$$L_{IA} \geq \frac{V_{DC}}{8\Delta i_{IA,\max} f_{\mathrm{sw}}}. \tag{6}$$

TABLE II
EXPERIMENTAL SETUP SPECIFICATION

Parameters	Value
Grid voltage	208 Vrms-ll
Grid frequency	60 Hz
Power	1 kW
Resistive load	150 Ω
V_{DC}	390 V

The detailed derivation of (5) is explained in Appendix.

C. Filter Capacitor Selection

If the current controller is applied to the converter-side inductor current, the reactive power generated by the filter capacitor decreases the power factor. Therefore, C_{f} should be limited to 5% of the base capacitance [14]. The base capacitance is expressed as

$$C_b = \frac{1}{\omega Z_b} \tag{7}$$

where ω is the angular line frequency, and Z_{b} is the base impedance and is defined based on the rated power (P_{in}) as the following:

$$Z_b = \frac{V_{\mathrm{rms},ll}^2}{P_{\mathrm{in}}}. \tag{8}$$

D. Damping Resistor Selection

At the resonant frequency, the magnitude of the filter trans-admittance is infinity, which leads to harmonic amplification at the resonant frequency and controller instability. Therefore, the resonant peak should be limited by placing a damping resistor R_{d} in series with the filter capacitor C_{f}. The value of R_{d} can be obtained as one-third of the filter capacitor C_{f} impedance at the resonant frequency [14], [30]

$$R_d = \frac{1}{3\omega_{\mathrm{res}} C_f}. \tag{9}$$

E. $\Delta\theta$ Selection

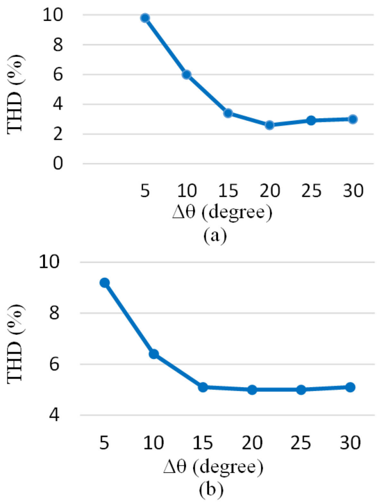
In the proposed topology, the C_{f} current is susceptible to sharp transients caused by the third-order harmonic as shown in Fig. 7. Therefore, to avoid spikes on the C_{f} current, the MDPWM method is used in which the third-order harmonic has soft transients in the interval of $\Delta\theta$. The parameter $\Delta\theta$ is selected to achieve the lowest grid current total harmonic distortion (THD). Therefore, a simulation is conducted for the parameters in Tables I and III to determine the optimum value of $\Delta\theta$ as shown in Fig. 10. According to that, the optimum value of $\Delta\theta$ is 20°.

F. Voltage Buffer

During each operation mode, one of the capacitors is disconnected. However, disconnected C_{f} needs a voltage buffer to avoid current spikes when it is reconnected in the following operation modes. The voltage buffer is realized by a simple resistor R_{P} across the LF switches, shown in Fig. 1(a). The value of R_{P} is

TABLE III
PARAMETERS OF CASE STUDY II

Parameters	Conventional topology	Proposed topology
L_{I}	3 mH	3 mH
L_{G}	0.347 mH	N/A
ΔI_{max}	0.647 A (23%)	0.647 A (23%)
$\Delta\theta$	20°	20°
f_{res}	6.35 kHz	2.5 kHz
f_{sw}	25 kHz	25 kHz
R_{d}	10 Ω	10 Ω
R_{p}	500 kΩ	500 kΩ
r	0.113	N/A
Harmonic attenuation	20%	3.7%



(a)
(b)

Fig. 10. Grid current THD versus different values of $\Delta\theta$: (a) Case I, (b) Case II.

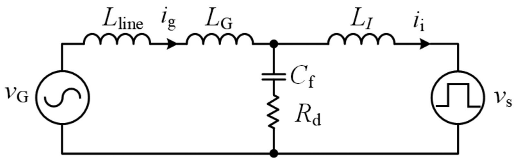


Fig. 11. Single-phase equivalent circuit of the conventional *LCL* filter.

determined based on the following two requirements, transition spikes on the grid current and power loss in R_{P}. In the target system, the best optimized value of R_{P} will be around 500 kΩ.

IV. FREQUENCY RESPONSE ANALYSIS

A. *Conventional* LCL *Filter*

To derive the frequency response of the conventional *LCL* filter, a single-phase equivalent circuit of the *LCL* filter, shown in Fig. 11, is considered. The source of harmonics is modeled by a voltage source v_{s} containing harmonics at the switching frequency and its multiples. By neglecting v_{G} at high frequencies, the trans-admittance of the conventional filter is defined as

$$Y_{\mathrm{Conv1}}(s) = \frac{i_g(s)}{v_s(s)} = \frac{R_dC_fs+1}{L_TL_IC_fs^3+(L_I+L_T)R_dC_fs^2+(L_I+L_T)s} \tag{10}$$

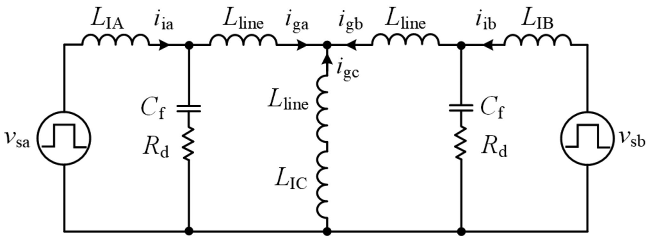


Fig. 12. HF equivalent circuit of the proposed topology in Mode 2.

where $L_{\mathrm{T}} = L_{\mathrm{G}} + L_{\mathrm{line}}$.

Moreover, the relationship between i_{i} and v_{s} is derived as

$$Y_{\mathrm{Conv2}}(s) = \frac{i_i(s)}{v_s(s)} = \frac{L_TC_fs^2+R_dC_fs+1}{L_IL_TC_fs^3+(L_I+L_T)R_dC_fs^2+(L_I+L_T)s}. \tag{11}$$

The harmonic attenuation rate between i_{g} and i_{i} is derived by combining (10) and (11) and expressed as

$$\frac{i_g(s)}{i_i(s)} = \frac{Y_{\mathrm{Conv1}}(s)}{Y_{\mathrm{Conv2}}(s)}. \tag{12}$$

In the conventional filter design, the filter capacitor is selected according to Section III-C, R_{d} is selected according to Section III-D, and the converter-side inductor L_{I} is determined to satisfy the current ripple requirement. Finally, the grid-side inductor L_{G} is determined to achieve desired harmonic attenuation. To this end, according to Fig. 13, the magnitude of (12) at the switching frequency is calculated as a function of *r*, i.e., the ratio of the total grid-side inductor (L_{T}) to the converter-side inductor. Then, based on the desired harmonic attenuation, the index *r* is determined, and L_{T} is obtained by

$$r = \frac{L_T}{L_I}. \tag{13}$$

By estimating the line impedance and having L_{T}, L_{G} is obtained. Line impedance is estimated based on the grid stiffness, which is defined by the short-circuit ratio (SCR). A weak grid SCR is in the rage of $2 \leq \mathrm{SCR} \leq 3$, and a strong grid has SCR > 3. By knowing SCR of the grid, the line impedance can be estimated [31].

By putting $R_{\mathrm{d}} = 0$ in (10), the resonant frequency of the conventional filter can be obtained as

$$f_{\mathrm{res\_conv}} = \frac{1}{2\pi}\sqrt{\frac{L_I+L_G}{L_IL_GC_f}}. \tag{14}$$

B. *Reconfigurable* LCL *Filter*

The frequency response of the reconfigurable *LCL* filter is derived by considering one of the equivalent circuits in Fig. 5. For instance, the HF equivalent circuit of Mode 2 is considered and shown in Fig. 12 in which v_{G} is neglected at the switching frequency, and switching actions are replaced with the source of harmonics v_{sa} and v_{sb}. Moreover, the line impedances are included in Fig. 12. Since the equivalent circuit in Fig. 12 cannot be simplified into a single-phase equivalent circuit, the superposition principle is used to derive the frequency response of the reconfigurable filter. By applying the superposition principle, two admittances are defined as

$$Y_{i_{gc}-v_{sa}}(s) = \left.\frac{i_{gc}(s)}{v_{sa}(s)}\right|_{v_{sb}=0}, Y_{i_{gc}-v_{sb}}(s) = \left.\frac{i_{gc}(s)}{v_{sb}(s)}\right|_{v_{sa}=0} \tag{15}$$

$$Y_{i_{gc}-v_{sa}}(s) = \frac{Z_2(Z_T Z_3 - Z_g Z_3 - Z_1 Z_2)}{(Z_g Z_3 + Z_1 Z_2)(Z_T Z_3 + Z_g Z_3 + Z_1 Z_2)} \tag{16}$$

where

$$Z_1 = L_I s, Z_g = L_{\text{line}} s, Z_2 = \frac{1}{C_f s} + R_d, Z_3 = Z_1 + Z_2$$

$$Z_T = \frac{(Z_1 + Z_g)(Z_1 Z_2 + Z_g(Z_1 + Z_2))}{(Z_1 + Z_g)(Z_1 + Z_2) + Z_g(Z_1 + Z_2) + Z_1 Z_2}. \tag{17}$$

Due to the symmetry in the HF equivalent circuit in Fig. 12, it is also deduced that

$$Y_{i_{gc}-v_{sa}}(s) = Y_{i_{gc}-v_{sb}}(s). \tag{18}$$

Finally, the complete response of i_{gc} to v_{sa} and v_{sb} is

$$i_{gc}(s) = Y_{i_{gc}-v_{sa}}(s) v_{sa}(s) + Y_{i_{gc}-v_{sb}}(s) v_{sb}(s). \tag{19}$$

By assuming

$$\begin{bmatrix} v_{sa}(s) \\ v_{sb}(s) \\ v_{sc}(s) \end{bmatrix} = \begin{bmatrix} 1 \\ e^{-\frac{2}{3}\pi j} \\ e^{\frac{2}{3}\pi j} \end{bmatrix} v_{sa}(s) \tag{20}$$

the trans-admittance of the reconfigurable filter is

$$Y_{\text{Recon1}}(s) = \frac{i_{gc}(s)}{v_{sa}(s)} = Y_{i_{gc}-v_{sa}}(s) + Y_{i_{gc}-v_{sb}}(s) e^{-\frac{2}{3}\pi j}. \tag{21}$$

Moreover, similar to Y_{Recon1}, the relationship between i_{ia} and v_{sa} is derived as

$$Y_{\text{Recon2}}(s) = \frac{i_{ia}(s)}{v_{sa}(s)} = Y_{i_{ia}-v_{sa}}(s) + Y_{i_{ia}-v_{sb}}(s) e^{-\frac{2}{3}\pi j} \tag{22}$$

where

$$\begin{aligned} Y_{i_{ia}-v_{sa}}(s) &= \frac{Z_g + Z_T + Z_2}{Z_2(Z_g + Z_T + Z_1) + Z_1(Z_g + Z_T)} \\ Y_{i_{ia}-v_{sb}}(s) &= \frac{-Z_2{}^2 (Z_1 + Z_g)(Z_g + Z_T + Z_2)}{(Z_3 Z_1 + Z_4)(Z_g + Z_T + Z_2)(Z_3 Z_T + Z_4)} \\ Z_4 &= Z_3 Z_g + Z_1 Z_2. \end{aligned} \tag{23}$$

By combing (21) and (22), the relationship between i_{gc} and i_{ia} is found as

$$\frac{i_{gc}(s)}{i_{ia}(s)} = \frac{Y_{\text{Recon1}}(s)}{Y_{\text{Recon2}}(s)}. \tag{24}$$

By putting $R_{\text{d}} = 0$ in (21), the resonant frequency of the reconfigurable filter can be obtained as

$$f_{\text{res\_Recon}} = \frac{1}{2\pi}\sqrt{\frac{3}{2 L_I C_f}}. \tag{25}$$

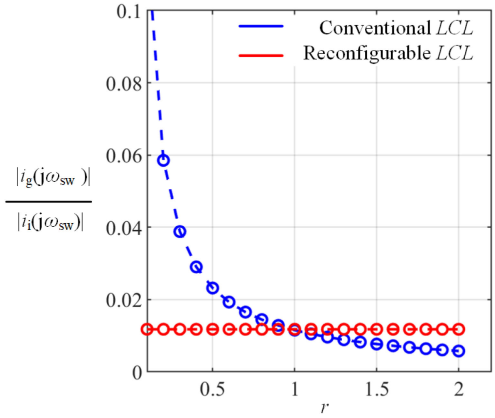


Fig. 13. Harmonic attenuation at the switching frequency as the function of *r*.

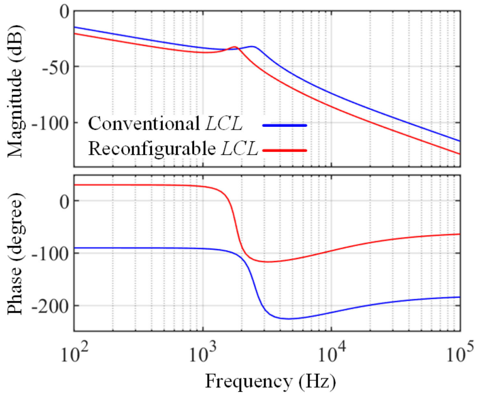


Fig. 14. Frequency responses of the conventional *LCL* filter and the reconfigurable filter.

C. Frequency Response Comparison and Evaluation

First, the harmonic attenuation and the frequency response of the conventional filter and the reconfigurable filter are compared for the parameters listed in Table I and assuming zero line impedance. The harmonic attenuation result is shown in Fig. 13. According to Fig. 13, the harmonic attenuation of the conventional filter varies by *r*. However, the harmonic attenuation of the reconfigurable filter is fixed since there is no grid-side inductor. It can be interpreted that the reconfigurable filter design has fewer degrees of freedom compared to the conventional one, but it should be noted that the intersection of the harmonic attenuations in Fig. 13 happens at $r = 1$. It means that the reconfigurable filter gives the same harmonic attenuation at the switching frequency as if the conventional one is used with $L_{\text{G}} = L_{\text{I}}$. The frequency responses of the conventional filter described in (10) and the reconfigurable filter described in (21) are shown in Fig. 14 with the parameters listed in Table I. The frequency response magnitude of the reconfigurable filter is lower than the conventional one in a wide range of frequencies, which shows the superior filtering performance of the reconfigurable filter. Second, the frequency response of the reconfigurable filter is evaluated in the presence of a line impedance. To this end, (21) is plotted for the parameters in Table I and $L_{\text{line}} = 1$ mH. The

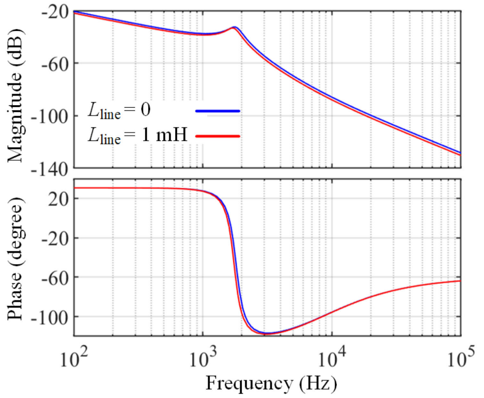


Fig. 15. Frequency responses evaluation of the reconfigurable filter with the presence of the line impedance.

result in Fig. 15 shows that the presence of the line impedance improves the filtering performance slightly since the magnitude of (21) reduces.

V. Design and Implementation

To verify the proposed PFC topology, two case studies are designed to evaluate the system in different working conditions. The experimental setup specifications are listed in Table II. In each case study, both the conventional topology and the proposed topology are included and compared.

A. Selection of the Filter Components

The first step is to determine the converter-side inductor. Both the conventional and the proposed topologies have the same method to determine the converter-side inductor. Referring to the steady-state characteristics and using (6), the converter-side inductor can be obtained. In Cases I and II, 12% and 23% current ripple are considered, respectively. The resultant L_{I} in Cases I and II is mentioned in Tables I and III, respectively.

In both case studies, the filter capacitor is selected according to Section III-C to limit C_{f} to less than 5% of the base capacitance. The resultant C_{f} is 3 μF. Considering the capacitor tolerance and available standard capacitors, C_{f} is selected to be 2.2 μF, which corresponds to 3.6% of the base capacitance. Moreover, the damping resistor is selected by (9). Regarding the conventional topology, there is one more step, i.e., grid-side inductor selection. In Cases I and II, 2.2% and 20% harmonic attenuations are considered, respectively, and the resultant r and L_{G} are mentioned in Tables I and III. Finally, the resonant frequencies are evaluated and mentioned in Tables I and III to make sure they do not conflict with the switching frequency. All the designed parameters are listed in Tables I and III.

B. Loss Analysis

A loss analysis is conducted to determine loss contribution of the proposed topology compared to the conventional topology. The dominant power losses are broken down to switching cell loss, magnetic loss, and filter loss.

1) Switching Cell Loss: A switching cell loss includes conduction loss and switching loss, which are calculated for a switching cell over half a line cycle. Given Fig. 8, which shows a switching cell in Mode 2, the conduction loss is contributed by the conduction loss of the main switch S_{A2} and the reverse channel of S_{A1}, which are expressed as the following, respectively:

$$P_{\text{cond\_}s} = f_{\text{grid}} \sum_{n=1}^{208} 0.11(id(n)-1)id(n)D(n) \tag{26}$$

$$P_{\text{cond\_}rs} = f_{\text{grid}} \sum_{n=1}^{208} 0.1id^2(n)(1-D(n)) \tag{27}$$

where f_{grid} is the grid frequency, *id* is the switch current, *D* is the duty cycle, and *n* is the sample number. Moreover, the turn ON and turn OFF switching losses are found as the following, respectively:

$$P_{\text{ON}} = f_{\text{grid}} \sum_{n=1}^{208} (24.375 + 3.65id_{\text{on}}(n)) \times 10^{-6} f_{\text{sw}} \tag{28}$$

$$P_{\text{OFF}} = f_{\text{grid}} \sum_{n=1}^{208} 14.625 \times 10^{-6} f_{\text{sw}} \tag{29}$$

where id_{on} is the switch current at the turn ON moment, which is equal to *id* - Δi. Thus, the total switching cell loss is

$$P_{ts} = 6(P_{\text{cond\_}s} + P_{\text{cond\_}rs} + P_{\text{ON}} + P_{\text{OFF}}). \tag{30}$$

2) Magnetic Loss: The magnetic loss consists of copper loss and core loss, which are expressed by the following, respectively:

$$P_{\text{copper}} = R_{\text{DC}} I_{\text{rms}} \tag{31}$$

$$P_{\text{core}} = 6.5 {f_{\text{sw}}}^{1.51} Bac^{1.74} Wt \tag{32}$$

where R_{DC} is the DC resistance of inductor winding, I_{rms} is the RMS value of the fundamental current component, B_{ac} is the flux density, and *Wt* is the core weight. In the conventional topology, the core loss of the grid-side inductors is ignored since the current ripple in the grid current is very small. Thus, the total magnetic loss in the proposed and conventional topologies are, respectively

$$P_{\text{tm,proposed}} = 3(P_{\text{copper}} + P_{\text{core}}) \tag{33}$$

$$P_{\text{tm,conv}} = \underbrace{3(P_{\text{copper}} + P_{\text{core}})}_{\text{converter side}} + \underbrace{3(P_{\text{copper}})}_{\text{grid side}}. \tag{34}$$

3) Filter Loss: Filter loss is caused by damping resistor loss and conduction loss of the bidirectional switches, in the case of the proposed topology. A simulation is conducted to determine harmonic content of C_{f} current in Cases I and II for both the proposed topology and the conventional topology, as shown in Fig. 17. The simulation parameters are listed in Table I, and the simulation step time is 1 μs. The filter loss in the conventional and the proposed topologies are described by the following,

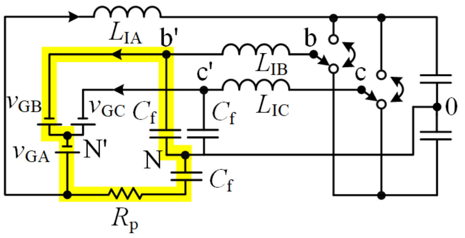


Fig. 16. Detailed equivalent circuit of the mode1 including R_p.

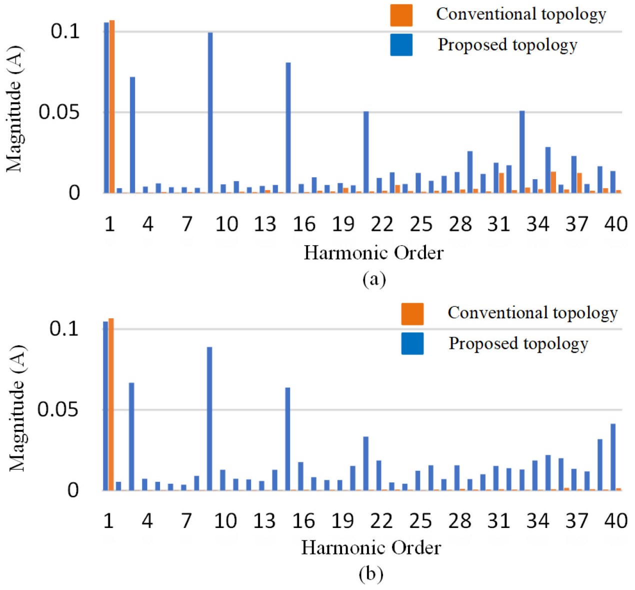


Fig. 17. Harmonic content of C_f current in the proposed topology and the conventional topology: (a) Case I, (b) Case II.

respectively:

$$P_{\text{filter,conv}} = R_d \sum_{m=1}^{600} i_c(m)^2 \tag{35}$$

$$P_{\text{filter,proposed}} = (R_d + R_{on}) \sum_{m=1}^{600} i_c(m)^2 \tag{36}$$

where m is the harmonic order and R_{on} is ON resistance of the bidirectional switches. Regarding to the proposed topology, R_P loss is not included in the total filter loss and assumed to be zero. To justify this assumption, R_P loss is evaluated by a detailed equivalent circuit of Mode 1, shown in Fig. 16, in which R_P is in series with C_f. At the fundamental frequency, the highlighted loop in Fig. 16 is considered in which C_f impedance is negligible compared to $R_P = 500$ kΩ. Therefore, the voltage across R_P is $v_{GAB} = 208$ V. It leads to 86 mW power loss in R_P, which is negligible and is not included in the total power loss.

According to the loss analysis, shown in Fig. 18, the magnetic loss is lower in the proposed topology for both cases due to the magnetic components reduction. However, the filter loss is higher in the proposed topology for both cases compared to the conventional topology. The higher filter loss in the proposed topology has two reasons. First, there are low order harmonics in C_f current, shown in Fig. 17(a) and (b), which are multiples of the third-order harmonic. The presence of the third-order harmonic in C_f voltage is elaborated in Section II-B. Second, the switching frequency harmonic in C_f current is higher in the proposed topology compared to the conventional topology. It is due to the fact that the proposed topology has higher harmonic attenuation rate as explained in Section IV-B. Moreover, the conduction loss in the bidirectional switches induced by R_{on} is negligible.

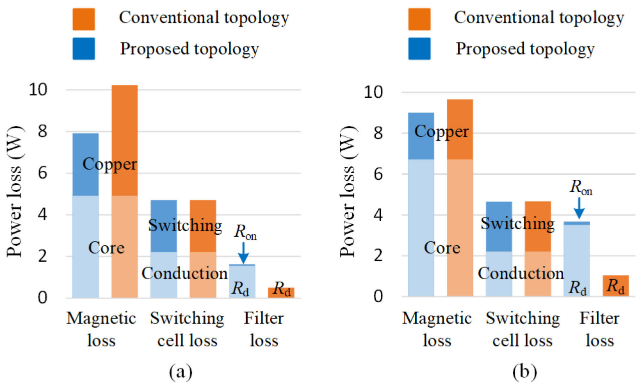


Fig. 18. Loss analysis: (a) Case I, (b) Case II.

C. Controller Design and Modeling

A dual-loop linear controller, shown in Fig. 19, is applied to the proposed topology. The outer loop aims to regulate output DC bus voltage, and the inner loop controls the converter-side inductor currents. To design the PI controllers and to conduct stability analysis, small-signal models of the inner loop and the outer loop are derived and shown in Fig. 20.

The first step is to design the inner loop controller. To this end, the state-space equation of the proposed topology is derived according to the general equivalent circuit in Fig. 7(a), and it is expressed as

$$\overrightarrow{v_{aN}} = -L_I \frac{d\overrightarrow{i_I}}{dt} - R_L \overrightarrow{i_I} + \overrightarrow{v_{a'N}} \tag{37}$$

where R_L is series resistance of the converter-side inductor. Afterwards, the inner loop plant transfer function ($T_{\text{plant,i}}$) is found by converting (37) to dq domain and adding decoupling terms as described in the following, respectively:

$$\begin{cases} v_{aN\_d} = -L_I \frac{di_{I\_d}}{dt} + \omega L_I i_{i\_q} - R_L i_{i\_d} + v_{a'N\_d} \\ v_{aN\_q} = -L_I \frac{di_{I\_q}}{dt} - \omega L_I i_{i\_d} - R_L i_{i\_q} + v_{a'N\_q} \end{cases} \tag{38}$$

$$\begin{cases} v_{aN\_d,\text{dec}} = -L_I \frac{di_{i\_d}}{dt} - R_L i_{i\_d} \\ v_{aN\_q,\text{dec}} = -L_I \frac{di_{i\_q}}{dt} - R_L i_{i\_q}. \end{cases} \tag{39}$$

The inner loop plant transfer function along with other transfer functions are shown in Fig. 20(a), in which T_s is the sampling time and $f_{c,i}$ is 25 kHz. Moreover, the outer loop plant transfer function ($T_{\text{plant,v}}$) is shown in Fig. 20(b) in which R_o is the resistive load and $f_{c,o}$ is 1 kHz. Finally, PI controllers of both

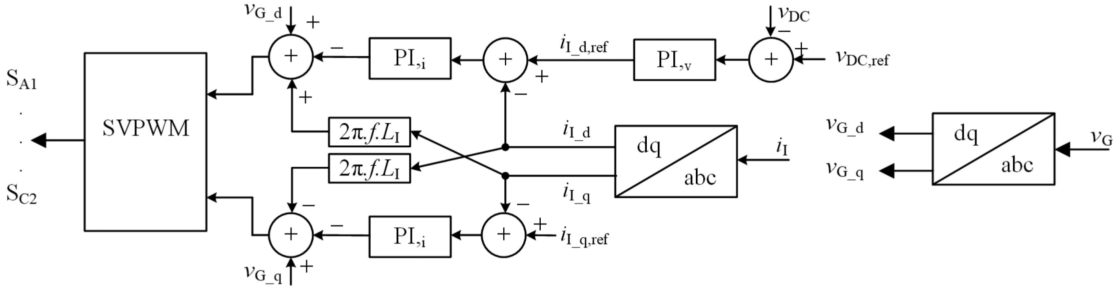
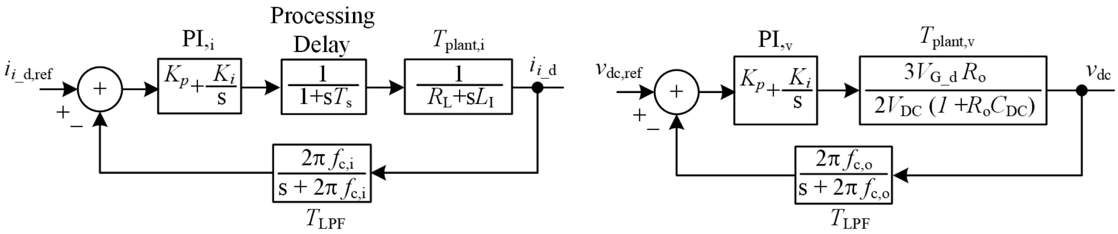


Fig. 19. Control block diagram of the proposed topology.



(a) (b)

Fig. 20. (a) Small-signal block diagram of the inner loop, (b) Small-signal block diagram of the outer loop.

TABLE IV
CONTROLLER DESIGN PARAMETERS

	Inner loop		Outer loop
	Case I	Case II	Case I and II
K_p	50 V/A	30 V/A	0.1 A/V
K_i	200 V/A/s	180 V/A/s	0.3 A/V/s
Phase margin	69°	66.3°	93°
Gain margin	26.5 dB	25.2 dB	61.7 dB
Band width	1.93 kHz	2.4 kHz	13 Hz

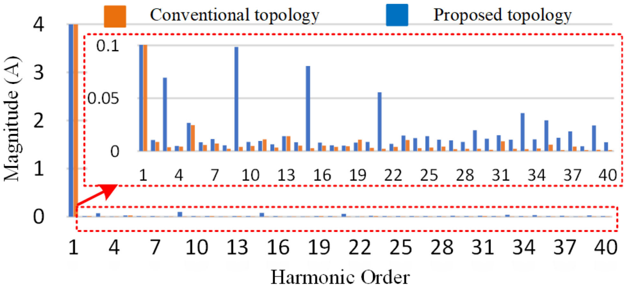
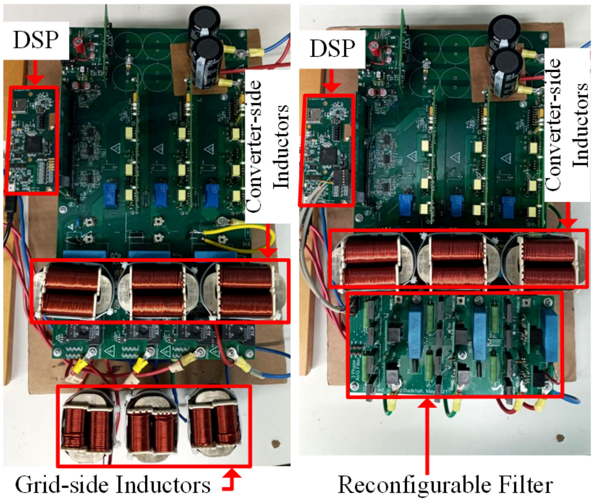


Fig. 21. Converter-side current harmonic comparison in Case I.

the inner loop and outer loop are designed to guarantee a stable operation. The controller parameters are listed in Table IV.

Since the converter-side current is under control, its current harmonic content is investigated to determine if LF switching of bidirectional switches create any extra LF harmonic. The simulation is conducted for the parameters in Table I with step time of 1 μs. According to the result shown in Fig. 21, LF switching of bidirectional switches does not create any significant LF harmonics compared to the conventional topology.

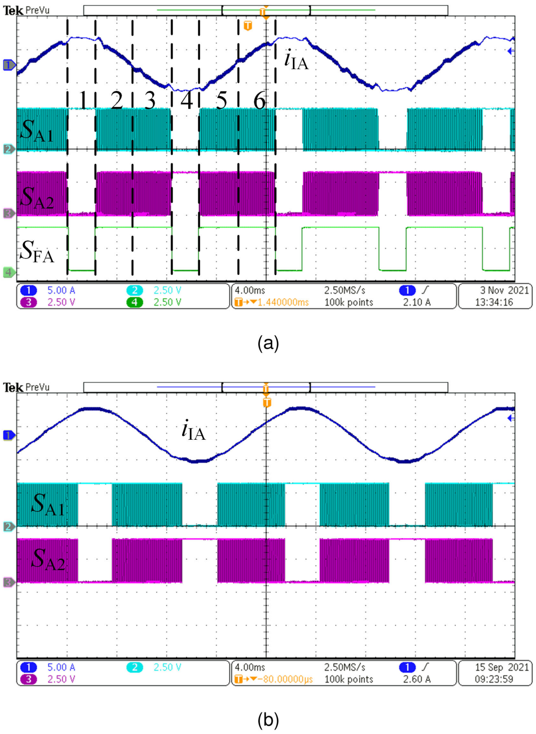


(a) (b)

Fig. 22. Experimental setup: (a) Conventional topology, (b) Proposed topology.

VI. EXPERIMENTAL VERIFICATION

The proposed topology is tested by an experimental prototype shown in Fig. 22. The base prototype is a two-level voltage source converter with the conventional filter. Moreover, the reconfigurable filter is also built and integrated into the system. So, it is possible to test both topologies and make a comparison. To verify the proposed topology and make a comparison with the conventional topology, two case studies are selected and designed in Section V. The prototype is tested for 1-kW,



(a)

(b)

Fig. 23. Case I, switching scheme: (a) Proposed topology, (b) Conventional topology.

TABLE V
COMPARISON RESULTS BETWEEN THE PROPOSED TOPOLOGY AND THE CONVENTIONAL TOPOLOGY

	Case I Conventional topology	Case I Proposed topology	Case II Conventional topology	Case II Proposed topology
Mean Current THD	2.7%	2.7%	4.532%	4.253%
Efficiency	98.318%	98.293%	98.553%	98.18%

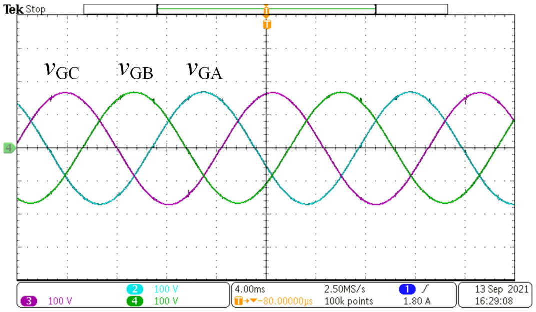


Fig. 24. Case I, the proposed topology: Grid voltage.

208 Vrms-ll (line-to-line)/60-Hz input, and 390-V output. The switching frequency and the sampling frequency are 25 kHz. The controller scheme is implemented in TI TMS320F28379D microcontroller. The same control scheme and the same switching frequency are also applied to the conventional topology to make a fair comparison. The experimental results are shown in Figs. 23–42 and Table V.

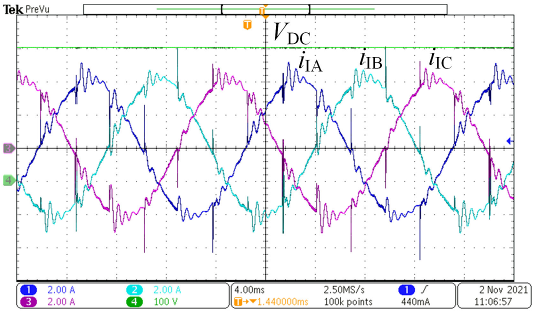
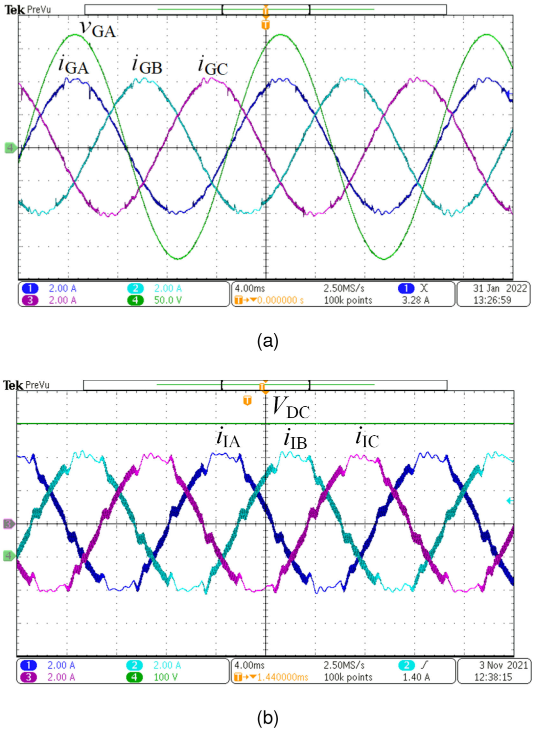


Fig. 25. Case I, the proposed topology: Grid current with DPWM.



(a)

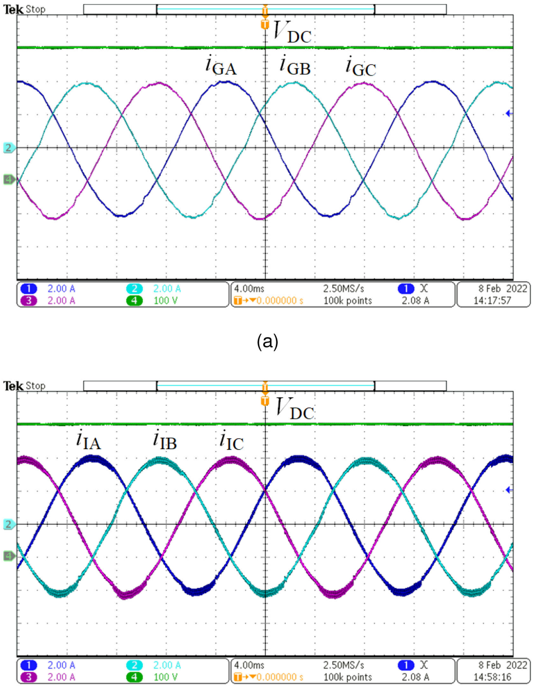
(b)

Fig. 26. Case I, the proposed topology: (a) Grid current, (b) Converter-side current.

A. Case Study I

The proposed topology is tested for the parameters of Case I listed in Table I. The switching scheme of phase A in the proposed topology is explored in Fig. 23(a). It shows that in Modes 1 and 4, phase A is disabled by turning S_{A1} and S_{A2} to ON or OFF. Moreover, the filter gate signal S_{FA} turns OFF in Modes 1 and 4 to change the role of L_{IA} from the converter-side inductor to the grid-side inductor. In Modes 2, 3, 5, and 6, phase A operates at HF, and the filter gate signal S_{FA} turns ON to change the position of L_{IA} from the grid side to the converter side. The conventional topology has the same switching scheme, shown in Fig. 23(b), with a fixed *LCL* filter structure. The grid voltage is shown in Fig. 24.

First, the proposed topology is tested with DPWM, and the resultant grid current is shown in Fig. 25. It shows that DPWM leads to spikes and ringing on the grid current. Second, the proposed topology is tested with MDPWM, and the grid current and



(a)

(b)

Fig. 27. Case I, the conventional topology: (a) Grid current, (b) Converter-side current.

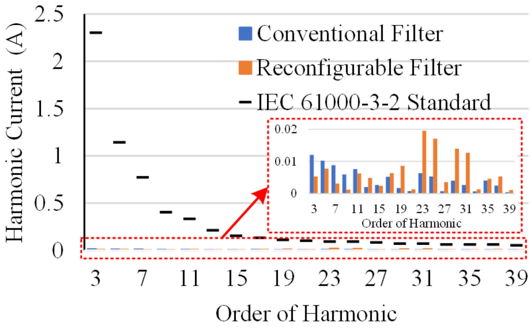


Fig. 28. Case I, the harmonic comparison.

the converter-side current are shown in Fig. 26(a) and (b), respectively. Moreover, the same test is conducted for the conventional topology and the results are shown in Fig. 27. The mean current THD is 2.7% for the proposed and the conventional topologies. It proves that the proposed topology achieves current quality as good as the conventional topology. Furthermore, the grid current harmonics of both topologies are compared with IEC61000-3-2 standard in Fig. 28. The comparison shows that the proposed topology meets the standard in all the harmonics with a great margin. The system efficiency is 98.293% and 98.318% for the proposed and conventional topologies, respectively. The power factor is 0.99 for both topologies, which shows that the reactive power is suppressed to almost zero.

The presence of the line impedance was shown to improve the filtering performance slightly according to Section IV-C. To verify the theoretical finding, the proposed topology is tested with the parameters in Table I along with adding $L_{\text{line}} = 1$ mH.

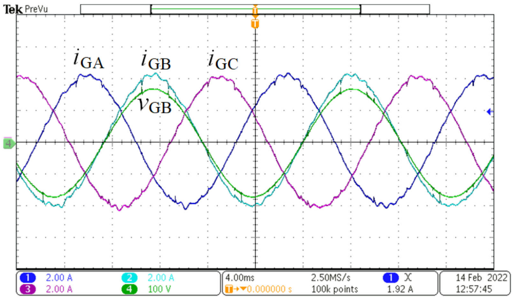


Fig. 29. Case I, the proposed topology: Effect of the line impedance on the grid currents and the grid voltage.

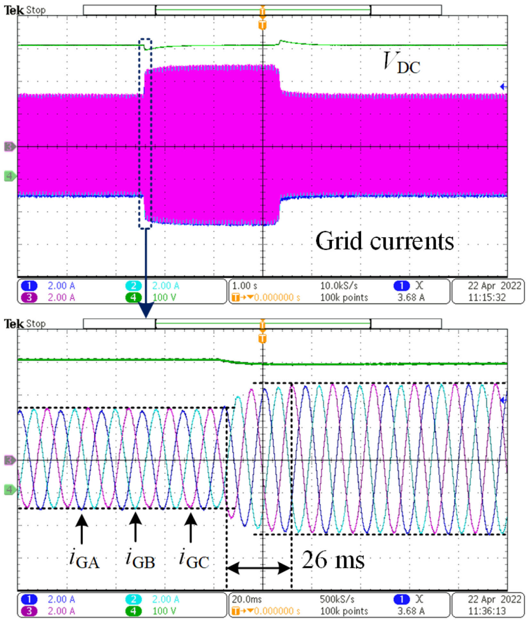


Fig. 30. Case I, the conventional topology: Dynamic response.

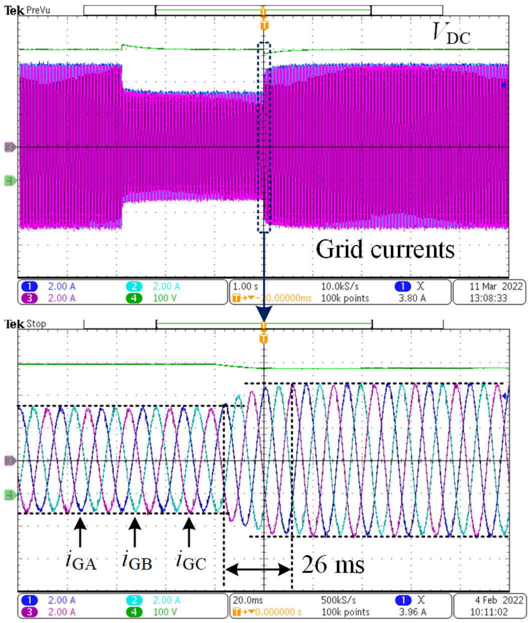


Fig. 31. Case I, the proposed topology: Dynamic response.

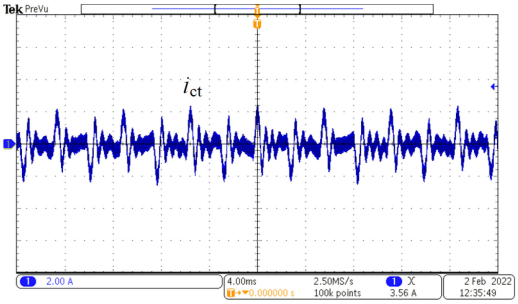


Fig. 32. Case I, the proposed topology: i_{ct}.

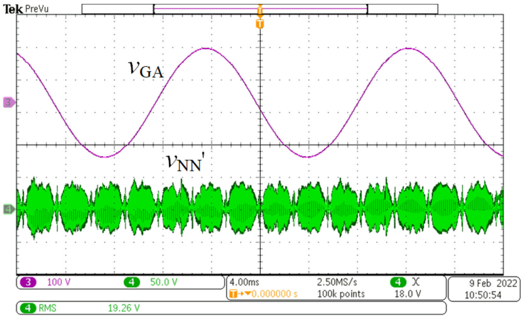


Fig. 33. Case I, the conventional topology: $v_{NN'}$.

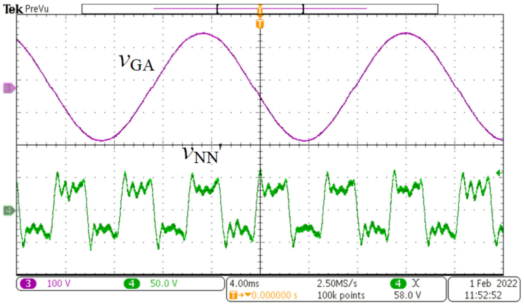


Fig. 34. Case I, the proposed topology: $v_{NN'}$.

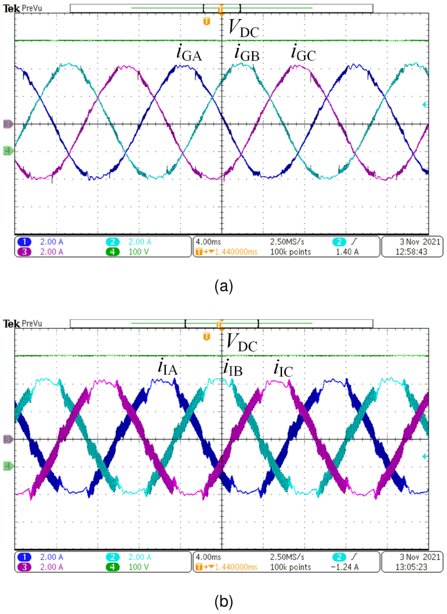


Fig. 35. Case II, the proposed topology: (a) Grid current, (b) Converter-side current.

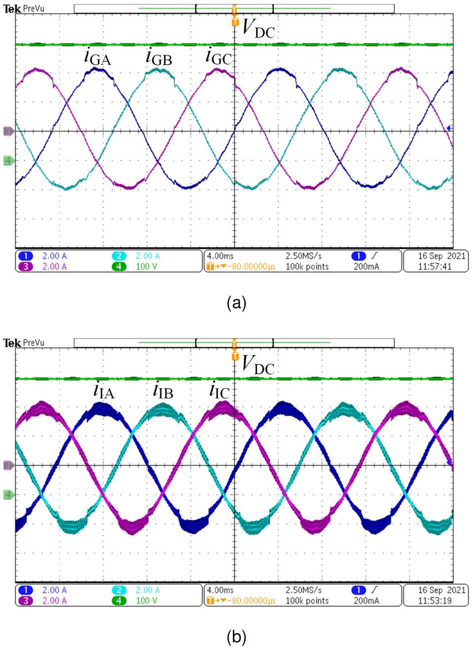


Fig. 36. Case II, the conventional topology: (a) Grid current, (b) Converter-side current.

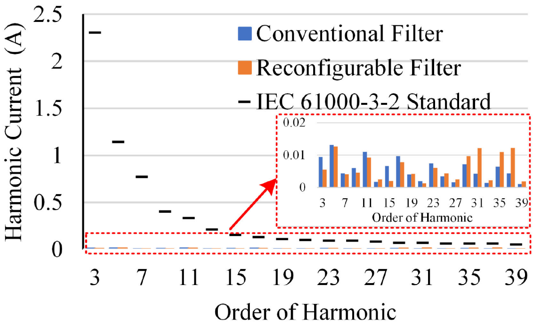


Fig. 37. Case II, the harmonic comparison.

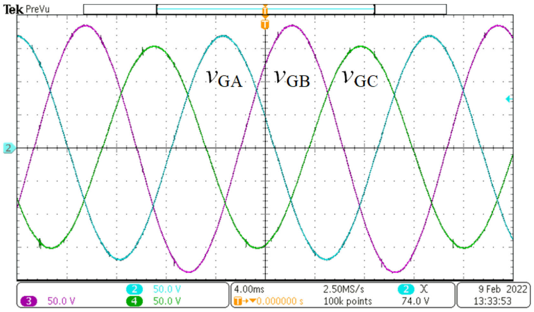


Fig. 38. Unbalanced grid voltage: $v_{GA} = 120$ V, $v_{GB} = 132$ V, and $v_{GC} = 108$ V.

The grid currents and Phase B grid voltage are shown in Fig. 29. The mean current THD reaches 2.5%, which shows the current THD improvement by 0.2 % compared to the similar case with $L_{\text{line}} = 0$. Moreover, the dynamic responses of the conventional and proposed topologies are investigated in Figs. 30 and 31, respectively, under a step change in the load. To this end, the load changes from 195 to 126 Ω, which corresponds to an increase

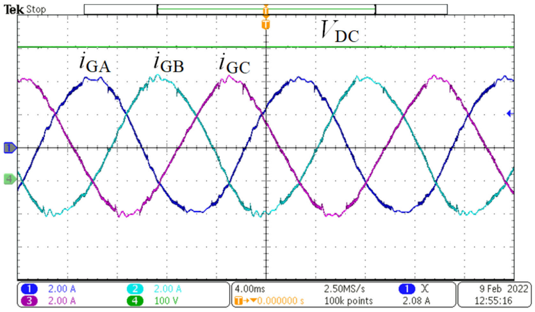


Fig. 39. Grid currents of the proposed topology under the unbalanced grid voltage.

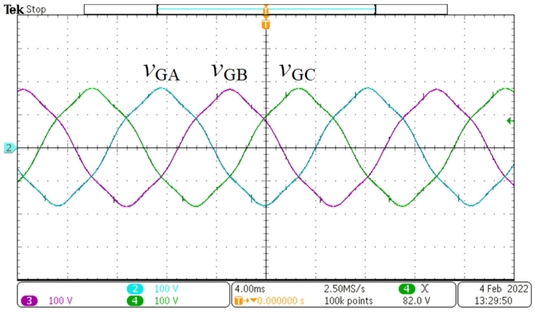


Fig. 40. Grid voltage containing the fifth harmonic with the magnitude of 5% of the fundamental harmonic.

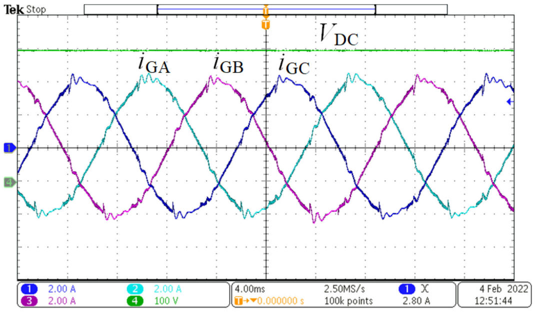


Fig. 41. Grid currents of the proposed topology under the grid voltage containing the fifth-order harmonic.

in the grid current from 2.16 to 3.33 A. The results in Figs. 30 and 31 show that the proposed and the conventional topologies with the settling time of 26 ms have almost the same dynamic response.

Two assumptions were made in Sections II-A and II-B, which are supported with experimental results in this section. In Section II-A, it is assumed that sum of the converter-side currents are zero at the fundamental frequency since i_{ct} contains only HF current ripples. The assumption is supported by measured i_{ct} in Fig. 32, which shows i_{ct} is mainly composed of HF current ripples. In Section II-B, the general equivalent circuits were derived for the conventional topology and the proposed topology in Figs. 6 and 7, respectively. In Fig. 6, $v_{\mathrm{NN'}}$ is assumed to be HF voltage with a small amplitude. The assumption is according to the measured $v_{\mathrm{NN'}}$ in Fig. 33, which shows that $v_{\mathrm{NN'}}$ is HF voltage with a small amplitude. Moreover, in Fig. 7, it is assumed that $v_{\mathrm{NN'}}$ contains the third-order harmonic. The assumption is according to the measured $v_{\mathrm{NN'}}$ in Fig. 34, which shows that $v_{\mathrm{NN'}}$ is composed of the third-order harmonic.

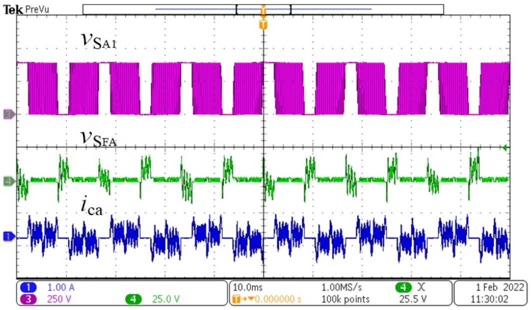


Fig. 42. Switch voltages and current of the proposed topology.

B. Case Study II

In this case study, the converter-side current ripple is increased, which means a smaller converter-side inductor is selected. Moreover, the harmonic attenuation of the conventional topology is decreased to see the effect of the grid-side inductor on the current quality. The grid current and the converter-side current are shown in Figs. 35 and 36 relating to the proposed and conventional topologies, respectively. In this test, 4.253% and 4.53% are the mean current THD of the proposed and conventional topologies, respectively. In Case II, the proposed topology achieves a better current quality compared to the conventional topology. The grid current harmonics of both topologies are compared with the IEC61000-3-2 standard in Fig. 37. The comparison proves that the proposed topology has a good compliance with the standard. The system efficiency in Case II is 98.18% and 98.553% for the proposed and conventional topologies, respectively, according to Table V. Comparing to Case I, the proposed topology achieves slightly lower efficiency in Case II. The lower efficiency is expected according to the loss comparison in Fig. 18, which was discussed in detail in Section V-B. However, it shows the drawback of the proposed topology, which decreases the system efficiency in all the cases.

C. Unbalanced and Nonideal Grid Voltage

The proposed topology is further validated under the unbalanced and nonideal grid voltage for the parameters in Table I. The unbalanced grid phase voltages are $v_{\mathrm{GA}} = 120$ V, $v_{\mathrm{GB}} = 132$ V, and $v_{\mathrm{GC}} = 108$ V, as shown in Fig. 38. Therefore, v_{GB} and v_{GC} are changed by 10% of the fundamental grid voltage harmonic. The resultant grid currents are shown in Fig. 39. The mean current THD in this case is 4%, which meets the standard. Moreover, the proposed topology is verified under a nonideal grid voltage by adding the fifth harmonic to the grid voltage with the magnitude of 5% of the fundamental grid voltage harmonic, as shown in Fig. 40. In this test, the proposed topology leads to a satisfactory grid current quality, shown in Fig. 41, with the mean current THD of 4%.

D. Proposed Topology Versus T-Type Topology

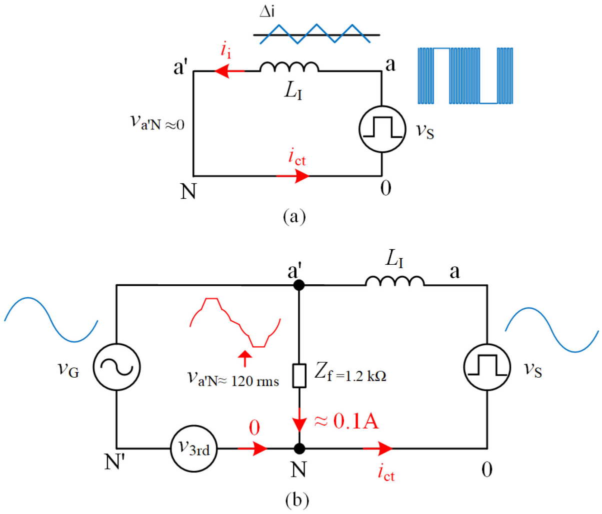
The proposed topology is compared with the conventional topology in different cases in Sections VI-A and VI-B. However, it may sound that the comparison is not fair or sufficient to prove the advantages of the proposed topology. The concern is raised since the proposed topology has more active switches compared to the conventional topology. Another candidate that may seem comparable at first glance is T-type topology [26]–[28] since it has the same number of active switches as the proposed topology. However, by scrutinizing the principle of operation of the topologies, there are profound differences, which make them incomparable. A few differences are explained in the following.

1) T-type topology is a three-level converter, while the proposed topology is a two-level converter. In T-type topology, the split capacitors are essential to create three voltage levels by connecting the star point of the bidirectional switches to the middle point of DC bus. However, in the proposed topology, the spilt capacitors are not essential, and the star point of the bidirectional switches can be connected to either positive DC bus, negative DC bus, or the middle point of the DC bus. In fact, the middle point of the DC bus is not used to create a voltage level in the proposed topology. The two-level operation of the proposed topology is evident from S_{A1} voltage, which is shown in Fig. 42.
2) The purpose of T-type topology is to reduce the current ripple, and it cannot eliminate the grid-side inductors. However, the purpose of the proposed topology is to eliminate the grid-side inductors. Moreover, the proposed topology can also be used in T-type topology to eliminate the grid-side inductors.
3) In T-type topology, each bidirectional switch needs two gate drivers if the common-emitter bidirectional switch configuration is used [32]; however, in the proposed topology, each bidirectional switch needs one gate driver. Moreover, the bidirectional switches in T-type topology act at HF, while the bidirectional switches in the proposed topology act at two times the line frequency. Thus, they need different type and number of gate drivers and different type of bidirectional switches, i.e., fast and slow switches.
4) The most important difference is the breakdown voltage of the bidirectional switches. In T-type topology, the breakdown voltage of the bidirectional switches is half of the DC bus voltage. However, in the proposed topology, the breakdown voltage of the bidirectional switches is less than 25 V according to S_{FA} voltage, which is shown in Fig. 42 along with S_{FA} current (i_{ca}).

As a result, due to the differences in the principle of operation, number of gate drivers, and breakdown voltage of the bidirectional switches, it is hard to draw a fair comparison between T-type topology and the proposed topology.

VII. CONCLUSION

This article presented a three-phase PFC with the reconfigurable filter. The reconfigurable filter changes the structure of the filter in each operation mode to fully utilize the magnetic components. To this end, three LF bidirectional switches are applied that act at two times the line frequency. The specific feature of the proposed topology is to achieve a satisfactory grid-current quality with only three inductors, while the same objective is met by the conventional topology with six inductors. The proposed topology is analyzed in detail in terms of equivalent circuits, the steady-state characteristic, and the frequency response. Moreover, the proposed topology is verified by the experimental prototype, and all the results show a good agreement with the theoretical concept.



(a)

(b)

Fig. 43. HF and LF analysis of Fig. 7(a): (a) HF analysis, (b) LF analysis.

APPENDIX

A. Proof of Section II-A

The equivalent circuit in Fig. 7(a) is analyzed from HF and LF point of views in Fig. 43(a) and (b), respectively. In HF analysis, the capacitor is assumed to be a short circuit, so i_{ct} is equal to HF current ripple. In LF analysis, the capacitor branch current is estimated to be 0.1 A, which is equal to i_{ct} and is negligible. Therefore, the assumption that states that i_{ct} consists of HF current ripple is proved.

B. Derivation of (2)

According to the volt-second balance, the average inductor voltage must be zero in a switching cycle. Therefore, using (1), the average inductor voltage during a switching cycle is expressed as

$$v_{\mathrm{ac}}(t)D(t)T_s + (v_{\mathrm{ac}}(t) - V_{\mathrm{DC}})(1 - D(t))T_s = 0 \tag{A.1}$$

where T_s is switching period. From (A.1), (2) is derived.

C. Derivation of (3)

The inductor charging characteristic during switch ON time is defined as

$$v_{L_{IA}} = L_{IA}\frac{2\Delta i_{IA}}{D(t)T_s} \tag{A.2}$$

where $2\Delta i_{IA}$ is the peak-to-peak current ripple. By substituting (2) into (A.2), (3) is found.

D. Derivation of (5)

The current ripple described in (3) can be simplified as

$$\Delta i_{IA}(t) = k v_{\text{ac}}(t)(V_{\text{DC}} - v_{\text{ac}}(t)) \tag{A.3}$$

where

$$k = \frac{1}{2L_{IA}f_{\text{sw}}V_{\text{DC}}}. \tag{A.4}$$

By applying (4) to (A.3), v_{ac}(t) is found as the following:

$$k\frac{dv_{\text{ac}}(t)}{dt}(V_{\text{DC}} - v_{\text{ac}}(t)) - k\frac{dv_{\text{ac}}(t)}{dt}v_{\text{ac}}(t) = 0 \tag{A.5}$$

$$v_{\text{ac}}(t) = \frac{V_{\text{DC}}}{2}. \tag{A.6}$$

By substituting (A.6) into (3), (5) is found.

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