High Efficiency Bidirectional Dual Active Bridge (DAB) Converter Adopting Boost-Up Function for Increasing Output Power

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***Abstract*—In this article, we proposed a bidirectional dual active bridge (DAB) converter adopting a boost-up function. The proposed converter can be implemented by adding only one capacitor to the high voltage side without additional active components. By utilizing the boost-up function, the proposed converter can achieve higher output power than the conventional DAB converter under the same leakage inductance condition. In comparison with the resonant converter in addressing the output power limitation, the proposed converter can reduce the switching and conduction losses due to the low turn-OFF and circulating currents, and complex control is not required to drive the synchronous rectifier. Furthermore, the direction of the output power can be easily changed with a simple control circuit. Experimental results from the proposed converter with a 3 kW rated power, 28-V low-side voltage, and 600-V high-side voltage are demonstrated to verify the proposed works.**

***Index Terms*—Bidirectional operation, boost-up function, capacitor adding, dual-active-bridge (DAB) converters.**

I. Introduction

BATTERY charging and discharging systems with bidirectional dc–dc converters are indispensable in energy storage systems, electric vehicles, and transportation systems. Generally, these applications use relatively low battery voltages, and require isolated dc–dc converters for safety reasons. For bidirectional isolated dc–dc converters, high efficiency, high power density, large conversion ratio for high power, and high reliability are significant challenges [1]–[9].

Various isolated dc–dc converters have been investigated for the bidirectional operation [10]–[29]. Among them, the dual active bridge (DAB) converter is widely used in many industrial applications owing to its simple structure and high performance. DAB converter was originally suggested in [10] and [11], and was analyzed comprehensively in [12] and [13]. Because the phase-shift-modulated DAB converter can operate under soft-switching conditions, it can minimize turn-ON switching losses. However, it exhibits high reverse energy and turn-OFF switching losses, which reduce the system efficiency. Various control techniques for DAB converters have been studied to improve their performance [14]–[19]. DAB converters with a resonant tank to achieve high efficiency were introduced in [20]–[23]. A modular design for increasing the output power was introduced in [24]–[29]. In [24], several modular bidirectional converters that use a DAB converter as the basic module were proposed. A composite modular energy storage system for a microgrid was investigated in [25]. Research on a parallel-input parallel output modular DAB converter for increasing the output power capability has been performed in [26]–[28]. Three modules of a 1.5 kW DAB converter were used in [29] for implementing a 4.5 kW electric vehicle charger. In various studies, the modular structure of the DAB converter with additional active components has been used to increase the output power because the output power of the DAB converter is limited by the leakage inductance determined by the structure of the transformer, which increases the cost and complexity. This is a critical problem for applications involving low-voltage batteries and high output power, because it is difficult to implement a small leakage inductance, which increases the number of modules.

In contrast to the DAB converter, the *LCC* resonant converter is a simpler solution for increasing the output power under the same leakage inductance by parallel resonance without a modular design. Furthermore, it offers several advantages, such as high efficiency and power density, owing to its soft-switching characteristics. In particular, because the *LCC* resonant converter operating in continuous conduction mode exhibits small conduction losses compared with the discontinuous conduction mode *LCC* resonant converter, it can be a suitable candidate

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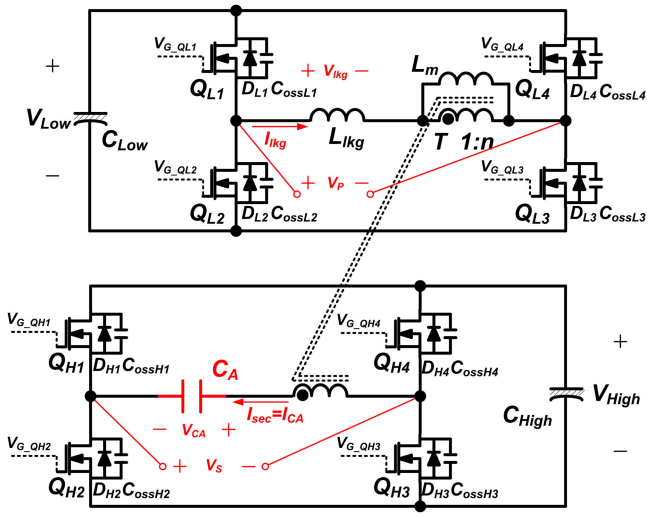


Fig. 1. Circuit diagram of the proposed converter.

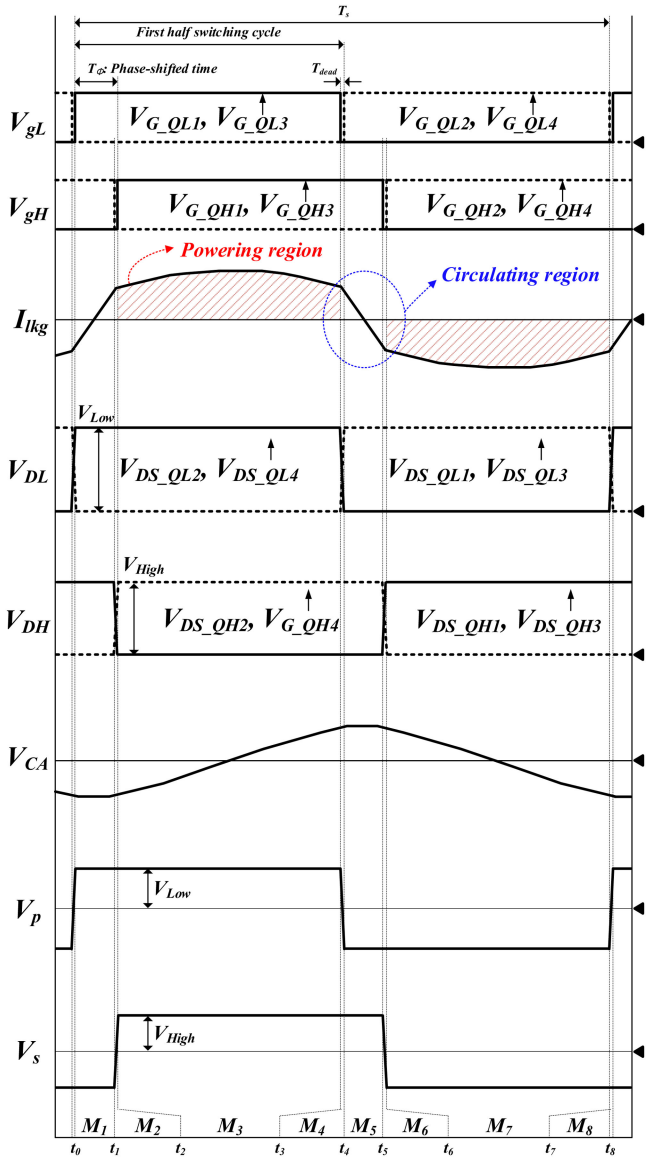


Fig. 2. Steady state waveforms of the proposed converter in step-up mode.

for applications with a high step-up ratio [30]–[36]. However, because resonant converters are based on frequency modulation, the optimal design of the passive components is difficult. In addition, large circulating and turn-OFF currents reduce efficiency. To solve these problems, phase-shifted modulated (PSM) *LCC* resonant converters were proposed in [37]–[38]. Although PSM control fixes the switching frequency, it reduces the zero voltage switching (ZVS) capability and increases the complexity of driving a synchronous rectifier (SR). Therefore, to address these problems, a hybrid control method involving a self-driven SR was used in [39], and the switched-capacitor method with a fixed frequency was presented in [40]. However, it is difficult to apply these methods to bidirectional dc–dc converters because of their asymmetrical circuit configurations.

In this article, we propose a bidirectional DAB converter adopting a boost-up function to address the aforementioned problems. In contrast to the conventional DAB converter, the output power is not limited by the leakage inductance owing to the boost-up function by the additional capacitor in the proposed circuit. Compared with the conventional *LCC* resonant converter, the proposed converter can be designed optimally owing to the phase-shift control with a fixed frequency, and it has low switching and conduction losses due to the reduced circulating current. Moreover, SR can be driven without a complicated control method. In addition, the power flow can be easily controlled using a simple circuit by changing the mode-selection signal. The performance of the proposed converter was confirmed through a prototype with 28 V low-side voltage, 600 V high-side voltage, and 3 kW rated power.

II. Proposed Converter

Fig. 1 shows the circuit configuration of the proposed converter. As shown in Fig. 1, the proposed converter is composed of capacitor filters ($C_{\rm Low}$ and $C_{\rm High}$), low-voltage (LV) side switches (Q_{L1}, Q_{L2}, Q_{L3}, and Q_{L4}), high-voltage (HV) side switches (Q_{H1}, Q_{H2}, Q_{H3}, and Q_{H4}), transformer (T), transformer leakage inductor (L_{lkg}), and auxiliary capacitor (C_A). The HV and LV side switches operate as SR in the step-up and step-down modes, respectively. In the proposed converter, C_A is a key component for increasing the output power through the boost-up function.

A. Operational Principle

Fig. 2 shows the steady state waveforms of the proposed converter in step-up mode. In Fig. 2, V_{gL} and V_{gH} are the gate-source voltages, and V_{DL} and V_{DH} are the drain-source voltages of the LV and HV-side switches, respectively. Q_{L1} and Q_{L2} (Q_{L3} and Q_{L4}) are operated in a complementary manner. After Q_{L1} (Q_{L3}) is turned ON, Q_{H1} (Q_{H3}) is turned ON with phase difference T_Φ. Q_{H1} and Q_{H2} (Q_{H3} and Q_{H4}) are operated in a complementary manner. As shown in Fig. 2, one switching

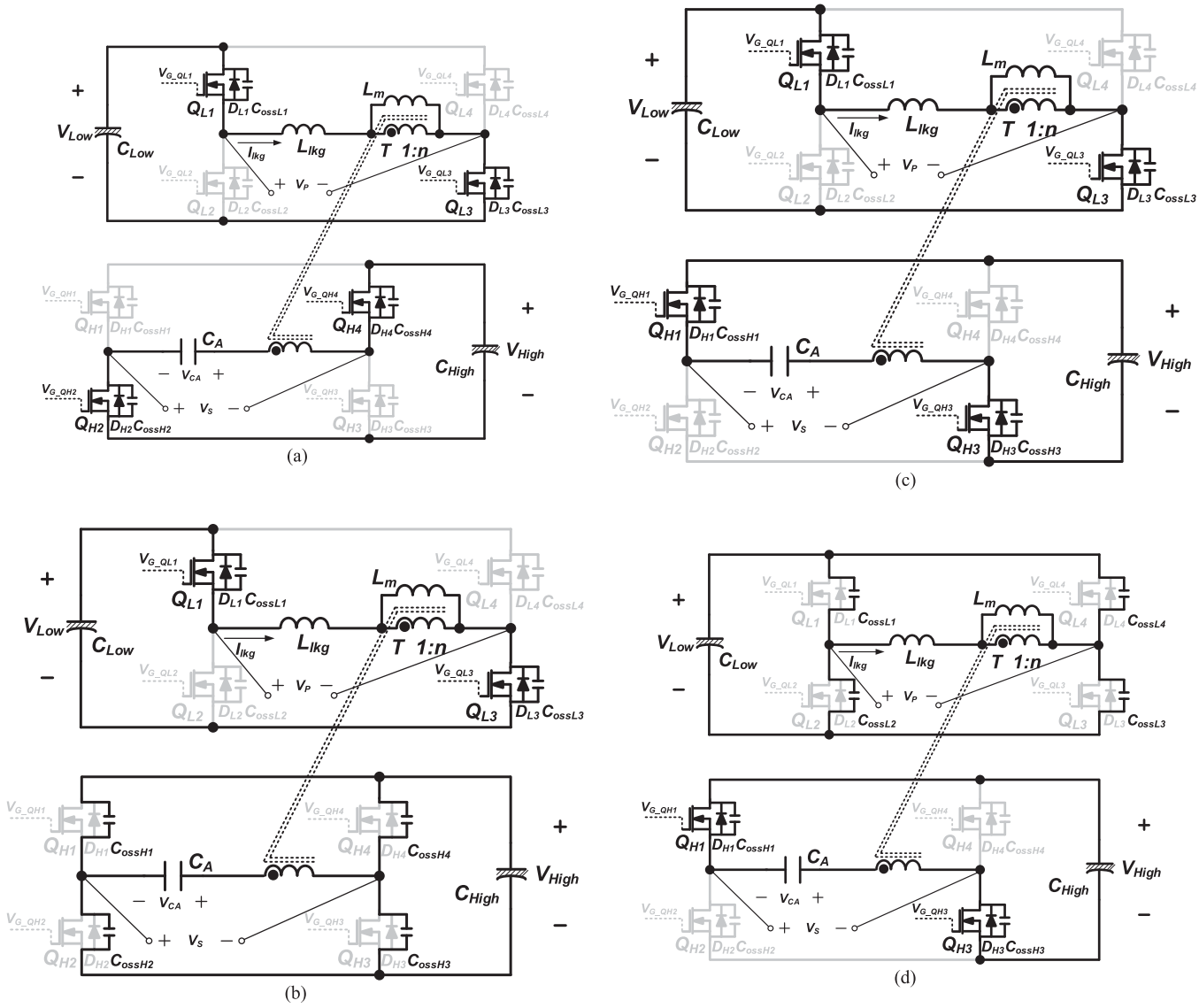


Fig. 3. Operating circuits during the first half cycle. (a) Mode 1. (b) Mode 2. (c) Mode3. (d) Mode 4.

period is divided into two half-periods (t_0–t_4 and t_4–t_8). Because the operation of each half-period is symmetrical, only the operation of the first half-period is explained. In addition, only the step-up mode operation is analyzed because the step-down operation is the same, except that the LV side switches are turned ON after the HV side switches are turned ON. Fig. 3 shows the operating circuits during the first half of the cycle. To perform mode analysis, the following assumptions were made.

1) Because $C_{\rm Low}$ and $C_{\rm High}$ are sufficiently large, $V_{\rm Low}$ and $V_{\rm High}$ can be considered as constant voltage sources.
2) All main switches are metal oxide semiconductor field effect transistors (MOSFETs) with parasitic diodes (D_{L1}, D_{L2}, D_{L3}, D_{L4}, D_{H1}, D_{H2}, D_{H3}, and D_{H4}).
3) The MOSFET output capacitances (C_{ossL1}–C_{ossL4} and C_{ossH1}–C_{ossH4}) are equal to C_{oss}.
4) The transformer magnetizing inductance L_m is sufficiently large, to allow the magnetizing current to be neglected.
5) The transformer turns ratio is $n = N_S/N_P$.

Mode 1 [t_0-t_1]: Mode 1 begins when Q_{H2} and Q_{H4} are in the ON-state, and Q_{L1} and Q_{L3} are turned ON with ZVS at t_0. In this mode, the primary-side voltage V_p is changed to positive, and the secondary-side voltage V_s and auxiliary capacitor voltage V_{CA} are negative. As shown in Fig. 4(a), the voltage difference between $V_{\rm Low}$ and (V_{CA}- $V_{\rm High}$)/n is applied to L_{lkg}. Thus, the leakage inductor current i_{lkg} increases linearly. V_{CA} remains almost constant because the sum of the charging and discharging currents of C_A is zero. Consequently, a large current builds up in the leakage inductor owing to the V_{CA}. The currents in this mode are expressed as follows:

$$I_{lkg}(t) = I_{lkg}(t_0) + \frac{V_{\rm Low} - (V_{CA} - V_{\rm High})/n}{L_{lkg}} \cdot t \quad (1)$$

$$I_{lkg}(t_0) = \frac{1}{2} \cdot \Delta i_{lkg} \quad (2)$$

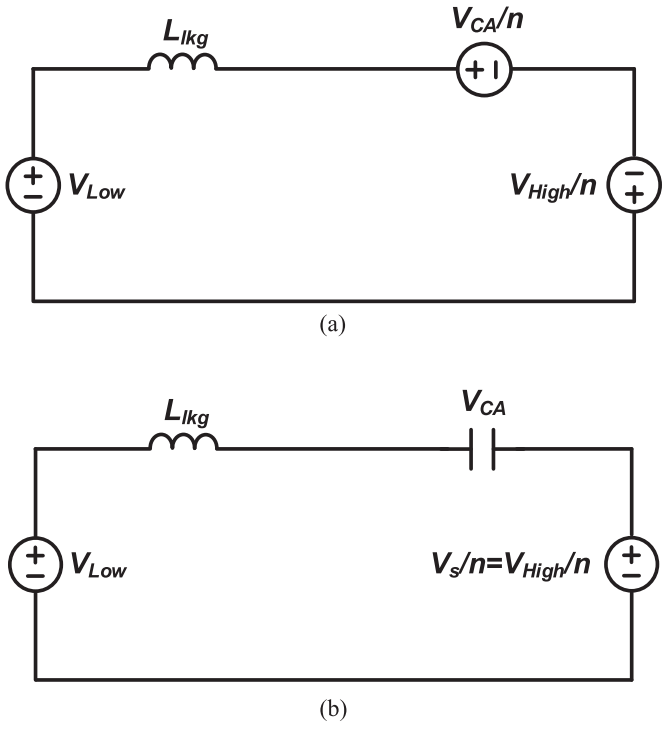


Fig. 4. Equivalent circuits of the proposed converter. (a) Mode 1. (b) Mode 3.

$$\Delta i_{lkg} = \frac{V_{\text{Low}} - (V_{CA} - V_{\text{High}})/n}{L_{lkg}} \cdot T_{\phi}. \tag{3}$$

Mode 2 [t_1-t_2]: Mode 2 begins when Q_{H2} and Q_{H4} are turned OFF at t_1. C_{Hoss2} and C_{Hoss4} are charged and C_{Hoss1} and C_{Hoss3} are discharged linearly by the reflected leakage inductor current I_{lkg}/n. Therefore, V_{QH1} and V_{QH3} decrease, and Vs increases with the slope as follows:

$$\text{Slope} = -\frac{I_{lkg}(t_1)/n}{4C_{OSS}} \approx -\frac{I_{lkg\_\text{peak}}/n}{4C_{OSS}}. \tag{4}$$

At the end of this mode, V_{QH1} and V_{QH3} reach zero, and V_s becomes V_{High}.

Mode 3 [t_2-t_3]: Mode 3 begins when Q_{H1} and Q_{H3} are turned ON, with ZVS at t_2. V_s is positive in this mode, as shown in Fig. 4(b). Owing to the resonance between C_A and L_{lkg}, V_{CA} becomes positive. i_{lkg} is reflected to the secondary side by the turns ratio n. Thus, the power is transferred from the primary to the secondary side through T, Q_{H1}, and Q_{H3}. The voltage and currents in this mode are expressed as follows:

$$i_{lkg}(t) = I_{lkg}(t_1) \cdot \cos w_r t - \frac{V_{CA}(t_2)}{Z_O} \cdot \sin w_r t \tag{5}$$

where, $w_r = \frac{1}{\sqrt{L_{lkg} \cdot n^2 \cdot C_A}}$, $Z_O = \sqrt{\frac{L_{lkg}}{n^2 \cdot C_A}}$

$$v_{CA}(t) = V_{CA}(t_2) \cdot \cos w_r t + Z_O \cdot I_{lkg}(t_2) \cdot \sin w_r t \tag{6}$$

$$i_{\text{sec}}(t) = i_{lkg}(t)/n. \tag{7}$$

Mode 4 [t_3-t_4]: Mode 4 begins when Q_{L1} and Q_{L3} are turned OFF at t_3. C_{ossL1} and C_{ossL3} are charged, and C_{ossL2} and C_{ossL4} are discharged linearly by the reflected leakage inductor current, I_{lkg}/n. Therefore, V_{QL2}, V_{QL4}, and V_P decrease with the slope, as follows:

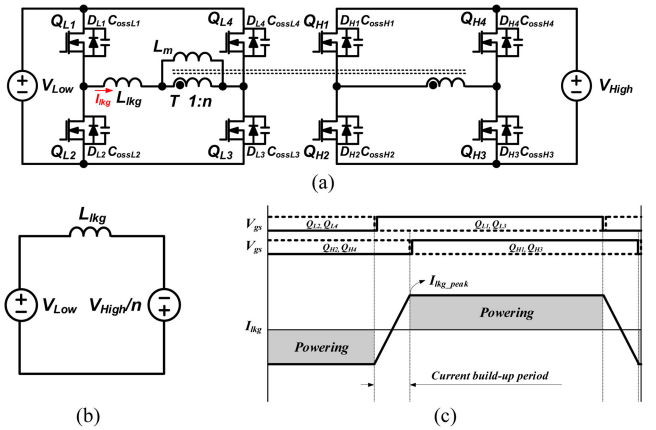


Fig. 5. Conventional DAB converter. (a) Circuit diagram. (b) Equivalent circuit in current build-up period. (c) Key waveforms.

$$\text{Slope} = -\frac{I_{lkg}(t_3)}{4C_{OSS}}. \tag{8}$$

At the end of this mode, V_{Q2}, V_{Q4}, and V_P become zero.

B. Features of the Proposed Converter

1) Increased Output Power: Compared with the conventional DAB converter, the proposed converter can achieve high power. Fig. 5 shows the circuit diagram, equivalent circuit in the current build-up period, and key waveforms of the conventional DAB converter. The sum of V_{Low} and V_{High}/n are applied to the leakage inductor, and the current increases, as shown in Fig. 5(b) and (c). In Fig. 5(c), the maximum current I_{Lkg_peak} is determined by the voltage applied to inductor V_{Low}+V_{High}/n, phase-shifted time T_{Φ}, and leakage inductance. To increase the output power, I_{Lkg_peak} should be increased by adjusting the aforementioned parameters. However, the leakage inductance limits I_{Lkg_peak} and the maximum output power despite changing other parameters.

The proposed converter can increase I_{Lkg_peak} by using the boost-up function of C_A without additional active components. Fig. 6 shows the circuit diagram, equivalent circuit in the current build-up period, and key waveforms of the proposed converter. As shown in Fig. 6(b), the voltage applied to the leakage inductor is the sum of V_{Low}, V_{High}/n, and V_{CA}/n. Thus, it is possible to generate a large current to supply power. Therefore, the proposed converter can increase the output power using large build-up current.

To compare the output power numerically, equations were derived using the following assumptions. The dead-time T_{dead} in Fig. 2 was ignored to simplify the analysis, because the duration was practically narrow. Moreover, the leakage inductor current during M3 is linearly approximated as the intermediate value of the changing current. Furthermore, we assumed that the voltage change of the auxiliary capacitor in M1 was sufficiently small

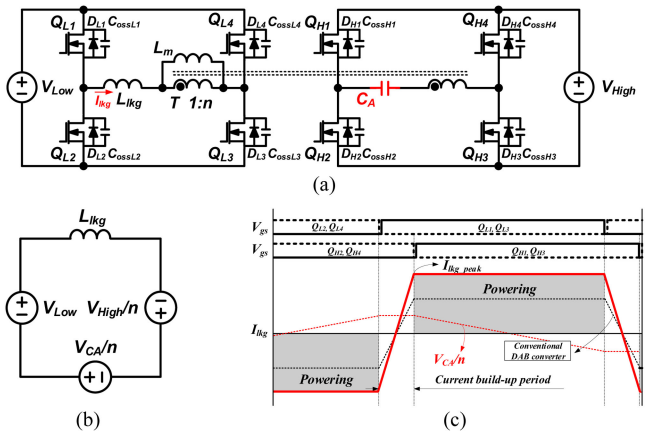


Fig. 6. Proposed converter. (a) Circuit diagram. (b) Equivalent circuit in current build-up period. (c) Key waveforms.

to be negligible. Consequently, the simplified waveforms shown in Fig. 7 can be obtained.

The input power P_{IN} can be calculated from the I_{lkg} waveform as

$$P_{IN} = 2 \cdot f_{sw} \cdot (-Q_1 + Q_2 + Q_3) \cdot V_{\text{Low}} \tag{9}$$

$$\text{where } Q_1 = Q_2 = \frac{1}{4} \cdot I_{lkg\_\text{peak}} \cdot \Delta t_1 \tag{10}$$

$$Q_3 = \int_{t_1}^{t_2} I_{lkg}(t)dt = I_{lkg\_\text{peak}} \cdot \Delta t_2. \tag{11}$$

The time duration of each section can be expressed as follows:

$$\Delta t_1 = \phi_r \cdot \frac{1}{f_{sw}} \tag{12}$$

$$\Delta t_2 = \frac{1}{f_{sw}} \cdot (0.5 - \phi_r) \tag{13}$$

where ϕ_r is the phase difference ratio between the LV and HV bridges ($T_\varnothing/T_s$). As Q_1 and Q_2 in Fig. 7 have the same value, the total power transferred to the output during t_0-t_1 is zero. From (9) and (11), the input power can be obtained as follows:

$$P_{IN} = 2 \cdot f_{sw} \cdot V_{\text{Low}} \cdot I_{lkg\_\text{peak}} \cdot \Delta t_2. \tag{14}$$

The actual build-up current without approximation $I_{lkg\_\text{peak}\_R}$ is half of the current build-up during t_0-t_1 and can be obtained as

$$I_{lkg\_\text{peak}\_R} = \frac{1}{2} \cdot \frac{V_{\text{Low}} + \frac{V_{\text{High}}}{n} + \frac{V_{CA\_\text{peak}}}{n}}{L_{lkg}} \cdot \Delta t_1. \tag{15}$$

By calculating the amount of charge accumulated during t_1-t_2, the peak voltage of the auxiliary capacitor V_{CA_peak} can be expressed as

$$V_{CA\_\text{peak}} = \frac{\frac{\Delta t_1 \cdot \Delta t_2}{4n \cdot C_A \cdot L_{lkg}} \cdot \left(V_{\text{Low}} + \frac{V_{\text{High}}}{n}\right)}{1 - \frac{\Delta t_1 \cdot \Delta t_2}{4n \cdot C_A \cdot L_{lkg} \cdot n}}. \tag{16}$$

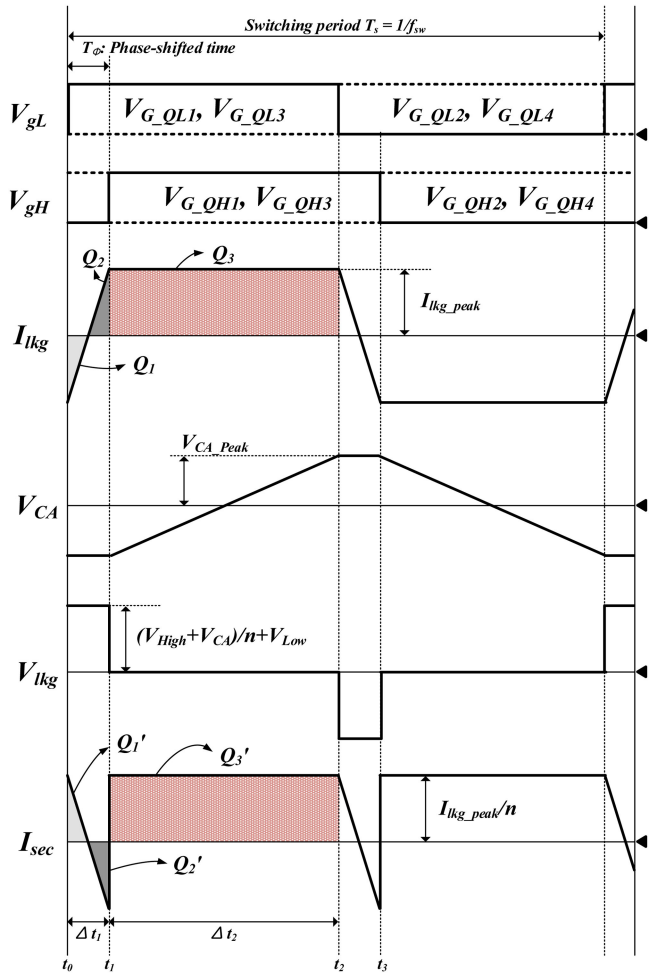


Fig. 7. Simplified operating waveforms of the proposed converter.

The approximated peak current in Fig. 7 can be calculated as follows:

$$I_{lkg\_\text{peak}} = I_{lkg\_\text{peak}\_R} + \frac{1}{2} \cdot \left[I_{lkg\_\text{peak}\_R} \cdot \cos\left[\tan^{-1}\left(\frac{V_{CA\_\text{peak}}}{n \cdot Z_O \cdot I_{lkg\_\text{peak}\_R}}\right)\right] + \frac{V_{CA\_\text{peak}}}{n \cdot Z_O} \cdot \sin\left[\tan^{-1}\left(\frac{V_{CA\_\text{peak}}}{n \cdot Z_O \cdot I_{lkg\_\text{peak}\_R}}\right)\right]\right]. \tag{17}$$

Assuming that the efficiency is η, the output power can be calculated using (15)–(17), and the following equation:

$$P_{\text{OUT}} = 2 \cdot \eta \cdot f_{sw} \cdot V_{\text{Low}} \cdot I_{lkg\_\text{peak}} \cdot \Delta t_2. \tag{18}$$

For example, let L_{lkg} = 1.3 uH, switching frequency f_{sw} = 23 kHz, low side voltage V_{Low} = 28 V, high side voltage V_{High} = 600 V, η = 95%, and auxiliary capacitor C_A = 220 nF. The estimated output power using the abovementioned equations and assumed parameters is shown in Fig. 8. To verify the derived equations, the simulated data of the proposed converter using PSIM are shown in Fig. 8. As observed from Fig. 8, the proposed converter has a higher output power than the conventional DAB converter with the same ϕ_r. In addition, the

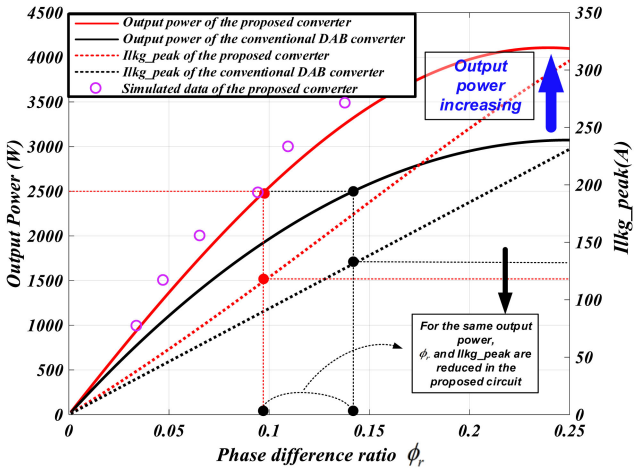


Fig. 8. Estimated output power and the peak value of the primary current.

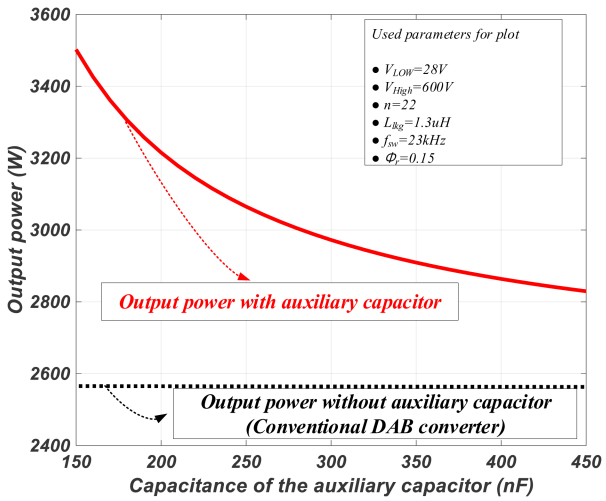


Fig. 9. Output power of the proposed converter according to the auxiliary capacitor value.

proposed circuit exhibits a smaller circulating loss because the phase differences ϕ_r and I_{lkg_peak} of the proposed converter are small for the same output power. In particular, Δt_1, the section in which reactive power occurs, is short. Fig. 9 shows the output power of the proposed converter based on the auxiliary capacitor value. As shown in Fig. 9, the proposed circuit can overcome the output power limitation caused by leakage inductance through the simple capacitor addition.

2) Reduced Switching and Conduction Losses: The proposed converter can reduce conduction and switching losses compared with the *LCC* resonant converter. The *LCC* resonant converter can promote a higher primary current and increase the output power than the conventional DAB converter under the same leakage inductance condition owing to the parallel resonance characteristics [30], [36]. However, the frequency modulation and parallel resonant characteristics cause large circulating current and turn-OFF switching losses. Fig. 10 demonstrates the I_{Lkg} waveforms of the *LCC* resonant converter according to the load conditions. As the load current decreased, the ratio of the

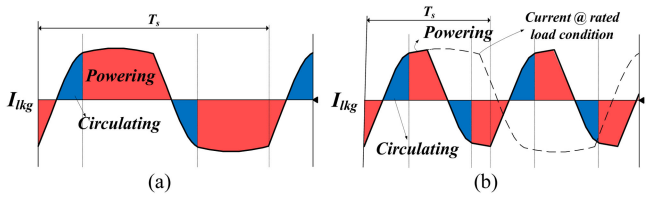


Fig. 10. Primary current waveforms of the *LCC* resonant converter as load decreases. (a) Rated load condition. (b) Light load condition.

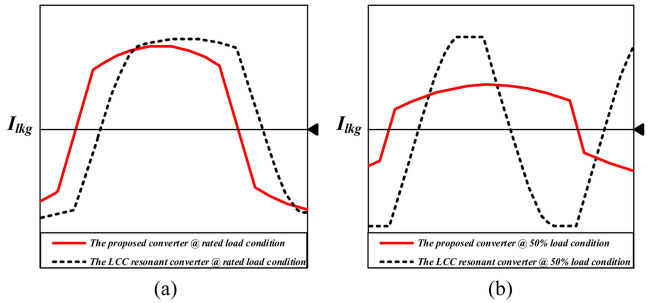


Fig. 11. Primary current waveforms of the *LCC* resonant converter and the proposed converter. (a) Rated load condition. (b) Light load condition.

circulating area to the powering area increased, which caused increased conduction losses. Because the current at the turn-OFF instant is maintained at a high value and the switching frequency increases under light load conditions, the turn-OFF switching losses become greater. The proposed converter primarily aims to provide a simple solution to increase the output power without the aforementioned problems that occur with the *LCC* resonant converter.

Fig. 11 shows the primary-side current waveforms of the *LCC* resonant converter and proposed converter according to the load conditions. As shown in Fig. 11(a), during the rated power operation, the current shapes of the resonant and proposed converters are similar. However, the current shape varies significantly under light load conditions, as shown in Fig. 11(b). The proposed converter reduces the build-up current according to the load condition using phase-shift control with a fixed frequency. Therefore, the proposed converter can obtain a higher output power than the conventional DAB converter while overcoming the disadvantages caused by the *LCC* resonant converter.

3) Simple Controller: A complex control circuit is required in the *LCC* resonant converter to drive SR switches in the powering region. However, in the proposed converter, the SR switches are automatically driven in the powering region using phase-shift control without an additional control circuit. In addition, by controlling the mode selection signal in the implemented controller, the power flow direction can be easily changed from the step-up mode (step-down mode) to the step-down mode (step-up mode).

III. Design and Implementation of the Proposed Converter

This section describes the design and implementation of the proposed 3-kW converter with the following specifications.

1) LV side voltage: $V_{Low} = 28$ V.
2) HV side voltage: $V_{High} = 600$ V.
3) LV side maximum current: $I_{Low} = 107$ A.
4) HV side maximum current: $I_{High} = 5$ A.
5) Switching frequency: $f_{sw} = 23$ kHz.

A. Design of the Proposed DAB Converter

1) Transformer Design: The power capacity handled by the transformer can be obtained from Fig. 2 as

$$P_{T\_\max} = V_{Low} \cdot I_{o\_\max} \cdot n \approx 3080\,[VA]. \tag{19}$$

The area product of magnetic core required for the power capacity can be expressed as

$$AP = W_a \cdot A_e = \frac{P_{T\_\max} \cdot 10^4}{4 \cdot \eta \cdot \Delta B \cdot f_{sw} \cdot K_u \cdot J} \approx 95\,\text{cm}^2 \tag{20}$$

where W_a is the available window area of the core in cm^2, A_e is the effective cross-sectional area of the core in cm^2, η is the transformer efficiency, ΔB is the flux density swing in T, f_{sw} is the switching frequency in Hz, K_u is the window utilization factor, and J is the current density in A/cm^2. To implement the transformer, it was assumed that $\eta = 0.85$, $\Delta B = 0.27$, $K_u = 0.15$, and $J = 120$ A/cm^2. Based on the abovementioned conditions, a ferrite core UI of 80×95×30, with $A_p = 128$ cm^4 and $A_e = 6$ cm^2, was selected to implement the transformer in the proposed converter. The minimum turns (N_P) on the LV side is obtained by

$$N_P \geq \frac{V_{P(\max)} \cdot 10^4}{4 \cdot \Delta B \cdot f_{sw} \cdot A_e} \approx 1.96. \tag{21}$$

The number of turns on the HV side is calculated from the N_P using the turns ratio (n). The voltage gain of the proposed converter (M) is $V_{\text{High}}/(\text{n}V_{\text{Low}})$, which it is the same as that of the conventional DAB converter because the applied average voltage applied by the V_{CA} to the transformer is zero. The actual primary and secondary turns in the prototype converter are Np = 2 and Ns = 44, respectively, considering a voltage gain of 1.

2) Measurement of Leakage Inductance: Many interrelated factors are considered in the design of the DAB converter. Therefore, after determining the transformer, the leakage inductance is measured, its value is fixed in this design. Leakage inductance is used as the energy-transfer element in the converter. With the short condition of the transformer secondary side, the leakage inductance was measured as 1.3 uH in the implemented transformer. Meanwhile, L_m should be designed to be at least ten times larger than L_{lk} to avoid power degradation of the converter.

3) Auxiliary Capacitor (C_A) Selection: Selection of an appropriate C_A value is important because C_A plays a crucial role in the boost-up function. To calculate the maximum value of the auxiliary capacitor $\text{C}_{A\_\max}$ for achieving the desired output power (P_{Desired}), (15), (16), and (18) are rearranged in terms of C_A as follows:

$$C_A \leq \frac{\frac{\Delta t_1 \cdot \Delta t_2 \cdot P_{\text{Desired}}}{4n^2}}{P_{\text{Desired}} \cdot L_{lkg} - \eta \cdot \Delta t_1 \cdot \Delta t_2 \cdot f_{\text{sw}} \cdot V_{\text{Low}} \cdot \left(V_{\text{Low}} - \frac{V_{\text{High}}}{n}\right)}.$$

$$= C_{A\_\max} \tag{22}$$

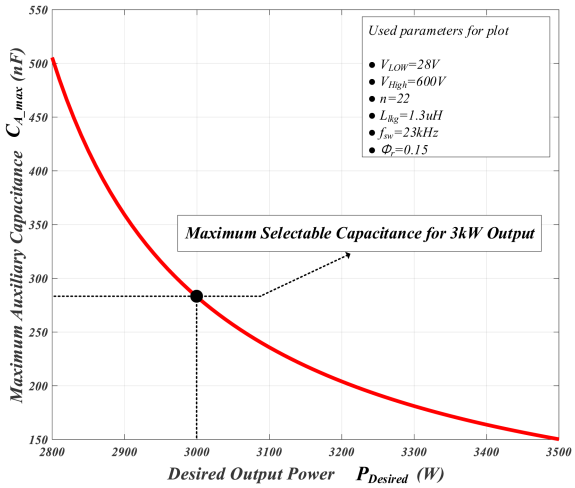


Fig. 12. Maximum auxiliary capacitance value of the proposed converter according to the desired output power.

Fig. 12 shows the maximum C_A value of the proposed converter according to P_{Desired} with a measured leakage inductance value of 1.3 uH. As shown in Fig. 12, $\text{C}_{A\_\max}$ decreases as P_{Desired} increases. Therefore, to obtain P_{Desired}, it is necessary to select a C_A value smaller than the $C_{A\_\max}$ calculated in (22). However, when the C_A value becomes too small, the current flowing through the entire circuit and voltage stress of the capacitor increase. The voltage stress of C_A is inversely proportional to the capacitor value, as shown in (16). The peak and rms values of the current flowing through the C_A can be derived from the primary current as follows:

$$I_{CA\_\text{peak}} = I_{lkg\_\text{peak}}/n \tag{23}$$

$$I_{CA\_\text{rms}} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I_{CA}(t)dt} \approx \frac{I_{CA\_\text{peak}}}{\sqrt{2}}. \tag{24}$$

These equations indicate that the voltage and current ratings of C_A increase as the output power increases. Therefore, when selecting the C_A, it should be appropriately designed based on the abovementioned considerations.

Meanwhile, to linearize V_{CA} during the powering period, the resonant period (T_{re}) of L_{lk} and C_A must be four times greater than Δt_2. If T_{re} is less than four times of Δt_2, subresonance of the V_{CA} occurs during the powering period. This generates a distortion of I_{lkg}, which significantly reduces the ZVS capability of the converter. Therefore, C_A should be selected by considering the resonant period of L_{lkg} and C_A as follows:

$$C_A \geq \frac{4 \cdot \Delta t_2^2}{\pi^2 \cdot n^2 \cdot L_{lkg}} = C_{A\_\text{MIN}}. \tag{25}$$

B. Implementation of Bidirectional Operation

Fig. 13 shows the control block diagram of the proposed converter. The control circuit consists of feedback, mode selection, control IC, power-flow selection, and protection. In this

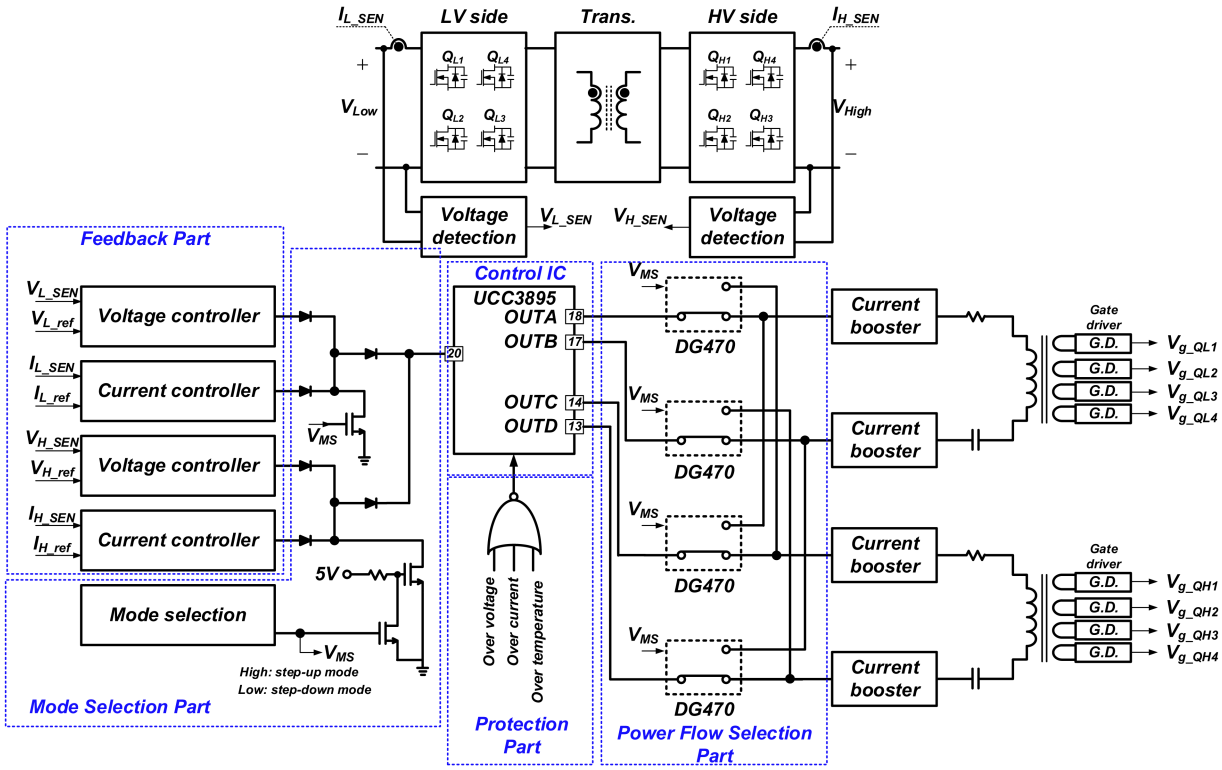


Fig. 13. Control block diagram of the proposed circuit.

controller, the input signal of the control IC can be changed using the mode (step-up or step-down) selection signal V_{MS}.

For example, when the converter is operating in step-up mode, it is necessary to employ the control signal generated from the HV side, to ensure that the V_{MS} is high to make the control signal from the LV side to 0. Consequently, the control signal on the HV side is applied to the control IC to regulate the output voltage. UCC3895 is employed as a control IC to generate phase-shifted signals. The gate signals generated from the control IC can be exchanged using DG470 switches, and the bidirectional operation can be easily implemented. By operating the DG470 using the V_{MS} without any additional signal, OUT *A* and OUT *B*, which are the leading signals compared to OUT *C* and OUT *D*, can be applied to the gate driver of the desired switches (the LV side or the HV side). Moreover, by applying OUT *C* and OUT *D* to the gate driver of the output-side switches, the output-side switches are operated as SR.

C. Gate Driving Circuit

Because the dead time required to charge and discharge the switch output capacitor differs according to the current value at the switch turn-OFF instant, the dead time should be changed depending on the load condition. Therefore, to achieve an effective ZVS of the switches under a wide load condition, a circuit that can flexibly change the dead time of the gate signal according to the load condition is required.

Fig. 14 shows the circuit diagram of the implemented gate driver, which was modified from the conventional gate driver in [36] to ensure flexible dead time. When the switch drain-source voltage reaches zero, D_3 is conducted and C_1 is rapidly charged up through R_3 and D_3. Therefore, the gate-source voltage becomes high, and the dead time is automatically adjusted.

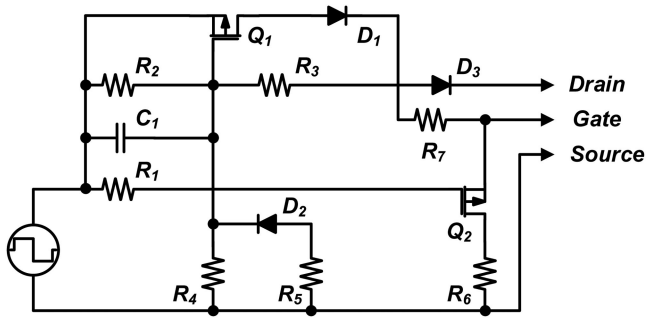


Fig. 14. Circuit diagram of the implemented gate driver.

The required dead time for ZVS, based on the current value at the switch turn-OFF instant, can be simply expressed as

$$T_{\text{dead\_requried}} = \frac{2 \cdot C_{oss} \cdot \Delta V}{I_{sw@\text{turn-off}}}. \tag{26}$$

Fig. 15 shows the required dead time for ZVS according to the current value at the switch turn-OFF instant on the LV side. As shown in Fig. 15, the maximum dead time must be greater than 250 ns to achieve ZVS under all load conditions. The maximum dead time is determined by time constant of R_4 and C_1. R_4 and C_1 values are selected as 500 Ω and 1 nF to set the maximum

TABLE I
COMPONENT LIST OF THE IMPLEMENTED GATE DRIVER

R_1, R_3	R_2	R_4	R_5	R_6, R_7	C_1	D_1	D_2	D_3	Q_1, Q_2
20Ω	10kΩ	500Ω(LV), 100Ω(HV)	30Ω	2Ω	1nF	SBE002	NSR1020MW	STTH112	PMV250EPEA

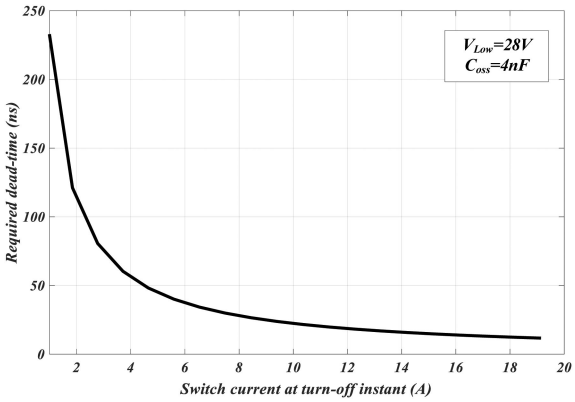


Fig. 15. Required dead time for ZVS according to the current value at switch turn-OFF instant on the LV side.

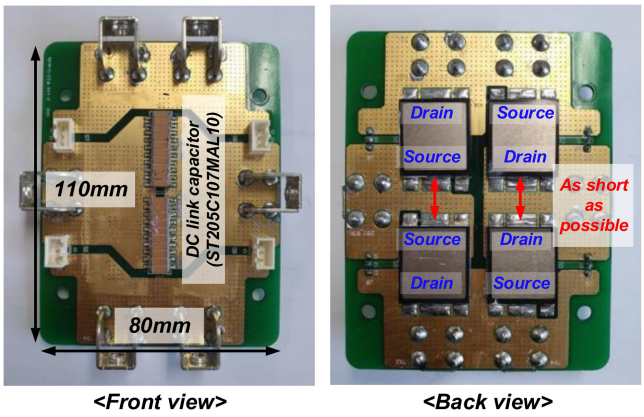


Fig. 16. Prototype photo of the inverter on the LV side.

dead time to 500 ns. The parameters of the gate driver of the HV side are also selected using the aforementioned method. Table I lists the gate driver components.

D. Inverter PCB on LV Side

Fig. 16 shows the photo of the implemented inverter on the LV side. As a large current flows through the inverter on the LV side, it is important to minimize the parasitic inductance that causes voltage ringing across the switch. In particular, the parasitic inductances between the drain nodes of the upper switches (Q_{L1}, Q_{L4}) and between the source nodes of the lower switches (Q_{L2}, Q_{L3}) directly affect the voltage ringing of the switch. Therefore, it is essential to keep the extensive current paths in the printed circuit board (PCB) pattern as short as possible. The drain terminals of the upper switches and the source terminals of the lower switches were placed opposite to each other on the PCB to minimize parasitic inductances. In addition, the inverter

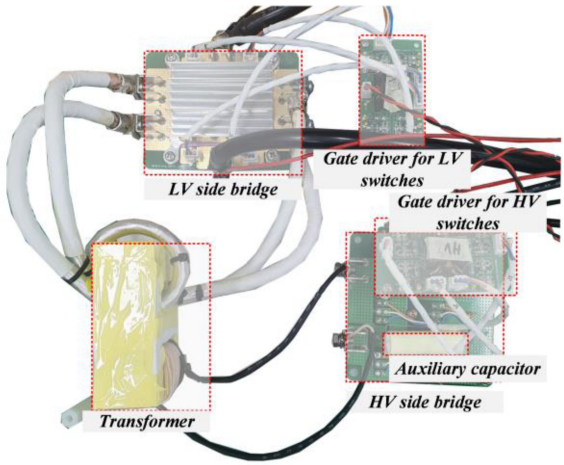


Fig. 17. Photo of the prototype converter.

TABLE II
COMPONENT LIST

Parameters	Proposed converter	Conventional LCC resonant converter
LV switches ($Q_{L1\text{-}L4}$)	MMIX1F520N075T2	
HV switches ($Q_{H1\text{-}H4}$)	C2M0025120D	
Main transformer (T)	Core : UI 80*95*30 N_p: 2T, N_s: 44T L_m: 14.7uH, L_{lkg}=1.3uH	
Auxiliary capacitor (C_A)	220nF	-
Series resonant capacitor (C_S)	-	560nF (on HV side)
Parallel resonant capacitor (C_p)	-	22nF (on the HV side, for the step-up mode) 10uF (on the LV side, for the step-down mode)
Controller	UCC3895	NCP1395

TABLE III
SIZE COMPARISON OF ADDITIONAL COMPONENTS

	Proposed converter	LCC resonant converter	
Component	C_A	Cp1 (on the LV side)	Cp2 (on the HV side)
Model	Icel film capacitor (PPA2123200)	Icel film capacitor (PHB1255100) X 4 EA	Icel film capacitor (PPA22522330) X 4 EA
Size [mm]			

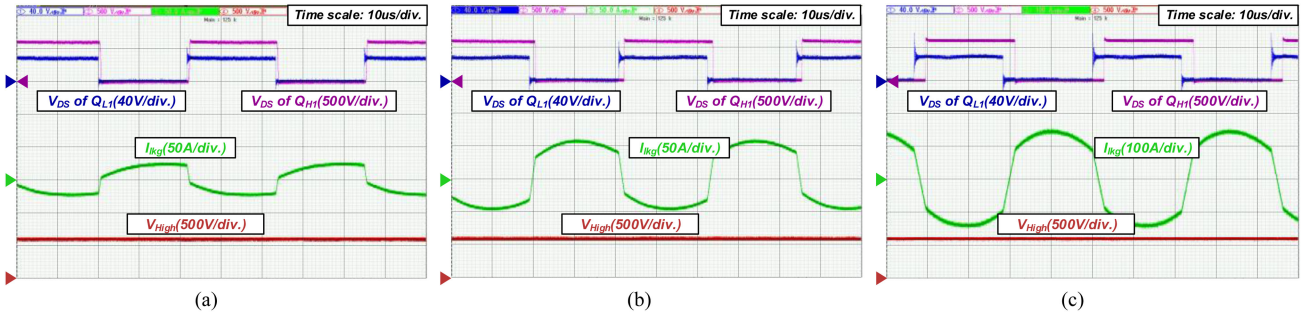


Fig. 18. Key experimental waveforms of the proposed converter during the step-up operation. (a) 20% load condition. (b) 50% load condition. (c) Full load condition.

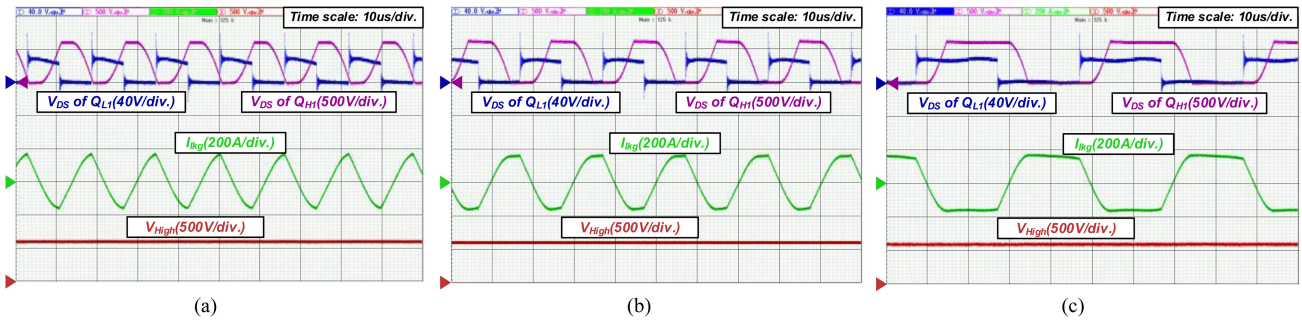


Fig. 19. Key experimental waveforms of the *LCC* resonant converter during the step-up operation. (a) 20% load condition. (b) 50% load condition. (c) Full load condition.

was implemented with MMIX1F520N075T2 switches in the SMPD-24 package, which allows for efficient heat dissipation. Furthermore, the PCB was designed to place the dc link capacitors (ST205C107MAL10, AVX) close to the switches to reduce the effects of parasitic inductance on the input line.

IV. Experimental Results

A prototype was built to verify the performance of the proposed converter, as shown in Fig. 17. The prototype converter consists of an LV side bridge, transformer, HV side bridge with an auxiliary capacitor, and gate drivers for LV and HV side switches. In addition, a conventional *LCC* resonant converter was implemented for performance comparison. The circuit parameters of them are listed in Table II. Additional components are added to the conventional DAB converter for both the proposed and *LCC* resonant converters to increase the output power. Table III shows the size comparison of the additional components of the proposed and *LCC* resonant converters. As shown in Table III, the additional component volume of the proposed converter is significantly smaller than that of the *LCC* resonant converter. As explained in Section II, the conventional DAB converter was excluded from the comparative experiments because of its limited output power. For a clear performance comparison, the switching frequency of the *LCC* resonant converter was designed to have a value similar to that of the proposed converter at the maximum output power.

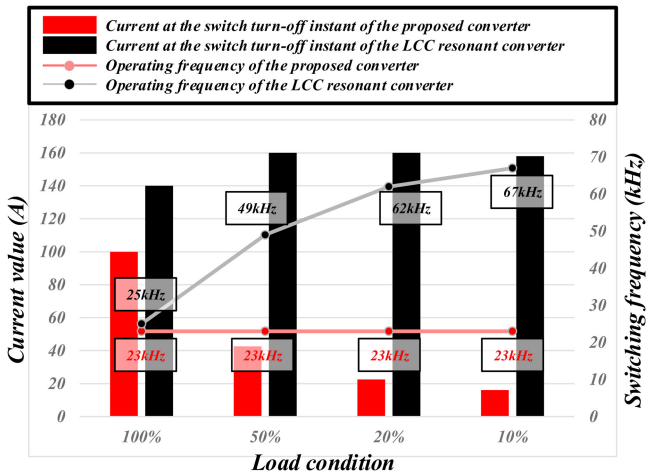
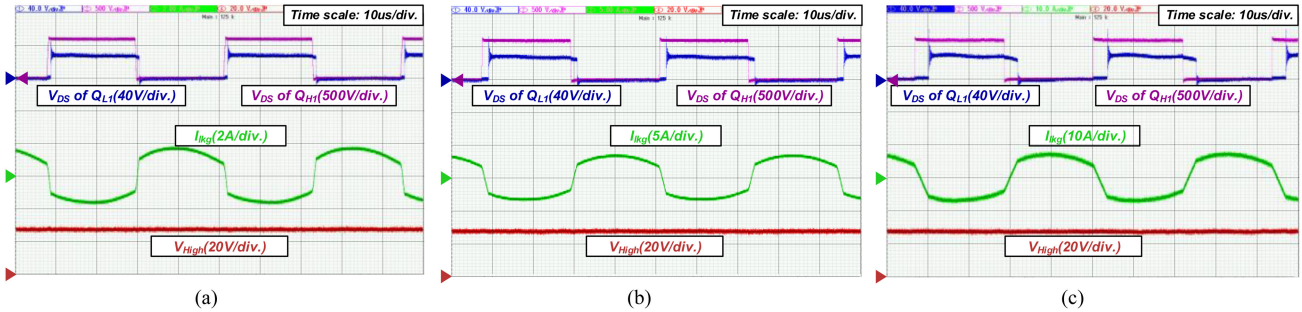


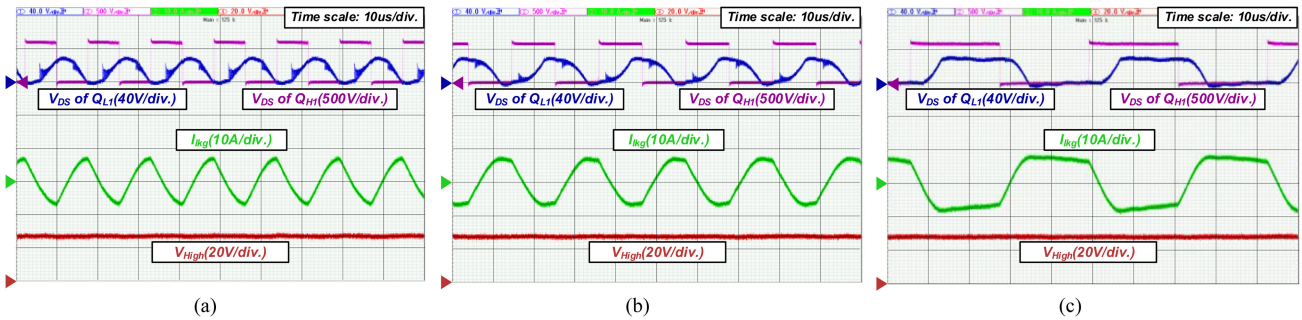
Fig. 20. Measured current value at the switch turn-OFF instant and the operating frequency depending on the load conditions of the proposed converter and the *LCC* resonant converter.

Figs. 18 and 19 demonstrate the key waveforms of the proposed and conventional *LCC* resonant converters according to the load conditions in the step-up mode. The measured waveforms in Fig. 18 follow the theoretical waveforms shown in Fig. 2. The operating frequency of the proposed converter is fixed at 23 kHz and that of the resonant converter is changed from 25–62 kHz depending on the load condition, as shown in Figs. 18 and 19. As described in Section II, the *LCC* resonant



(a) (b) (c)

Fig. 21. Key experimental waveforms of the proposed converter during the step-down operation. (a) 20% load condition. (b) 50% load condition. (c) Full load condition.



(a) (b) (c)

Fig. 22. Key experimental waveforms of the *LCC* resonant converter during the step-down operation. (a) 20% load condition. (b) 50% load condition. (c) Full load condition.

converter uses parallel resonance to generate large current and controls the output voltage via frequency modulation. Owing to the parallel resonance characteristics, the primary-side build-up current does not decrease, even if the load current decreases. As the frequency increases, the power transfer region in a period decreases, resulting in a large circulating current and power loss. However, in the proposed converter, the output voltage is controlled by phase-shifted control with a fixed frequency, which can adjust the primary-side build-up current. Therefore, if the load current decreases, the current on the primary side and circulating current decrease, reducing power losses. In addition, as shown in Fig. 18, V_{DS} is zero during the powering period, indicating that the SR switches are automatically driven.

Both converters can eliminate turn-ON switching losses caused by ZVS. However, turn-OFF switching losses cannot be ignored because of the high current on the LV side. Therefore, the switching losses are proportional to the current value at the switch turn-OFF instant and the operating frequency of the converter. Fig. 20 shows the measured current value at the switch turn-OFF instant and operating frequency depending on the load conditions of the proposed and conventional resonant converters. In the *LCC* resonant converter, the current value at the turn-OFF instant is large regardless of the load current, and the operating frequency increases as the load current decreases; thus, the switching losses are large. However, in the proposed converter, when the load current is reduced, the current value at the turn-OFF instant is reduced, and the operating frequency is fixed, which is beneficial in terms of switching losses.

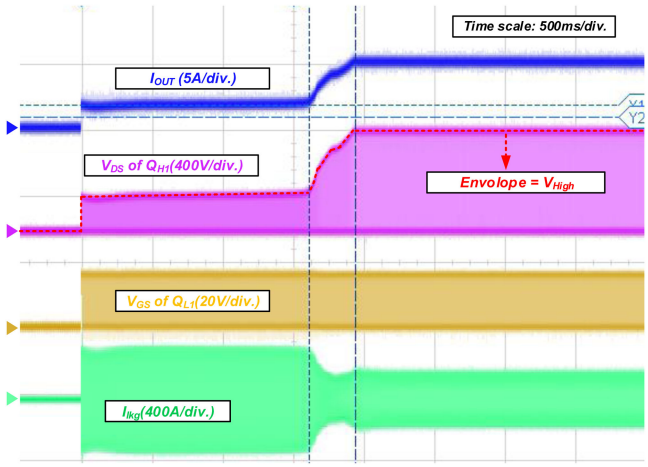


Fig. 23. Transient response of the proposed converter with rated condition in step-up mode during start-up.

Figs. 21 and 22 show the experimental waveforms during the step-down operation. The aforementioned interpretation can also be applied to this mode.

Fig. 23 shows the transient response of the proposed converter with rated conditions in step-up mode during start-up. As shown in Fig. 23, the output voltage and current are well regulated without overshoots.

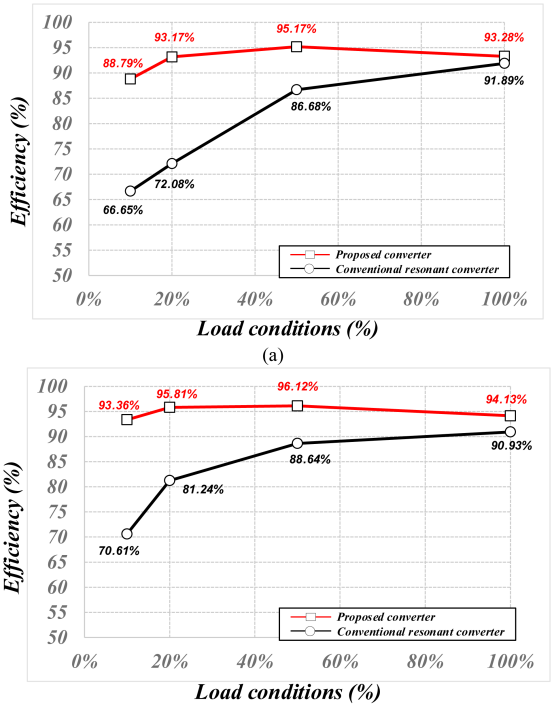


Fig. 24. Measured efficiencies under different load conditions. (a) Step-up operation. (b) Step-down operation.

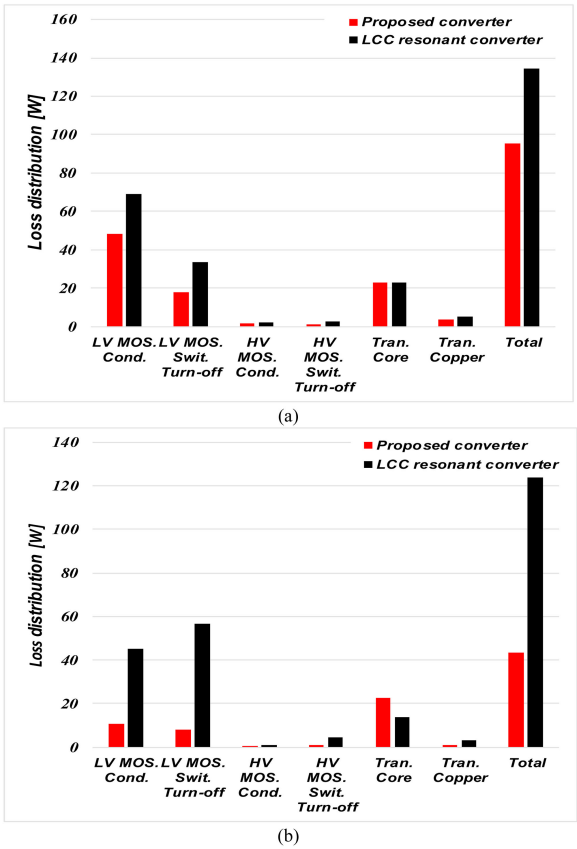


Fig. 25. Loss distribution of the proposed converter and the *LCC* resonant converter (a) 3 kW (rated condition). (b) 1.5 kW (half load condition).

Fig. 24 shows the measured efficiency of the proposed and conventional *LCC* resonant converters during step-up and step-down operations. The current is measured using digital clamp meter FLUKE-337 and current clamp FLUKE-i30 for the LV and HV sides, respectively. Voltages are measured using digital multimeter FLUKE 15B+ for both sides. As shown in Fig. 24, the proposed converter has a maximum efficiency of 95.17% in the step-up mode and 96.12% in the step-down mode. It achieves a significant improvement in efficiency because the proposed converter has smaller conduction and switching losses than those of the *LCC* resonant converter. Fig. 25 shows the loss distribution of the main components in the proposed converter and *LCC* resonant converter. As shown in Fig. 25(b), although the proposed converter has a larger core loss than the *LCC* resonant converter, the conduction and turn-OFF switching losses are significantly reduced under half-load condition.

V. Conclusion

In this article, we presented a bidirectional DAB converter that adopts a boost-up function for battery charging and discharging applications. While maintaining the good characteristics of the conventional DAB converter, it can achieve high power using a boost-up operation. In contrast to the *LCC* resonant converter, the proposed converter can achieve high efficiency by low switch turn-OFF loss and small circulating current. In addition, it can drive the SR switches easily without complex control methods. Additionally, the direction of the output power can be easily changed using a simple control circuit. The proposed converter shows a maximum efficiency of 95.17% and 96.12% during step-up and step-down operations, respectively. It was verified that the proposed converter exhibits a higher efficiency than that of the conventional *LCC* resonant converter. Therefore, the proposed circuit is suitable for battery charging and discharging systems such as ESSs, electric vehicles, and transportation.

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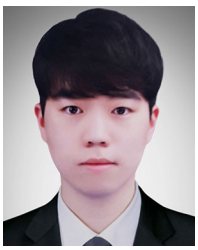

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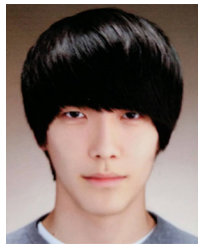

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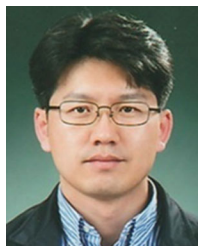

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