High-Efficiency High-Density MHz Cellular DC/DC Converter for On-Board Charger

Gao Fan, Xinke Wu, *Member, IEEE*, Tianji Liu, and Yuhao Xu

***Abstract*—In this article, a high efficiency and high power density Regulated dc Transformer (RDCX) is proposed for on-board charger (OBC). In this circuit, high input and output voltages are undertaken by series connected low-voltage devices. Owing to the low new figure of merit (NFoM, $R_{\mathrm{dson}} \times C_{\mathrm{oss}}$)(Il-Jung et al., 1995), (Wu and Shi, 2020) characteristic of low-voltage devices, the conduction loss of switches can be reduced. Mathematical modeling and verification are also carried out. In addition, by applying cascaded buck as the regulation part of RDCX, the volt-second of buck inductor can be reduced compared with the traditional two-level buck circuit. As a result, the size of the inductor can be reduced. Furthermore, since all dc buses of the cascaded buck converter are from the rectifiers whose windings are coupled to the same transformer, those bus voltages can be naturally balanced. A 2.3 kW prototype based on 60V device with 388–412 V input and 250–450 V output voltage range is built up to verify the analysis, achieving 98% peak efficiency and 910 W/in^3 power density.**

***Index Terms*—MHz, multilevel, natural voltage balance, on-board charger (OBC), partial power processing, regulated dc transformer (RDCX).**

I. Introduction

FOR the booming electric vehicles industries, on-board charger (OBC) plays a significant role to connect the electric vehicle battery with ac grid. It usually needs to have the characteristics of high efficiency and high density because of the limited space and heat dissipation capacity in electric vehicles. Two-stage architecture is generally adopted in OBC application [3]–[7]. The first stage ac/dc is responsible for power factor correction, and the second stage dc/dc realizes galvanic isolation and wide voltage regulation for battery load. For the dc/dc stage, the dual active bridge is widely used for its simpleness and bidirectional power processing capability. Through phase shift between the primary and secondary full-bridges, which is named single-phase-shift (SPS) control, it can control the direction and magnitude of the energy flow, and realize zero voltage switching (ZVS) [8]. However, ZVS can only be achieved under heavy load in SPS, and reactive power flowing in the circuit brings large circulating current loss. Moreover, the switches are turned OFF at the peak current under SPS control, which would bring large turn-OFF loss at high frequency operation. In order to solve the above problems, some other control variables are introduced, such as phase shift between the two the gate signals of the diagonal switches in the primary or secondary full bridge, and duty cycle of each side. Nevertheless, multiple control variables complicate the circuit control [9]–[14].

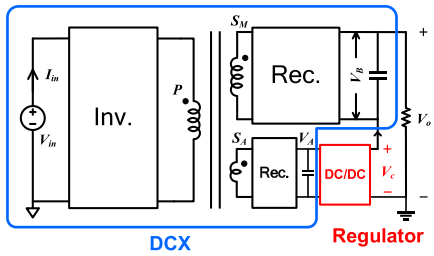

Fig. 1. RDCX structure used in [15].

Another solution for the dc/dc stage is resonant isolated converter, such as *LLC* and *CLLC*, which can achieve both ZVS in primary switches and ZCS in synchronous rectifiers (SRs) within a wide load range, making it suitable for high frequency operation. In these topologies, output voltage regulation is normally achieved by frequency-modulation method [3], [16]–[18]. However, the converter efficiency decreases when its switching frequency deviates from the resonant frequency for voltage regulation, as transformer performance degrades. This problem becomes more severe in dc/dc for OBC, as a wide frequency range is needed for wide range voltage regulation. Thus, many methods that keep the resonant converter working at its optimal operating frequency have been proposed. Two-stage dc/dc structure is used in [19]–[24], in which voltage regulation and isolation functions are achieved by two converters respectively, thus both stages can be optimized more easily. However, as all of the output power is processed by both stages, the total system efficiency is sacrificed. In order to reduce the power flow through the regulator stage, quasi-single-stage architecture is proposed in [15] and [25]–[27]. Since this type of circuit is typically constructed by combining a dc transformer (DCX) and a regulator, which is normally a pulsewidth modulation (PWM) converter, it is also called regulated dc transformer (RDCX). Fig. 1 shows the RDCX topology used in [15], the output of

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regulator is in series with the main secondary rectifier output of DCX to achieve output voltage regulation. It can be observed that only part of the output power flows through the regulator stage, thus it is expected to be more efficient compared with the two-stage architecture. However, in OBC, due to the large volt-second caused by wide output voltage range, a large filter inductor is often needed in regulation circuit, which decreases circuit power density. Topologies like cascaded H-Bridge and flying-capacitor converter can achieve low volt-second through multilevel operation and thus can easily achieve very high density [28], [29], and high efficiency at the same time as low voltage devices with low FoM characteristic can be used. But voltage balance control is need in multilevel converter, which make the system more complicated.

Same as the regulator, DCX can also benefit from low voltage device. In [2], an input series output parallel (ISOP) 384/12V *LLC* DCX with low voltage device is reported, which shows more than 800 W/in^3 density and 98.3% peak efficiency. Wu and Shi [2] revealed that in *LLC* DCX, the primary device minimum conduction loss is proportional to its new figure of merit (NFoM), thus low voltage device can achieve lower conduction loss than high voltage device for its lower NFoM value. However, it only analyzed the device condition loss and design methodology of primary side. In RDCX structure, a three port DCX is often needed, so a model extension is needed for multiport DCX case.

In this article, a low voltage device based RDCX topology is proposed. As for the DCX part, device conduction loss model is derived for multiple *CLLC* DCX, and it shows that the DCX device minimum conduction loss is proportion to its device NFoM. On the strength of the conduction loss model, a multiport *CLLC* DCX based on low-voltage cell circuit is proposed. Thanks to the low-voltage device in the cell circuit with low NFoM value, the designed DCX can greatly reduce the conduction loss of the devices compared with the traditional DCX using high-voltage devices. A transformer winding is designed in every DCX cell circuits, and by coupling it to a same transformer, voltage balance between them can be naturally achieved by magnetic coupling. The design methodology for the proposed circuit is also given. For the voltage regulation part, a cascaded buck circuit is proposed. Through its multilevel operation, the volt-second of the buck filter inductor is reduced, thereby small buck inductor can be used, which benefits converter power density. What's more, as the buses of bridges of cascaded buck circuit are paralleled with different output of DCX rectifier cell circuits, the bus voltages of these buck bridges are naturally balanced by magnetic coupling of DCX transformer, which simplifies the control strategy and the sampling system. Furthermore, a balancing winding is designed in every transformer core for voltage balancing between different transformer cores in case there are multiple cores used in the proposed RDCX circuit for less printed circuit board (PCB) layers. Finally, a 2.3 kW prototype with ~910 W/in^3 power density and over 98% efficiency in full load is presented to verify the circuit working principle and design methodology.

The rest of this article is organized as follows: In Section II, the device conduction loss model of three port *CLLC* DCX is derived, in which the parasitic output capacitances of all ports are considered. Details of RDCX circuit design considerations including device voltage balance, turn ratio, device number, regulator structure and transformer are analyzed in Section III. In Section IV, a 2.3 kW prototype with ~910 W/in^3 power density and over 98% efficiency in full load is presented, along with its working waveforms in steady-states and during dynamic voltage regulation. Section V concludes this article.

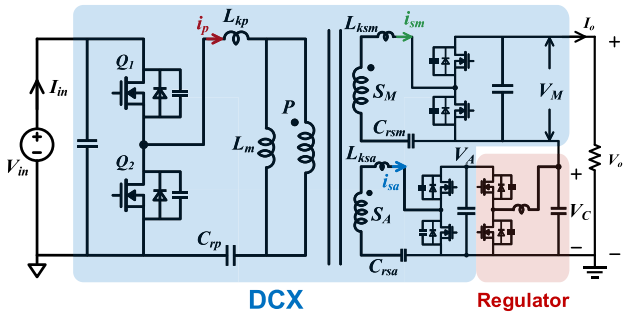

Fig. 2. RDCX topology used in this article.

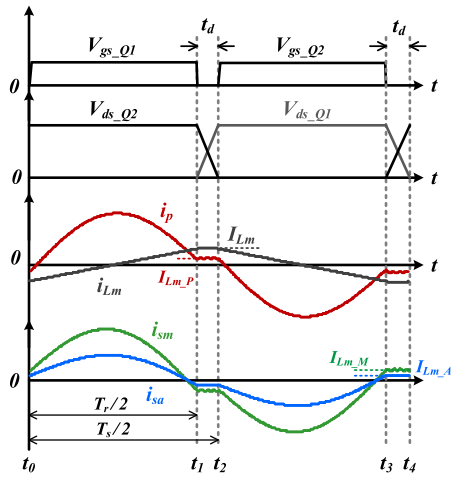

Fig. 3. Key Waveforms for three-port DCX in Fig. 2.

II. Conduction Loss Derivation of Switches in Three Port SRC DCX

Fig. 2 shows the circuit schematic of a three port DCX based RDCX converter. Three port *CLLC* is used here for its soft-switching and bidirectional operation capability [30], and a buck regulator is used to regulate the output voltage. In Fig. 2, L_{kp}, L_{ksm}, and L_{ksa} are the leakage inductance of primary side winding P, main secondary side winding S_M and auxiliary secondary winding S_A respectively, and C_{rp}, C_{rsm}, and C_{rsa} are the resonant capacitors corresponding to them one-to-one, with the relationship of $L_{kp} \cdot C_{rp} = L_{ksm} \cdot C_{rsm} = L_{ksa} \cdot C_{rsa}$; L_m is the transformer magnetizing inductance. Here main is defined as the rectifier whose processed power is output directly to the load. As for auxiliary secondary side, its output power would further be processed by a regulator. V_M and V_A are their corresponding output voltage. Fig. 3 gives the key current and

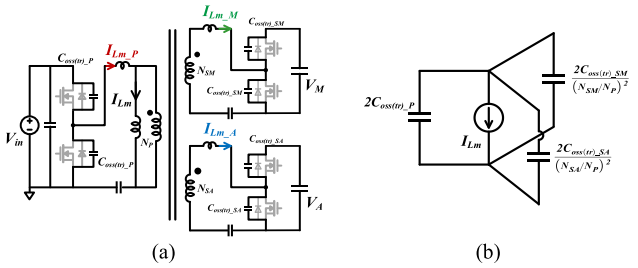

Fig. 4. ZVS transition mode of circuit in Fig. 2. (a) Equivalent circuit during dead time. (b) its simplified circuit.

voltage waveforms of the three port *CLLC*. Some key variables are defined in Fig. 3, where t_0 is the beginning of a resonant period, t_d is the dead time for ZVS transition, T_r is the resonant period and T_s is the switching period; i_p, i_{sm}, and i_{sa} are the resonant current of primary, main secondary and auxiliary side respectively and i_{Lm} is the magnetizing current. V_{ds_Q1} and Vds_Q2 are the drain to source voltages of switch Q_1 and Q_2, respectively, and V_{gs_Q1} and V_{gs_Q2} are their corresponding driving voltages.

With the parameter definition in Fig. 3, the conduction loss of primary MOSFETs in Fig. 2 can be calculated as

$$P_{\mathrm{Con\_}P} = \frac{\int_{t_0}^{t_0+T_r/2} (i_p)^2 \cdot dt}{T_S/2} \cdot R_{\mathrm{dson\_}P} \tag{1}$$

where R_{dson_P} stands for the ON-resistance of primary switches. During $t_0 \sim t_1$, i_p can be expressed as [31]

$$i_p(t) = A_r \sin\left(\frac{2\pi}{T_r}t + \theta_r\right) + A_m \sin\left(\frac{2\pi}{T_m}t + \theta_m\right). \tag{2}$$

where T_m is the resonant period between L_m and C_{rp}, C_{rsm}, C_{rsa} and A_r, θ_r, A_m, and θ_m are terms decided by the load conditions. Considering that L_m is much larger than leakage inductance in DCX in most cases, the resonant frequency between resonant capacitors (e.t. C_{rp}, C_{rsm}, C_{rsa}) and L_m is much larger than the converter conducting period T_r, so i_{Lm} can be seemed as a triangle current during this period for simplicity. Equation (2) can then be simplified as

$$i_p(t) = \mathrm{I_p} \sin\left(\frac{2\pi}{T_r}t\right) + \left(\frac{4I_{Lm\_P}}{T_r}t - I_{Lm\_P}\right). \tag{3}$$

In (3), I_p is the magnitude of $i_p(t)$, and I_{Lm_P} stands for the current to charge and discharge the equivalent output capacitor of the primary switches ($C_{\mathrm{oss}(tr)\_P}$) during dead time, which is utilized to achieve their ZVS. Fig. 4 shows the equivalent circuit of DCX circuit in Fig. 2 during dead time, where the magnetizing current i_{Lm} works as a constant current source to charge the output capacitance of switches in each port. In order to guarantee the ZVS operating of Q_1 and Q_2 in transition time, the needed I_{Lm_P} can be calculated as

$$I_{Lm\_P} = \frac{2\mathrm{C_{oss(tr)\_P}} \cdot V_{in}}{t_d}. \tag{4}$$

Considering the power balance in transformer primary side, the relationship between total output power P_o and i_p can be expressed as (5), in which the circuit loss is ignored

$$\int_{t_0}^{t_0+T_r/2} \frac{V_{\mathrm{in}}}{2} \cdot i_p(t) \cdot dt \approx P_o \cdot \frac{T_S}{2}. \tag{5}$$

Substituting (3) into (5), I_p can be derived as

$$I_P = \frac{P_o}{V_{in}} \cdot \frac{\pi T_S}{T_r}. \tag{6}$$

By substituting (3), (4), (6) into (1), the conduction loss of primary switches $P_{\mathrm{Con\_}P}$ can be gotten

$$P_{\mathrm{Con\_P}} = \left(\frac{P_o^2\pi^2 T_S}{2V_{in}^2 T_r} + \frac{4T_r V_{in}^2 C_{\mathrm{oss}(tr)\_P}^2}{3T_S t_d^2}\right) \cdot R_{\mathrm{dson\_P}}. \tag{7}$$

Considering the product of the MOSFET intrinsic parasitic output capacitance, $C_{\mathrm{oss}\,(tr)}$, and its on resistance, R_{dson} is almost a constant, which namely is NFoM $= R_{\mathrm{dson}} \cdot C_{\mathrm{oss}\,(tr)}$ [1], [2], the primary conduction loss (7) can be rewritten as:

$$P_{\mathrm{Con\_P}} \approx \frac{P_o^2\pi^2 T_S}{2V_{\mathrm{in}}^2 T_r} R_{\mathrm{dson\_P}} + \frac{4T_r V_{\mathrm{in}}^2 \mathrm{NFoM_P^2}}{3T_S t_d^2 \cdot R_{\mathrm{dson\_P}}} \tag{8}$$

where NFoM$_P$ stands for the NFoM value of primary switches, that is to say

$$\mathrm{NFoM_P} = \mathrm{C_{oss(tr)\_P}} \cdot \mathrm{R_{dson\_P}}. \tag{9}$$

Equation (8) shows that the primary MOS conduction loss is a hook function about $R_{\mathrm{dson\_}P}$ under a given circuit specification, which means there is a minimum loss point as $R_{\mathrm{dson\_}p}$ varies. This can be understood from (3), (4), and (9), as $R_{\mathrm{dson\_}p}$ increases, I_{Lm_P} decreases, thus the RMS value of i_p decreases, which benefits the conduction loss reduction. However, the conduction loss would sacrifice from the on resistance increasement at the same time. As a result, there would be a minimum conduction loss point when $R_{\mathrm{dson\_}p}$ changes. As derived in Appendix, the minimum conduction loss is

$$\min\left(P_{\mathrm{Con\_P}}\right) = 2\pi \cdot \sqrt{\frac{2}{3}} \cdot \frac{P_o \cdot \mathrm{NFoM_P}}{t_d}. \tag{10}$$

Same as primary, the conduction loss of main secondary and auxiliary secondary switches, namely $P_{\mathrm{Con\_}MS}$ and $P_{\mathrm{Con\_}AS}$ can be derived respectively as follows:

$$P_{\mathrm{Con\_MS}} \approx \frac{P_M^2\pi^2 T_S}{2V_M^2 T_r} R_{\mathrm{dson\_SM}} + \frac{4T_r V_M^2 \mathrm{NFoM_{SM}^2}}{3T_S t_d^2 \cdot R_{\mathrm{dson\_SM}}} \tag{11}$$

$$P_{\mathrm{Con\_AS}} \approx \frac{P_A^2\pi^2 T_S}{2V_A^2 T_r} R_{\mathrm{dson\_SA}} + \frac{4T_r V_A^2 \mathrm{NFoM_{SA}^2}}{3T_S t_d^2 \cdot R_{\mathrm{dson\_SA}}} \tag{12}$$

where subscripts MS and AS represent the physical quantities related to the main secondary side and auxiliary secondary side respectively. P_M is the power delivered by the main secondary circuit and P_A represents processed power of auxiliary secondary rectifier. It can be observed that (11) and (12) are both hook function about their port switch on resistance, same as (8). This is because the tradeoff between the port switch R_{dson} and the magnetizing current for its ZVS, which is proportion to its $C_{\mathrm{oss}\,(tr)}$, all exits in each port. The minimum loss of each port

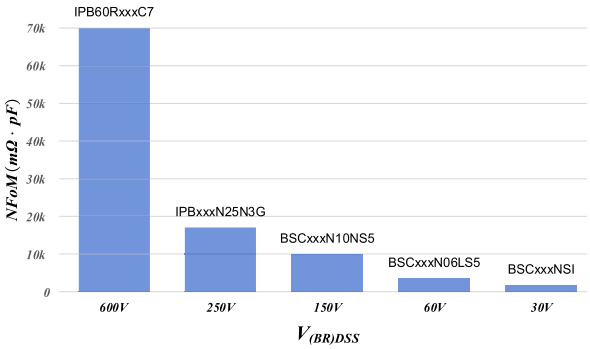

Fig. 5. NFoM of different voltage level device (Infineon).

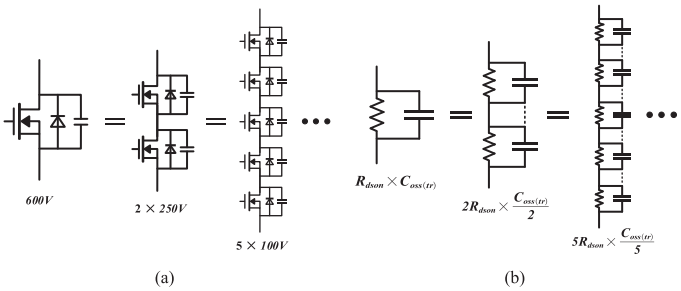

Fig. 6. Series low voltage device to undertake high voltage stress. (a) Device in series diagram. (b) Equivalent circuit.

when their R_{dson} varies can be derived respectively as follows:

$$\min\left(P_{\mathrm{Con\_MS}}\right) = 2\pi \cdot \sqrt{\frac{2}{3}} \cdot \frac{P_{\mathrm{M}} \cdot \mathrm{NFoM_{SM}}}{t_d} \tag{13}$$

$$\min\left(P_{\mathrm{Con\_AS}}\right) = 2\pi \cdot \sqrt{\frac{2}{3}} \cdot \frac{P_{\mathrm{A}} \cdot \mathrm{NFoM_{SA}}}{t_d}. \tag{14}$$

Observing (10), (13), and (14), it can be found that when the circuit specifications are determined, the minimum conduction loss of each port in Fig. 2 is proportional to the NFoM of their corresponding device. So, we can improve the efficiency of the DCX part by choosing a device with NFoM value as low as possible. Ref.[2] pointed out that low-voltage Si devices have much lower NFoM than high-voltage Si devices, as shown in Fig. 5 [32], where $V_{(BR)\mathrm{DSS}}$ signifies the device breakdown voltage. Moreover, the equivalent high-voltage device obtained by connecting low-voltage Si devices in series has the same NFoM as a single low-voltage Si device, as shown in Fig. 6, that is to say

$$\mathrm{NFoM} = \mathrm{n} \cdot \mathrm{R_{dson}} \times \frac{\mathrm{C_{oss(tr)}}}{\mathrm{n}}. \tag{15}$$

So, series low voltage device can be used to substitute the single high voltage MOS in DCX in Fig. 2 to get lower conduction loss. From Fig. 5, when the device $V_{(\mathrm{BR})\mathrm{DSS}}$ is lower than 60V, NFoM reduce little with the decrease of the single device's $V_{(\mathrm{BR})\mathrm{DSS},}$ so as its contribution to conduction loss reduction; furthermore, compared to 60 V device, using 30 V devices in series will double the device quantity needed, which means higher costs and complexity. Finally, based on the analysis above, 60 V device is chosen to build the DCX circuit in this article.

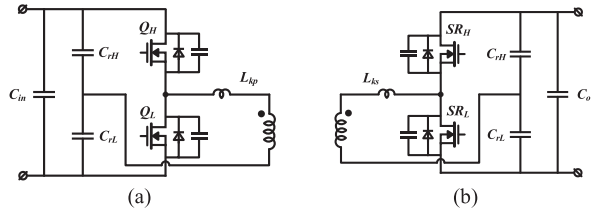

Fig. 7. DCX low voltage cell circuit. (a) DCX inverter cell. (b) DCX rectifier cell.

III. Design Considerations for Low FoM Device-Based RDCX

Based on the analysis above, low voltage device in series is used to substitute the high voltage device used in Fig. 2 to reduce DCX conduction loss. However, sampling and control is needed to ensure the voltage balance between devices in series for circuit reliability. In order to simplify circuit control, series-connected cell circuits instead of series-connected devices are used in this article. Fig. 7 shows the basic cell circuit used in inverter side and rectifier side, and the switches used in them are all rated at 60 V. L_{kp} and L_{ks} stands for the leakage inductance of inverter cell and rectifier cell, respectively. By coupling the transformer windings of all cell circuits to a same core, all cell circuits could be regarded as paralleled in ac side as the all their windings are coupled to a same flux, which means there is a current circulation path between those cell circuits. This helps them to achieve voltage balance. For example, if the bus voltage of one of the cell circuits gets higher than others, part of the bus capacitor charge of this cell would flows to the bus capacitors of other cells via transformer, thus the bus voltages could be balanced. Thus, the voltage balance between cell devices can be achieved naturally by the magnetic coupling.

The number of DCX basic cell in series used in each port is related to the total voltage stress of each port and the transformer turn ratio. The turn ratio could be designed based on the input and output voltage range and the voltage regulation principle of RDCX topology in Fig. 2 [33]. The input voltage range of dc/dc stage is around 388–412 V as it is normally from the output of PFC; the output voltage is around 250–450V for a battery load. The detailed circuit design based on low voltage device will be discussed in this part.

A. Turn Ratio Design

In order to get higher efficiency, the designed turn ratio should make as much energy as possible flowing through the main secondary port, as this part of power would only be processed by the DCX stage. To simplify the power distribution analysis,

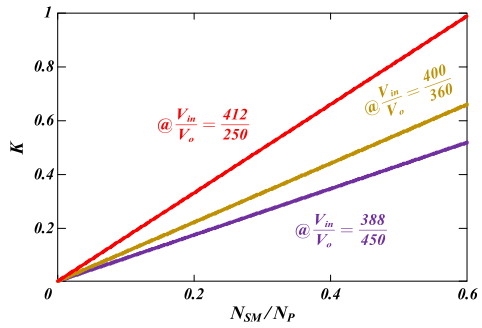

Fig. 8. K versus $N_{\rm SM}$ / N_P with different $V_{\rm in}$ / V_o.

here the single-stage energy flow ratio K is defined

$$K=\frac{P_M}{P_o}=\frac{V_M\cdot I_o}{V_o\cdot I_o}=\frac{N_{\rm SM}}{N_P}\cdot\frac{V_{\rm in}}{V_o} \tag{16}$$

where P_M represents the output power of the main secondary side in Fig. 2; P_o represents the total output power of RDCX, and K stands for the proportion of P_M in P_o, which means that the larger the value of K, the more energy flows through only DCX stage at a certain output power, and the less energy flows through both DCX and regulator stages. Equation (16) shows that K is the product of the main secondary and primary winding turns ratio $N_{\rm SM}$ / N_P and the input voltage and output voltage ratio $V_{\rm in}$ /V_o. Considering the RDCX input and output voltage specifications, the range of $V_{\rm in}$ /V_o can be obtained as

$$\frac{250}{412}\le\frac{V_{\rm in}}{V_o}\le\frac{450}{388}. \tag{17}$$

Since the RDCX output voltage V_o, which is the sum of V_M and V_C, needs be adjusted to a minimum of 250 V, and the regulator output voltage $V_C\ge 0$ in Fig. 2, V_M should be less than 250 V. Then, we can get the range of $N_{\rm SM}$ / N_P

$$0\le\frac{N_{\rm SM}}{N_P}=\frac{V_M}{V_{\rm in}}\le\frac{250}{412}\approx 0.6. \tag{18}$$

Based on (16), the figure of K varies with $N_{\rm SM}$ / N_P under different $V_{\rm in}$ / V_o can be plotted in Fig. 8.

It can be seen that K increases with the increase of $N_{\rm SM}$ / N_P under any $V_{\rm in}$ / V_o. Therefore, $N_{\rm SM}$ / $N_P=0.6$, the maximum value determined by (18) is chosen here to get maximum K value.

The turn ratio of auxiliary secondary to primary winding N_{SA} / N_P is related to V_A and $V_{\rm in}$. Considering the relationship between input and output voltage of buck regulator, the range of N_{SA} / N_P can be obtained as

$$\frac{N_{SA}}{N_P}=\frac{V_A}{V_{\rm in}}\ge\frac{\max(V_C)}{V_{\rm in}} \tag{19}$$

where max(V_C) means the maximum value of V_C when V_o varies. Considering the turn ratio N_{SM} / N_P designed above, V_C can be obtained as follows:

$$V_C=V_o-V_M=V_o-0.6V_{\rm in}. \tag{20}$$

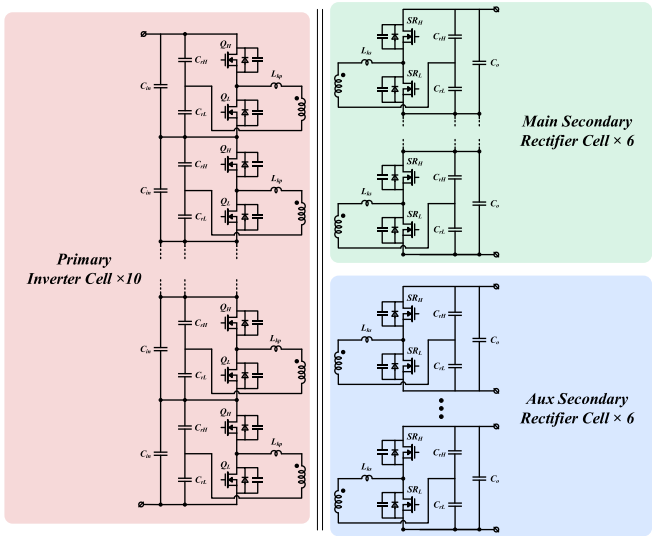

Fig. 9. DCX based on cell circuit with low NFoM device.

TABLE I
KEY PARAMETERS OF THE PROTOTYPE

Description	Parameters	Description	Parameters
P_{o_max}	2300 W	Core Material	DMR51W
V_{in}	388–412 V	BUCK MOS/SR	BSZ037N06LS5
$V_{battery}$	250–450 V	DCX MOS/SR	BSZ037N06LS5
L_m	1.6 uH	DCX Cell C_{in}	3.3 uF/100 V
L_{kp} and L_{ks}	~ 3 nH	DCX Cell C_o	3.3 uF/100 V
C_{rH} and C_{rL}	4.9 uF	BUCK C_C	2.2 uF/630 V
P:S_M:S_A	10:6:6	BUCK inductor	XGL5020-332×2
$f_{s\_\rm DCX}$	1 MHz	Controller	TMS320F280049
$f_{s\_\rm BUCK}$	120 kHz		

By substituting (20) into (19), the relationship between N_{SA} / N_P and $V_{\rm in}$ and V_o can be obtained

$$\frac{N_{SA}}{N_P}\ge\frac{\max(V_o-0.6V_{\rm in})}{V_{\rm in}}=\frac{450}{V_{\rm in}}-0.6. \tag{21}$$

As (21) should be satisfied in the whole range of $V_{\rm in}$, the minimum value of N_{SA} / N_P can be obtained at $V_{\rm in}=388$ V, which means that

$$\frac{N_{SA}}{N_P}\ge\frac{450}{388}-0.6\approx 0.6. \tag{22}$$

Here, the minimum value of N_{SA} / N_P is chosen to get higher efficiency for the buck regulator, as its output voltage range and current specifications are already determined by the circuit specification. Then, we can get the total turn ratio as

$$N_P{:}N_{SM}{:}N_{SA}=5:3:3. \tag{23}$$

B. DCX Design Based on Low NFoM Device

As the windings of cell circuits in Fig. 7 are all coupled on same magnetic core, and same voltage level device are chosen for all cells, the winding turns are same for all cell circuit. For design simplicity, single turn of winding is used for all cells. Therefore,

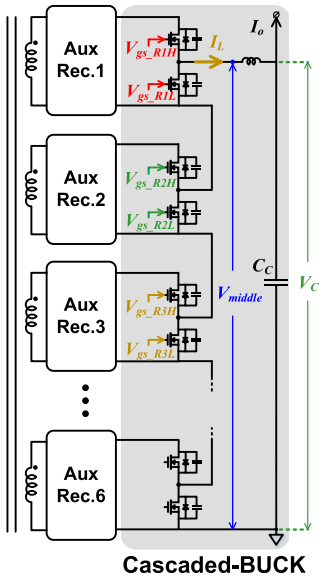

Fig. 10. Cascaded buck converter.

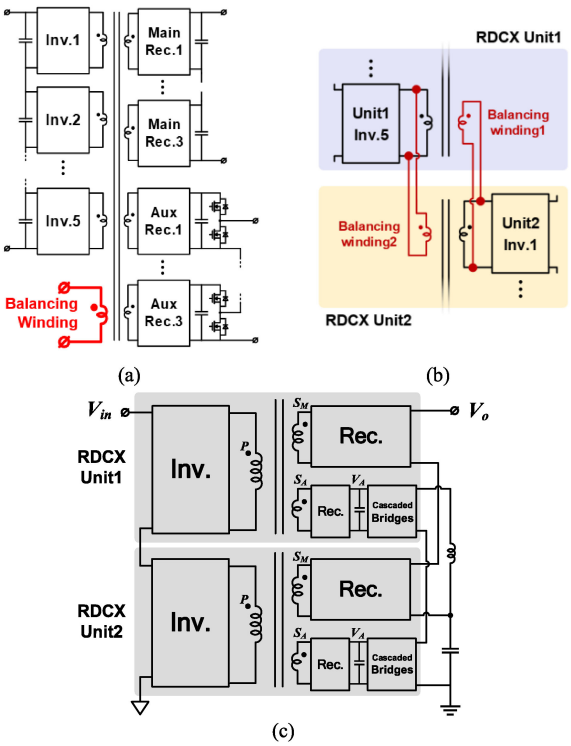

Fig. 11. RDCX Unit Circuit. (a) Circuit diagram. (b) Voltage balance connection. (c) Connection between units.

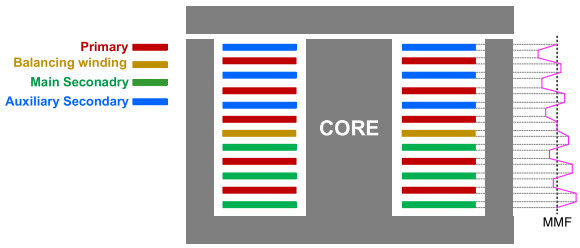

Fig. 12. PCB winding arrangement of single transformer.

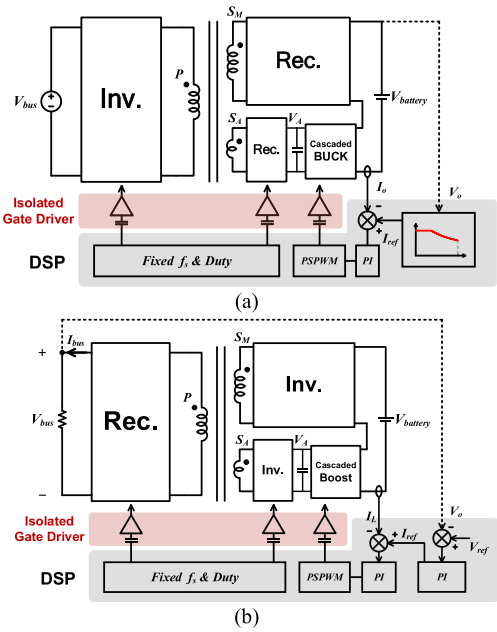

Fig. 13. Simplified system schematics of the proposed RDCX converter during: (a) Charging mode. (b) Discharging mode.

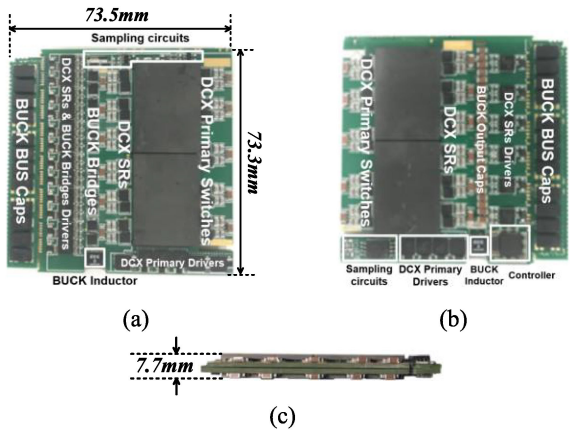

Fig. 14. Photos of the prototype. (a) Top view. (b) Bottom view. (c) Side view.

for primary side, the relationship between cell number $N_{\text{cell\_}p}$ and total winding turns N_P can be derived

$$N_P = N_{\text{cell\_p}}. \tag{24}$$

In consideration of the total voltage stress of primary side cells in series, the cell number should satisfy that

$$N_{\text{cell\_p}} \cdot 60\text{V} \geq 412V. \tag{25}$$

Therefore, $N_{\text{cell\_}p}$ should be greater than 7. With a view to the turn ratio designed in (23), the primary turn number should be a multiple of 5, like 5, 10, 15, 20… and so on. $N_{\text{cell\_}p} = 10$ is chosen here for simplicity. Then, the number of main and auxiliary secondary cells, namely $N_{\text{cell\_SM}}$ and $N_{\text{cell\_AS}}$, respectively, can be deduced from (23), that is to say, $N_{\text{cell\_SM}} = 6$ and $N_{\text{cell\_AS}} = 6$. Then, the 60

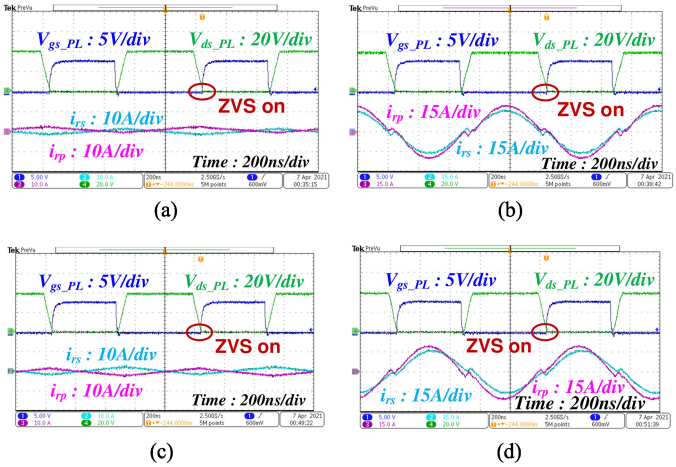

Fig. 15. Key waveforms of DCX cell circuits under: (a) null load during charging mode; (b) full load during charging mode; (c) null load during discharging mode; and (d) full load during discharging mode condition.

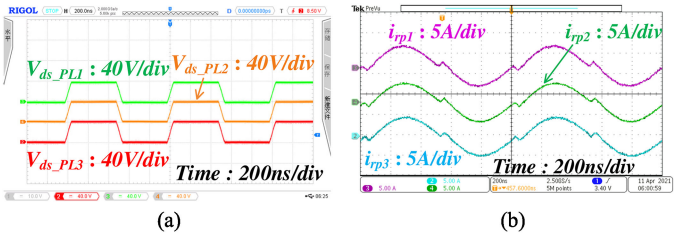

Fig. 16. Voltage and current sharing among three primary cells. (a) V_{ds} waveform of low-side switches. (b) Resonant current waveform.

V device based multiport DCX topology can be depicted in Fig. 9.

C. Regulator Design Based on Low NFoM Device

For RDCX structure in Fig. 2, a regulator is in series with the output of main secondary rectifier to realize output voltage regulation. If the traditional two-level buck circuit is used, a large inductor may be needed due to the large volt-second caused by the high input voltage and wide output voltage regulating range, which is not good for the circuit power density. By applying multilevel circuit, the volt-second can be largely reduced while maintaining same switching frequency. What's more, low voltage device can be adopted, which means the circuit can benefits from the device low FoM characteristic and so can achieve higher efficiency and power density [29]. Considering that the DCX outputs of auxiliary secondary low-voltage cell circuits in Fig. 9 can be isolated from each other, and their bus voltages are naturally balanced since the windings of every auxiliary secondary cell rectifier are coupled to same magnetic core, the cascaded buck circuit shown in Fig. 10 is chosen as the regulator in this article. The chopper circuit of this cascaded buck is formed by cascading 6 half bridges, so multilevel operation can be achieved by carrier phase shift and common duty control. The buses of these half bridges are connected with the outputs

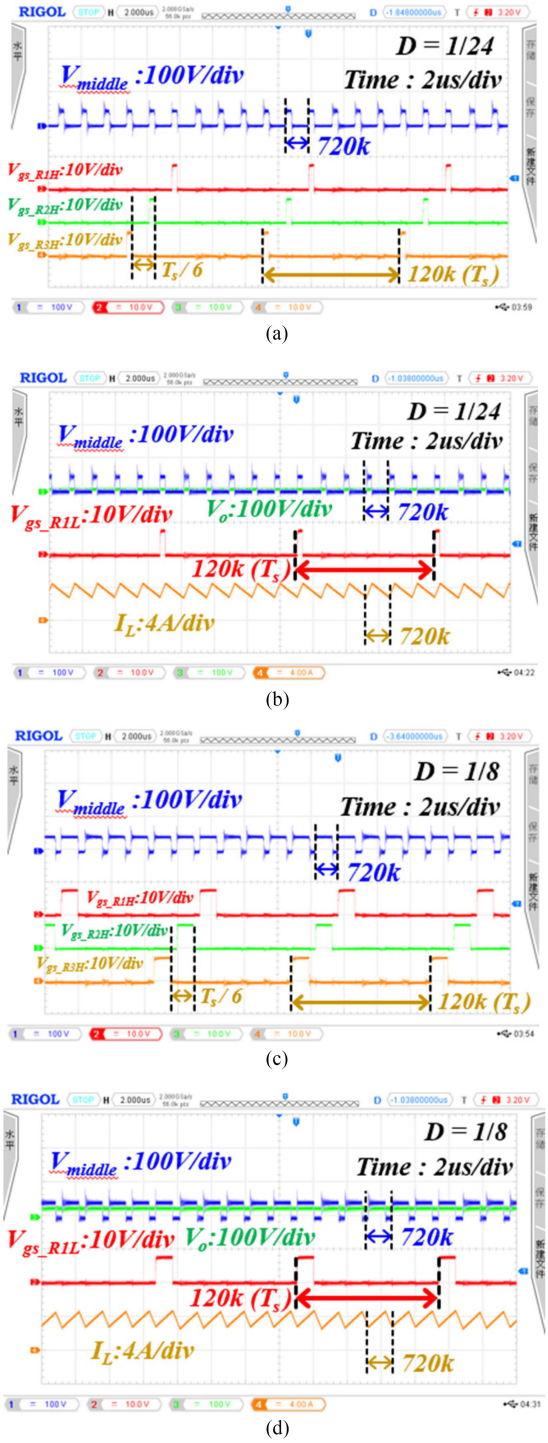

Fig. 17. Key waveforms of regulator when RDCX working under charging mode. (a) Low side switch gate voltages @D = 1/24. (b)Inductor current waveform @D = 1/24. (c) Low side switch gate voltage @D = 1/8. (d) Inductor current waveform @D = 1/8.

of six auxiliary cell rectifiers in Fig. 9 in one-to-one correspondence, as shown in Fig. 10. The "Aux Rec." in Fig. 10 denotes the auxiliary rectifier, whose detailed diagram is shown in Fig. 7(b).

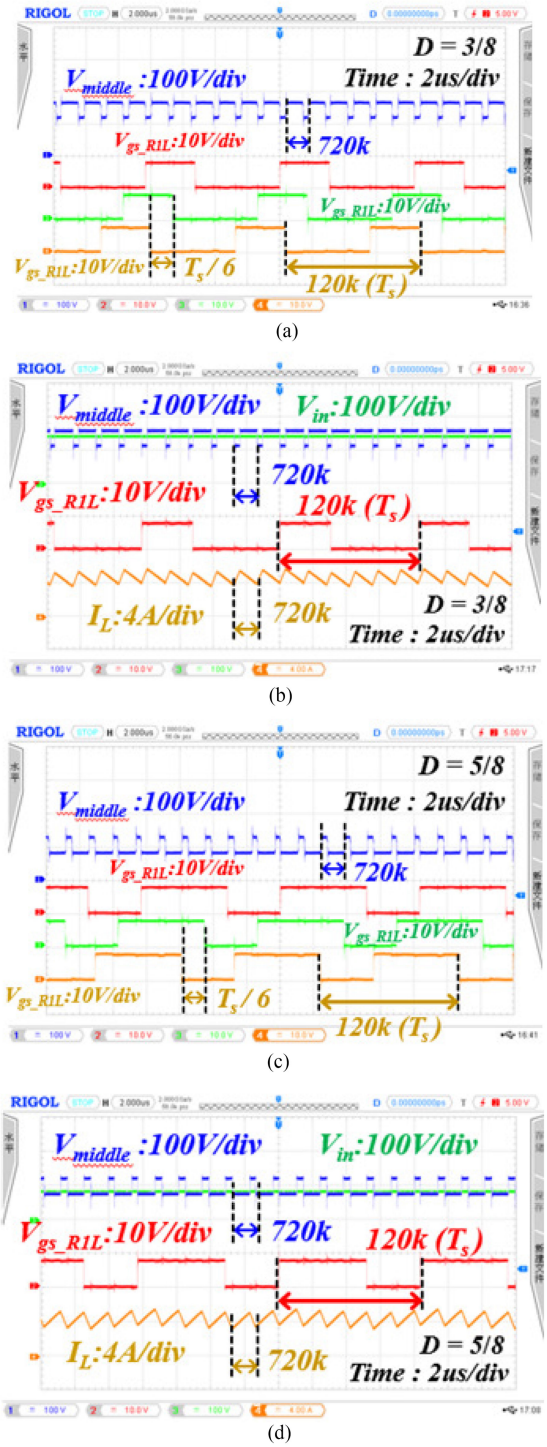

Fig. 18. Key waveforms of regulator when RDCX working under discharging mode. (a) High side switch gate voltages @$D = 3/8$. (b) Inductor current waveform @$D = 3/8$. (c) High side switch gate voltages @$D = 5/8$. (d) Inductor current waveform @$D = 5/8$.

D. Transformer Design Considerations

One layer one turn transformer structure is used in this article for design simplicity. As at least 22-layer PCB would be needed for DCX in Fig. 9 when their windings are wound to same core leg, two transformers are adopted to reduce the needed

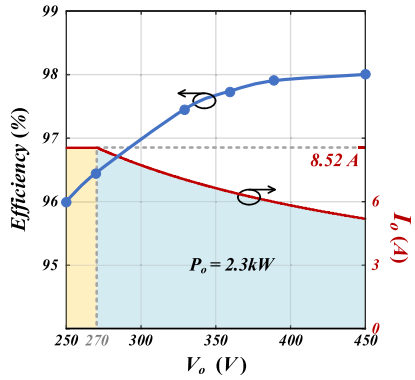

Fig. 19. Predefined charging curve and measured efficiencies under charging mode.

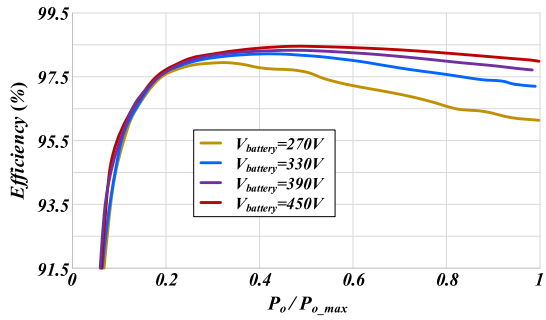

Fig. 20. Measured efficiencies at different battery voltages under discharging mode.

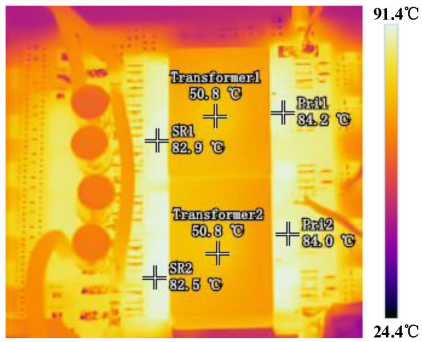

Fig. 21. Thermal image of RDCX prototype at full load and $V_{\text{battery}} = 450$ V.

PCB layers and save expense. By distributing the windings evenly to two transformers, the number of PCB layers needed can be cut by half. The single transformer related RDCX unit topology is shown in Fig. 11(a), where "Inv." stands for the DCX inverter cells, "Rec." stands for the DCX rectifier cells. The connection between units is shown in Fig. 11(c), where single inverter block (Inv.) is used to represent the multiple inverter cells in series in Fig. 11(a) for simplicity, so as the main secondary and auxiliary rectifier, which are both represented by a rectifier block (Rec.). As the connection in Fig. 11(c) is an input series and output series (ISOS) structure, a balancing winding is added in each RDCX unit for voltage balance between them. The connection of balancing winding is shown

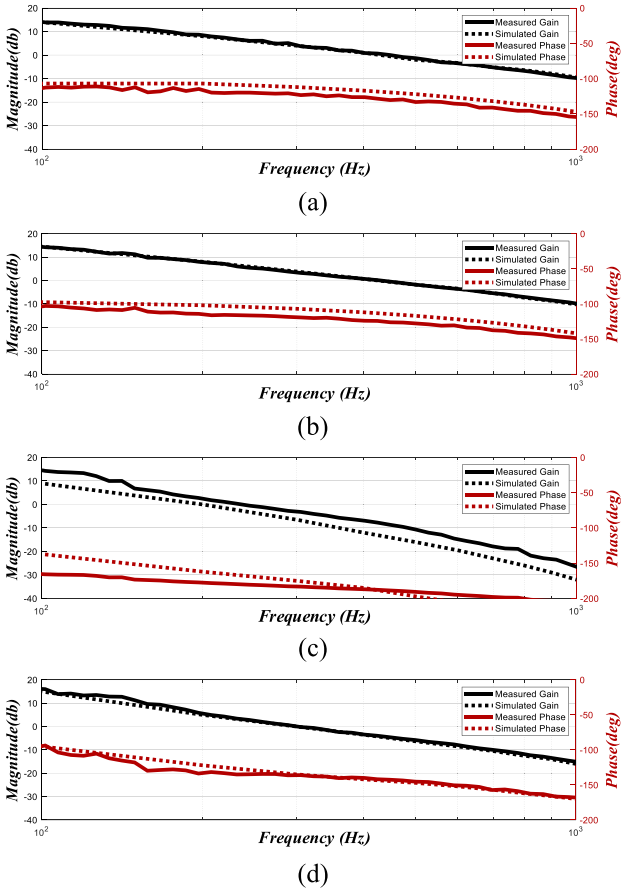

Fig. 22. Measured and simulated bode plots of the prototype under charging mode with different working conditions. (a)$V_{\text{battery}} = 270$ V and $I_o = 1$ A. (b) $V_{\text{battery}} = 270$ V and $I_o = 5$ A. (c) $V_{\text{battery}} = 360$ V and $I_o = 5$A. (d) $V_{\text{battery}} = 360$ V and $I_o = 5$ A.

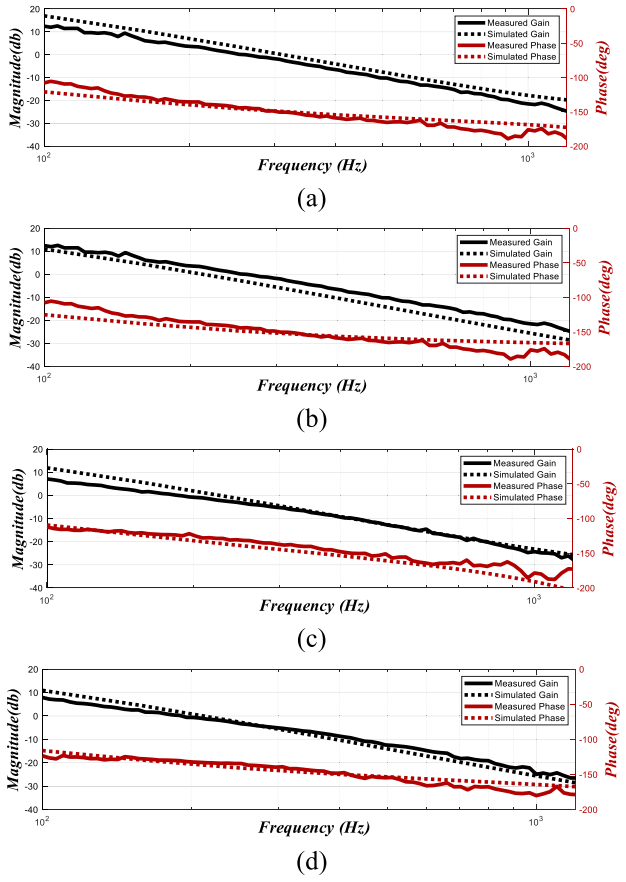

Fig. 23. Measured and simulated bode plots of the prototype under discharging mode with different working conditions. (a)$V_{\text{battery}} = 270$ V and $I_o = 1$ A. (b) $V_{\text{battery}} = 270$ V and $I_o = 5$ A. (c) $V_{\text{battery}} = 450$ V and $I_o = 5$ A. (d) $V_{\text{battery}} = 450$ V and $I_o = 5$ A.

in Fig. 11(b), where the balancing winding of RDCX unit1 is paralleled with the winding of one inverter cell from RDCX unit2; and vice versa. As a result, the voltage per turn of the two RDCX units' transformers is forced to be same and voltage balance between them can be achieved. Finally, an interleaving transformer structure with EI core for each RDCX unit in Fig. 11 is adopted to reduce eddy current loss, as shown in Fig. 12.

IV. Experimental Verifications

In order to evaluate the proposed low FoM device based RDCX converter and the design guidelines mentioned above, a 388–412 V/250–450 V 1MHz RDCX prototype with rated power of 2.3 kW is built up. The simplified system schematic is given in Fig. 13, including charging mode and discharging mode. Single inverter block (Inv.) and rectifier block (Rec.) is used to represent the multiple inverter cells and rectifier cells in Fig. 11 for simplicity, so as the transformer. When the circuit works in discharging mode, power flows from secondary side to primary side, thus the primary circuits work as rectifier and secondary circuits work as inverter, as shown in Fig. 13(b). In both modes, driving signals with fixed frequency and duty for DCX switches are given by a digital signal processer. Isolated gate drivers are used to drive switches with different reference ground. Under charging mode, a current loop is used to control the output current and its reference value is calculated based on the sampled output voltage and charging curve predefined. Under discharging mode, a voltage loop is employed for bus voltage control. In addition, a current loop is added for circuit stability, since the regulator works as a boost converter in discharging mode. Common duty control and phase shift modulation are applied to the regulator in both modes for multilevel operation. Based on the circuit design methodology in [2] and [29], device and circuit parameters can be chosen for DCX and cascaded buck converter. Finally, the prototype is shown in Fig. 14, in which power circuit, driving system, sampling and control circuits are included, and its key parameters are given in Table I.

The measured resonant current, low side switch drain-to-source voltage and gate voltage of one primary inverter cell, namely i_{rp}, $V_{ds\_PL,}$ and V_{gs_PL}, respectively, along the resonant current of one secondary rectifier cell, namely i_{rs}, of DCX in Fig. 9 are shown in Fig. 15, under full and null load in charging and discharging condition. It can learn from Fig. 15 that ZVS on is achieved under all conditions mentioned above for DCX.

In order to evaluate the voltage and current sharing capability in the proposed converter, the low-side switch drain-to-source voltage and resonant current of three different primary inverter cells in Fig. 9 are measured and shown in Fig. 16. It should be noted that the waveforms labeled with subscript "1" and "2" is from cells in RDCX unit1, and waveforms labeled with subscript "3" is from cell in RDCX unit 2 in Fig. 11(c). Thus, Fig. 16(a) and (b) shows that the voltage balance and current sharing among cells is all achieved well, respectively, both in single RDCX unit and between RDCX units.

Fig. 17 shows the key waveforms of the cascaded buck regulator at different duty ratio (noted as D for short) when RDCX working under charging mode. The high-side switches gate voltages of the upper three bridges, along with the inductor current and its chopper side voltage, which is noted V_{gs_R1H}, V_{gs_R2H}, V_{gs_R3H}, I_L and V_{middle} respectively in Fig. 10 are measured and shown in Fig. 17. In Fig. 17(a) and (b), the duty cycle equals 1/24; in Fig. 17(c) and (d), the duty cycle is 1/8. It can be observed that the switching frequency of single bridge is 120 kHz, and the driving pulse width of three bridges are same. The three driving pulses are sequentially lagged by 1/6 switching cycles, which means phase shift modulation is achieved. As a result, $V_{\rm middle}$ is in 720 kHz, and its peak-to-peak value is around 40 V, same as the bus voltage of single half bridge in Fig. 10. This leads to the 720 kHz inductor current I_L, indicating that the multilevel function has been successfully achieved, as shown in Fig. 17(b)[$D = 1/24$] and Fig. 17(d)[$D = 1/8$].

Fig. 18 shows the key waveforms of the regulator at different duty cycle when RDCX working under discharging mode. $V_{\rm middle}$ and gate voltages of low-side switches of the upper three bridges (noted as V_{gs_R1L}, V_{gs_R2L}, and V_{gs_R3L} in Fig. 10) are measured, since the regulator works as a boost converter under discharging mode. Same as in charging mode, phase shift modulation and common duty control is achieved. As a result, the current frequency is 720 kHz, meaning that the multilevel function is well achieved.

The predefined charging curve used in this article is drawn in Fig. 19. When the battery voltage is between 250–270 V, 8.52 A constant current charging is used; whereas when the battery voltage is between 270–450 V, 2.3kW constant power charging is used. The measured efficiencies of the RDCX prototype based on the charging curve are also shown in Fig. 19. It shows that the prototype has a peak efficiency of 98% under full load @$V_{\rm battery} = 450$ V, with power density around 910 W/in^3. In the discharging process, the measured prototype efficiencies versus normalized output power are illustrated in Fig. 20, with different battery voltages and bus voltage fixed to be 400 V. The peak efficiency is about 98.5% under half load when battery voltage equals 450 V. Driving loss is not included in efficiency measurement in Figs. 19 and 20, since the bias system for the multiple isolated drivers is out of the scope of this article and hence is not included in the prototype. The driving loss is estimated as 5.5 W based on device datasheet and converter working frequency, and would result in 0.24% efficiency loss under full load condition.

The thermal image of the prototype at full load with forced air cooling when battery voltage equals 450 V under charging mode is shown in Fig. 21. The temperature of two transformers is measured around 50 °C under 1 MHz working. Devices temperatures are all around 80 °C, which means that the balance of power flow and losses among different cells and RDCX units are well achieved.

The measured and simulated bode plots of the prototype with different load and battery voltage conditions are presented in Fig. 22 under charging mode, and in Fig. 23 under discharging mode, which indicate that the system can achieve stable under different working conditions.

V. Conclusion

In this article, an RDCX converter suitable for wide range voltage regulation and its overall design procedure are proposed. For the DCX part, a detailed conduction loss model is given for multiport *CLLC* DCX. The model shows that by using low-voltage devices in series, the low FoM characteristic of low-voltage device can be used to reduce the circuit conduction loss. Low voltage cell circuit is used for voltage balancing between low voltage devices in series. By coupling the winding of all cells to a same transformer, they could easily achieve voltage balance. For the regulation part, a cascaded buck structure is proposed to reduce the inductor size. By implementing carrier phase shift modulation and common duty control, this converter can achieve multilevel operation, making it very suitable for wide voltage range regulation. Because the bus of the cascaded buck converter is connected to the outputs of the DCX low voltage rectifier cells, the bus voltage can be naturally balanced. Moreover, a paralleled winding structure for voltage balance between ISOS RDCX units is proposed. Thus, the circuit can be easily extended to higher voltage level based on less PCB layers. Finally, a prototype with 910 W/in^3 power density and 98% peak efficiency is built based on the proposed topology to verify the rationality of the theoretical analysis.

Appendix
Derivation of Minimum Conduction Loss of Primary MOSFETs in Three Port *CLLC* DCX

This appendix derives the minimum conduction loss of primary MOSFETs in three port *CLLC* DCX. All variables are same as those utilized in Section II.

Equation (8) can be simplified as

$$P_{\rm Con\_P} \approx A \cdot R_{\rm dson\_P} + \frac{B}{R_{\rm dson\_P}} \tag{26}$$

by defining A and B as

$$\begin{aligned} A &= \frac{P_o^2 \pi^2 T_S}{2 V_{\rm in}^2 T_r} \\ B &= \frac{4 T_r V_{\rm in}^2 {\rm NFoM}_{\rm P}^2}{3 T_S t_d^2}. \end{aligned} \tag{27}$$

Based on the AM–GM inequality, which is

$$a + b \geq 2\sqrt{ab} \ \ (a \geq 0,\ b \geq 0) \tag{28}$$

the minimum value of (26) can be derived

$$P_{\rm Con\_P} \approx A \cdot R_{\rm dson\_P} + \frac{B}{R_{\rm dson\_P}} \geq 2\sqrt{AB}. \tag{29}$$

Combining (27) and (29), we get

$$P_{\mathrm{Con\_P}} \geq 2\pi \cdot \sqrt{\frac{2}{3}} \cdot \frac{P_o \cdot \mathrm{NFoM_P}}{t_d}. \tag{30}$$

Equation (30) means the minimum conduction loss of primary MOSFETs in three port *CLLC* DCX, min($P_{\mathrm{Con\_P}}$), is

$$\min\left(P_{\mathrm{Con\_P}}\right) = 2\pi \cdot \sqrt{\frac{2}{3}} \cdot \frac{P_o \cdot \mathrm{NFoM_P}}{t_d} \tag{31}$$

which is (10) in Section II.

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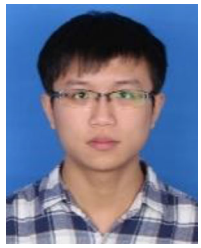

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