Design and Validation of the Parallel Enhanced Commutation Integrated Nested Multilevel Inverter Topology

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***Abstract*—In this article, a promising design of power electronics in the field of battery electric vehicles is proposed. The presented parallel enhanced commutation integrated nested multilevel inverter is a symmetrical cascaded multilevel inverter characterized by a minimal number of semiconductor switches compared to its range of functions. In addition to regular four-quadrant operation, the topology is able to reconfigure individual battery cells between serial and parallel interconnection to minimize the internal resistance of the reconfigurable battery system during operation. In particular, by separately considering the internal resistance of the power electronics and the variable internal resistance of the reconfigurable battery, a minimum overall internal resistance is achieved. After a detailed review of related modern topologies, the topology's inherent structural advantages are presented. Functional spectrum, internal resistance, and efficiency behavior are compared with related topologies frequently studied in the literature. Measurements on a 17-level three-phase prototype show the function and performance of the proposed structure in terms of functional spectrum, low total harmonic distortion, and efficiency. It turns out that the parallel enhanced commutation integrated nested multilevel inverter is a competitive topology that should be investigated further.**

***Index Terms*—Drivetrain, electric vehicles, enhanced commutation integrated nested (ECIN), modular multilevel converter (MMLC), parallel enhanced commutation integrated nested (PECIN), power electronics.**

Nomenclature

BEV	Battery electric vehicle.
BCS	Bridge-type connected source.
BtB	Back-to-back.
CHB	Cascaded H-bridge.
Cl	Closing (unit).
CCS	Cascaded cross-switched.
CS	Cross-switched.
ECIN	Enhanced commutation integrated nested.
FPGA	Field-programmable gate array.
M2B	Modular multilevel battery.
MLI	Multilevel inverter.
MMLC	Modular multilevel converter.
MMSPC	Modular multilevel series/parallel converter.
MOSFET	Metal–oxide–semiconductor field-effect transistor.
NLC	Nearest level control.
OCV	Open-circuit voltage.
PCB	Printed circuit board.
PECIN	Parallel enhanced commutation integrated nested.
SM	Submodule.
SOC	State of charge.
SVC	Space vector control.
THD	Total harmonic distortion.
TU	Termination unit.

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I. Introduction

BESIDES battery technology, efficient power electronics is the key enabler for modern BEVs. Since space and weight are limiting factors for the battery in a vehicle, only a finite amount of energy-storing active material can be installed. Therefore, the efficiency and the total utilization of the energy potential of every single battery cell is an essential differentiator for the usable energy in the powertrain. Recent research shows that the MLI addresses these aspects and is a promising approach to improve electric drive technology further [1]–[4]. The MLI was first introduced by Baker and Bannister in 1975 [5]. The proposed inverter is nowadays known as CHB inverter and is part of the family of cascaded MLIs. Over the past few decades, different topologies have been developed and investigated [6], [7]. Furthermore, in addition to cascaded MLIs, the family branches of flying capacitor MLIs [8] and neutral-point-clamped MLIs [9] have emerged. In particular, cascaded MLIs have received special attention due to their simple conception and good scalability [6]. Cascaded MLIs have a smallest unit called SM. It contains a specific structure of an electrical network called *microtopology* and a dc supply. "Cascaded" means that several of these SMs are connected in the same way. Since the cascade is a relatively simple and defined process, the topology can be extended by simply adding additional SMs to meet the requirements of the application. The interconnection of SMs leads to an overall function of the entire system [7]. The design of this interconnection is called *macrotopology*. The *macrotopology* is not limited to one phase strand, as shown

in [10], and serves the original idea of the MLI that, in contrast to the conventional two-level inverter, the MLI can intrinsically generate a large number of output voltages [11]. By reconfiguring the electrical circuit within the cascade of SMs, it can set intermediate voltage levels that better match the desired voltage. Thereby, the current limitation and the current signal's quality become less dependent on the switching frequency. In general, these effects increase with the number of levels and lower step height of the output voltage steps. As a result, MLIs intrinsically achieve low THD output current values [12]. Thus, on the one hand, special filter components for the output of the inverter are no longer needed or can be reduced in size [13]. On the other hand, this allows decreasing switching frequencies and, therefore, switching losses. In drive applications, low THD leads to lower iron and copper losses, which increases efficiency [1]. Conventional traction systems consist of a separate battery and inverter system. The battery system has a fixed configuration, and its constant output voltage is the supply for the dc link, which supplies the conventional inverter. However, due to the high number of individual battery cells, a modern traction battery already provides the structure for building a cascaded MLI [1], [2], [14], [15]. The battery cells supply a relatively low and galvanically isolated output voltage, allowing a high number of output voltage levels. To achieve MLI functionality, the ability to add and remove these battery cells from the load path during operation must be provided. On the one hand, reconfiguration allows the output voltage of the battery system to be adjustable, making the reconfigurable battery itself an inverter system. On the other hand, this opens up new possibilities in single-cell battery management. Symmetrical MLIs use the same type of dc power source in each SM [6]. This implies that there are a lot of redundant switching states to achieve a single voltage level as voltage sources are interchangeable. As with ac signals, the desired output voltage changes permanently, resulting in a permanent choosing on which cells adding up to achieve the desired voltage value. A controller can decide for every control step which cells should be operated. An important aspect for MLIs is charge balance control [4]. Of interest is that the cells all together hit end-of-charge (charging case) or end-of-discharge (discharging case) to prevent unusable charging stuck inside the battery cells. Charge balancing procedures are also described in the literature [4] for MLIs with serial and parallel reconfiguration [16]. The reconfiguration is achieved by interconnecting the cells with semiconductor switches [6], [7]. Since the switches in the MLI can be designed for the low battery cell voltage, primarily MOSFETs can be used. Although the higher number of inserted switches increases the internal resistance, the comparatively low conduction and switching losses of MOSFET technology mitigate this effect [2], [3]. In addition, the semiconductor switches perform fewer switching operations due to lower switching frequencies. However, while switching losses dominate in conventional inverter systems, conduction losses dominate in MLI, and switching losses are almost negligible [2]. Therefore, the MLI has an efficiency advantage, especially in partial load situations [3]. Particularly, in dynamic applications such as BEVs, with mostly partial load operation, the MLI can increase the overall efficiency of the system [1]–[3]. Not least because of its simple scalability and excellent efficiency, the basic principle of MLIs is interesting for BEVs. Like a conventional inverter, an MLI can adjust its output voltage according to a controller demand during operation. Therefore, the MLI can be directly tied to an electrical traction machine or on an electrical grid and be operated without additional power electronics. In addition, they can further simplify the drive system by combining the energy storage system, the inverter, and the charging system [15]. Even though the MLI concept generally has advantageous properties, there are significant differences in the realization of advantageous MLI topologies.

This article proposes a novel MLI, named PECIN MLI, in the context of battery electric drive technology. For the design, a combination of the advantageous features from advanced MLI topologies in the current literature has been extracted and considered as design criteria for the new MLI. The inverter is designed for maximum efficiency by considering the combined optimization of battery and inverter losses and providing full single-cell battery management capability. Since the design of a suitable topology is the most fundamental aspect in MLI applications, this article, on the one hand, provides a solid basis for designing and evaluating the performance of MLI systems and, on the other hand, presents a high-performance new MLI.

The following is a comprehensive analysis of related topologies to identify general beneficial features of an MLI. Next, the PECIN structure is presented in Section II-B with a theoretical comparison between the topologies and measurement results in Section III. Finally, Section IV concludes this article.

II. Design of the PECIN MLI Topology

A. Review on Related MLI Topologies

The following review covers selected topologies that were relevant to the development process of the PECIN topology. To illustrate important aspects, Fig. 1 shows the discussed topologies in a comparable format. Since the switching elements in the MLIs are intended to operate as ideal switches, they are represented with ideal switching symbols, as defined in Fig. 3. For practical implementation, MOSFET technology is used today [4]. Fig. 3 provides the link to practical implementation. The switching and graphical symbols are directly interchangeable in all the figures in this article. Great importance must be attached to the installation direction, which is indicated in Fig. 3 by the designation of the connections. In the discussion, reference is made to specific parts of the illustration. Each row contains a phase string of a particular topology, with a cascading of four associated SMs in the columns. One SM of every topology is framed, and its components are highlighted in green. Some of the topologies require a TU or a Cl at the beginning or end of the phase strand. An exemplary valid load path is drawn in each topology to underline the discussed functionalities of the topologies. A load or additional phase strings can be connected to the phase terminals *N* and *L*.

1) CHB MLI and MMLC: As the efficiency analyses of MLI systems in [1]–[3] have shown, conduction losses are the main driver of losses in the MLI. Since every electrical device has an internal resistance, the goal in designing a high-efficiency MLI

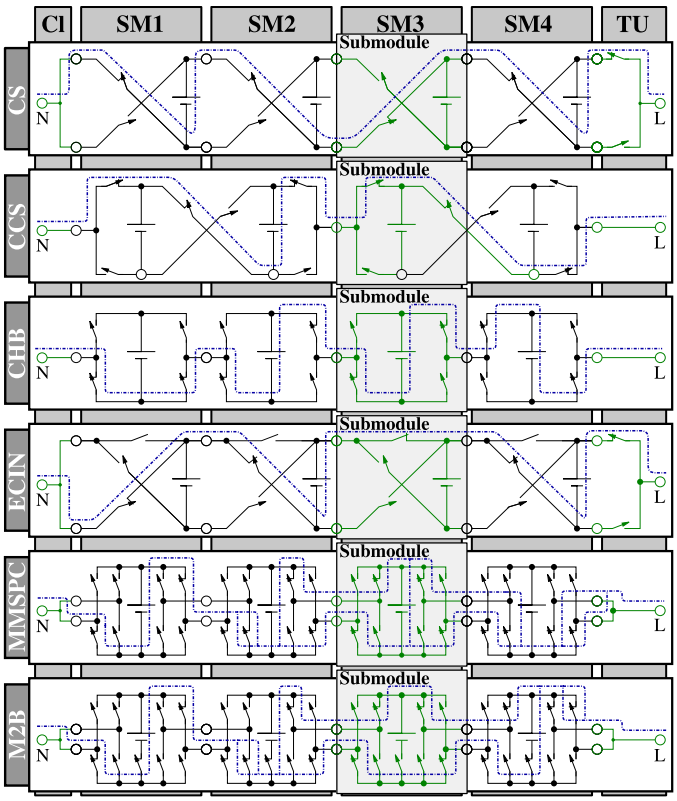


Fig. 1. Topology in an exemplary embodiment with four SMs and exemplary current paths for CS, CCS, CHB, ECIN, MMSPC, and M2B MLIs. For the notation of the switching symbols, see Fig. 3.

is to reduce its internal resistance. Since each component has its own internal resistance, reducing the internal resistance of the inverter is often accompanied by a reduction in the number of components in the load path. In an MLI circuit, the electrical components are mainly switching devices and battery cells. One of the best-known MLI topologies is the MMLC developed by Lesnicar and Marquardt [17]. The MMLC is built out of very few components, provides a dc link but has only half of the dc-link voltage as ac output voltage amplitude. The well-known CHB MLI can, in turn, generate four times the output voltage amplitude with the same number of battery cells as the MMLC. Since the level of the output voltage is determined by adding additional voltage sources, the MMLC needs four times the number of SMs than the CHB MLI to achieve the same output voltage. Since each SM has its own internal resistance, this increases the conduction losses for the MMLC. Therefore, MLI circuits that inherently produce a high output voltage are advantageous. The higher reachable output voltage of the CHB MLI is achieved through the individual commutation capability of each SM, which the MMLC topology does not have. Thus, each SM contributes to the positive and negative output voltage of the inverter by being able to provide positive and negative cell voltages at its terminals. The CHB MLI realizes this through an SM that enables four-quadrant operation. Polarity commutation is not a standard for MLIs (cf. [6] and [7]), but is the first driver for highest efficiency as it decreases the number of SMs needed.

2) CS MLI: The second driver is to minimize the internal resistance of the remaining SMs. Since SMs of the same structure are used in a cascaded MLI and the type of voltage source is usually specified, the number of switches per SM is a good comparison value between different topologies. For the CHB, this value is 2 for every operating state of the SM (cf. CHB in Fig. 1). However, the CHB MLI has twice the demand for semiconductor switches and gate drivers as the MMLC. The CS MLI has the same number of semiconductor switches as an MMLC and provides immanent polarity commutation like the CHB MLI (cf. CS in Fig. 1) [18]. Therefore, it has the same output voltage characteristic. However, the CS MLI introduces an important new idea by moving the individual commutation capability from the SM level to the phase string level. Individual SMs, therefore, cannot provide a bipolar cell voltage at their terminals, as the bipolar output voltage is only generated by the cascade of SMs. The CS MLI achieves this by forming SMs not as two poles but quadripoles. This design makes it possible to provide both the positive and negative output voltages of the string with significantly fewer components. However, there is a disadvantage in the case of cells to be bridged for the CS MLI. Bridging means that in a string of cascaded SMs, one or more cells should be in an idle state, while the phase string is still operable. Bridging occurs, for example, during normal operation because some cells are not needed to provide the current output voltage, for charge balancing or during error handling where a particular cell needs to be disconnected from the battery string. For these cases, the operation of the remaining cells should not be affected, and the energy supply to the load should not be interrupted. The bypass capability of individual cells is, therefore, crucial to the advanced single-cell battery management capability of an MLI [4]. While MMLC and CHB MLI provide this functionality, the CS MLI does not. A previous or a subsequent neighboring cell must be bridged to bridge a single battery cell (cf. CS:SM2-SM3 in Fig. 1). For the CS MLI, this technically guarantees that the polarity of all the cells is consistent, which is necessary to generate the desired output voltage. Therefore, the number of modulation schemes that can be applied to the CS MLI is limited. For example, charge balance control methods, which are crucial for normal MLI operation, are not operable without restrictions. Additional balancing hardware may need to be installed, which, in turn, increases cost, weight, and complexity. As the limitation in reconfiguration was recognized, an improved version, the CCS MLI, was developed in [19]. The CCS MLI can independently bypass each cell (cf. CCS:SM3 in Fig. 1). However, it has the disadvantage of 1.5 switches per SM in the load path for each operating state. While this is better than the CHB MLI, it has a negative impact on system conduction losses compared to the CS MLI.

3) ECIN MLI: The ECIN MLI [20] was developed as an extension of the *Marx* inverter presented in [21]. The ECIN MLI, unlike the *Marx* inverter, has inherent polarity commutation capability at the string level. Thus, as shown in Fig. 2, switch A must withstand both a positive and a negative cell voltage U_{cell}. Since a single MOSFET only fully blocks unidirectionally, a bidirectional blocking BtB MOSFET must be used, as shown

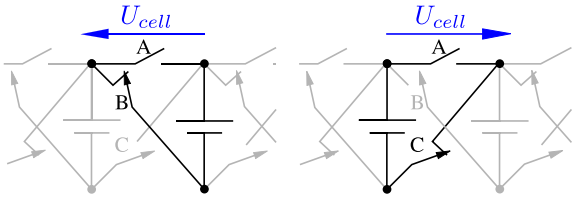


Fig. 2. Possible voltage drop at switch A of the ECIN MLI.

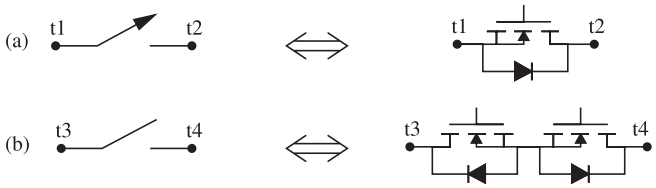


Fig. 3. (a) MOSFET: switching symbol (left) and graphical symbol (right). (b) BtB MOSFET: switching symbol (left) and graphical symbol (right) (cf. [22]).

in Fig. 3(d). Advantageously, both the MOSFETs of the BtB MOSFET can be operated from a common gate driver, since the BtB MOSFET is used as one discrete switch. However, it has twice the resistance of a single MOSFET. Although the ECIN MLI has the same functionalities as the CCS MLI, it has only one switch in the load path for active cells. For bypassed cells, an intelligent operation strategy would exploit the following methodology. If there is an even number of bridged cells between two active cells (cf. CS:SM2-SM3 in Fig. 1) or several bridged cells between an active cell and a string terminal (cf. ECIN:SM1 in Fig. 1), all the SMs can be operated with only one single MOSFET in the load path. Only if there is an odd number of bypassed cells between two active cells, exactly one SM has to be operated with a BtB MOSFET in the load path, while all other SMs use only single MOSFETs (cf. ECIN:SM3 in Fig. 1). Therefore, the internal resistance is minimized, and a value close to one switch per cell is achievable.

4) Modular Multilevel Series/Parallel Converter: In general, the circuit arrangement of electrical components is either possible in a serial or parallel fashion. All previously presented topologies focus on a serial connection of cells. In conventional battery systems, cells are often connected in parallel to increase charge and current carrying capacity. Goetz *et al.* [23] introduced this idea into MLI research with the MMSPC design. It is able to reconfigure battery cells between serial and parallel interconnection during operation (cf. MMSPC in Fig. 1). One SM is a quadripole and consists of two H-bridges. There are two switches per H-bridge in the load path independent of the switching state in normal operation. However, this can be reduced by operating the two high-side and the two low-side switches of each H-bridge simultaneously (cf. MMSPC:SM1 & SM2 in Fig. 1). Thus, the MMSPC has the effective resistance of one switch per SM in the load path with serial cascading and a total of eight switching elements per SM. As an extension, Helling *et al.* [15] developed the M2B, which can connect nonadjacent cells in parallel by bridging cells in between. For this purpose, another switch is connected in series to each cell,

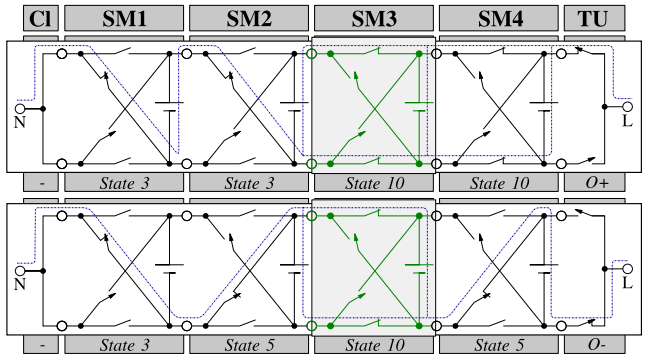


Fig. 4. Proposed PECIN MLI in a nine-level embodiment: exemplary positive output voltage (top) and exemplary negative output voltage (bottom).

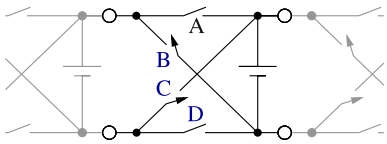
increasing the cells' internal resistance. As a result, the M2B has a total of nine switches per cell. Comparing the MMSPC and the M2B to previous topologies, the number of needed switches is undesirably high. Despite this disadvantage, an interesting idea and highly efficient inverters were created. The MMSPC is superior to the presented topologies in terms of efficiency, considering the excellent low number of switches in the current path. In addition, it offers the potential of cell parallelization to reduce the internal resistance of the circuit further.

The literature review has shown the differences in the quality and functionality of different cascaded MLI circuits. It has been shown that the crucial technical requirements for a highly efficient cascaded MLI design are a low internal resistance for each switching state. Here, intrinsic commutation capability, the lowest possible internal resistance of the SM, and a parallel reconfiguration were identified as ways of reducing the internal resistance. In addition, low complexity of the circuitry and reduced amount of needed electronic devices are to be aimed for.

B. PECIN MLI

The results of the previous review determine the design of the PECIN MLI. The PECIN MLI extends the BCS inverter presented in [24] and is depicted in Fig. 4. It is a bidirectional MLI that, in contrast to the BCS MLI, connects cells both in serial and in parallel during operation, while cell individual bypassing is possible at any time. Like the MMSPC topology and in contrast to the asymmetric BCS MLI, it is thus able to reduce the internal resistance of the system by reducing the power electronic resistance and cell internal resistance. In addition, the PECIN MLI offers single-cell battery management capability such as charge balancing and bad block management due to its symmetrical design [4]. For this reason, the functional scope of the topology is equivalent to that of the MMSPC but decreases a key parameter, the number of needed components.

1) Microtopology: The microtopology already contains most of the characteristics of the inverter since attributes scale with the number of cascaded SMs. An advantageous way of forming SMs for the PECIN topology is shown in Fig. 4. An SM consists of a battery cell and four switching elements.



Switching State	Switch A	Switch B	Switch C	Switch D	Function
1	0	0	0	0	idle / blocking
2	1	0	0	0	bypass / negative active
3	0	1	0	0	bypass / positive active
4	1	1	0	0	short circuit cell
5	0	0	1	0	bypass / negativ active
6	1	0	1	0	short circuit prior cell
7	0	1	1	0	short circuit cell and prior cell
8	1	1	1	0	short circuit cell and prior cell
9	0	0	0	1	bypass / positive active
10	1	0	0	1	bypass / parallel
11	0	1	0	1	short circuit prior cell
12	1	1	0	1	short circuit cell and prior cell
13	0	0	1	1	short circuit cell
14	1	0	1	1	short circuit cell and prior cell
15	0	1	1	1	short circuit cell and prior cell
16	1	1	1	1	short circuit cell and prior cell

Fig. 5. Possible switching states and associated functions of the PECIN SM.

There are two switches with unidirectional and two switches with bidirectional blocking capability. The SM is a quadripole. This design is necessary for the parallelization of cells but also offers redundant switching patterns in serial operation. The basic principle of the SM is that the output terminals of the SM are each directly connected to a cell terminal. In addition, the other two input terminals of the SM can each be connected to a cell terminal via switches.

2) Macrotopology: However, the phase string must become two-pole to connect to the load via the terminals *N* and *L*. For this reason, the ends of the cascade of PECIN SMs at the beginning and end of the phase string must be rejoined to form one terminal. Since one side of the microtopology provides direct access to both the cell terminals, only one cell terminal can be connected to the string terminal *L* at a time. On the other hand, exclusive access to both the cell terminals is necessary for bipolar voltage generation. Therefore, the cascade of SMs needs a TU to be operated. An advantageous setup is shown in TU in Fig. 4, where the TU consists of two individual switches.

As with the development from the MMSPC to the M2B, it is also possible to seamlessly integrate bypass capability for parallel cells with the PECIN MLI, as the concept is straightforward. However, an additional switch needs to be inserted into the active path of each cell. This massive disadvantage for efficiency barely outweighs the advantages of parallel bypassing in most applications. For this reason, this was not considered further.

3) Control Mechanism

a) General: From the logic theory, each PECIN SM has four individual switches and, therefore, 2^4 *switching states*. Of these 16 *states* listed in Fig. 5, six *states* are of practical relevance. Therefore, the ten other *switching states* must be avoided. These create short circuits in the SM, in SMs connected in parallel, and in the preceding SMs.

b) Safety: In a string of cascaded PECIN SMs, the valid six *switching states* can be applied arbitrarily to SMs without causing short circuits. From a safety point of view, the *states* of successive SMs are, thus, not dependent on preceding or following *SM states*. Therefore, safe operation at SM and string level can be guaranteed via logical hardware monitoring at SM level. In Fig. 5, the *switching states* to be avoided are marked (purple). The logical monitoring function (1) can be derived from these as an indicator for unallowed switching operations

$$y = AB \vee AC \vee BC \vee BD \vee CD. \tag{1}$$

As soon as (1) states logical level *true*, a *switching state* is set, which is not permissible. Based on this consideration, it is also possible to define dominant *switching states* at the hardware interlock level according to the application's requirements. These can ensure safe operation as an additional safety layer if control errors or disturbances occur that correspond to a prohibited *switching state*.

c) Function: In general, it is recommended to create a valid path through the PECIN topology using the defined *switching states* in Fig. 5 and avoid control logic for individual switches. The defined valid *switching states* represent safe switching operations. An arbitrary sequence of *switching states* applied to several cascaded SMs always forms a valid current path that connects both the terminals of the phase string. This characteristic is due to the efficient design of the PECIN MLI, in which each current path is assigned several functions. However, to create a desired function in the phase string, a higher level function (e.g., Table I) must specify the switching pattern in accordance with the preceding and following SM states. Furthermore, a good operating strategy serves the PECIN topology in such a way that only single MOSFETs are used for serial cascading (cf. Table I). In the *parallel mode*, the cells are connected in parallel with other cells that are not needed to achieve the desired output voltage. This strategy applies without restriction to normal operations. Only in exceptional situations, cells may have to be bypassed, and an operation of BtB MOSFETs might be necessary. Here, the strategy presented for the ECIN topology can be applied (cf. Section II-A3) to use the energetically favorable single MOSFETs whenever possible.

TABLE I
EXEMPLARY SWITCHING PATTERN OF A 17-LEVEL PECIN MLI: *SERIAL MODE:* UNUSED CELLS ARE BYPASSED; *PARALLEL MODE:* CELLS NOT NEEDED FOR VOLTAGE GENERATION ARE CONNECTED IN PARALLEL WITH OTHER ACTIVE CELLS

	Submodule State: *serial mode* | *parallel mode*								
Level	SM1	SM2	SM3	SM4	SM5	SM6	SM7	SM8	TU
-8	5 | 5	5 | 5	5 | 5	5 | 5	5 | 5	5 | 5	5 | 5	5 | 5	O- | O-
-7	5 | 5	5 | 10	2 | 5	5 | 5	5 | 5	5 | 5	5 | 5	5 | 5	O- | O-
-6	5 | 5	5 | 10	2 | 5	5 | 10	2 | 5	5 | 5	5 | 5	5 | 5	O- | O-
-5	5 | 5	5 | 10	2 | 5	5 | 10	2 | 5	5 | 10	2 | 5	5 | 5	O- | O-
-4	5 | 5	5 | 10	2 | 5	5 | 10	2 | 5	5 | 10	2 | 5	5 | 10	O+ | O-
-3	5 | 5	5 | 10	3 | 10	5 | 5	5 | 10	3 | 10	5 | 5	5 | 10	O+ | O-
-2	5 | 5	5 | 10	3 | 10	5 | 10	2 | 5	5 | 10	3 | 10	5 | 10	O+ | O-
-1	5 | 5	5 | 10	3 | 10	5 | 10	3 | 10	5 | 10	3 | 10	5 | 10	O+ | O-
0	3 | 3	5 | 5	3 | 3	5 | 5	3 | 3	5 | 5	3 | 3	5 | 5	O+ | O+
1	3 | 3	3 | 10	5 | 10	3 | 10	5 | 10	3 | 10	5 | 10	3 | 10	O- | O+
2	3 | 3	3 | 10	5 | 10	3 | 10	9 | 3	3 | 10	5 | 10	3 | 10	O- | O+
3	3 | 3	3 | 10	5 | 10	3 | 3	3 | 10	5 | 10	3 | 3	3 | 10	O- | O+
4	3 | 3	3 | 10	9 | 3	3 | 10	9 | 3	3 | 10	9 | 3	3 | 10	O- | O+
5	3 | 3	3 | 10	9 | 3	3 | 10	9 | 3	3 | 10	9 | 3	3 | 3	O+ | O+
6	3 | 3	3 | 10	9 | 3	3 | 10	9 | 3	3 | 3	3 | 3	3 | 3	O+ | O+
7	3 | 3	3 | 10	9 | 3	3 | 3	3 | 3	3 | 3	3 | 3	3 | 3	O+ | O+
8	3 | 3	3 | 3	3 | 3	3 | 3	3 | 3	3 | 3	3 | 3	3 | 3	O+ | O+

III. EXPERIMENTAL RESULTS AND ANALYSIS

A new test stand was built to analyze and test the PECIN MLI (cf. Figs. 6 and 7). The test stand includes a measurement and

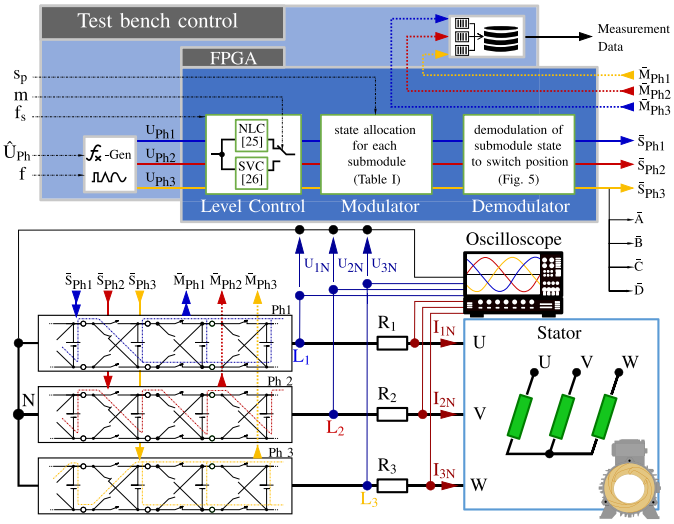


Fig. 6. Schematic of the PECIN MLI test bench setup with component wiring, measuring points, and control schematic.

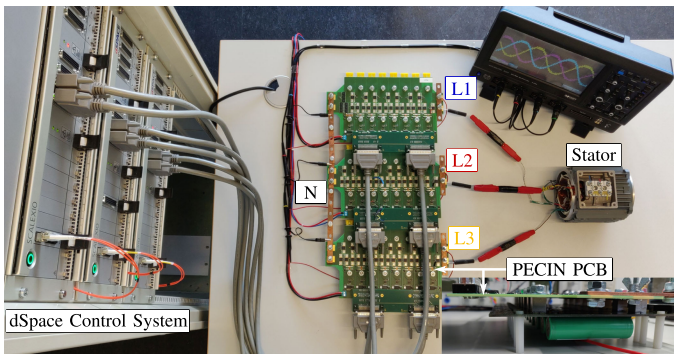


Fig. 7. Three-phase PECIN MLI test bench setup: Three 17-level PECIN MLI demonstrator boards with battery cells and dSpace control system.

control system, the newly developed PECIN board, battery cells, and a load to operate the inverter.

A. Battery Cells

Samsung INR18650-25R battery cells with a nominal capacity of 2500 mAh (4.2 V to 2.5 V, 0.2 C) are used to provide the voltage for the individual SMs as well as the energy to drive the load. They have a nominal voltage of $U_0 = 3.6$ V and a nominal dc resistance of $R_i = 28$ mΩ. The battery cells are used in the range between 3 V and 4 V. Therefore, the usable capacity is 2200 mAh.

B. Printed Circuit Board

The PECIN circuit board was designed for $N = 8$ SMs. With 17 voltage steps, the inverter, thus, has a nominal peak output voltage of 28.8 V. Enhancement mode n-channel MOSFETs of type ON Semiconductor NTMTS0D6N04CL with a nominal $R_{\mathrm{DS,on}}$ of 420 $\mu\Omega$ were used.

C. Control of PECIN MLI

A dSpace Scalexio processing unit is used to control the test stand. The control of the circuit board is implemented on a DS6602 FPGA baseboard with a Xilinx Kintex UltraScale+ KU15P FPGA. The FPGA was programmed using the dSpace toolchain and the Vivado Design Suite from Xilinx. This setup allows fundamental functions to be implemented at the logic level. NLC [25] and SVC [26] are implemented and selectable by the user during operation. In SVC, a switching frequency f_{s} in the range of 1–20 kHz can be specified. Control signals are generated for each MOSFET individually, and the PECIN circuit board is connected via a DS2655 M2 digital I/O module. A deadtime of 800 ns is used for all the switches. The value was selected empirically.

D. Measuring System

Each cell has an individual voltage and current measurement with a sampling rate of 500 kHz. The ADS7853 analog-to-digital converter from Texas Instruments can sample two measurement signals simultaneously. The cell voltage is measured directly, whereas the current sensing is implemented with a current sensing resistor. The measurement data are transferred to the FPGA via serial peripheral interface. The 24 analog-to-digital converters are triggered synchronously by the same signal. Thus, measurements of the voltage and current of single cells and measurements of the cells among each other take place simultaneously.

E. Load

The main load for the experiments is a stator of an SEW Eurodrive DRS71M2 (0.55 kW) asynchronous machine. For the evaluation of the inverter, a fixed operating point was created by removing the rotor of the electric machine, thus creating a static ohmic-inductive load. For the test setup, a winding resistance of 12.5 Ω and an inductance of 65 mH were determined by the evaluation of the current step response. 5 Ω power resistors are used as pure ohmic load, and 1 Ω 1% power resistors are used as current sense resistors for phase current measurement with an oscilloscope. A three-phase system was set up with the MLI, and the load in a star configuration with separate star points.

F. Results and Analysis

Fig. 8 depicts the resulting three-phase output voltage with $f = 50$ Hz and $U_{\mathrm{Ph,peak}} = 28.8$ V as well as the associated inductive line currents. Fig. 9 shows the corresponding amplitude spectra of current and voltage, whereby the noise was eliminated by a separate noise measurement. The amplitudes are normalized by the amplitude of the fundamental component for better visibility. The analysis shows that the THD of the current is 2.5%. MLI typical is very low and agrees with the results of [12] and [26] considering the switching frequency and the number of voltage levels used. Multiples of the third harmonic are pronounced, but their amplitudes are well below the single-digit range. The third harmonic of the fundamental component is the highest at 0.46%. This article aims to put the PECIN MLI in

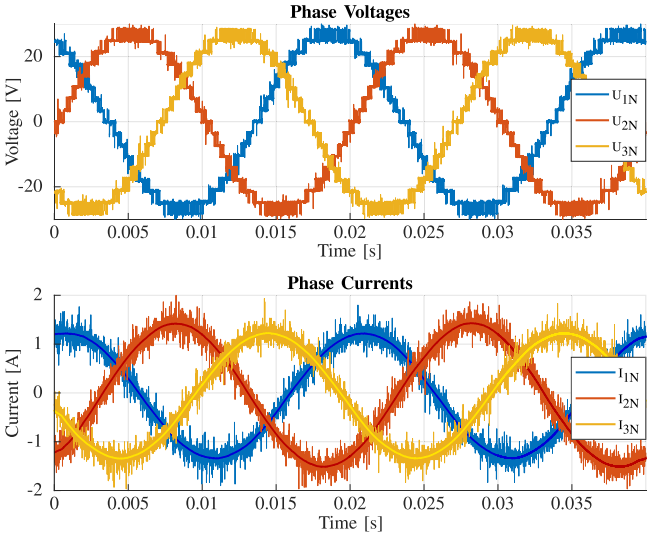


Fig. 8. Voltages and currents of the three phases of the PECIN MLI.

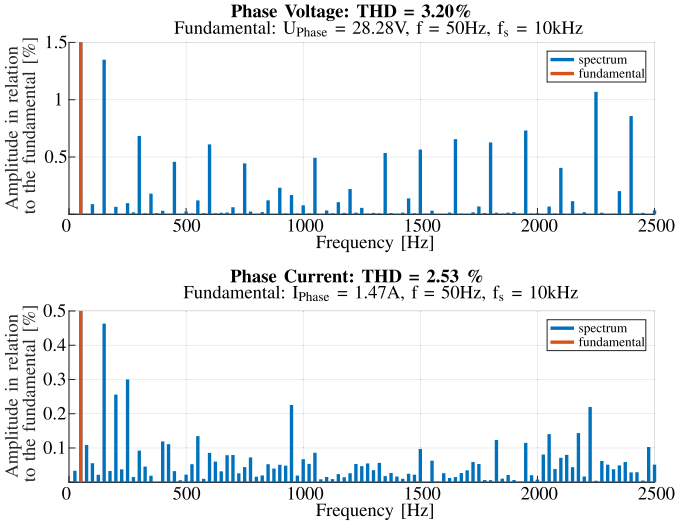


Fig. 9. Amplitude spectrum of the output voltage (top) and the inverter load current (bottom) (cf. Fig. 8) normalized to the fundamental component.

the context of other inverters published in the literature. For this reason, essential characteristics are compared in Table II. For example, the complexity and number of components of the MLI circuit design have a significant impact on the hardware design. For this reason, conceptional differences are statements on how likely an efficient circuit design is achievable. All the listed MLIs are bipolar in their output voltage and can generate $2N+1$ voltage levels. In general, a trend can be identified, whereby more functionalities require a higher number of components. However, even with the same functions, the MMSPC requires almost twice as many gate drivers and control signals as the PECIN MLI and a third more semiconductor switches. Because the MMSPC contains two separately controlled H-bridges, the MOSFET of the MMSPC requires separate housings, controls, and connections for eight switches, while the PECIN MLI operates with four. This decreases semiconductor space on the PCB.

TABLE II
IMPORTANT ATTRIBUTES OF DIFFERENT MLI TOPOLOGIES

	number of levels	serial bipolar	serial bypass	parallel bipolar	parallel bypass	total number of switches	effective switches in the load path	number of gate drivers
CHB	$2N$+1	yes	yes	no	no	$4N$	$2N$	$4N$
CS	$2N$+1	yes	no	no	no	$2N$+2	N+1	$2N$+2
CCS	$2N$+1	yes	yes	no	no	$3N$	$1.5N$	$3N$
ECIN	$2N$+1	yes	yes	no	no	$4N$+2	$\sim N$+1	$3N$+2
MMSPC	$2N$+1	yes	yes	yes	no	$8N$	$\leq N$	$8N$
M2B	$2N$+1	yes	yes	yes	yes	$9N$	$\leq 2N$	$9N$
PECIN	$2N$+1	yes	yes	yes	no	$6N$+2	$\leq N$+1	$4N$+2

Since resistance plays such an important role, the number of components in the load path is particularly significant [1]–[3]. A key differentiator is the amount of resistance added to the load path by the switching devices, as the number and internal resistance of the cells are identical for all the topologies. For better comparability of the resistance specifications, these are given as *effective switches* in the load path by multiples of a switch internal resistance. If the TU is neglected, the PECIN topology has the same number of *effective switches* in the load path as the best-in-class MMSPC topology. Furthermore, to provide similar test conditions in a comparative study, the switching frequency, the number of switching operations, and the load current can be assumed to be the same for different inverters. Therefore, the essential criterion for evaluating the efficiency of different MLI topologies is the internal resistance of the inverter. In this regard, a specific comparison of the internal resistance of different MLI topologies is given within this publication. Thus, the PECIN topology can already be classified with respect to other MLIs. In general, the internal resistance of the inverter is determined by the sum of the internal resistances of active and bypass paths, including the sum of internal resistances of active cells. Therefore, bypass paths also contribute to the internal resistance, although their SMs do not actively contribute to the output power. It is important to note that the internal resistance also includes the contributions of the internal resistances of the active cells. Thus, the contribution of the cells internal resistance to the total resistance of the phase string is variable due to reconfiguration. The parallel connection of SMs, thus, addresses two issues. On the one hand, cells are connected in parallel to reduce the network's internal resistance, especially battery cell internal resistance. On the other hand, cells permanently contribute to the load supply, avoiding inactive cells and resistances due to bypass paths. While for the purely serial reconfiguring CHB, CS, and CCS MLIs, the *effective switches* in the load path can be given unambiguously, this is not possible for the ECIN MLI, since the use of the BtB MOSFETs depends on the operating point. An exact specification is also not possible for the parallel reconfiguring MLIs. If the MMSPC is operated with purely serial reconfiguration, it has N switches in the load path. However, parallel reconfiguration can reduce this value further. Therefore, an upper limit for the *effective switches* is given for parallel reconfiguring MLIs. Since the behavior of the internal

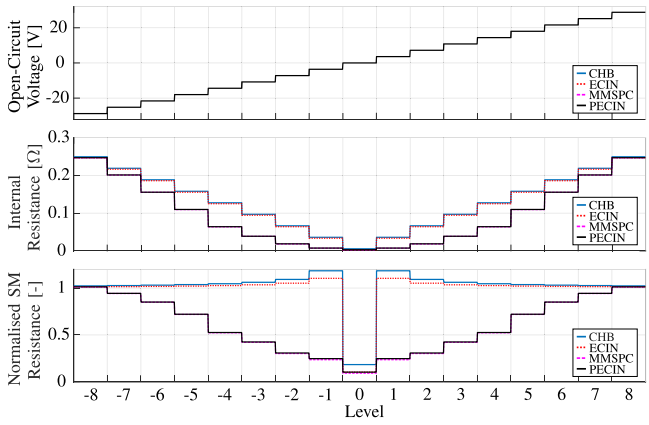


Fig. 10. Thévenin model of CHB, ECIN, MMSPC, and PECIN MLI for all the achievable output levels: OCV U_{th} (top) internal resistance R_{th} (middle) individual effective internal resistance of an SM normalized by the resistance of a single cell R_{thn} (bottom).

resistances of inverters reconfiguring in parallel is not trivial, a simulative investigation based on an example will give the reader an impression of how the internal resistance of these circuits behaves. The inverter can be seen as an adjustable voltage source for each level. Therefore, it is possible to derive the equivalent circuit model applying Thévenin's theorem. The reduced set of parameters $\{U_{\mathrm{th}}, R_{\mathrm{th}}\}$ can be used as a performance indicator for the newly developed inverter. However, Thévenin's theorem has the limitation that the losses of the derived model are not necessarily the same as those of the original system. For serial reconfiguration, the loss modeling holds even if the voltage sources are not ideal or resistances are not equal with each cell. In general, it does not hold for the PECIN or MMSPC topologies. Due to the parallelization of cells with component-related deviations, hidden equalization currents caused by internal recharges are probable. These internal currents cannot be represented by the Thévenin model. However, as a starting point, it seems sensible to represent each battery cell in the PECIN topology by the internal resistance R_i and the constant voltage source U_0. MOSFETs are represented with internal resistance $R_{\mathrm{DS,on}}$. For this equivalent circuit model, losses of the original PECIN and MMSPC circuits match the losses of their models. Fig. 10 presents the equivalent circuit model for CHB, ECIN, MMSPC, and PECIN MLI. All the inverters are made up of eight SMs and can, therefore, reach voltage levels between $+8U_{\mathrm{cell}}$ and $-8U_{\mathrm{cell}}$. In addition, the normalized effective internal resistance R_{thn} for an SM is given, which is calculated by

$$R_{\mathrm{thn}} = \frac{R_{\mathrm{th}}}{n_{\mathrm{level}} \cdot R_i}. \tag{2}$$

The OCV U_{th} is the sum of serially connected battery cells and is equal for all the models. In general, the purely serial MLIs and the MLIs with parallel reconfigurability behave similarly. Since the CHB MLI uses twice as many MOSFETs in the load path as the PECIN MLI for purely serial reconfiguration, the internal resistance of PECIN MLI is generally lower. This can be observed especially with *level 0*. The resistance of the MOSFETs is significantly smaller than the resistance of the cells. However, the effect of the additional internal resistance due to bypassed cells for CHB MLI can be seen particularly well in Fig. 10 with the smaller levels in the normalized internal resistance because many cells are bypassed here. While the internal resistance of a CHB SM in level ± 1 exceeds the internal resistance R_i of a single cell by about 20%, the PECIN MLI manages to reduce this resistance to less than a quarter of a cell resistance R_i. However, the higher the needed output voltage, the more SMs need to be connected in serial. Therefore, the resistances of CHB and PECIN MLI are converging toward higher and lower voltage levels since more and more parallel networks have to be separated into smaller parallel networks until only serial strands remain. Only at this operating point, the PECIN MLI and the MMSPC have a comparably high internal resistance as the purely serially reconfiguring ECIN and CHB MLI. However, PECIN MLI, ECIN MLI, and MMSPC always have a lower internal resistance than CHB MLI. For further analysis, the measurements of single-cell currents are presented in Fig. 11 for *serial* and *parallel modes* of the PECIN MLI. For better visibility, the NLC method is chosen, and a purely resistive load is used consisting of the 5 Ω load resistor and the 1 Ω measuring shunt. All the cells carry the total current with the *serial mode* as soon as they are switched into the load path, while parallel cells in the *parallel mode* share the current. Equalizing currents are to be expected with parallel cells. They are occurring especially with deviating cell states and low load currents and deteriorate the efficiency. To incorporate the effects of equalization currents, a relatively high standard deviation of 3% SOC was used for the test cells. If the SMs are perfectly balanced, the equalizing currents are negligible. This setup is shown with the Thévenin model in Fig. 10. However, if the cells differ in their SOC, their OCV will differ because it is a function of the SOC. In this case, balancing currents are expected in parallel cells. These currents increase with increasing SOC difference between parallel cells and low load currents and degrade the inverter's efficiency. The measured data presented in Fig. 11 were recorded with cells with the highest expectable SOC differences. This is where the highest equalizing currents occur. Therefore, it allows a worst-case evaluation of the parallel operation of the demonstrator.

For a first impression of the capability of the inverter, a loss breakdown estimation for the current demonstrator is provided in Fig. 11(c)–(f) based on power measurements on a single phase for every level in serial and parallel reconfiguration. Internal conduction losses of the battery, losses due to the internal resistance of the PCB and the MOSFET switching elements, are considered. Due to the chosen measuring points of current and voltage in the demonstrator, it is possible to measure the listed losses directly, as described in the following. It is assumed that the SOC does not change over short operating periods for the battery loss calculation. The unchanged SOC assumption is valid for a sufficiently short operating time and the used cell capacity. The resting voltage can be used to estimate the internal source voltage of the cell. The resting voltage is recorded before the start of the experiment in the cell's resting state. Therefore, a source power can be calculated during operation for every cell with the measured cell currents. Due to energy conservation, the

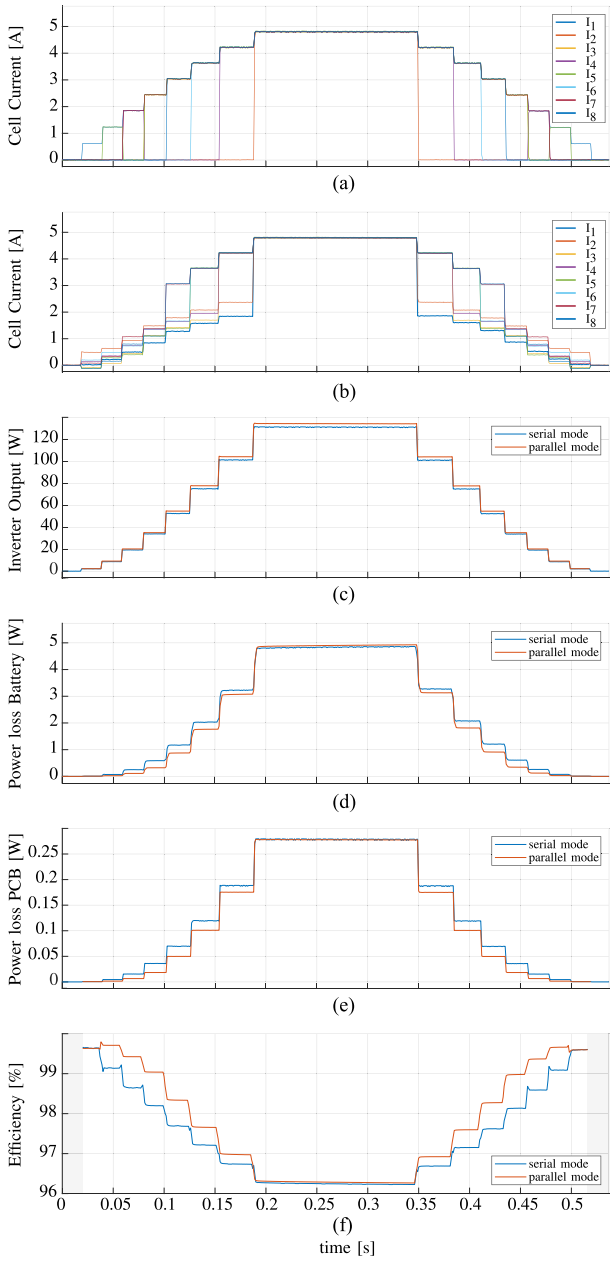


Fig. 11. Comparison of measurements of cell currents, power, and efficiency of the demonstrator for serial and parallel operation. (a) Cell currents in the serial mode. (b) Cell currents in the parallel mode. (c) Output power at the terminals of the inverter. (d) Power dissipation in the battery cells. (e) Contact losses in the PCB including MOSFETs. (f) Measured efficiency of the PECIN MLI demonstrator in serial and parallel modes.

sum of the internal cell powers is the total available power to the inverter and the input power for the efficiency calculation. If a load current flows, the terminal voltage of the cell drops. The cell's terminal voltage deviation during the operating phase from the resting voltage can, thus, be regarded as a voltage drop across internal resistances and, therefore, battery cell power loss. The terminal voltage and current are measured for every cell and used to calculate the power delivered by the cell's terminals. The sum of all the cell terminal powers is the output power of the battery system. The difference between the battery system's

TABLE III
IDENTIFIED PARAMETERS OF THE THÉVENIN EQUIVALENT CIRCUIT MODEL OBTAINED FROM THE CHARACTERIZATION EXPERIMENTS IN FIG. 12. THE PARAMETERS ARE USED FOR EFFICIENCY COMPARISON BETWEEN CHB MLI, ECIN MLI, PECIN MLI, AND MMSPC

	Q	R_i	R_1	R_2	R_3	C_1	C_2	C_3
Battery Cell	2.2 Ah	25.5 mΩ	0.1 mΩ	0.3 mΩ	4 μΩ	800 F	20 kF	90 kF

	$R_{\mathrm{DS,on}}$	R_{Gate}	U_{Dr}
MOSFET	420 μΩ	2.5Ω	10V

	R_{Cu}
PCB	700 μΩ

internal and terminal power is shown in Fig. 11(d) as the power loss of the battery. The product of terminal current and voltage of the inverter provides the output power of the inverter P_{out} shown in Fig. 11(c) as inverter output. From the difference in the terminal power of the battery system and the inverter output power, the losses in the PCB, including the losses of the MOSFET switches of the demonstrator, can be determined. These are shown in Fig. 11(e) as power loss of the PCB. In consistency with the previously performed resistance analysis, it is shown that the parallel mode further reduces losses. The efficiency can be increased even if equalization currents are present. However, in addition, deviations in the cells SOC can be efficiently minimized by methods of charge balancing control and prevented by operating strategies [4], [6], [16]. Fig. 11 shows the efficiency of the individual levels. The operating efficiency results from a value in which the entire operating period is considered, and the efficiencies of the levels are time weighted. Therefore, in the following, the PECIN MLI will be compared in terms of efficiency with the CHB MLI, the ECIN MLI, and the MMSPC in a three-phase sinusoidal operating scenario. The comparison is made simulative, using a model for the different inverter types based on the PECIN demonstrator. Therefore, it is parameterized by the measurement data obtained with the demonstrator and its component characteristics (cf. Table III).

The battery model was parameterized based on obtained measurement data. As model structure, the well-known Thévenin equivalent circuit model is chosen for the battery cells. The used model consists of an internal OCV U_{OCV}, an internal ohmic resistance R_i, and three RC elements ([R_1,C_1], [R_2,C_2], and [R_3,C_3]) connected in series (cf. [3] and [27]). The model was optimized with the pulse excitation and relaxation tests according to Fig. 12(a). For validation, the voltage response of the cell to an excitation current resulting from MLI operation, according to Fig. 8, was used. Here, the mean absolute error for the model is less than 1.5 mV. The demonstrator design was analyzed to calculate the trace resistance P_{Cu} from the used trace dimensions according to IPC-2221. As a design decision, P_{Cu} was also used for the other topologies to account for a particular inverter design. Therefore, in addition to the MOSFET contact resistance, the PCB trace resistance was added to each current path in an SM of the different topologies. The datasheet values were used to establish comparability for modeling the MOSFET switch. In contrast to the previous consideration, the switching losses are now included. The switching losses were calculated according to [2], [28], and Table III assuming the datasheet values of the demonstrator MOSFET. PECIN MLI and

TABLE IV
RESULTS OF THE EFFICIENCY ANALYSIS WITH SEPARATELY LISTED LOSS SHARES OF THE CONSIDERED LOSS MECHANISMS AND THE ACHIEVED EFFICIENCIES FOR THE COMPARED MLI TYPES AT DIFFERENT POWER REQUIREMENTS

	$\hat{I}_{1N,f0}$	1.1A		2.2A		4.3A		8.4A		16.2A		30.1A	
Output	S_{out}	46.4VA		92.7VA		185.2VA		354.9VA		663.5VA		1158.6VA	
	Q_{out}	35.4var		70.6var		141.1var		270.2var		505.3var		883.1var	
	P_{out}	**30W**		**60W**		**120W**		**230W**		**430W**		**750W**	
CHB MLI	P_V	0.38W		1.12W		4.03W		14.96W		55.84W		198.45W	
	$P_{V,Batt}$	*0.21 W*	*56.33%*	*0.85 W*	*76.12%*	*3.42 W*	*84.93%*	*13.21 W*	*88.31%*	*50.10 W*	*89.71%*	*179.54W*	*90.47%*
	$P_{V,Inv}$	*0.02 W*	*5.93%*	*0.09 W*	*7.99%*	*0.36 W*	*8.88%*	*1.37 W*	*9.17%*	*5.13 W*	*9.18%*	*17.88 W*	*9.01%*
	$P_{V,Sw}$	*0.14 W*	*37.74%*	*0.18 W*	*15.89%*	*0.25 W*	*6.18%*	*0.38 W*	*2.52%*	*0.62 W*	*1.11%*	*1.03 W*	*0.52%*
	P_{OCV}	30.38 W		61.12 W		124.03 W		244.96 W		485.84 W		948.45 W	
	η	**98.75%**		**98.17%**		**96.75%**		**93.89%**		**88.51%**		**79.08%**	
ECIN MLI	P_V	0.44 W		1.18 W		4.05 W		14.80 W		54.92 W		194.63 W	
	$P_{V,Batt}$	*0.21 W*	*49.05%*	*0.85 W*	*72.56%*	*3.42 W*	*84.46%*	*13.21 W*	*89.24%*	*50.08W*	*91.20%*	*179.36W*	*92.15%*
	$P_{V,Inv}$	*0.02 W*	*3.99%*	*0.07 W*	*5.90%*	*0.28 W*	*6.84%*	*1.06 W*	*7.18%*	*3.97 W*	*7.23%*	*13.85 W*	*7.12%*
	$P_{V,Sw}$	*0.20 W*	*46.96%*	*0.25 W*	*21.55%*	*0.35 W*	*8.70%*	*0.53 W*	*3.58%*	*0.86 W*	*1.57%*	*1.42 W*	*0.73%*
	P_{OCV}	30.44W		61.18W		124.05W		244.80W		484.92W		944.63W	
	η	**98.57%**		**98.08%**		**96.73%**		**93.95%**		**88.67%**		**79.40%**	
PECIN MLI	P_V	0.37 W		0.97 W		3.32 W		12.06 W		44.65 W		158.18 W	
	$P_{V,Batt}$	*0.17 W*	*46.61%*	*0.69 W*	*70.40%*	*2.75 W*	*82.87%*	*10.61 W*	*87.97%*	*40.22 W*	*90.07%*	*144.11W*	*91.11%*
	$P_{V,Inv}$	*0.02 W*	*4.35%*	*0.06 W*	*6.57%*	*0.26 W*	*7.70%*	*0.98 W*	*8.12%*	*3.66 W*	*8.21%*	*12.80 W*	*8.10%*
	$P_{V,Sw}$	*0.18 W*	*49.04%*	*0.22 W*	*23.03%*	*0.31 W*	*9.43%*	*0.47 W*	*3.91%*	*0.77 W*	*1.72%*	*1.26 W*	*0.80%*
	P_{OCV}	30.37 W		60.97 W		123.32 W		242.06 W		474.65 W		908.18 W	
	η	**98.79%**		**98.40%**		**97.31%**		**95.02%**		**90.59%**		**82.58%**	
MMSPC	P_V	0.36 W		0.97 W		3.30W		12.00 W		44.46 W		157.53 W	
	$P_{V,Batt}$	*0.17 W*	*47.04%*	*0.69 W*	*70.86%*	*2.75 W*	*83.28%*	*10.60 W*	*88.35%*	*40.21 W*	*90.43%*	*144.06W*	*91.45%*
	$P_{V,Inv}$	*0.02 W*	*4.20%*	*0.06 W*	*6.31%*	*0.24 W*	*7.39%*	*0.93 W*	*7.79%*	*3.50 W*	*7.87%*	*12.23 W*	*7.76%*
	$P_{V,Sw}$	*0.18 W*	*48.76%*	*0.22 W*	*22.83%*	*0.31 W*	*9.33%*	*0.46 W*	*3.87%*	*0.76 W*	*1.70%*	*1.24 W*	*0.79%*
	P_{OCV}	30.36 W		60.97 W		123.30 W		242.00 W		474.46 W		907.53 W	
	η	**98.80%**		**98.41%**		**97.32%**		**95.04%**		**90.63%**		**82.64%**	

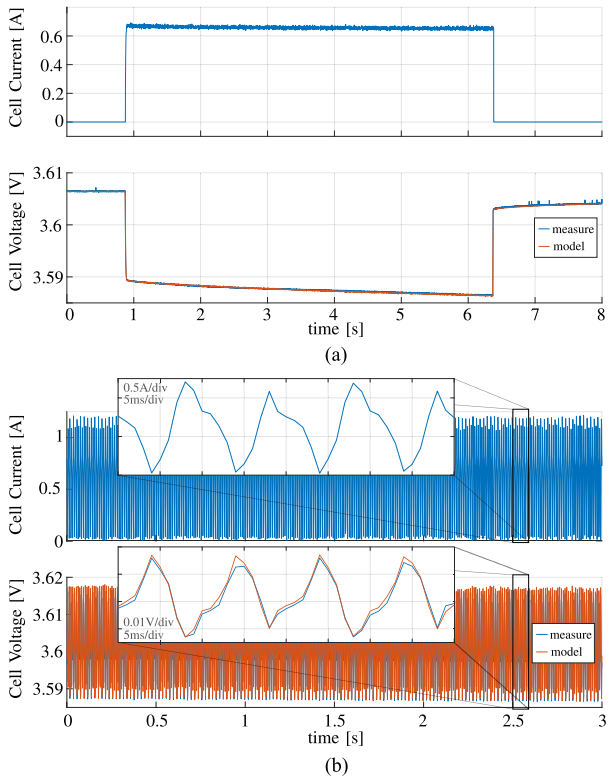


Fig. 12. Pulse characterization test to determine the parameters of the equivalent circuit model of the cell and validate the voltage response with (a) extended pulse test and (b) excitation of the cell with pulsewidth modulation according to the scenario of Fig. 8.

MMSPC are thereby operated in the parallel mode. However, the ECIN MLI corresponds to the PECIN MLI in the serial mode. The switching patterns were chosen to produce the lowest possible internal resistance for the different MLIs (cf. Section II-A). Thus, the interconnection of the cells is known, allowing all the internal electrical quantities to be calculated using the mesh current method according to [27]. Through the procedure, all currently flowing currents in the network can be calculated, and conduction and switching losses can be determined for the individual components. For the power calculation, it was considered that the MLIs are switching systems with nonsinusoidal quantities, where the reactive power contains deformed reactive power. As a basis for comparison, identical output powers are requested from the different topologies, for which the efficiencies of the individual topologies are calculated. Table IV lists the achieved performance data. $\hat{I}_{1N,f0}$ describes the amplitude of the fundamental in the current of phase 1. The power P_{out} is the power at the output terminals of the inverters. For all the cases, the three-phase output voltage is $U_{OCV} = U_{Ph,peak}$ and $f = 50\,Hz$, using the SVC method with 10 kHz. For the experiments, a phase angle of 48° inductive applies between the fundamental wave of the phase voltage and the fundamental wave of the phase current. Thus, case 1.1A is comparable to Fig. 8. It is found that the parallel reconfiguring MLIs generally have higher efficiencies than the serial reconfiguring MLIs. In addition, it can be seen that parallel connection helps to keep the efficiency high even for higher powers. The PECIN MLI behaves very similarly to the MMSPC and is in no way inferior to it, despite the additional switch in the TU. Although the CHB MLI has one more switch per SM than the ECIN MLI, this is not directly significant for this demonstrator comparison because the conduction losses through the PCB account for a significant portion. If the different loss mechanisms are evaluated, the conduction losses account for the most significant part of the losses for all the inverter variants. This holds especially true for higher powers. Conduction losses through the PCB of the current demonstrator are not negligible and should be optimized in future demonstrators. In particular, for MLIs with several levels, switching loss is a loss mechanism that can be further reduced since the THD is inherently good due to the stepped fine replica of the desired output voltage. The investigations have shown that the minimization of the series resistance and the parallel connection can increase inverter efficiency. In future work, an improved demonstrator version for high-power applications will be built. It allows an efficiency analysis to be carried out for high-power traction applications. In addition to the understanding of the topology, operation strategies will be investigated to control the PECIN MLI optimally.

IV. CONCLUSION

This article introduced the PECIN MLI. The design process is presented based on an overview of well-known MLI circuits from the literature. The comparison of different topologies has shown that the circuit design significantly influences the performance of an MLI. In particular, a minimum internal resistance is the decisive point for an efficient MLI. Three critical factors

are identified in this context: intrinsic commutation capability, the SMs' lowest possible internal resistance, and serial–parallel reconfigurability. In addition, the bypass capability of individual cells and a low total number of electronic components have been identified as advantageous properties. The inverter is designed based on these attributes and combines all of them in one efficient circuitry. Fundamental control of the inverter is shown in terms of safety issues, basic switching patterns, and the generation of string voltages. A test stand was presented using a 17-level demonstrator that was operated to prove the function of the novel inverter. A simulative study has shown that parallel reconfiguration addresses two issues. On the one hand, it avoids bypass resistances, and on the other hand, it reduces the contribution of internal cell resistances. The inverter efficiency considerations are supported by measurements on the prototype, making the proposed inverter an interesting topology to investigate further.

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REFERENCES

[1] M. Quraan, P. Tricoli, S. D'Arco, and L. Piegari, "Efficiency assessment of modular multilevel converters for battery electric vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2041–2051, Mar. 2017, doi: 10.1109/TPEL.2016.2557579.

[2] C. Korte, E. Specht, M. Hiller, and S. Goetz, "Efficiency evaluation of MMSPC/CHB topologies for automotive applications," in *Proc. IEEE 12th Int. Conf. Power Electron. Drive Syst.*, 2017, pp. 324–330, doi: 10.1109/PEDS.2017.8289145.

[3] A. Kersten et al., "Inverter and battery drive cycle efficiency comparisons of CHB and MMSP traction inverters for electric vehicles," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. P.1–P.12, doi: 10.23919/EPE.2019.8915147.

[4] L. Komsiyska et al., "Critical review of intelligent battery systems: Challenges, implementation, and potential for electric vehicles," *Energies*, vol. 14, no. 18, 2021, Art. no. 5989, doi: 10.3390/en14185989.

[5] R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent 3 867 643, Feb. 1975.

[6] A. El-Hosainy, H. A. Hamed, H. Z. Azazi, and E. E. El-Kholy, "A review of multilevel inverter topologies, control techniques, and applications," in *Proc. 19th Int. Middle East Power Syst. Conf.*, 2017, pp. 1265–1275, doi: 10.1109/MEPCON.2017.8301344.

[7] J. Venkataramanaiah, Y. Suresh, and A. K. Panda, "A review on symmetric, asymmetric, hybrid and single dc sources based multilevel inverter topologies," *Renewable Sustain. Energy Rev.*, vol. 76, pp. 788–812, 2017, doi: 10.1016/j.rser.2017.03.066.

[8] T. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. 23rd Annu. IEEE Power Electron. Spec. Conf.*, 1992, vol. 1, pp. 397–403, doi: 10.1109/PESC.1992.254717.

[9] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA- 17, no. 5, pp. 518–523, Sep. 1981, doi: 10.1109/TIA.1981.4503992.

[10] F. Helling, J. Glück, A. Singer, H.-J. Pfisterer, and T. Weyh, "The ac battery a novel approach for integrating batteries into ac systems," *Int. J. Elect. Power Energy Syst.*, vol. 104, pp. 150–158, 2019, doi: 10.1016/j.ijepes.2018.06.047.

[11] K. Sang-Hoon, "Pulse width modulation inverters," in *Electric Motor Control*. New York, NY, USA: Elsevier, 2017, ch. 7, pp. 265–340.

[12] G. Singh and V. K. Garg, "THD analysis of cascaded H-bridge multi-level inverter," in *Proc. 4th Int. Conf. Signal Process., Comput. Control*, 2017, pp. 229–234, doi: 10.1109/ISPCC.2017.8269680.

[13] R. Mahalakshmi and K. S. Thampatty, "Grid connected multilevel inverter for renewable energy applications," *Procedia Technol.*, vol. 21, pp. 636–642, 2015, doi: 10.1016/j.protcy.2015.10.076.

[14] A. Emadi, *Advanced Electric Drive Vehicles*, 1st ed. Boca Raton, FL, USA: CRC Press, 2014.

[15] F. Helling, J. Glück, A. Singer, and T. Weyh, "Modular multilevel battery (M2B) for electric vehicles," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, 2016, pp. 1–9, doi: 10.1109/EPE.2016.7695480.

[16] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, "Control of modular multilevel converter with parallel connectivity—Application to battery systems," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8381–8392, Nov. 2017, doi: 10.1109/TPEL.2016.2645884.

[17] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf. Proc.*, 2003, vol. 3, p. 6, doi: 10.1109/PTC.2003.1304403.

[18] M. F. Kangarlu and E. Babaei, "Cross-switched multilevel inverter: An innovative topology," *IET Power Electron.*, vol. 6, no. 4, pp. 642–651, 2013, doi: 10.1049/ietpel.2012.0265.

[19] M. F. Kangarlu, E. Babaei, and M. Sabahi, "Cascaded cross-switched multilevel inverter in symmetric and asymmetric conditions," *IET Power Electron.*, vol. 6, pp. 1041–1050, 2013, doi: 10.1049/iet-pel.2012.0563.

[20] C. Terbrack, J. Stöttner, and C. Endisch, "Operation of an externally excited synchronous machine with a hybrid multilevel inverter," in *Proc. 22nd Eur. Conf. Power Electron. Appl.*, 2020, pp. 1–12, doi: 10.23919/EPE20ECCEEurope43536.2020.9215895.

[21] J. Rodriguez and S. Leeb, "A multilevel inverter topology for inductively-coupled power transfer," in *Proc. 18th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2003, vol. 2, pp. 1118–1126, doi: 10.1109/APEC.2003.1179357.

[22] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008, doi: 10.1109/TPEL.2008.2005192.

[23] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel module connectivity: Topology and control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 203–215, Jan. 2015, doi: 10.1109/TPEL.2014.2310225.

[24] K. K. Gupta and S. Jain, "Topology for multilevel inverters to attain maximum number of levels from given DC sources," *IET Power Electron.*, vol. 5, pp. 435–446, 2012, doi: 10.1049/iet-pel.2011.0178.

[25] Kamaldeep and J. Kumar, "Switch reduction and performance analysis using different modulation technique in multilevel inverter," in *Proc. IEEE 1st Int. Conf. Power Electron., Intell. Control Energy Syst.*, 2016, pp. 1–4, doi: 10.1109/ICPEICES.2016.7853068.

[26] H. Zhang, Y. Meng, L. Ning, Y. Zou, X. Wang, and X. Wang, "Fast and simple space vector modulation method for multilevel converters," *IET Power Electron.*, vol. 13, pp. 14–22, 2020, doi: 10.1049/iet-pel.2019.0264.

[27] T. Bruen and J. Marco, "Modelling and experimental evaluation of parallel connected lithium ion cells for an electric vehicle battery system," *J. Power Sources*, vol. 310, pp. 91–101, 2016, doi: 10.1016/j.jpowsour.2016.01.001.

[28] D. Graovac, M. Puerschel, and A. Kiep, *MOSFET Power Losses Calculation Using the Data-Sheet Parameters* (Application note). München, Germany: Infineon Technol. AG, 2016.

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