Comparisons of Two Turn-off Failures Under Clamped Inductive Load in Planar FS 3.3 kV/50 A IGBT Chip

Jiayu Fan, Yaohua Wang, Feng He, Mingchao Gao, Zhibin Zhao, Xuebao Li, Xiang Cui, *Senior Member, IEEE*, and Zhong Chen

***Abstract*—Turn-OFF failure under clamped inductive load, is one of the most concerns in insulated gate bipolar transistor (IGBT) chips. Besides, this turn-OFF failure can be attributed to two causes, i.e., the dynamic latch-up and the secondary breakdown. Despite great simulation work investigated previously, the experimental research should be further focused. Up to now, the typical features and differences for these two turn-OFF failures still remain unclear. In this article, two failures' waveforms are first compared in experiment. Moreover, their internal current, electric field, and temperature distributions are compared by simulation in detail. Then, two different failure features, focusing on the failure cell structures, are summarized from the scanning electron microscope (SEM) results for the first time. The marked signatures of these failures, such as the current filament path and the mixture region, are further analyzed in this article. According to the SEM results, the lateral and vertical current paths can be observed in dynamic latch-up chip and secondary breakdown chip, respectively. These failure signatures in waveforms and SEM results can contribute to the distinguished method to the failure causes in IGBT device, and enhance the chip's performance more effectively.**

***Index Terms*—Distinguished method, dynamic latch-up, insulated gate bipolar transistor (IGBT), marked signatures, secondary breakdown.**

I. Introduction

INSULATED gate bipolar transistor (IGBT) devices are widely used in the renewable power system, the electric vehicles, and the aerospace industry [1]. In light of the extreme thermo-electrical stress, high current capability is required during IGBT chip turned OFF under clamped inductive load (CIL). Meanwhile, turn-OFF failures under CIL are one of the most common failure modes in the actual application [2], [3]. Therefore, the reverse bias safe operation area (RBSOA) is considered as one of the most important performances in IGBT devices [4]. The investigations about turn-OFF failures, can not only enhance chip's property, but also help to distinguish the failure cause in engineering [5]. The relevant physics of failure contributes to the device aging evaluation and health management as well [6]. Up to now, many detection approaches have been proposed on the bond wire faults in IGBT devices [7], [8], but there are few methods to distinguish the turn-OFF failures under CIL in IGBT devices.

Hence, more experimental researches should be focused on the turn-OFF failures in IGBT chip under CIL, since great simulations have been studied extensively. Especially for the comparisons of different failure causes, their features and marked signatures still remain unclear so far.

The device manufactures have made great efforts to improve device's RBSOA performance. In 2001, based on the semiconductor numerical simulation, Yoshikawa *et al.* [9] at Fuji Electric analyzed the impact ionization rates in IGBT chips with different concentration profiles. He investigated the relationships between the RBSOA and the gate resistance as well. In 2004, Rahimo *et al.* [10] at ABB Switzerland Ltd., first demonstrated the IGBT devices with switching-self-clamping-mode (SSCM). It was shown that the turn-OFF capability could be extend over three times rated current with low losses. Since then, Rahimo [11] summarized the future trends in IGBT devices in 2013, he proposed that the RBSOA margins and the SSCM played an important role for developing the high temperature operation and integration. Besides, Ogura *et al.* [12] at Toshiba Microelectronic Center researched the turn-OFF destruction mechanism in high-voltage IGBT devices in 2004. The analytical model considering dynamic avalanche generation explained the relation between the RBSOA and gate conditions in IGBT chip. Moreover, the device manufactures, like Infineon and Dynex, have put forward their novel IGBT structures to enhance chips' RBSOA performances successively [13], [14]. In 2016, Shiba *et al.* [15] studied the current filament during IGBT's turn-OFF process by semiconductor numerical simulation, and reported the simulation setting. The current filament was regarded as the vital

Manuscript received 8 May 2022; revised 11 July 2022; accepted 18 July 2022. Date of publication 21 July 2022; date of current version 6 September 2022. This work was supported by the National Natural Science Foundation of China-State Grid Corporation Joint Fund for Smart Grid under Grant U1766219. Recommended for publication by Associate Editor B. Shao. *(Corresponding authors: Xuebao Li; Yaohua Wang.)*

Jiayu Fan, Zhibin Zhao, Xuebao Li, and Xiang Cui are with the State Key Laboratory of Alternate Electrical Power System With Renewable Energy Sources, North China Electrical Power University, Beijing 102206, China (e-mail: fanjiayu@ncepu.edu.cn; zhibinzhao@ncepu.edu.cn; lxb08357x@ncepu.edu.cn; x.cui@ncepu.edu.cn).

Yaohua Wang, Feng He, and Mingchao Gao are with the State Key Laboratory of Advanced Power Transmission Technology, Beijing Institute of Smart Energy, Beijing 102211, China (e-mail: wangyaohua@geiri.sgcc.com.cn; hefeng@geiri.sgcc.com.cn; gaomingchao@geiri.sgcc.com.cn).

Zhong Chen is with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA (e-mail: chenz@uark.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3192922.

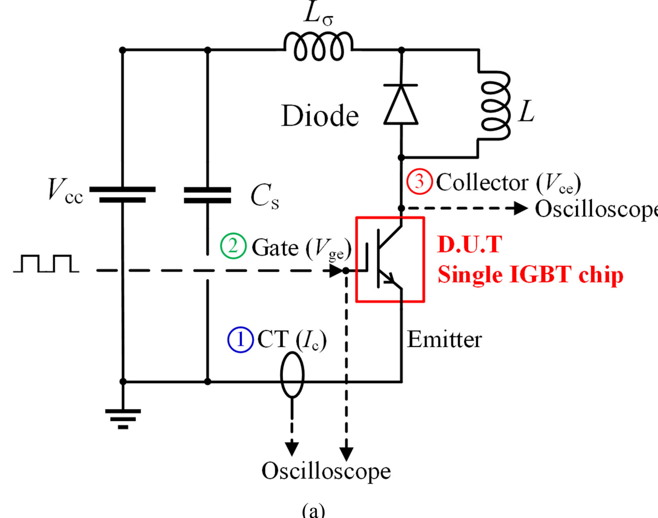
Digital Object Identifier 10.1109/TPEL.2022.3192922

signature in the turn-OFF failures, which limited the RBSOA of IGBT chip. Based on the detailed simulation analysis, the chip performance can be improved effectively. Nevertheless, the shortcoming of the IGBT devices can be unearthed after using in the practical use, especially for the CIL with high current, which is one of the most extreme conditions in engineering.

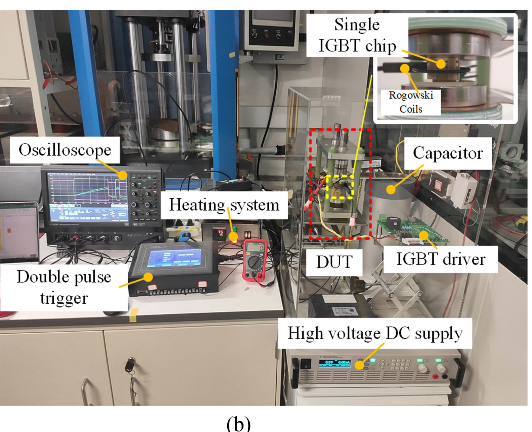
As for the IGBT's users, it is vital to distinguish the turn-OFF failure causes. In 1998, Trivedi and Shenai [5] at the University of Illinois studied the turn-OFF failure in IGBTs under CIL by simulation. According to his analysis, the avalanche multiplication was the main reason that leads IGBT device's turn-OFF failure. Since then, he compared the turn-OFF failures between the CIL and the short circuit. Because the overheated areas were different in CIL and short-circuit, their performances and concentration profiles ought to be optimized respectively [16]. In 2007, Castellazzi *et al.* [17] at ETH Zurich proposed a IGBT model, which included the self-heating effects and the parasitic *n–p–n* bipolar junction transistor (BJT). The simulation results showed that the current imbalance internal the parallel IGBT chips would lead to the dynamic latch-up failure during the turn-OFF period. In 2011, Perpiñà *et al.* [18], [19] at the Institute of Microelectronics of Barcelona confirmed that there were two different failures causes during IGBT turned OFF under CIL, which were the dynamic latch-up and the secondary breakdown. These two failure causes were firstly compared by simulation, whereas the experimental comparisons still need further attention. Moreover, it was found that not only the cell structure, but also the gate runner layout would affect the current crowding among cells internal the IGBT chip [20]. After that, they designed the new layout for the active region and terminal region, to optimize the electric field and temperature distributions in the IGBT chip [21], [22].

At present, two turn-OFF failure causes in IGBT chip under CIL have been investigated extensively. However, the features and marked signatures of these turn-OFF failures are unknown. Considering the physical processions are too complex to study by numerical simulation, it is still a challenge to carry out the failure analysis after the failures. For example, the detailed comparisons for these failures' waveforms are lacking. After the turn-OFF failure occurs, a more direct experimental method is needed, to observe the failure characteristics in chips and distinguish the failure causes. Therefore, the work in this article provides a good supplement for IGBT device's turn-OFF failure. The conclusions in this article make a deeper understanding to the turn-OFF failure in IGBT chip under CIL, and further contribute to distinguish failure causes.

In this article, the experimental setup and the simulation conditions are firstly introduced in Section II. Second, the two failures' waveforms and mechanisms are systematically compared in Section III. Then, the failure features observed by scanning electron microscope (SEM), as well as their internal thermoelectrical conditions are analyzed in Section IV, respectively. Meanwhile, the marked signatures in SEM results like current filament path and mixture region size are summarized in detail. Finally, according to the IGBT failure waveforms and failure cells structures, the distinguished methods to the failure causes in IGBT chip under CIL are put forward for the first time in Section V.



(a)



(b)

Fig. 1. IGBT's RBSOA platform. (a) Equivalent circuit. (b) Photography [23].

II. Experiment Setup and Simulation

A. Measurement Setup

The equivalent circuit of the RBSOA platform is shown in Fig. 1(a). The device under test is the planar field-stop (FS) IGBT chip, whose rated parameters are 3.3 kV and 50 A, respectively. To further carry out the SEM scanning conveniently, these chips are packaged as press pack IGBT chips. The dc-link voltage is determined by the dc source and the capacitor (C_s), and the inductance load (L) is 0.72 mH. Besides, the free-wheeling diode is DZ950N44K, whose rated parameters for voltage and current are 4.4 kV and 950 A. Meanwhile, the collector voltage V_{ce} and gate voltage V_{ge} are measured by the high-voltage probe PINTECH P6028A (200 MHz, −3 dB) and the high-voltage probe LeCroy PP026 (500 MHz, −3 dB), respectively. The load current I_c is measured by the Rogowski Coil CWT Mini (30 MHz, −3 dB) [23].

In Fig. 1(b), it is displayed that the thermostat determines the chip's temperature T_j. The load current I_c that IGBT chip turns OFF can be adjusted by the single pulse trigger. In general, the current limit of the IGBT chip is several times as much as its rated current (50 A). Whereas, this limits of each IGBT chip are different due to the non-ideal chip parameters. At $V_{ce} = 2.5$ kV,

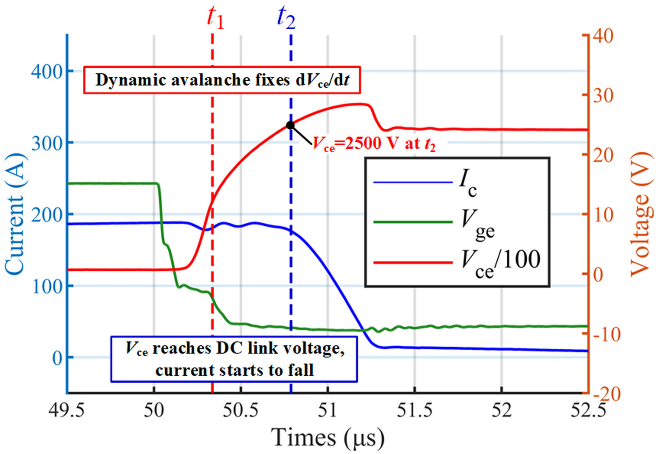


Fig. 2. Typical turn-OFF waveforms of the IGBT chip under CIL ($V_{ce} = 2.5$ kV, $I_c = 190$ A, $R_g = 5\ \Omega$, and $T_j = 150$ °C).

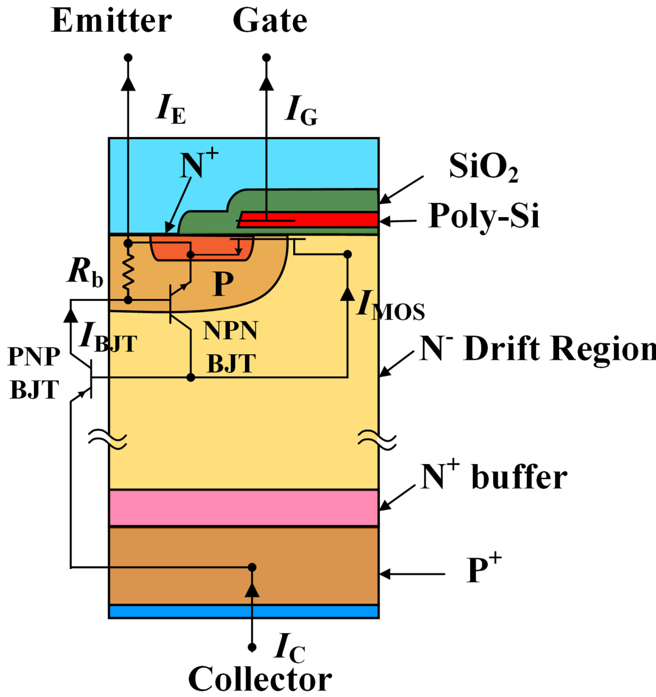


Fig. 3. Schematic cross section view of the FS IGBT cell [19].

$R_g = 5\ \Omega$, $T_j = 150$ °C, the current limit in this article is in the range of 150–190 A. Based on this RBSOA platform, the typical turn-OFF waveforms under CIL with 190 A load current are demonstrated in Fig. 2.

As shown in Fig. 2, the dc-link voltage is set as 2.5 kV, and the load current is 190 A. Besides, the gate resistance R_g is 5 Ω, and the chip temperature T_j is 150 °C. In such overload conditions, the electrothermal interactions in the IGBT chip is intense. During the turn-OFF period, the voltage slope dV_{ce}/dt changes at t_1, which indicates the dynamic avalanche occurs internal the IGBT chip. Meanwhile, the collector current is almost constant before t_2. At this period, although the collector voltage is lower than 2.5 kV, the overcurrent might lead IGBT chip failure. After that, when the collector voltage V_{ce} reaches the dc-link voltage, the collector current starts to fall at t_2. The load current is switched to the free-wheeling diode branch. At this moment, the electric field peak and the accumulated heat are still harmful to the IGBT chip. Then, the turn OFF period of the IGBT chip ends with the voltage overshoot and current tail.

B. IGBT Model and Cell Structure

The internal current, electric field, and temperature distributions are analyzed by the two-dimensional (2-D) semiconductor numerical simulation in this article. The circuit in the simulation is shown in Fig. 1(a), which is the same as the experiment equivalent circuit. The schematic cross-sectional view of the FS IGBT cell is demonstrated in Fig. 3 [19].

In Fig. 3, it is shown that there are *p–n–p* BJT and MOS structures in the IGBT cell, which realizes the voltage control and bipolar device at the same time. Meanwhile, the parasitic *n–p–n* BJT is inevitably brought in. The latch-up phenomenon will take place when the voltage drop across the base resistance R_b is greater than activation voltage V_{bi}. When the latch-up occurs, the high current density under the high electric field and high temperature destroys the cell and the whole chip instantaneously. Besides, in the IGBT cell, the collector voltage V_{ce} is sustained by the P well/N^-drift junction. With the increasing of the temperature and current density, the impact ionization and the avalanche multiplication are enhanced, which might lead this junction breakdown.

The latch-up and the junction breakdown are labeled as dynamic latch-up and the secondary breakdown during IGBT turned OFF, respectively. It is indicated that the dynamic latch-up failure and secondary breakdown failure are more likely to happen at high temperatures. Therefore, the temperature dependencies in the IGBT chip should be considered in the simulation. The self-heating model, thermal insulation boundary, and the impact ionization model are added as well.

The physical parameters for the IGBT chip in the simulation have been adjusted to match its static and dynamic characteristics. Meanwhile, the IGBT chip is set as the thermal insulation, and the initial temperature is set as 150 °C (423 K). In the simulation, the load current I_c is 150 A, the dc-link voltage is 2.5 kV, and the gate resistance R_g is 5 Ω, respectively. According to the simulation results, the current, electric field, and temperature distributions internal the IGBT chip are analyzed. Based on the 2-D simulation, the different trigger conditions of two turn-OFF failures are compared in detail, which are consistent with the SEM results in Section IV.

III. Failure Mechanisms Under CIL in IGBT Chip

In this section, the dynamic latch-up failure and secondary breakdown failure are compared by experiment for the first time. In 2007, Castellazzi *et al.* [17] at ETH proposed the IGBT model to investigate the dynamic latch-up failure in the IGBT devices. Whereas, the relevant experiment research, especially for single IGBT chip, is lacking. Up to now, the experiment research on the dynamic latch-up failure, as well as the comparisons between these two failures, have not been reported yet.

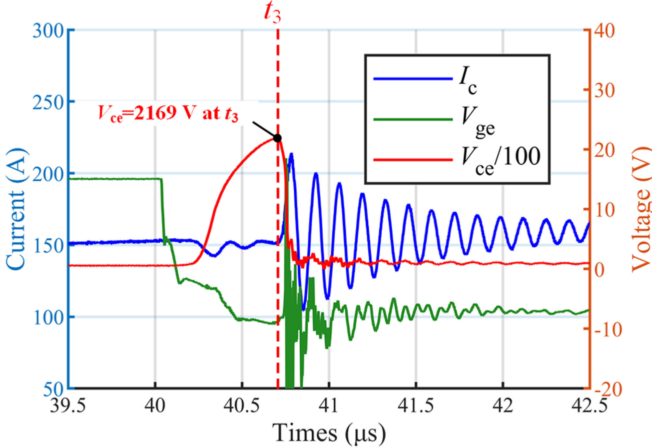


Fig. 4. Typical experiment waveforms of IGBT's dynamic latch-up failure ($V_{ce} = 2.5$ kV, $I_c = 150$ A, $R_g = 5\ \Omega$, and $T_j = 150$ °C).

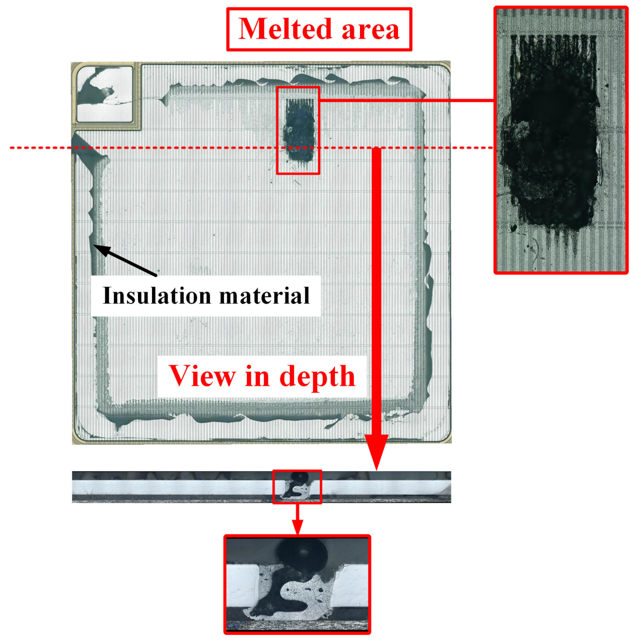


Fig. 5. Photography of the dynamic latch-up IGBT chip's active region.

A. Dynamic Latch-Up Failure

Based on the platform, the typical experiment waveforms of IGBT's dynamic latch-up failure are shown in Fig. 4.

In Fig. 4, the dc-link voltage is 2.5 kV, the load current is 150 A, the gate resistance is 5 Ω, and the chip temperature T_j is set as 150 °C. It is shown that the highest collector voltage V_{ce} reaches 2169 V at t_3, which is less than the dc-link voltage. Therefore, the collector current increases over 220 A rather than falling. After t_3, the oscillations in collector voltage, load current and gate voltage are observed, which indicates the failure occurs. In light of the parasitic *n–p–n* BJT, the dynamic latch-up failure in IGBT chip occurs when the voltage drop across the base resistance R_b is over the activation voltage V_{bi}. The activation voltage V_{bi} can be expressed as

$$V_{bi} = R_b(I_P + I_{\mathrm{DIS}}) \tag{1}$$

where $\mathrm{I_P}$ is the hole current component, and I_{DIS} is the corresponding displacement current component.

Besides, the base resistance $\mathrm{R_b}$ can be written as

$$R_b = \frac{1}{q\mu_P N_A}\frac{L_P}{Z} \tag{2}$$

where q is the elementary charge, μ_P is the hole carrier mobility, N_A is the acceptor concentration in the P well region, L_P and Z are the lateral current flow path and cross section, respectively. The hole current component I_P is related to the load current I_c, and the displacement current component I_{DIS} is proportional to the voltage slope dV_{ce}/dt. Compared with the waveforms in Fig. 2, the dynamic latch-up failure in IGBT chip is more likely to happen at the initial stage of the turn-OFF period, before the collector current starts to fall. Furthermore, the failure waveforms in Fig. 4 are consistent with the simulation results in [17], which confirms that the IGBT failure in Fig. 4 belongs to the dynamic latch-up failure.

It should be noted that Cortes *et al.*[21], [22] reported the dynamic latch-up failure in the IGBT devices, which occurred when the collector current was falling. It is because that the hole current component I_P in (1) can be generated by the avalanche multiplication as well. This special phenomenon is led by the high electric field strength, which is located at junction between the active region and the terminal region.

For most typical dynamic latch-up failure, its waveforms are similar to the ones shown in Fig. 4, which is the focus in this article as well. Due to the dynamic latch-up failure takes place at the position which is close to the chip's surface, it is inferred that the melted area in the IGBT chip is relatively shallow. Besides, the photography of the IGBT chip after the dynamic latch-up failure is displayed in Fig. 5.

According to the top view of the IGBT chip, it can be seen that the evident melted area on the surface of the IGBT chip. While, the melted area is a through-hole in the cross section view. Therefore, it is no longer effective to distinguish the failure causes by the melted areas depths, and more detailed signatures should be investigated to obtain the typical features of the dynamic latch-up failure in IGBT chip.

B. Secondary Breakdown Failure

Correspondingly, the typical experiment waveforms of IGBT's secondary breakdown failure are displayed in Fig. 6.

As displayed in Fig. 6, the collector voltage V_{ce} rises to its maximum at t_4, and the load current drops to its minimum at the same time. After that, the current increases to 432.5 A rather than reducing to zero, and the voltage can no longer be sustained. Meanwhile, the oscillation in the gate voltage waveform can be observed, which indicates the IGBT's turn-OFF failure.

At IGBT's turn-OFF period, the collector voltage V_{ce} is sustained by the P well/ N^{-}drift junction, and the electric field peak is close to this PN junction as well. According to the semiconductor physics, the electric field can be written as

$$\mathrm{div}\ \boldsymbol{E} = \frac{q}{\varepsilon_{Si}}(N_D - N_A + p - n) \tag{3}$$

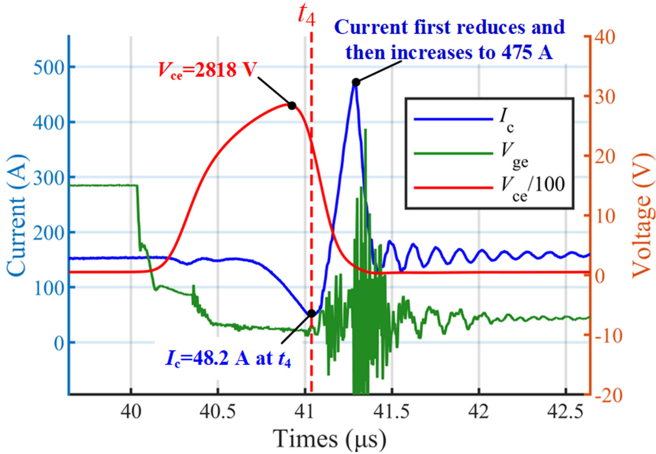


Fig. 6. Typical experiment waveforms of IGBT's secondary breakdown failure ($V_{ce} = 2.5$ kV, $I_c = 170$ A, $R_g = 5\ \Omega$, and $T_j = 150$ °C).

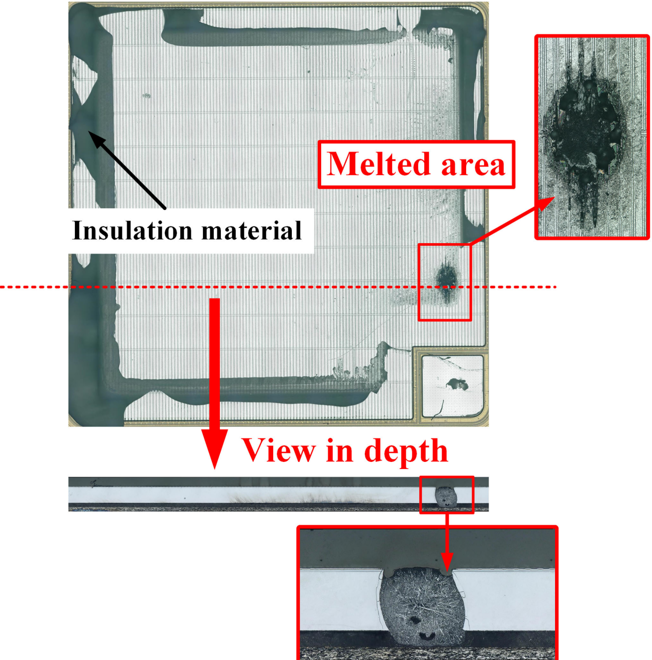


Fig. 7. Photography of the secondary breakdown IGBT chip's active region.

where $\boldsymbol{E}$ is the electric field, ε_{Si} is the dielectric constant of silicon, N_D is the donor concentration, p is the hole carrier concentration, and n is electron carrier concentration.

At the turn-OFF period, the carriers present into the P well/N^-drift junction are the holes. Therefore, (3) can be simplified as

$$\text{div}\ \boldsymbol{E} = \frac{q}{\varepsilon_{Si}}\left(N_D + \frac{J_P}{qv_{\text{sat}}}\right) \tag{4}$$

where J_P is the hole current density, v_{sat} is the hole saturation velocity. Moreover, since the carriers in the depletion region are hole carriers, the hole current density J_P is equal to the load current density J_C, that is

$$\text{div}\ \boldsymbol{E} = \frac{q}{\varepsilon_{Si}}\left(N_D + \frac{J_C}{qv_{\text{sat}}}\right). \tag{5}$$

Then, the breakdown voltage BV_{RBSOA} in the depletion region can be expressed as

$$BV_{\text{RBSOA}} = \frac{5.34 \times 10^{13}}{\left(N_D + \frac{J_C}{qv_{\text{sat}}}\right)^{3/4}}. \tag{6}$$

The breakdown voltage BV_{RBSOA} is related to the impact ionization. According to (4) and (6), it is indicated that the hole carriers generated by impact ionization will strength the electric field peak, and further lower the breakdown voltage. The generation G by impact ionization can be simplified as

$$G = \frac{1}{q}\left(\alpha_n\left|J_n\right| + \alpha_p\left|J_p\right|\right) \tag{7}$$

where α_n and α_p are the electron and hole ionizations, J_n and J_p are the electron and hole current density, respectively. The carrier ionizations can be expressed as

$$\alpha_n, \alpha_p = A\exp[-(b/E)] \tag{8}$$

where the constant values in silicon semiconductors are given as $A = 3.80 \times 10^6$ cm^{-2}, $b = 1.75 \times 10^6$ V/cm for electron carriers, and $A = 2.25 \times 10^7$ cm^{-2}, $b = 3.26 \times 10^6$ V/cm for hole carriers.

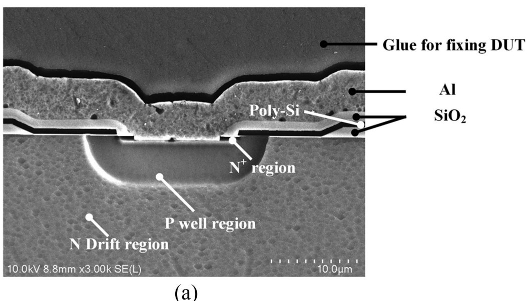
According to (5) and (6), the electric filed peak internal the IGBT chip is related to the load current. Therefore, when the dc-link voltage increases under the CIL, the current limit will decrease for the secondary breakdown failure. It is shown in (7) and (8) that the generation component G is increasing with the current density and the electric field. Then, the generation carriers will further enhance the electric field peak. Therefore, the positive feedback between the carrier concentration and electric field leads the secondary breakdown failure during the turn-OFF period. The photography of the secondary breakdown IGBT chip is shown in Fig. 7.

It was reported in 2011 that the depth of the melted area in the secondary breakdown was 50 μm [19]. However, in this article, the experiment results show there is a through-hole in the cross section view, which is similar as the one in Fig. 5.

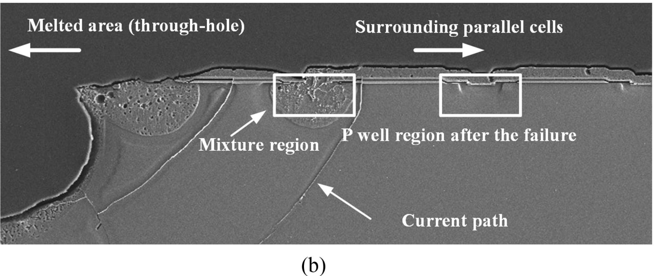
In short, it is shown that the cross section of the failure IGBT chips are similar, which might not distinguish the failure causes effectively. Whereas, according to the failure waveforms, it is indicated that the typical dynamic latch-up failure happens at the initial stage of the turn-OFF period. At that time, the collector voltage does not reach the dc-link voltage due to the activation of the parasitic n–p–n BJT. As for the secondary breakdown failure, it is demonstrated in Fig. 6 that the collector current first reduces, and then increases after the failure occurs. Furthermore, although the through-hole cannot provide more information about the failure causes, more detailed features for the failure IGBT chips can be further investigated by SEM analysis.

IV. Failure Signatures Observed By SEM Analysis

Since the cross section views in both failure chips are similar, more signatures should be investigated. For example, typical SEM results for the failure chip cells are shown in Fig. 8.



(a)



(b)

Fig. 8. SEM results for the IGBT chip. (a) IGBT cell. (b) Failure structures.

The relatively complete IGBT cell is displayed in Fig. 8(a). The gate oxide structures and the doping concentration profiles are shown in Fig. 8(a). According to the principle of SEM, the darker region in SEM results represents the higher doping concentration. Therefore, the darkest region in Fig. 8(a) corresponds the N^+ region in Fig. 3. It is shown that there is a through-hole in the failure IGBT chip, which is on the left of the Fig. 8(b). Besides, although the surrounding cells failed, their structures remain relatively complete. Moreover, the damage degree of these parallel cells decreases with the increasing distance from the melted area.

Due to the electrothermal effect during the turn-OFF period, it is difficult to analyze failure procession internal the IGBT chip. Whereas, more information can be obtained by the failures' SEM results. Meanwhile, the simulation at turn-OFF period can provide the auxiliary explain to the observation results. After comparing nearly 100 failure cell structures, the failure signatures, including their differences and similarities, are investigated in detail in Section IV.

A. Dynamic Latch-Up Failure

After comparing the failure cells in five chips, ten typical failure features after dynamic latch-up failure are summarized from nearly one hundred cells, which are shown in Fig. 9.

According to the SEM results, for the IGBT cell which is closer to the melted area, there are more heats and higher carrier concentration during the turn-OFF period. Meanwhile, it is well-known that there are complex relationships between the electric field and heats in the failure processing, which is difficult to simulate. In light of the different carrier concentrations and thermal conditions, the distributions of the electric field are different as well. Thus, these failure features cannot represent the development processions in the dynamic latch-up failures.

From Fig. 9(a)–(e), it is demonstrated the *P* well region structures are relatively intact, and their features are closer to the cells that is successfully turned OFF. For example, in Fig. 9(a), there is a local bright area at the boundary of the *P* well region, which indicates the original doping concentration has been changed. Moreover, with the increasing of the heats and carrier concentrations, there are two gaps at the boundary of the *P* well region, which is under the gate electrode in Fig. 9(b). The similar results are highlighted in Fig. 9(c) as well, and other *P* well structures remain relatively complete.

Moreover, the conditions that dynamic latch-up failure occurs are researched by simulation. At the initial stage of the turn-OFF period, the internal current, electric field, and temperature distributions in the IGBT chip are analyzed in simulation, to investigate the trigger conditions before the dynamic latch-up failure. The simulation results are displayed in Fig. 10.

During the turn-OFF period, the heat, generated by electric field and current flow internal the IGBT chip, cannot be transferred the cool medium, so the thermal insulation boundaries are set in the simulation. As shown in Fig. 10(a), the internal temperature distribution is relatively uniform, which is close to 150 °C (423 K). The area that local temperature increases is under the gate electrode, which is at the boundary of the *P* well region as well. Besides, the highest temperature is about to 164 °C (437 K). Meanwhile, the trigger conditions of dynamic latch-up failure are simulated in Fig. 10(b). According to the electric field simulation results, the electric field strength is high at the boundary of the *P* well region. At the initial stage of the turn-OFF period, the highest electric field strength is about 8×10^4 V/cm. Considering the plenty of electron carriers near the emitter electrode, the inversion layer and the electron channel under the gate electrode has not disappeared at this time. Furthermore, it is shown the current density, the electric field strength, and the temperature are extremely high around the *P* well region. Besides, these current flow paths are mainly lateral. Hence, due to large current flows, the dynamic latch-up failure occurs during the turn-OFF period. Eventually, with the activation of the parasitic *n–p–n* BJT, large amounts of current and heats lead the IGBT's turn-OFF failure.

According to the results in Fig. 10, the gaps' locations in Fig. 9(b) and (c) are consistent with where the current accumulates internal the IGBT chip. It is shown in Fig. 10 that the high current density, high temperature and the high electric field strength are the main reasons to cause the gaps at the boundary of the *P* well region. When the failure occurs, the current density and temperature increase rapidly. Then, the current density and the local hotspot leads the gaps at the boundary of the *P* well region. Even, for the cells fail more severely, it is shown that there are lateral current paths in Fig. 9(f), (g), and (j).

In Fig. 9(a) and (b), it is demonstrated that there is a local bright area at the boundary of the *P* well region. Based on the simulation results in Fig. 10(b), the bright area in the failure cell corresponds to the position with high electric field strength in simulation. It is indicated that the original doping concentration is changed by the high temperature and high electric field strength after the failure, which further leads the bright area in the failure cell. Moreover, it is shown that the boundary of *P*

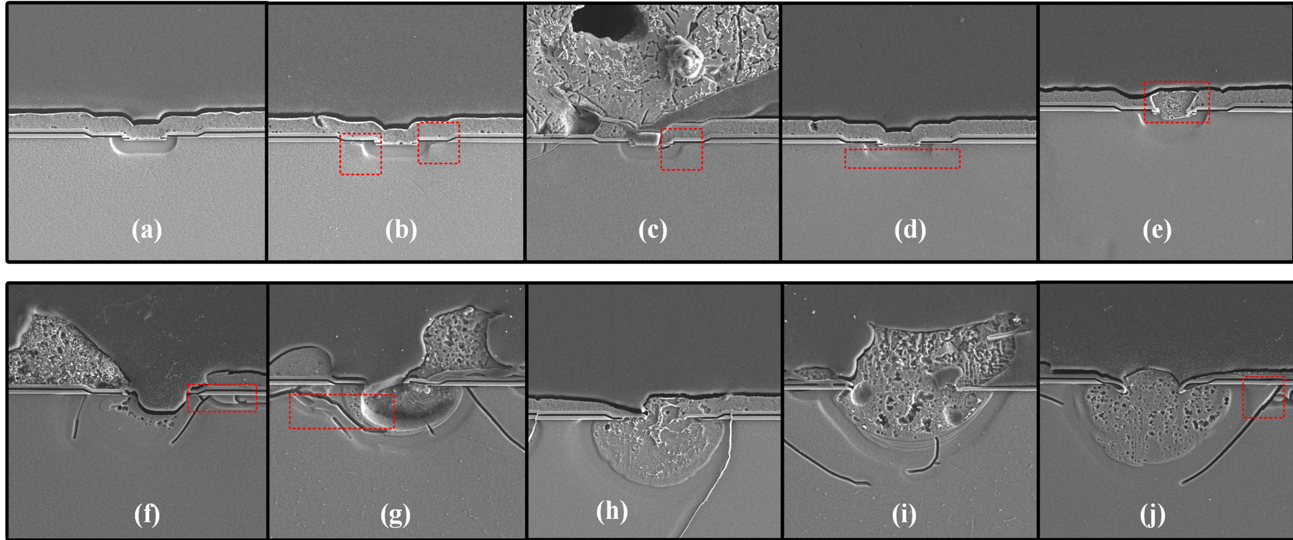


Fig. 9. Failure features after the dynamic latch-up failure.

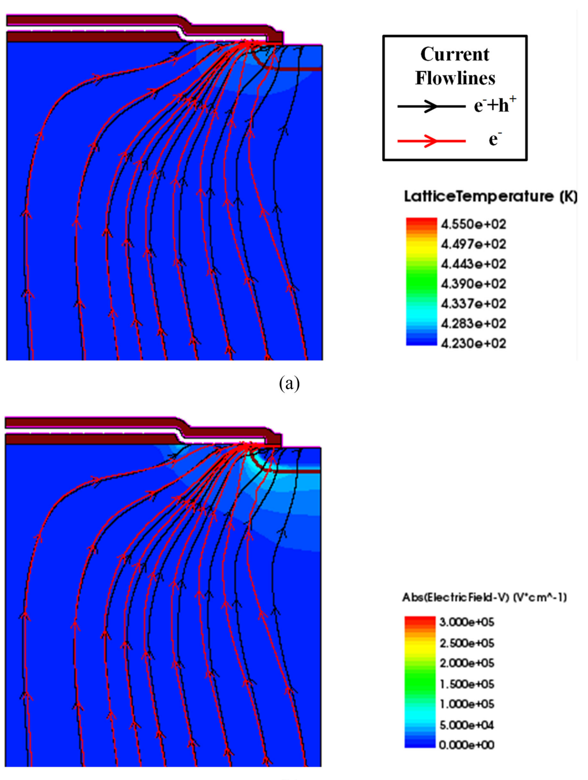


Fig. 10. Current, electric field, and temperature distributions in IGBT chip before dynamic latch-up failure ($V_{ce} = 2.5$ kV, $I_c = 150$ A, $R_g = 5\ \Omega$, and $T_j = 150$ °C). (a) Current and temperature. (b) Current and electric field.

well /N^{-}drift junction becomes indistinct, which are shown in Fig. 9(d) and (e). Taking Fig. 9(d) as an example, no gaps under the gate electrode can be observed. When it comes to Fig. 9(e), both P well region gap and the indistinct boundary are evident. Then, the heats melted the metal material on the chip's surface, which means the failure further develops.

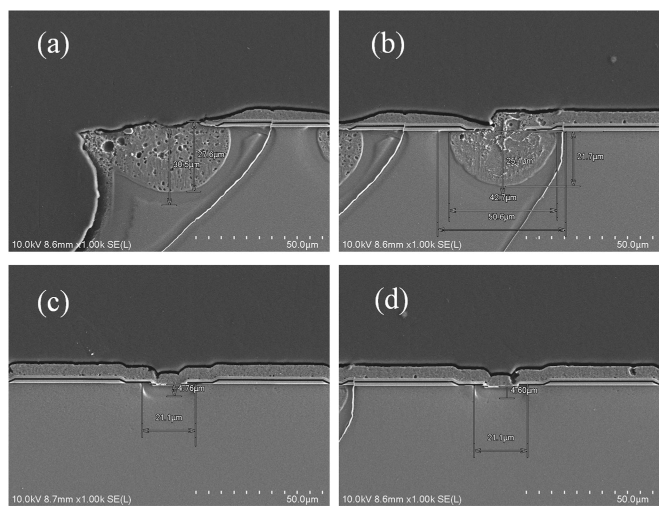


Fig. 11. Detailed signatures of the dynamic latch-up failure in IGBT chip.

As for the SEM results from Fig. 9(f)–(j), it is shown that the P well structures are destroyed, forming the mixture region with the electrode metal at high temperature. According to the results in Fig. 9, the mixture region internal the failure chip starts at the emitter electrode. After developing laterally and vertically, the mixture region even reaches the N^{-}drift region. In Fig. 8(b), it is indicated that the size of the mixture area decreases with the distance from the center of the through-out hole. Furthermore, the detailed signatures of the dynamic latch-up failure in IGBT chip are shown in Fig. 11.

The maximum depth of the mixture region can reach 27.6 μm in Fig. 11(a), and the maximum width reaches 42.7 μm in Fig. 11(b). The width of the P well region is 21.1 μm, which is half of the maximum width in Fig. 11(b). Moreover, the depth of the P well region is about 4.6 μm, which is one-sixth as deep as the mixture region one in Fig. 11(b). Except for the size of

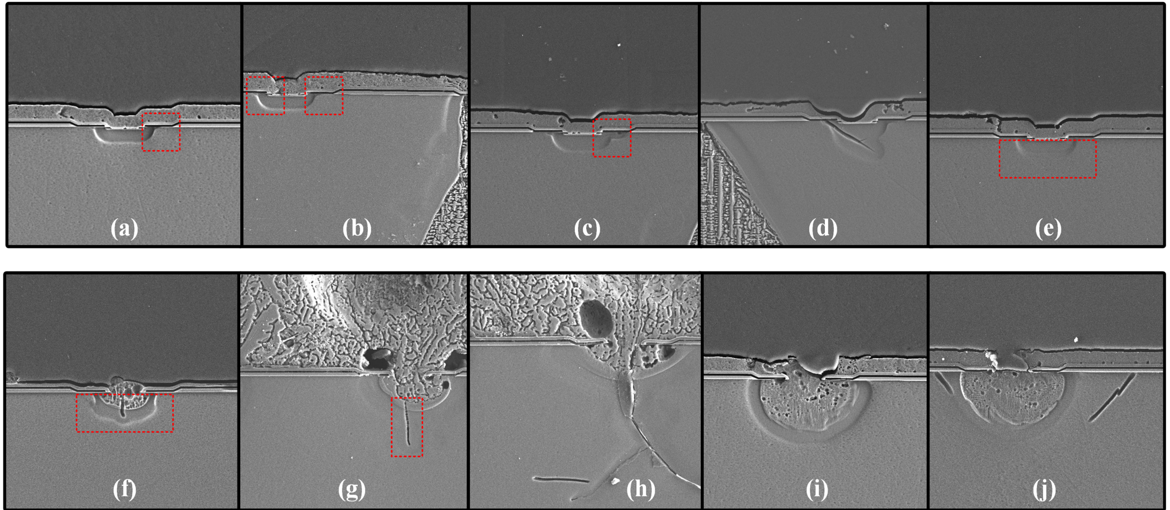


Fig. 12. Failure features after the secondary breakdown failure.

the P well region, other two signatures in the dynamic latch-up IGBT chip can be observed. One is the current filament path. It is shown in Fig. 9(f), (g) and (j) that there are current filament paths nearby the gate electrode. So many lateral current paths indicate that the inversion layer and the electron channel exist, which are consistent with the simulation results in Fig. 10(a). The other one is the gate structure in the cell. Due to the local concentration of the heat and current density, the damage to the gate structure is severe, which is shown in Fig. 9(h) and (i). Based on the SEM results, the gate oxide and metal materials are badly damaged in dynamic latch-up failure.

B. Secondary Breakdown Failure

When it comes to the secondary breakdown failure, 5 failure chips with nearly 100 cells are compared. The different failure cells are summarized and classified as well, which are displayed in Fig. 12.

In Fig. 12, there are ten different typical cell structures. From Fig. 12(a)–(e), the P well region gap and the indistinct boundary are observed as well, where the P well structures are relatively intact. Especially in Fig. 12(c) and (d), the P well region gaps are obvious, which are similar to SEM results in the dynamic latch-up failure.

To further compare the differences between the dynamic latch-up failure and the secondary breakdown failure, the trigger conditions that secondary breakdown occurs are analyzed by simulation, which are shown in Fig. 13.

Compared Fig. 13(a) with Fig. 10(a), it is found that the current density under the gate electrode is much lower. Besides, the temperature in the IGBT chip increases with the decrease of the collector current, and the highest temperature appears at the P well/N^{-} drift junction. At the initial stage of the turn-OFF period, the highest temperature is 164 °C (437 K), then it reaches 182 °C (455 K) in Fig. 13(a). The electric field strength is increasing at the same time, and the highest electric field strength reaches 3×10^{5} V/cm. Hence, the impact ionization and the avalanche multiplication are enhanced at the P well/ N^{-}drift junction, which are led by the high electric field strength and the high temperature. In the secondary breakdown failure, although the current density internal the IGBT chip decreases with the chip turned OFF, the heats continue to accumulate and finally causes the P well/ N^{-}drift junction breakdown.

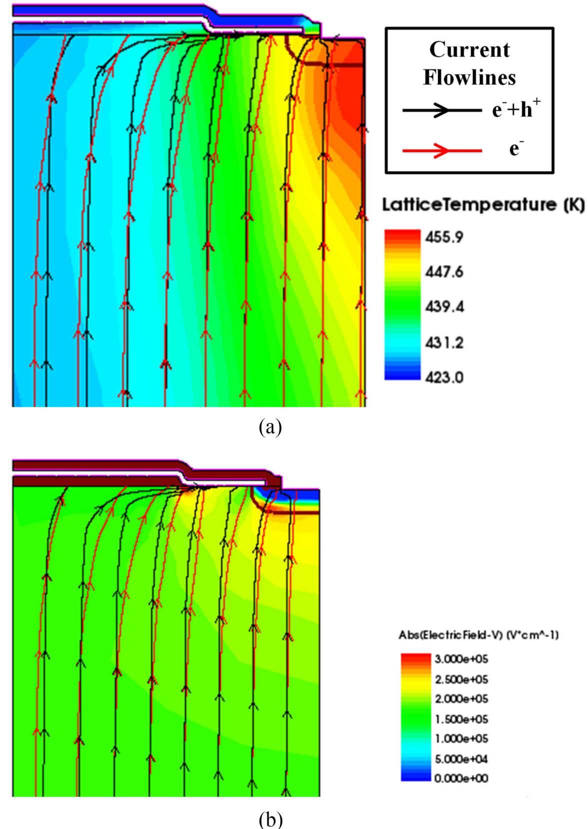


Fig. 13. Current, electric field, and temperature distributions in IGBT chip before secondary breakdown failure ($V_{ce} = 2.5$ kV, $I_c = 150$ A, $R_g = 5\ \Omega$, and $T_j = 150$ °C). (a) Current and temperature. (b) Current and electric field.

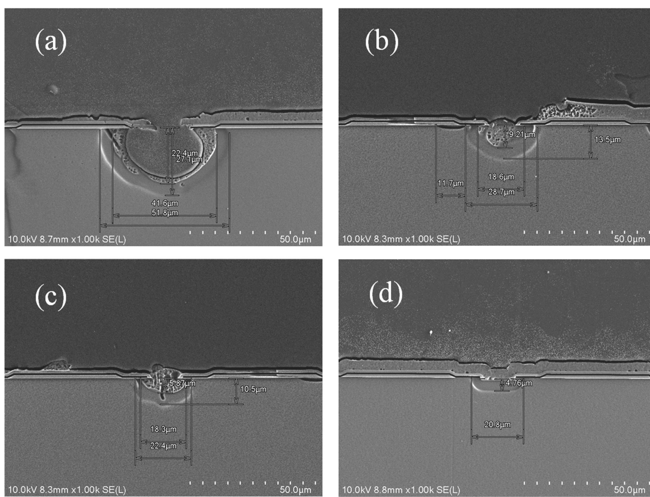


Fig. 14. Detailed signatures of the secondary breakdown IGBT chip.

In the secondary breakdown failure, the gaps at the boundary of the *P* well region are similar to the ones in the dynamic latch-up failure. Whereas, the lateral current paths in the failure cells are not observed. It is indicated that the lateral current density decreases with the collector voltage increases. Thus, the lateral current density and the high temperature causes the gaps during the failure process, while their energies are not enough to form the lateral current paths in the failure cells. As for the bright area in Fig. 12(a) and (b), it is displayed in Fig. 13(b) that the electric field strength at the corresponding area is extremely high. Then, the original doping concentration will be changed with the temperature increases in the failure process.

Furthermore, from the Fig. 12(f)–(j), more different failure cell structures in parallel cells are demonstrated. It is shown in Fig. 12(f)–(h) that there is a clear current path, which forms under the *P* well/ N^{-}drift junction. The current path locates exactly as the results simulated in Fig. 13(a), where there are amounts of current and heats. Hence, these vertical current paths can be regarded as the signature of the secondary breakdown failure. Compared with the *P* well region in the dynamic latch-up failure, there are many *P* well structures with smaller size of the mixture region. Taking Fig. 12(f) and (j) as the examples, the size of the mixture region is close to the *P* well region. Besides, the sizes of different mixture regions are recorded and compared in Fig. 14.

In Fig. 14(a), it is shown that the maximum depth of the mixture region is 22.4 μm, and the maximum width reaches 41.6 μm. The maximum depth in secondary breakdown failure is smaller than that in dynamic latch-up failure (27.6 μm). Meanwhile, the maximum width in Fig. 14(a) is close to the one (42.7 μm) in Fig. 11(b). Thus, it is not always effective to distinguish the failure causes by the maximum depth of the mixture region. Whereas, there are many mixture regions in the secondary breakdown failure, whose sizes are much smaller than those in the dynamic latch-up failure. The depths of the mixture region in Fig. 14(b) and (c) are 9.21 and 5.87 μm, respectively. Correspondingly, their widths in Fig. 14(b) and (c) are 28.7 and 18.3 μm, respectively. The size of the mixture

TABLE I
SUMMARY OF THE FAILURE SIGNATURES

Features		Dynamic latch-up failure	Secondary breakdown failure
V_{ce} and I_c waveforms	**V_{ce} reaches DC link voltage**	×	○
	I_c first decreases then increases	×	○
P well region	Local bright area	○	○
	P well region gap	○	○
	Indistinct boundary	○	○
	Vertical current path	×	○
Gate Structure (When the mixture region observed)	**Lateral current path**	○	×
	Gate oxide and metal material	Damaged	Unbroken
Mixture region	Size	Many are bigger than P well region	Many are similar in size to P well region
	Max. depth	27.6 μm	22.4 μm
	Max. width	42.7 μm	41.6 μm

○: Observed ×: Not observed

region indicates that the secondary breakdown failure is less damaging, compared with the dynamic latch-up failure. The gate structures in Figs. 12 and 14 validate this conclusion as well. In the secondary breakdown failure, the gate oxide and the metal material are still unbroken. Even in Figs. 12(j) and 14(a), it can be seen that the gate structures in the cell still remain relatively intact. According to simulation in Figs. 10 and 13, in light of the different overheated locations, the failure causes can be effectively judged by the gate structure.

V. Failure Discussions

The planar FS IGBT chips are tested in this article, whose rated parameters are 3.3 kV/ 50 A. To carry out the SEM analysis conveniently, the devices under test are packaged as PRESS pack IGBT chips. The dynamic latch-up failure and the secondary breakdown failure are systematically introduced in Section III. Then, in Section IV, the SEM results of two failure IGBT chips are displayed and compared in detailed. Different failure modes will lead different features in the failure chip. Therefore, these signatures can be used to distinguish to failure causes. Although it is hard to investigate the failure process internal the IGBT chip, the semiconductor numerical simulation can provide the auxiliary explain to the SEM results. Moreover, in this section, the summary of these failure signatures is given in Table I.

As discussed above, the moment that the dynamic latch-up failure occurs is at the initial stage of the turn-OFF period, when the inversion layer and the electron channel still exist. Therefore, in Fig. 10(a), there are heats and current crowding under the gate electrode, which make the parasitic *n–p–n* activate. After that, the dynamic latch-up occurs and finally leads to the IGBT chip failure. For the secondary breakdown failure, it is shown that the overheated area in the IGBT cell is close to the *P* well/ N^{-}drift junction. Although the current density isn't as high as the one at

the beginning of the IGBT turned OFF, the increasing of the temperature enhances the avalanche multiplication. With more generated carriers and higher electric field peak, the breakdown happens and the junction can no longer sustain the collector voltage.

As given in Table I, the local bright area, the *P* well region gap and the indistinct boundary can be observed in both dynamic latch-up failure and secondary breakdown failure. However, with the increase of the electric field and thermal stress, the two different failure chips have different features in the current filament path, the gate structure, and the mixture region. The lateral current paths are observed in Fig. 9(f), (g), and (j), where their positions are under the gate electrode. According to the simulation results in Fig. 10, such high current density activates the parasitic *n–p–n* BJT. The currents direction and their positions are consistent with the SEM results in Fig. 9. As for the secondary breakdown failure, there are vertical current paths in Fig. 12(f) to (h). Based on the simulations results, these vertical current paths are caused by the avalanche multiplication at the *P* well/ N^{-} drift junction. The simulation in Section IV verifies the SEM results, which shows the current filament path can be regarded as the marked signatures to distinguish to failure causes.

Except for the current filament path, the gate structure and the mixture region in the failure cell can also be the auxiliary signatures. It is shown that the gate structures in the secondary breakdown failure chip remain unbroken. Taking Fig. 12(j) as an example, the gate oxide and the metal material in the IGBT cell are intact after the secondary breakdown failure. Compared with the dynamic latch-up failure like Fig. 11(b), the gate structures are damaged by the heats and the current. Even, the gate structures are completely destroyed in Fig. 9(i) after the dynamic latch-up failure.

Since there is a through-hole in the failure IGBT chip, the depth of the melted area is no longer effective to distinguish the failure causes. During the failure progressing, the metal at the emitter electrode is first melted and further forms the mixture region at high temperature, which is shown in Fig. 9(e). In general, the mixture regions are bigger than the *P* well region in the dynamic latch-up failure, whereas the mixture regions in the secondary breakdown are similar in size to the *P* well region. Besides, the maximum depth of the mixture region in the dynamic latch-up failure is close to the one in the secondary breakdown failure. The maximum widths of the mixture region in the two failures are similar as well.

Based on the interactions among the current, electric field, and the temperature during the failure process, the distinguished method is proposed in this article. Considering the packaging has limited influence on the temperature and electric field internal the chip, this method can be applicable to the IGBT devices with different packaging. For the chips with different doping profiles and structures, the SEM results to the failure cells signatures can contribute to the failure analysis. Hence, the analysis and proposed method have the referential significance for IGBT turn-OFF failure under CIL.

VI. Conclusion

The features of the dynamic latch-up failure and the secondary breakdown failure are systematically compared by experiment and simulation in this article. Then, according to the SEM scanning, the marked signatures, for the turn-OFF failure under CIL are put forward to distinguish to failure causes. The following conclusions can be summarized.

1) The features of the dynamic latch-up failure and the secondary breakdown failure are compared by experiment and simulation for the first time. It is shown that the typical dynamic latch-up failure occurs at the initial stage of the turn-OFF period, and the secondary breakdown failure happens after the collector current starts to fall. High current density and local high temperature under the gate electrode activates the *n–p–n* BJT in the dynamic latch-up failure. As for the secondary breakdown failure, the highest temperature reaches 182 °C at the *P* well/N^{-} drift junction, which further leads the avalanche multiplication and junction breakdown.
2) The failure cells characteristics for two turn-OFF failures are firstly compared by SEM observation. The SEM observation focuses on the parallel cells structures surrounding the melted area. The results show that the current filament path, the gate structure, and the mixture region can be regarded as the marked signatures of the failure causes. This proposed method contributes to the deeper failure analysis in the IGBT devices.
3) The distinguished method to the failure cause for the IGBT chip under CIL is put forward. For the waveforms characteristics, the secondary breakdown failure happens when collector voltage reaches dc-link voltage, and the load current has fallen at that time. For the SEM results, the lateral current path and the vertical current path are obvious in the dynamic latch-up failure and the secondary breakdown failure, respectively. Moreover, the gate structure and the size of the mixture region can be the auxiliary signatures as well.

References

[1] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2010.

[2] A. Abuelnaga, M. Narimani, and A.S. Bahman, “A review on IGBT module failure modes and lifetime testing,” *IEEE Access*, vol. 9, pp. 9643–9663, 2021.

[3] F. Iannuzzo, C. Abbate, and G. Busatto, “Instabilities in silicon power devices: A review of failure mechanisms in modern power devices,” *IEEE Ind. Electron. Mag.*, vol. 8, no. 3, pp. 28–39, Sep. 2014.

[4] R. Simpson et al., “Press-pack IGBTs for HVDC and FACTs,” *CSEE J. Power Energy Syst.*, vol. 3, no. 3, pp. 302–310, 2017.

[5] M. Trivedi and K. Shenai, “Turn-off failure of IGBTs under clamped inductive load,” in *Proc. 29th Annu. IEEE Power Electron. Specialists Conf.*, 1998, pp. 1191–1195.

[6] M. Pecht, “Prognostics and health management of electronics,” in *Encyclopedia of Structural Health Monitoring*, New York, NY, USA: Wiley, 2009.

[7] C. Chen, V. Pickert, M. Al-Greer, C. Jia, and C. Ng, “Localization and detection of bond wire faults in multichip IGBT power modules,” *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7804–7815, Aug. 2020.

[8] D. Luo, M. Chen, W. Lai, H. Xia, H. Li, and K. Yu, “A fault detection method for partial chip failure in multichip IGBT modules based on turn-off delay time,” *IEEE Trans. Electron Devices*, vol. 69, no. 6, pp: 3319–3327, Jun. 2022.

[9] K. Yoshikawa, T. Koga, T. Fujii, A. Nishiura, and Y. Takahashi, “A study on wide RBSOA of 4.5 kV power pack IGBT,” in *Proc. 13th Int. Symp. Power Semicond. Devices ICs*, 2001, pp. 117–120.

[10] M. Rahimo, A. Kopta, S. Eicher, U. Schlapbach, and S. Linder, "Switching-self-clamping-mode 'SSCM', a breakthrough in SOA performance for high voltage IGBTs and diodes," in *Proc. 16th Int. Symp. Power Semicond. Devices ICs*, 2004, pp. 437–440.
[11] M. Rahimo, "Future trends in high-power bipolar metal-oxide semi-conductor controlled power semi-conductors," *IET Circuit, Devices, Syst.*, vol. 8, no. 3, pp. 155–167, 2013.
[12] T. Ogura, H. Ninomiya, K. Sugiyama, and T. Inoue, "4.5-kV injection-enhanced gate transistors (IEGTs) with high turn-off ruggedness," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 636–641, Apr. 2004.
[13] J. G. Bauer, O. Schilling, C. Scheaffer, and F. Hille, "Investigations on the ruggedness limit of 6.5 kV IGBT," in *Proc. 17th Int. Symp. Power Semicond. Devices ICs*, 2005, pp. 71–74.
[14] P. Bhatnagar, P. Waind, L. Coulbeck, I. Deviny, and J. Thomson, "Improvements in SOA ruggedness of 6.5 kV IGBTs," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–8.
[15] Y. Shiba, I. Omura, and M. Tsukuda, "IGBT avalanche current filamentaion ratio: Precise simulations on mesh and structure effect," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 339–342.
[16] M. Trivedi and K. Shenai, "Failure mechanisms of IGBT's under short-circuit and clamped inductive switching stress," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 108–116, Jan. 1999.
[17] A. Castellazzi, M. Ciappa, W. Fichtner, J. Urresti-Ibanez, and M. Mermet-Guyennet, "Integrated compact modelling of a planar-gate nonpunch-through 3.3kV-1200A IGBT module for insightful analysis and realistic interpretation of the failure mechanisms," in *Proc. 19th Int. Symp. Power Semicond. Devices ICs*, 2007, pp. 133–136.
[18] X. Perpiñà et al., "IGBT module failure analysis in railway applications," *Microelectron. Rel.*, vol. 48, pp. 1427–1431, 2008.
[19] X. Perpiñà et al., "Analysis of clamped inductive turnoff failure in railway traction IGBT power modules under overload conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2706–2714, Jul. 2011.
[20] X. Perpiñà, I. Cortés, J. Urresti-Ibañez, X. Jordà, J. Rebollo, and J. Millán, "Clamped inductive turn-off failure in high-voltage NPT-IGBTs under overloading conditions," *Proc. 24th Int. Symp. Power Semicond. Devices ICs*, 2012, pp. 361–364.
[21] I. Cortes et al., "Study of layout influence on ruggedness of NPT-IGBT devices by physical modelling," *Microelectronics Rel.*, vol. 52, no. 9, pp. 2471–2476, 2012.
[22] X. Perpiñà, I. Cortes, J. Urresti-Ibañez, X. Jorda, and J. Rebollo, "Layout role in failure physics of IGBTs under overloading clamped inductive turnoff," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 598–605, 2013.
[23] C. Peng, X. Li, J. Fan, Z. Zhao, X. Tang, and X. Cui, "Experimental investigations on current sharing characteristics of parallel chips inside press-pack IGBT devices," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10672–10680, Sep. 2022.

Jiayu Fan was born in Zhejiang Province, China, in 1996. He received the B.Sc. degree in electrical engineering in 2018 from North China Electric Power University, Beijing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

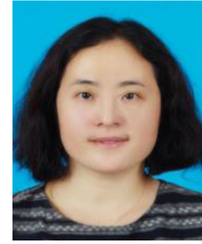
His main research interest is high-voltage power semiconductor device packaging.

Yaohua Wang was born in Henan Province China, in 1981. He received the B.D. degree from Xidian University, Xi'an, China.

He is currently with Beijing Institute of Smart Energy, Beijing, China. His research interests include the research and development of high-voltage power semiconductor devices design and process.

Feng He was born in Hebei Province China, in 1989. He received the Master degree from Peking University, Beijing, China, in 2015.

He is currently with Beijing Institute of Smart Energy, Beijing, China. His research interests include the research and development of high-voltage power semiconductor chips and devices.



Mingchao Gao was born in Shandong Province, China, in 1981. She received the Master degree from Dalian University of Technology, Dalian, China, in 2009.

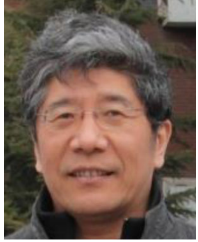
Her current research interests in high-voltage silicon power semiconductor devices and silicon carbide power devices.

Zhibin Zhao was born in Hebei province, China, in 1977. He received the Ph.D. degree in electrical engineering from North China Electric Power University, Baoding, China, in 2005.

He is currently a Professor with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University. His main research interests include computational electromagnetics and electromagnetic compatibility in power electronics.

Xuebao Li was born in Tianjin, China, in 1988. He received the B.Sc. and Ph.D. degrees in electrical engineering from North China Electric Power University, Beijing, China, in 2011 and in 2016, respectively.

He is currently an Associate Professor with the School of Electrical and Electronic Engineering, North China Electric Power University. His research interests include the electromagnetic environment and electromagnetic compatibility in power systems, and insulation problems in high-voltage apparatus.



Xiang Cui (Senior Member, IEEE) was born in Baoding, Hebei Province, China, in 1960. He received the B.Sc. and M.Sc. degrees in electrical engineering from North China Electric Power University, Baoding, China, in 1982 and 1984, respectively, and the Ph.D. degree in accelerator physics from the China Institute of Atomic Energy, Beijing, China, in 1988.

He is currently a Professor and the Vice Director of the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University. His research interests include computational electromagnetics, electromagnetic environment and electromagnetic compatibility in power systems, insulation and magnetic problems in high-voltage apparatus.

Dr. Cui is a Standing Council Member of the China Electrotechnical Society and a Fellow of *IET*. He is currently an Associate Editor for the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY.

Zhong Chen received the bachelor's degree from Zhejiang University, Hangzhou, China, in 2002, the master's degree in electrical and computer engineering from the National University of Singapore, Singapore, in 2004, and the Ph.D. degree electrical and computer engineering from North Carolina State University, Raleigh, NC, USA, in 2008.

He is currently an Assistant Professor in electrical engineering with the University of Arkansas. For seven years, he was an ESD specialist with Analog Technology Development at Texas Instruments (TI). At TI, he has been providing ESD solutions for various analog and digital applications in automotive, power management, power interface, high-speed product, audio and imaging products and motor drives. He was recognized as a TMG Member of Technical Staff for his contribution and leadership at TI. His research interests include novel device for harsh environment, integrated circuit and system level ESD and reliability; power electronics and power devices; wide-bandgap material, devices and packaging.

Dr. Chen is currently a Technical Committee Member for the ESD/Latchup chapter of the International Reliability Physics Symposium and the Electrical Overstress/Electrostatic Discharge Symposium