Letters

Comparison and Optimization of Datasheet-Driven Extraction of Gate-Drain Overlap Oxide Capacitance in IGBT Modeling

Yuwei Wu, *Student Member, IEEE*, Laili Wang, *Senior Member, IEEE*, Jianpeng Wang, *Student Member, IEEE*, Zenan Shi, *Student Member, IEEE*, and Jin Zhang, *Student Member, IEEE*

***Abstract*—Extracting gate-drain overlap oxide capacitance (C_{oxd}) is a necessary step for almost all kinds of insulated-gate bipolar transistor (IGBT) compact models. There are two datasheet-driven methods that are universally accepted, one is based on reverse capacitance voltage characteristics (*C–V* method), and the other uses gate charge characteristics (*Q–V* method). This letter is to reveal the underlying mechanism of these two methods. It is found that the *C–V* method has an inescapable shortcoming which will mistake the turn-OFF delay time forecasted by IGBT models. In this letter, the internal capacitance system of IGBT is modeled and demonstrated completely. Based on this model, the accuracy and feasibility of the *C–V* and *Q–V* methods are analyzed. Moreover, the effect of C_{oxd} on IGBT compact models is studied and further verified by experiments and circuit simulations.**

***Index Terms*—IGBT modeling, parameter extraction.**

I. Introduction

THE datasheet-driven method is popular for power devices' modeling [1]–[5]. It is attractive that this method could help users to quickly extract model parameters with the information provided by manufacturer's datasheet, avoiding supplementary experiments. As for gate-control devices, the gate-drain overlap oxide capacitance (C_{oxd}) is a basic device parameter that exists in almost all kinds of models. The incorrect extraction will cause an inaccurate forecast of switching time, which further leads to errors in switching loss estimation and dead time design [5], [6]. Therefore, extracting C_{oxd} correctly is essential for compact models to guide the design of power electronic systems effectively.

As far as we know, there are two universally accepted datasheet-driven methods to extract C_{oxd}, which are the *C–V* and *Q–V* methods. For *C–V* method, it is based on reverse capacitance (C_{res}) voltage characteristics. As shown in Fig. 1(a), it regards the maximum point of the C_{res} as C_{oxd}, i.e.,

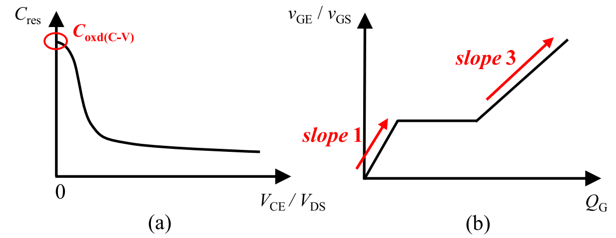

Fig. 1. Illustrations of (a) *C–V* method and (b) *Q–V* method.

$$C_{\text{oxd}(C-V)} = \max(C_{\text{res}}). \tag{1}$$

This method is convenient and widely adopted by datasheet-driven models of power MOSFET and IGBT [2]–[5]. For *Q–V* method, it uses gate charge characteristics for C_{oxd} extraction. The gate charge characteristics is the gate-emitter/ gate-source voltage waveform tested under a constant gate current I_{G}. As shown in Fig. 1(b), the curve has three phases with different slopes. Using the slopes in phase 1 and phase 3, C_{oxd} is deduced that

$$C_{\text{oxd}(Q-V)} = \frac{1}{\text{slope3}} - \frac{1}{\text{slope1}}. \tag{2}$$

This method was firstly proposed for parameter extraction of Hefner IGBT model and has been packaged into commercial simulation software [7], [8].

As for power MOSFET, the two methods are almost equivalent. However, it is reported that *C–V* method might cause a significant error for IGBT. For example, Bryant *et al.* [9] used the *C–V* method to extract C_{oxd} and had to take a great effort for parameter optimization. However, the optimization is not aimed at C_{oxd} but all model parameters, so that other parameters would also be adjusted and thereby diverged from their real values. Further, owing to time and resource constraints, the procedure can only be conducted under limited operating conditions, consequently restricting the model accuracy in multicondition simulation. Yang *et al.* [10] have noticed the inaccuracy of the *C–V* method. They proposed a current-dependent correction formula for miller capacitance, but the form of it is simply based on assumption without any physical derivation. Moreover, its parameter must be extracted by experiment waveforms, which deviates from the original intention of datasheet-driven method.

Manuscript received 22 May 2022; revised 7 July 2022; accepted 23 July 2022. Date of publication 26 July 2022; date of current version 6 September 2022. This work was supported by the Fund of the Natural Science Foundation of China under Grant U1966212. *(Corresponding author: Laili Wang.)*

The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: wywei99552017@stu.xjtu.edu.cn; llwang@mail.xjtu.edu.cn; wangjackmvp@stu.xjtu.edu.cn; szn961021@gmail.com; z062626@stu.xjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3194023.

Digital Object Identifier 10.1109/TPEL.2022.3194023

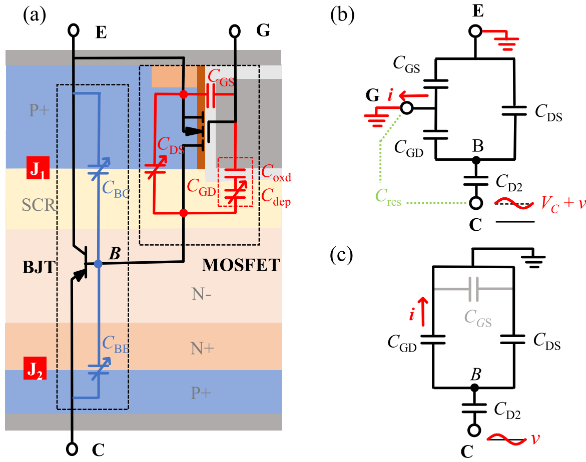

Fig. 2. Diagrams of a trench gate IGBT. (a) Vertical section and capacitance distribution. (b) Simplified network of $C_{\rm res}$ testing circuit. (c) AC network of Fig. 2(b).

From the results of investigation, most papers directly applied the capacitance distribution of power MOSFET to IGBT compact models, ignoring the difference in internal structure between them [6], [9], [11].

The motivation of this letter is to clear the underlying mechanism of the two extraction methods and quest a general $C_{\rm oxd}$ datasheet-driven extraction process for IGBT modeling. In Section II, the internal capacitance model of IGBT is established completely. Based on this model, the inherent flaw of the *C–V* method is revealed and the feasibility of the *Q–V* method is explained for the first time. In Section III, an expression is derived relating $C_{\rm oxd}$ and turn-OFF delay time to give a qualitative description of the effect of the *C–V* method on IGBT modeling. These findings provide not only a deeper understanding of the mechanism of IGBT, but also a significant improvement for IGBT modeling.

II. Comparison of *C–V* and *Q–V* Method

A. *Internal Capacitance Model of IGBT*

Fig. 2(a) shows the vertical section of an IGBT cell, the equivalent circuit is superimposed on it. IGBT works like a BJT driven by a MOSFET, and the distribution of capacitance is directly related to these two parts. As for MOSFET, $C_{\rm GS}$ and $C_{\rm GD}$ are MOS capacitances and $C_{\rm DS}$ is the junction capacitance of J_1. $C_{\rm GD}$ is composed of the gate oxide capacitance $C_{\rm oxd}$ in series with the depletion capacitance $C_{\rm dep}$.

Considering that J_1 is always reverse-biased, $C_{\rm DS}$ equals the depletion capacitance. All of them have nonlinear features with voltage [12]. According to the working mechanism of IGBT, the injected holes from J_2 produces the emitter current of P-N-P BJT [13]. Among them, $C_{\rm BE}$ is the junction capacitance of J_2 which consists of two parts: the diffusion capacitance $C_{\rm d2}$ and the depletion capacitance $C_{\rm D2}$ [14]. The effect of these two capacitances depends on the working state of IGBT, it is approximate that

$$\begin{cases} C_{\rm BE} = {\rm C}_{\rm d2}, {\rm ON-state} \\ C_{\rm BE} = {\rm C}_{\rm D2}, {\rm OFF-state} \end{cases} . \quad (3)$$

Meanwhile, the BJT's base-collector capacitance is composed of the depletion capacitance $C_{\rm D1}$ of J_1 and the space-charge capacitance $C_{\rm sc}$ due to injected charges [14]. Conceptually, $C_{\rm D1}$ is equal to $C_{\rm DS}$ of the MOSFET part, so it need not be recounted. Therefore, $C_{\rm BC}$ equals $C_{\rm sc}$. The $C_{\rm sc}$ is defined by $dQ_{\rm sc}/dV_{\rm BC}$ and $dQ_{\rm sc}$ means the change of space charges driven by injected holes. The theoretical expression of $C_{\rm sc}$ has been derived in [15], named as charge extraction capacitance.

B. *Analysis of* C–V *Method*

The nonlinear feature of reverse transfer capacitance ($C_{\rm res}$) is displayed in datasheet of both IGBT and power MOSFET. $C_{\rm res}$ is tested with the increase of $V_{\rm CE}/V_{\rm DS}$, and $V_{\rm GE}/V_{\rm GS}$ is set to be zero. The $C_{\rm res}$ and $C_{\rm GD}$ when $V_{\rm CE}/V_{\rm DS}$ is zero are represented by $C_{\rm res}(0)$ and $C_{\rm GD}(0)$. To be distinguished from IGBT, the $C_{\rm res}$ of power MOSFET is represented by $C_{\rm res(MOS)}$. For power MOSFET, it satisfies that [2]

$$C_{{\rm oxd}(C-V)} = C_{\rm res(MOS)}(0) = C_{\rm GD}(0) = C_{\rm oxd(real)} \quad (4)$$

where $C_{\rm oxd(real)}$ is the real value of $C_{\rm oxd}$. Therefore, $C_{\rm oxd}$ can be extracted from the *C–V* method for power MOSFET. However, as for IGBT, $C_{\rm res}$ is not equal to $C_{\rm GD}$. The $C_{\rm res}$ of IGBT is the equivalent capacitance of the series-parallel connection of $C_{\rm GD}$ and other capacitances, which leads to the inaccuracy of the *C–V* method. Therefore, it is necessary to find the relation between $C_{\rm res}$ and $C_{\rm GD}$ to evaluate the error of the *C–V* method.

The $C_{\rm res}$ curve is tested in OFF-state, where there is no excess charge injected into base region. Considering that $C_{\rm sc}$ is injected-charge-related, it is neglected in OFF-state because of no injected charge. Thus, the equivalent circuit of internal capacitance can be simplified into a four-capacitance system. On the other hand, the $C_{\rm res}$ curve in datasheet is obtained by power device analyzer which is based on ac guard technique [16]. This procedure is equivalent to applying a dc bias voltage and an ac small signal to terminal C, then calculating the impedance by the ac voltage applied to terminal C and the current flowing out of terminal G. The simplified network of the testing circuit and the equivalent circuit of the four-capacitance system are shown in Fig. 2(b). The ac network is shown in Fig. 2(c). As it is seen, $C_{\rm GS}$ is shorted in the ac network. Using the laplace transform to analyze the network, there are

$$v_{\rm B} = \frac{\frac{1}{s(C_{\rm GD}+C_{\rm DS})}}{\frac{1}{s(C_{\rm GD}+C_{\rm DS})} + \frac{1}{sC_{\rm D2}}} \cdot v = \frac{C_{\rm D2}}{C_{\rm GD}+C_{\rm DS}+C_{\rm D2}} \cdot v \quad (5)$$

$$\frac{v_{\rm B}}{i} = \frac{1}{sC_{\rm GD}}. \quad (6)$$

Combining (5) and (6), the relation between $C_{\rm res}$ and internal capacitances is derived as

$$C_{\rm res} = \left|\frac{i}{v}\right| = \frac{1}{1+\frac{C_{\rm GD}}{C_{\rm D2}}+\frac{C_{\rm DS}}{C_{\rm D2}}} C_{\rm GD}. \quad (7)$$

It implies that $C_{\rm res}$ is equal to $C_{\rm GD}$ multiplied by a coefficient which is less than 1. The coefficient is associated with the value of $C_{\rm GD}$, $C_{\rm DS}$, and $C_{\rm D2}$. The depletion capacitance $C_{\rm D2}$ is considered as a fixed value because J_2 is always in zero or forward bias. Meanwhile, the nonlinear capacitances $C_{\rm GD}$ and $C_{\rm DS}$ decrease sharply with the rise of collector voltage V_C [3].

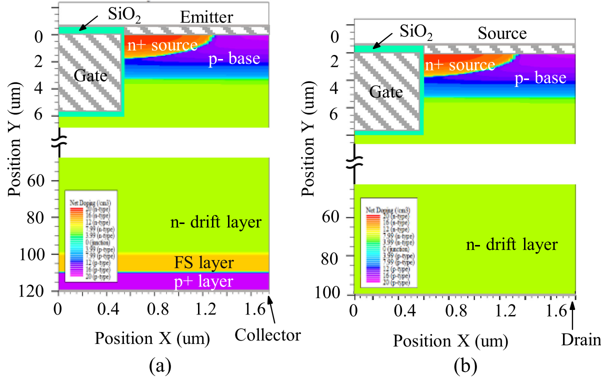

Fig. 3. (a) IGBT and (b) power MOSFET finite-element device models.

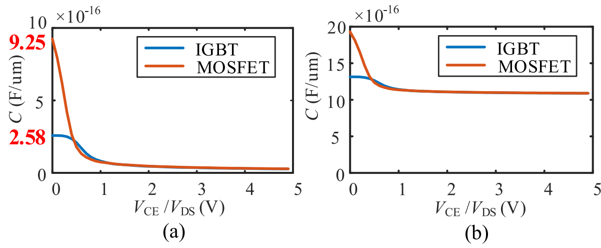

Fig. 4. Capacitance voltage characteristics of IGBT and MOSFET finite-element models in Fig. 2(a) C_{res} and (b) C_{ies}.

Therefore, the coefficient in (7) reaches its minimum value when V_C is zero-bias and gradually approaches 1 with the increase of collector voltage. It means that $C_{\mathrm{oxd}(C-V)}$ is much less than $C_{\mathrm{oxd(real)}}$.

To verify the conclusion above, finite-element device simulations are adopted. An example of IGBT cell simulated in Silvaco TCAD is illustrated in Fig. 3(a). It is based on a 1200 V trench gate IGBT structure illustrated in [13]. For comparison, a power MOSFET cell is constructed by removing $P+$ substrate and FS layer of the IGBT structure above, as shown in Fig. 3(b). By applying small-signal ac analysis, C_{res} and C_{ies} (i.e., input capacitance) curves of both structures are obtained in Fig. 4. Fig. 4(a) implies that C_{res} of IGBT (shorten to C_{res}) is obviously less than C_{res} of MOSFET (shorten to $C_{\mathrm{res(MOS)}}$) when V_{CE} /V_{DS} has a low voltage magnitude. Besides, $C_{\mathrm{res}}(0)$ is only 27.9% of $C_{\mathrm{res(MOS)}}(0)$.

From the theoretical analysis and simulation results, the relations between several capacitances of IGBT are concluded

$$C_{\mathrm{oxd}(C-V)} = C_{\mathrm{res}}(0) < C_{\mathrm{GD}}(0) = C_{\mathrm{oxd(real)}}. \tag{8}$$

C. Analysis of Q–V Method

The gate charging curve provided by datasheet is v_{GE}-Q_G tested under a constant gate current I_G. Fig. 5(a) shows the curve with its corresponding i_C and v_{CE}. The whole process can be divided into three phases: 1, 2, and 3 (phase 1b is a transient process whose time duration is much less than the other three, so it is neglected here). The Q–V method extracted C_{oxd} by the slopes of v_{GE}-Q_G curve in phases 1 and 3. J_2 is zero-bias during phase 1, and forward-bias with a constant current during phase 3. Both of them are static states, so that there is no capacitance effect of J_2 during these two phases. Ignoring the voltage drop

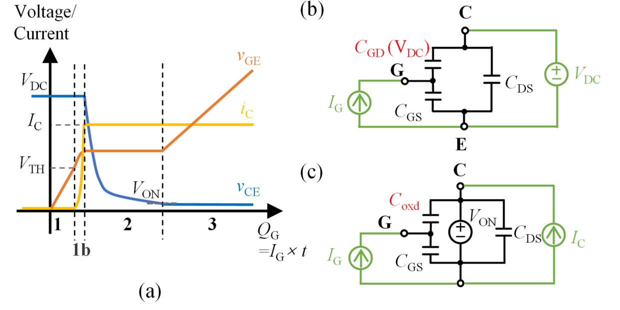

Fig. 5. (a) Waveforms of gate charging with a constant gate current I_{G} and (b) the equivalent circuit during (b) phase 1 and (c) phase 3.

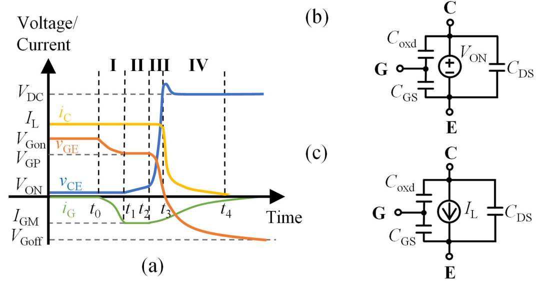

Fig. 6. (a) Waveforms of IGBT turn-OFF transient with inductance load and the equivalent circuit model of IGBT during (b) phase I and (c) II.

on J_2 (smaller than 0.7 V), the equivalent circuit during phases 1 and 3 are shown in Fig. 5(b) and (c). During phase 1, IGBT is forward-blocking with $V_{\mathrm{CE}} = V_{\mathrm{DC}}$. Consider the response of I_G

$$I_G = [C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DC}})]\frac{dv_{\mathrm{GE}}}{dt}. \tag{9}$$

Because V_{DC} is always set to be high, $C_{\mathrm{GD}}(\mathrm{V_{DC}})$ is several orders of magnitude smaller than C_{GS}, and the slope of the v_{GE}-Q_G curve in phase 1 is approximate to

$$\mathrm{slope1} \approx \frac{1}{C_{\mathrm{GS}}}. \tag{10}$$

During phase 3, C_{GD} equals C_{oxd} because the gate voltage is higher than the collector voltage, so the response of I_G is

$$I_G = (C_{\mathrm{GS}} + C_{\mathrm{oxd}})\frac{dv_{\mathrm{GE}}}{dt}. \tag{11}$$

Thereby, the slope of v_{GE}-Q_G curve in phase 3 is

$$\mathrm{slope3} = \frac{1}{C_{\mathrm{GS}} + C_{\mathrm{oxd}}}. \tag{12}$$

It is feasible to extract C_{oxd} from (2), (11), and (12).

III. Influence of Coxd on IGBT Modeling

Incorrect C_{oxd} causes errors in modeling of IGBT's turn-OFF delay time ($t_{d\mathrm{off}}$). The process of IGBT turn-OFF transient is divided into four phases, as illustrated in Fig. 6(a). In this letter, the turn-OFF delay time is defined as the time duration from phases I to III. To establish the relation between C_{oxd} and $t_{d\mathrm{off}}$, it is necessary to identify the phases in which C_{oxd} is active.

During phase I, the region under the gate involves a high-concen tration accumulation layer because of the forward

bias of V_{GC} (gate-collector voltage), so C_{GD} equals C_{oxd}. During phase II, the accumulation layer gradually declines with the decrease of V_{GC} and disappears at t_2. Because the depletion layer does not form, C_{GD} is equal to C_{oxd} too. On the other hand, the collector current maintains I_L during phases I and II, and J_2 is in a static forward-bias state. Besides, there is no extra high-frequency ac signal applied to J_2. Therefore, J_2 has no capacitance effect in phases I and II. The equivalent circuit models of IGBT during phases I and II are shown in Fig. 6(b) and (c), respectively. After t_2, the depletion layer starts to grow with the increase of collector voltage, and C_{GD} is the series combination of C_{oxd} and depletion capacitance C_{dep}. In general, C_{GD} is approximate to C_{dep} in phase III for $C_{\mathrm{oxd}} >> C_{\mathrm{dep}}$. Therefore, it is concluded that C_{oxd} works in phases I and II. The expressions of gate delay duration of these two phases are studied as follows.

The gate delay duration $\Delta t_1(t_1\text{-}t_0)$ is derived in [6], i.e.,

$$\Delta t_1 = R_g(C_{\mathrm{oxd}} + C_{\mathrm{GE}}) \ln\left(\frac{V_{\mathrm{Gon}} - V_{\mathrm{Goff}}}{V_{\mathrm{GP}} - V_{\mathrm{Goff}}}\right) \quad (13)$$

where R_g is the gate resistance, V_{GP} is the miller voltage given in [17], V_{Gon} and V_{Goff} are the gate driver's turn-ON and turn-OFF voltage, respectively.

In phase II, the collector voltage rises slightly. Meanwhile, a negative feedback from V_C to V_G is established which slows down the reduction of gate voltage [15]. Assumed that in a short period Δt, the gate-emitter voltage was reduced by ΔV_{GE} ($\Delta V_{\mathrm{GE}} < 0$). According to the path of the negative feedback, it is deduced that

$$\Delta V_{\mathrm{CE}} = -g_m/C_{\mathrm{O}} \times \Delta V_{\mathrm{GE}} \quad (14)$$

$$\Delta V_{\mathrm{GE}} = -\frac{V_{\mathrm{GP}} - V_{\mathrm{Goff}}}{R_{\mathrm{g}}} \frac{1}{C_{\mathrm{GE}} + (g_m/C_{\mathrm{O}} + 1)C_{\mathrm{oxd}}} \quad (15)$$

where C_{O} is the charge extraction capacitance, it remains constant with a fixed collector current [15]. In IGBT compact models, the parameter V_{TD} is the gate-drain overlap depletion threshold voltage, When V_{CG} reaches $-V_{\mathrm{TD}}$, phase II ends. Therefore, the gate delay duration $\Delta t_2(t_2\text{-}t_1)$ satisfies

$$V_{\mathrm{ON}} + \int_0^{\Delta t_2} \frac{\mathrm{d}V_{\mathrm{CE}}}{\mathrm{d}t} - \left(V_{\mathrm{GP}} + \int_0^{\Delta t_2} \frac{dV_{\mathrm{GE}}}{dt}\right) = -V_{\mathrm{TD}}. \quad (16)$$

Taking limit and substituting (14) and (15) into (16) gives an expression of Δt_2

$$\Delta t_2 = R_g \frac{V_{\mathrm{GP}} - V_{\mathrm{TD}} - V_{\mathrm{ON}}}{V_{\mathrm{GP}} - V_{\mathrm{Goff}}} \left(\frac{C_{\mathrm{GE}}}{g_{\mathrm{m}}/C_{\mathrm{O}} + 1} + C_{\mathrm{oxd}}\right). \quad (17)$$

From (13) and (17), it is concluded that the simulated miller platform would have a more significant voltage drop and Δt_2 be shorter than the real value if the *C–V* method is used.

IV. Verification

A. Comparison of C–V and Q–V Methods

To verify the analysis of *C–V* and *Q–V* methods, four different discrete IGBT devices (A: AUIRGP4062D, B: DGTD65T60S2PT, C: IKW25N120H3, D: IXYK30N170CV1) and a power MOSFET (E: IPA60R060P7) are selected as devices under test (DUTs). In this letter, double pluse tests are set to obtain standard C_{oxd} [18]. As analyzed in Section III, C_{oxd} is active during phase II in turn-OFF transient, which is used to extract C_{oxd}. The equivalent circuit and experimental waveforms are shown in Fig. 7. Considering that v_{GE} is maintained to V_{GP}, the gate current i_G is a constant value (I_{GM})

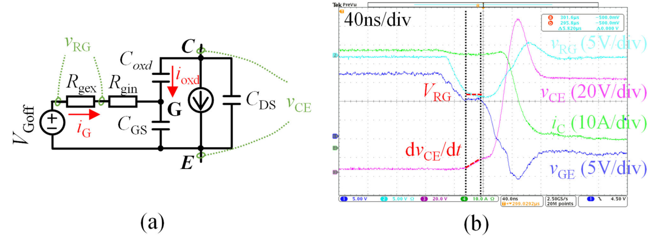

Fig. 7. (a) Equivalent circuit and (b) experimental waveforms used to extract C_{oxd} during phase II of turn-OFF transient.

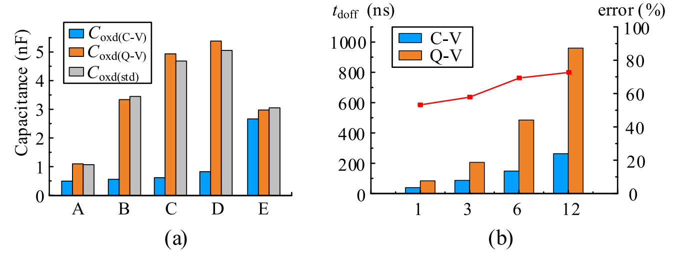

Fig. 8. Comparative results of different extracting methods. (a) C_{oxd} value. (b) Turn-OFF delay time (left *y*-axis) and the relative error of $t_{\mathrm{doff}\,(C-V)}$ (right *y*-axis) with different number of IGBT chips in parallel.

$$i_G = I_{\mathrm{GM}} = \frac{V_{Goff} - V_{\mathrm{GP}}}{R_{\mathrm{gex}} + R_{\mathrm{gin}}} \quad (18)$$

where V_{Goff} is the driver's output voltage to turn the IGBT off. Using Kirchhoff's Current Law to node G, it satisfies that

$$-I_{\mathrm{GM}} = i_{\mathrm{oxd}} = C_{\mathrm{oxd}} \frac{dv_{\mathrm{CE}}}{dt}. \quad (19)$$

In the experimental measurement, I_{GM} is transferred to the voltage across the external gate resistance

$$V_{\mathrm{RG}} = R_{\mathrm{gex}} I_{\mathrm{GM}}. \quad (20)$$

A 5.1 Ω SMD resistance was chosen to be the external gate resistance R_{gex}, and v_{RG} is measured by a 500 MHz differential probe with the range of 42 V pk. Meanwhile, v_{CE} is measured by a 500 MHz voltage probe with a range of 300 V. Combining (19) and (20), $C_{\mathrm{oxd(std)}}$ is extracted by

$$C_{\mathrm{oxd(std)}} = -\frac{V_{\mathrm{RG}}}{R_{\mathrm{gex}}} \frac{1}{dv_{\mathrm{CE}}/dt}. \quad (21)$$

Then, C_{oxd} extracted by different methods are compared in Fig. 8(a). It can be seen that $C_{\mathrm{oxd}(C-V)}$ is significantly smaller than $C_{\mathrm{oxd(std)}}$ while $C_{\mathrm{oxd}(Q-V)}$ is close to $C_{\mathrm{oxd(std)}}$ as for IGBT. However, the extracted results of the three methods share similar values as for power MOSFET.

B. Effect of C_{oxd} on Turn-off Delay Time

The IGBT model supported by PSpice library is chosen to evaluate the influence of C_{oxd} on IGBT modeling, the detailed

TABLE I
PARAMETERS OF THE IGBT MODEL

Parameter	Value	Units	Parameter	Value	Units
TAU	7.1 u	sec	JSNE	3e-12	A/cm^2
KP	4	A/V^2	KF	4.5	none
AREA	1e-5	m^2	VTD	-10	V
AGD	5e-6	m^2	CGS	2.66e-8	F/cm^2
VT	6.2	V	COXD	1.23e-8 (C–V) 9.8e-8 (Q–V)	F/cm^2
NB	2e14	1/cm^3			

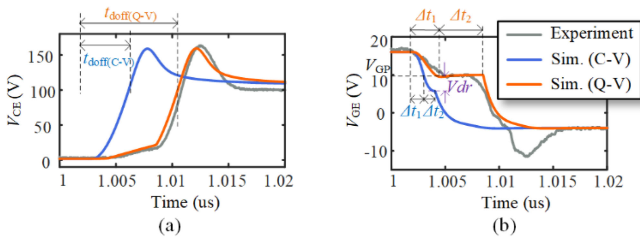

Fig. 9. Simulated and experiment turn-OFF waveforms of (a) V_{CE} and (b) V_{GE}.

TABLE II
EXPERIMENT AND SIMULATION RESULT OF T_{dOFF}

	Δt_1(ns)	Δt_2(ns)	t_{doff} (ns) /relative error
Experient	29.5	38.0	86.0
Sim. (C–V)	9.0	10.2	39.4 / **54.2%**
Sim. (Q–V)	24.8	42.8	84.0 / **2.3%**

description of it is in [19]. The Infineon IGBT IKW25N120H3 is selected as DUT. Model parameters are extracted from its characteristics curves in datasheet, as given in Table I. No extra intelligent algorithm for parameter optimization is adopted. The turn-OFF waveforms of simulation and experiment are shown in Fig. 9. It is seen that the simulated turn-OFF waveform with $C_{\mathrm{oxd}(C-V)}$ has a much shorter t_{doff} and a more evident voltage drop (V_{dr}) during miller platform. The concrete value and relative error are given in Table II. Moreover, simulations with different numbers of devices in parallel are carried out. The results are concluded in Fig. 8(b). It suggests that the error of the *C*–*V* method augments with the rise in the quantity of paralleled IGBT chips. The absolute error of t_{doff} caused by the *C*–*V* method reaches 697 ns when 12 chips are in parallel, which might misguide the design of dead time significantly.

V. CONCLUSION

In this letter, two datasheet-driven methods to extract C_{oxd} of IGBT are analyzed and compared. It is found that C_{oxd} is underestimated seriously by the *C*–*V* method, and it will cause a significant error in IGBT modeling. The Infineon IGBT IKW25N120H3 was selected as an example. Results show that the turn-OFF delay time is underestimated by 54.2% when the *C*–*V* method is applied. Moreover, the error is more noticeable with multi-chips connected in parallel. In the situation of 12 chips in parallel, the $t_{\mathrm{doff}(C-V)}$ is 697 ns shorter than $t_{\mathrm{doff}(Q-V)}$. The underestimated t_{doff} will lead to a shorter design margin of dead time, which might cause reliability issues because of shoot-through problem. Consequently, it is encouraged to use the *Q*–*V* method rather than the *C*–*V* method to extract C_{oxd} in IGBT modeling.

Furthermore, the conclusion of this letter might be suitable for SiC IGBT too. It is expected that this would also be an important issue in SiC IGBT modeling, which needs to be studied further.

REFERENCES

[1] Q. Cheng, Z. J. Wang, G. Xin, and X. Shi, "Datasheet driven switching loss, turn-on/off overvoltage, di/dt and dv/dt prediction method for SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9551–9570, Aug. 2022.

[2] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, "Datasheet driven silicon carbide power MOSFET model," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, May 2014.

[3] S. Perez et al., "A datasheet driven unified Si/SiC compact IGBT model for N-channel and P-channel devices," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8329–8341, Sep. 2019.

[4] A. U. Rashid, M. M. Hossain, A. I. Emon, and H. A. Mantooth, "Datasheet-driven compact model of silicon carbide power MOSFET including third-quadrant behavior," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11748–11762, Oct. 2021.

[5] B. Shi, Z. Zhao, and Y. Zhu, "Piecewise analytical transient model for power switching device commutation unit," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5720–5736, Jun. 2019.

[6] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, "Junction temperature extraction approach with Turn-off delay time for High-voltage high-power IGBT modules," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5122–5132, Jul. 2016.

[7] A. Hefner and S. Bouche, "Automated parameter extraction software for advanced IGBT modeling," in *Proc. 7th Workshop Comput. Power Electron.*, 2000, pp. 10–18.

[8] R. Withanage, N. Shammas, S. Tennakoorr, C. Oates, and W. Crookes, "IGBT parameter extraction for the Hefner IGBT model," in *Proc. 41st Int. Univ. Power Eng. Conf.*, 2006, pp. 613–617.

[9] A. T. Bryant, X. Kang, E. Santi, P. R. Palmer, and J. L. Hudgins, "Two-Step parameter extraction procedure with formal optimization for physics-based circuit simulator IGBT and PIN diode models," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 295–309, Mar. 2006.

[10] X. Yang, M. Otsuki, and P. R. Palmer, "Physics-based insulated-gate bipolar transistor model with input capacitance correction," *IET Power Electron.*, vol. 8, no. 3, pp. 417–427, 2015.

[11] X. Kang, E. Santi, J. L. Hudgins, P. R. Palmer, and J. F. Donlon, "Parameter extraction for a physics-based circuit simulator IGBT model," in *Proc. IEEE Appl. Power Electron. Conf.*, 2003, pp. 946–952.

[12] K. Chen, Z. Zhao, L. Yuan, T. Lu, and F. He, "The impact of nonlinear junction capacitance on switching transient and its modeling for SiC MOSFET," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 333–338, Feb. 2015.

[13] B. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2010.

[14] S. Sze and K. K. Ng, *Physics of Semiconductor Devices*. 3rd ed., Hoboken, NJ, USA: Wiley, 2006.

[15] A. Bryant et al., "Investigation into IGBT dV/dt during turn-off and its temperature dependence," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 3019–3031, Oct. 2011.

[16] Reference Guides, Keysight, "Step by step measurement handbook for measuring datasheet parameters of IGBT," Santa Rosa, CA, USA, 2014. Accessed: Jul. 28, 2022. [Online]. Available:https://www.keysight.com.cn/cn/zh/assets/9018-03869/reference-guides/9018-03869.pdf

[17] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "Switching-behavior improvement of insulated gate-controlled devices," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 645–653, Jul. 1997.

[18] Y. Duan, "Research on the Lumped-charge model and parallel modeling of high power IGBTs," 2019.

[19] A. R. Hefner, Jr., *Semiconductor Measurement Technology: INSTANT - IGBT Network Simulation and Transient Analysis Tool*, Special Publication (NIST SP), Nat. Inst. Standards Technol., Gaithersburg, MD, 1992.