Boosting Wide-Range Conversion Efficiency With Dynamic Voltage-Domain Stacking

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***Abstract*—This article presents dynamic voltage-domain stacking, which incorporates the attractive efficiency benefits of voltage-domain stacking into a wide-input-range conversion system. This is achieved by combining two novel switched-capacitor converter topologies with an integrated finite-state machine into a highly reconfigurable system. First, a zooming gearbox converter efficiently enables a wide input range while only implementing three conversion ratios. Second, a reconfigurable ladder converter continuously compensates for imbalance between the dynamically stacked voltage domains. A prototype has been fabricated in a 40-nm baseline CMOS technology to provide a stable supply voltage to four loads across an input voltage range from 4 V down to 0.55 V. Measurements show a best-in-class average efficiency of 80.1% and a peak efficiency of 92.1%.**

***Index Terms*—DC–DC converter, fully integrated, reconfigurable, switched capacitor (SC), voltage-domain stacking (VDS), wide input range.**

I. Introduction

SUPPLY independence is one of the main features in today's and future electronic devices. Therefore, considerable research attention has been focused on small-form energy harvesters and accompanying conversion circuits [1], [2]. But no matter the design effort, the output power of energy harvesters will always be relatively low and environmentally dependent. To bypass both the issues, the harvested energy could be continuously accumulated on a storage device. Once this energy storage device is sufficiently charged, it can deliver the accumulated energy in a short peak of high power to the duty cycled load, as illustrated in Fig. 1 [3]–[5]. Consequently, energy storage provides a stable supply with high power from energy harvesters and, therefore, unlocks supply independence to many more small-form-factor devices.

Whereas the accumulated energy could be temporally stored on a battery, a storage capacitor can handle more charging cycles and is better suited for integration. However, because the load discharges the storage capacitor (C_{store}) when active, the voltage across C_{store} (V_{cap}) drops from V_{high} to V_{low}, as shown in Fig. 1.

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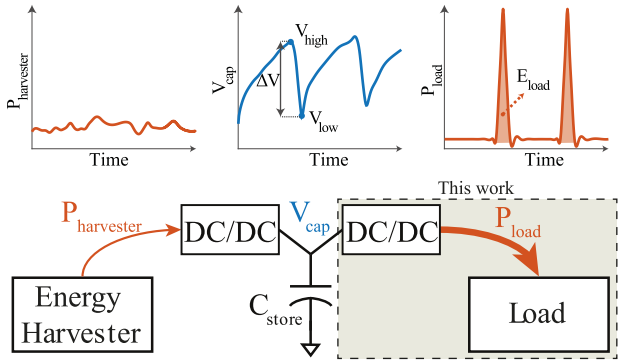

Fig. 1. Power flow and voltage swing in capacitive energy storage applications.

This varying V_{cap} implies the need for two dc–dc converters to guarantee a stable voltage at the harvester and the load. While increased losses of the converter at the harvester side demand a larger harvester, the losses of the converter at the load side determine the minimal requirements for the storage device. In (1), these losses are characterized as the average efficiency of the converter ($\overline{\eta}$), while the available energy is determined by the quadratic energy–voltage relation on C_{store}

$$E_{\text{load}} = \frac{C_{\text{store}}\left(V_{\text{high}}^2 - V_{\text{low}}^2\right)}{2} \cdot \overline{\eta}. \tag{1}$$

To minimize the cost determining C_{store} for a given E_{load}, one should maximize $\overline{\eta}$ and deeply discharge the storage capacitor, i.e., increasing ΔV on C_{store}. Because C_{store} is connected to the input of the converter, this requires a converter with a wide input voltage range (ΔV_{in}) and a high $\overline{\eta}$ across this range. However, current state-of-the-art fully integrated converters fail to combine both. The most popular monolithic approach is the switched-capacitor (SC) gearbox converter, wherein many conversion ratios are combined in a single converter. In such converters, the most efficient conversion ratio can be chosen based on the actual input voltage. However, owing to their increased complexity with more ratios, they only achieve either a mediocre average efficiency [6]–[12] or a rather limited input range [13]–[16].

To boost the wide-range efficiency of fully integrated converters, this article introduces dynamic voltage-domain stacking (DVDS) [17]. The DVDS topology extends conventional voltage-domain stacking (VDS), also commonly called charge recycling, which is proven to be highly efficient with reported

TABLE I
OVERVIEW OF USED ACRONYMS AND PARAMETERS

Acronyms		Parameters	
VDS	Voltage-domain Stacking	N	Number of stackable loads
DVDS	Dynamic voltage-domain stacking	S	Number of stacked voltage domains
DLS	Dynamic-load Stack	M	Number of loads in each voltage domain
(M)IS	(Movable) Input Stage		$S = N/M$
FSM	Finite-State Machine		
(i)VCR	(ideal) Voltage Conversion Ratio		

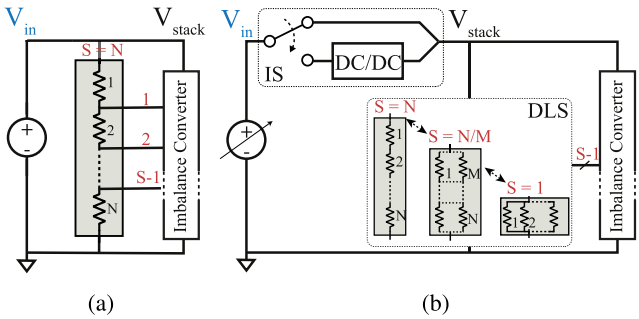

Fig. 2. Comparison between (a) conventional VDS and (b) proposed dynamic VDS.

efficiencies up to 99.6% [18]–[24]. Both DVDS and VDS split the total load power in approximately equal parts and stack them on top of each other. The stacked loads may include passive devices (e.g., LEDs), digital circuitry with, e.g., multicore operation [24]–[27], or analog components with similar quiescent currents as shown in [28] with stacked trans-impedance amplifiers (TIAs). In contrast to VDS, DVDS stacks the loads either more in series or in parallel, based on the actual V_{in}. As such, DVDS allows a wide ΔV_{in} while still taking advantage of the efficiency benefits of VDS. Consequently, DVDS boosts $\overline{\eta}$ and outperforms state-of-the-art wide ΔV_{in} converters.

Whereas our previous work [17] briefly introduces the DVDS principle, this article delivers more insight into the design decisions and the implementation details. Section II first explains DVDS. Then, Section III reveals some system optimizations. Next, Section IV elaborates on the implementation details of the key enablers of DVDS. The control strategies are discussed in Section V, while Section VI presents the measurements on a 40-nm prototype and compares them with the state of the art. Finally, Section VII concludes this article.

II. PROPOSED DYNAMIC VOLTAGE-DOMAIN STACKING

In the continuation of this article, three parameters and several acronyms will be regularly used to describe the proposed system. An overview is provided in Table I.

A. Voltage-Domain Stacking

Fig. 2(a) illustrates how VDS splits the total load power in N approximately equal parts and stacks them in series [18]. The resulting voltage at the top of the S stacked voltage domains (V_{stack}) is the sum of all the voltage domains

$$V_{\text{stack}} = \sum_{s=1}^{S} V_{\text{domain},s} \quad \text{with} \begin{cases} S = N \text{ (VDS)} \\ S \leq N \text{ (DVDS)} \end{cases}. \tag{2}$$

With conventional VDS, V_{in} equals V_{stack}, which eliminates the need for a converter and enables a theoretically lossless $S:1$ conversion. Such a lossless conversion is, however, only possible under the condition that all the stacked loads draw identical current. In order to maintain the current balance, any current mismatch requires to be compensated for by sourcing (or sinking) the shortage (or excess) of current on the intermediate nodes. Therefore, VDS always implements a dc–dc converter, which compensates for imbalance, as shown in Fig. 2(a) [19], [20], [22]–[24]. Although inducing losses, this converter barely degrades the conversion efficiency as it only has to convert the imbalance power, which is a fraction of the total load power. Consequently, VDS is the ideal candidate for a highly efficient conversion. The direct connection between V_{in} and V_{stack}, however, limits VDS to a fixed V_{in}.

B. Dynamic Voltage-Domain Stacking

DVDS transforms the highly efficient VDS into an efficient wide ΔV_{in} conversion system. Fig. 2(b) depicts the two modifications to conventional VDS in order to enable DVDS: the input stage (IS) and the dynamic load stack (DLS).

The first modification is the IS, which allows a ΔV_{in} without altering V_{stack} by implementing a switch and a converter. In case V_{in} equals V_{stack}, the switch provides a direct connection between both the nodes, as in conventional VDS. Because such a direct connection leaves the converter with associated losses idle, it is highly efficient and, thus, desirable. In the other case, when V_{in} differs from V_{stack}, the switch cuts the direct connection, and the converter converts V_{in} into the desired V_{stack}. This comes, however, at the cost of a degraded efficiency since all the load power has to pass through this converter. Moreover, a wider gap between V_{in} and V_{stack} further degrades $\overline{\eta}$ due to its increased conversion range and associated complexity. Accordingly, a tradeoff between $\overline{\eta}$ and ΔV_{in} still emerges.

The second modification in Fig. 2(b) is the DLS, which overcomes this tradeoff and enhances $\overline{\eta}$ without reducing ΔV_{in}. Instead of stacking N loads in series ($S = N$), the proposed DLS adapts the number of stacked voltage domains (S) when V_{in} changes, by placing loads in parallel within the same voltage domain (M). By changing S, the DLS allows V_{stack} to discretely track V_{in}, which has a twofold efficiency advantage, as plotted in Fig. 3. First, the DLS continuously minimizes the voltage gap between V_{in} and V_{stack}. This tackles the earlier discussed tradeoff between $\overline{\eta}$ and ΔV_{in}. Second, the green stars highlight how the DLS enables multiple V_{in} ranges, where a highly efficient direct connection between V_{in} and V_{stack} is allowed, instead of only one in the system without a DLS. These multiple highly efficient V_{in} ranges further boost the average efficiency.

While multiple V_{in} ranges are enabled for a direct connection, the width of these ranges depends on how much margin (V_{margin}) the voltage domains tolerate on their nominal supply (V_{dd}). Because V_{stack} is the sum of all the domains (2), this margin also

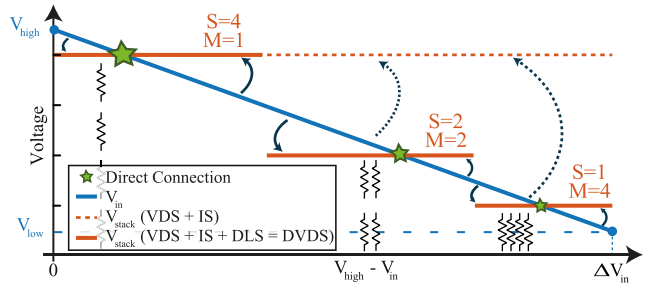

Fig. 3. Comparison of V_{stack} over a wide ΔV_{in} between a fixed and a DLS with four loads.

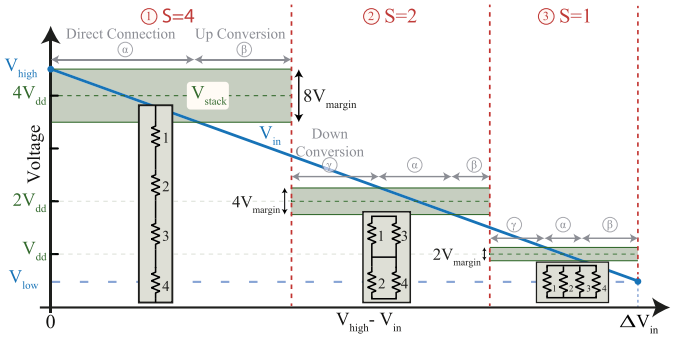

Fig. 4. DVDS conversion system supplying $N = 4$ loads from a discharging storage capacitor with annotated load (1–3) and conversion (α-γ) configurations.

sets an upper and lower boundary for V_{stack} (3). Accordingly, it also extends the width of the V_{in} ranges, allowing a direct connection between V_{in} and V_{stack}

$$S \cdot V_{dd} - S \cdot V_{\text{margin}} \leq V_{\text{stack}} \leq S \cdot V_{dd} + S \cdot V_{\text{margin}}. \quad (3)$$

To visualize the effect of V_{margin} and the operation of DVDS, Fig. 4 illustrates the working principle with four loads. Three different load configurations exist: 1) all the loads in series ($S = N$); 2) a 2-by-2 series/parallel configuration ($S = N/2$); and 3) all the loads in parallel ($S = 1$). Following (3), each load configuration has its own range for V_{stack}, as indicated in Fig. 4. Besides three load configurations, three conversion states can be distinguished. The first and preferred state (α) is the direct connection between V_{in} and V_{stack}, omitting the input converter. Second (β), once V_{in} dropped below the lower limit of V_{stack}, the input switch connects V_{in} to the input converter, which upconverts V_{in} to a stable V_{stack}. Third, to minimize the voltage gap between V_{in} and V_{stack}, the system switches to the next load configuration with lower V_{in}. This introduces the third and final conversion state (γ), where the input converter performs a downconversion. As shown in Fig. 4, these steps are repeated until all the loads are placed in parallel ($S = 1$ and $M = N$). To span an even wider ΔV_{in}, DVDS can be extended by increasing the amount of stackable loads N.

III. System-Level Optimizations

A. Zoom Approach

Although the DLS minimizes the voltage gap between V_{in} and V_{stack}, the IS has to interface directly with the wide ranging V_{in},

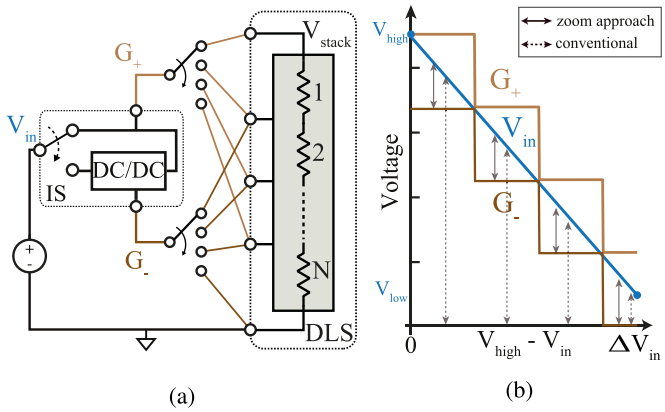

Fig. 5. (a) Conceptual implementation of the Zoom approach with (b) associated waveforms, showing how it reduces the voltage range with a factor $N = 4$.

which deteriorates the performance. First, a wide ΔV_{in} requires the input converter to implement many different ideal voltage conversion ratios (iVCRs) to operate over such a wide voltage range [29]. Second, the high absolute voltages prohibit the use of the preferred thin-oxide switches and high-density capacitors since their breakdown voltage might be exceeded.

Therefore, this article presents a conversion topology, based on zoom analog to digital converters (ADCs), which virtually reduces the input range with a factor N. Fig. 5 illustrates how a movable voltage domain, containing the input converter, is dynamically placed in parallel with one of the stacked voltage domains from the DLS. This movable voltage domain tracks the decreasing V_{in} by connecting to a lower voltage domain of the DLS once V_{in} crosses its bottom terminal (G_-). As such, V_{in} is always kept between the movable supply rails (G_+/G_-), and one can refer it to G_- instead of to the ground, as highlighted by the arrows in Fig. 5(b). Compared with a zoom ADC, the input converter performs the fine conversion, while the DLS performs the coarse conversion. Thanks to the zoom approach, the DVDS system reuses each VCR of the input converter N times and virtually reduces the input range of the input converter with the same factor. As a result, the DVDS system is still able to convert the same ΔV_{in} with the same resolution, but with a less complicated and more efficient converter. Because of its movable supply rails, the IS is referred to as the movable input stage (MIS) in the continuation of this article.

Similar to the input converter, the input switch is exposed to the wide ΔV_{in} implying the need for a high-voltage device. However, since all the load current flows through this switch, R_{on} should be minimized and a thin-oxide implementation is preferred. Therefore, the input switch also benefits from the virtually reduced voltage range in the MIS, allowing a thin-oxide implementation.

B. Flying Capacitor Allocation

In any fully integrated SC converter, the flying capacitors dominate the area and the cost and, consequently, limit either the efficiency or the power-handling capacity [30]. Therefore,

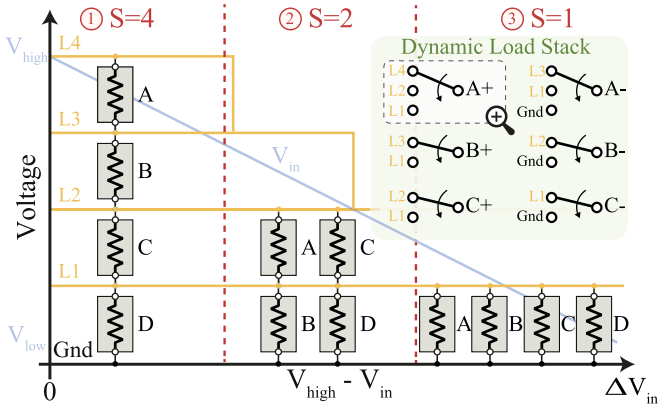

Fig. 6. Global levels $L_{1..4}$ versus V_{in} and how they are used by the DLS to set the different load configurations.

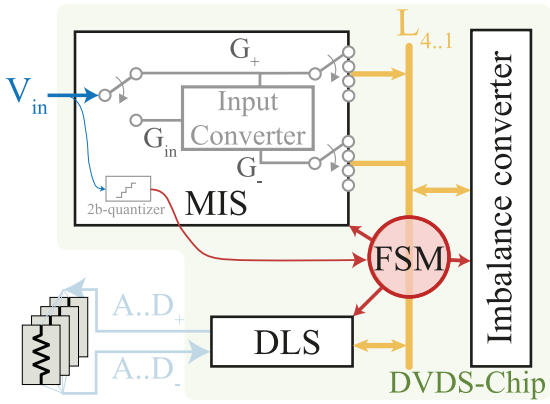

Fig. 7. Structure diagram of the DVDS system.

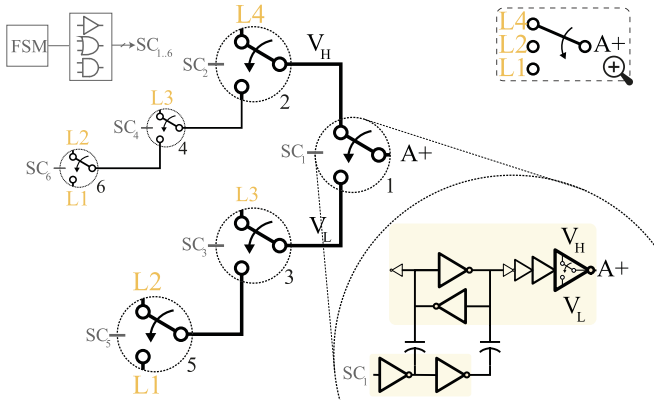

Fig. 8. Basic switch implementation (bottom right) and how it is used to build configuration switches to connect to the global levels as in the DLS in Fig. 6.

the usage of the costly capacitors in both the input and imbalance converters should be maximized.

The earlier discussed zoom approach is a perfect example of an optimized flying capacitor allocation. It places all the capacitors of the input converter *where the conversion has to be performed* is crucial info to determine which of the four voltage domains is talked about. Furthermore, it limits the voltages across the capacitors, allowing a high-density implementation.

The imbalance converter, on the other hand, has to regulate all the stacked voltage domains continuously, prohibiting the zoom approach. A convenient solution for an imbalance converter with N stacked loads is a ladder converter with $N-1$ dc nodes [23]. However, because DVDS gradually reduces the number of stacked voltage domains (S), there is no need to always generate N stacked voltage domains or to compensate imbalances between them. Therefore, instead of implementing a conventional ladder converter with fixed $N-1$ dc nodes, this article introduces a reconfigurable ladder converter with variable $S-1$ dc nodes. To reduce the number of dc nodes, the flying capacitors are dynamically placed in parallel, similar to the loads in the DLS. As a result, all the available capacitance is always placed in parallel with the stacked loads and not partially left idle. Section IV-B elaborates on the implementation of this converter.

C. Global Stacked Voltage Domains

Both the MIS and the imbalance converter rely on the stacked voltage domains to operate. A trivial option seems to directly use the stacked voltage domains from the DLS for this. However, a change in the load configuration would, then, result in abrupt supply variations in system, risking excessive power losses, malfunction, or even breakdown.

To prevent this, the presented system generates N global levels ($L_{1..N}$) from which each block controls its own supply. To illustrate this, Fig. 6 shows how the DLS uses these levels to set the different load configurations in a system with four loads. The graph in Fig. 6 also reveals that the global levels L_4 and L_3 are not constant over the whole V_{in} range. This is due to the optimized flying capacitor allocation of the imbalance converter because it stops regulating domains L_4/L_3 and L_3/L_2 once not used anymore.

IV. Implementation Details

In the conceptual overview of Fig. 7, one can distinguish the three major blocks of DVDS: 1) the DLS; 2) the imbalance converter; and 3) the MIS. Internally, the system creates and regulates the four global levels ($L_{1..4}$) from V_{in}, which are used as a supply by each of these blocks. In addition, a finite-state machine (FSM) has been added to the system, which determines, based on the actual value of V_{in}, the optimal configuration for each block, as will be discussed in Section V-B.

A. Configuration Switches

As discussed earlier, all the blocks require configuration switches to properly connect to the global levels: the MIS to connect its supply rails (see Fig. 5), the DLS to set the load configurations (see Fig. 6), and the imbalance converter to connect its internal dc nodes (discussed later). Two major design challenges arise concerning the switch implementation: 1) high blocking voltages, and 2) nonconstant global levels L_4 and L_3. To tackle both, all the configuration switches use the same basic switch, which is depicted in the corner of Fig. 8.

In this basic switch, a capacitive levelshifter first shifts the switch control signal (SC_x) to the high-voltage domain (V_H/V_L). This signal is then fed into an inverter chain of which

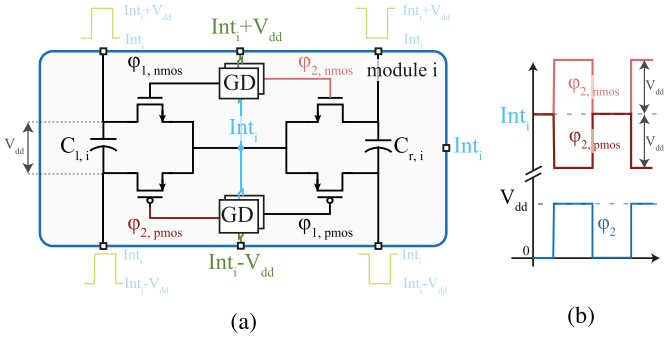

Fig. 9. (a) Implementation details of one module of the reconfigurable imbalance converter with (b) associated waveforms.

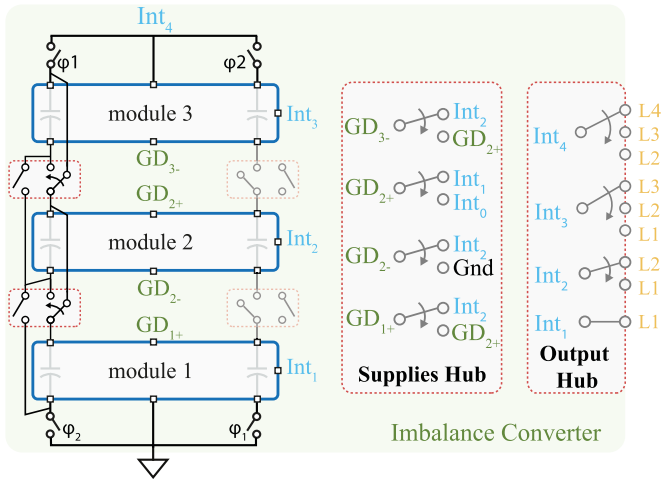

Fig. 10. Reconfigurable imbalance converter with the switches between the modules, the supplies hub, and the output hub to connect to the global levels.

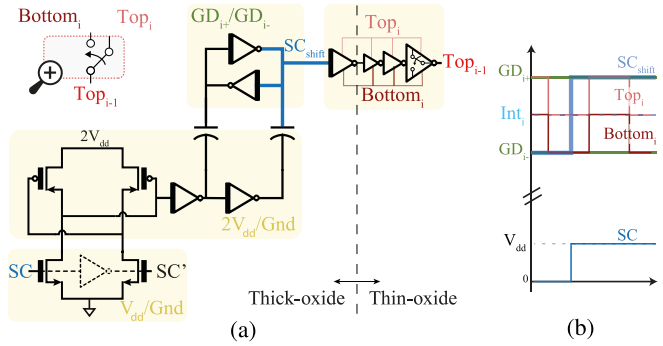

Fig. 11. (a) Implementation details of the configuration switches with floating nodes to interconnect the modules of the imbalance converter of Fig. 10 with (b) associated waveforms.

the final stage acts as the actual switch and connects the output to either V_L or V_H. The thin-oxide devices in the inverters limit the blocking voltage of this basic switch to V_{dd}. Therefore, several basic switches are cascaded to withstand higher blocking voltages. Fig. 8 shows the implementation of one of the configuration switches in the DLS. It illustrates how three basic switches (1-3-5) are cascaded to shield L_1 (V_{dd}) from the output of the switch (A+), which can be as high as $4V_{dd}$ when all the loads are stacked in series.

Each basic switch needs a V_{dd}-wide dc supply (V_H/V_L) for the inverters. To guarantee this, even more switches are necessary due to the nonconstant global levels L_4 and L_3. Therefore, any basic switch with its V_H connected to either L_4 or L_3 requires an interchangeable V_L. Accordingly, in Fig. 8, switch 4 guarantees a V_{dd}-wide supply for switch 2, but, since switch 4 is on its turn connected to L_3, switch 6 is required to select its V_L.

B. Reconfigurable Imbalance Converter

The imbalance converter is a symmetrical ladder converter as in [23], which can be implemented by stacking identical modules. Fig. 9 depicts such a module in which one can distinguish two flying capacitors and four power switches with gate drive (GD) circuitry. Whereas the top and bottom terminals of both the flying capacitors swing with an amplitude of V_{dd}, each module also generates an internal dc node Int_i.

This dc node simplifies the GD circuitry since, now, only a V_{dd} offset to this nonfloating node is required to drive the switches, as illustrated in Fig. 9(b). Because the internal dc nodes of adjacent stacked modules are V_{dd} apart from each other, $Int_i \pm V_{dd}$ levels are readily available. Combining these levels with Int_i enables two V_{dd}-wide supplies, which can be used to drive the gates with a simple buffer chain. As such, the GD circuit is identical to the driving circuit of the basic switch in Fig. 8 with a capacitive levelshifter and buffer chain.

To optimize the flying capacitor allocation, as discussed earlier, this article presents a reconfigurable ladder converter of which the modules can be gradually placed in parallel. Therefore, the red-dotted lines in Fig. 10 reveal three extra blocks, besides the three modules for a conventional ladder converter. As discussed earlier, the dc nodes from adjacent modules could be used to supply the GD circuits since they are either V_{dd} higher or lower than the dc node in the actual module. However, in the reconfigurable converter, these modules change positions. Therefore, a first modification is the addition of the supply hub, which selects the appropriate dc nodes for the GD circuits in each configuration. A second modification is the output hub, which connects the internal dc nodes ($Int_{4..1}$) to the proper global levels of the DVDS system ($L_{4..1}$) based on the actual configuration of the imbalance converter and the global levels. A final modification is the insertion of configuration switches in between the modules to actually connect the modules either in series or in parallel. When all four loads are stacked in the DLS, the three modules in the converter are connected in series and regulate the four stacked voltage domains between Int_4 and ground.

As can be seen in Fig. 10, the switches in between the modules are connected to the terminals of the flying capacitors. Consequently, those switches do not have dc terminals, which is a requirement to implement them with the earlier discussed basic switches. Therefore, a new type of configuration switches is proposed to allow floating terminals, as shown in Fig. 11 for a switch between module $i-1$ and i. Herein, the swing

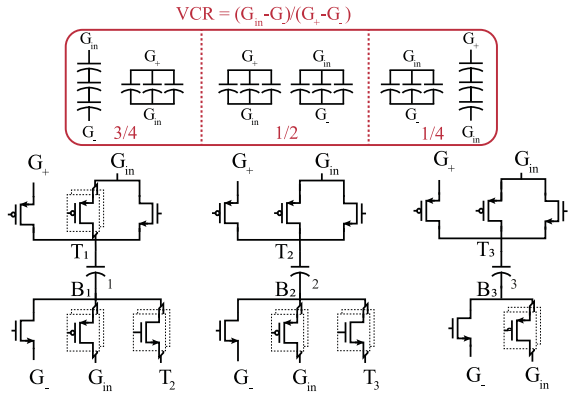

Fig. 12. Topologies of the three iVCRs and the transistor implementation of the gearbox-type input converter.

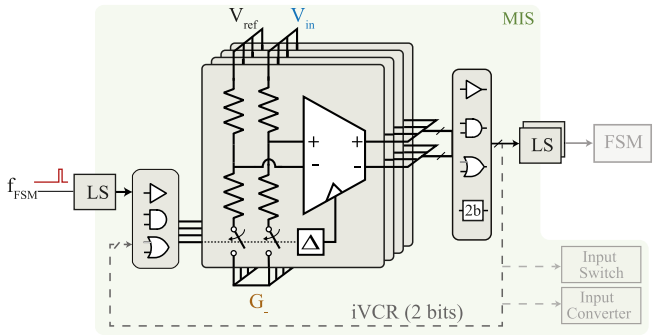

Fig. 13. Overview of the MIS in which a 2-bit quantizer senses V_{in} to trigger the FSM and set the iVCR.

of the control signal (SC) is first doubled before being shifted by a thick-oxide capacitive levelshifter toward the $2V_{dd}$-wide voltage domain $\text{GD}_{i+}/\text{GD}_{i-}$. As seen earlier, these supplies are already available in module i to drive the power switches. The output of this levelshifter ($\text{SC}_{\text{shifted}}$) is, then, either the highest or lowest voltage of one of the toggling switch terminals Top_i or Bottom_i, as shown in Fig. 11(b). Therefore, it can be used as an input of an inverter chain between these toggling terminals. Although the first stage of this chain contains thick-oxide devices to prevent excessive gate–drain voltages, the rest of this chain is implemented with thin-oxide devices. Conclusively, these new configuration switches again benefit from the preferred thin-oxide devices with a similar implementation as the ones with dc terminals.

C. Movable Input Stage

As already hinted in Fig. 7, the MIS contains three circuits in a floating deep n-well (DNW) domain: the input switch, the input converter, and a 2-bit quantizer. The input switch connects V_{in} either directly to the load stack, via G_+ and the global levels, or first to the input of the input converter (G_{in}).

The input converter is a gearbox-type converter to efficiently convert G_{in} to G_+. It implements three equally spaced iVCRs (3/4, 1/2, and 1/4) of which the different topologies are shown in the top half of Fig. 12. Enabling these topologies requires three flying capacitors and 14 ideal power switches. The transistor implementation in the bottom half of Fig. 12, however, reveals 23 transistors. Based on the available overdrive voltage, which may heavily vary due to G_{in} ranging from supply (G_+) to ground (G_-), the ideal switches have been implemented differently. A first category contains the switches connected to either G_+ or G_-. For these switches, an implementation with a single pMOS or nMOS device is sufficient since the nominal overdrive voltage is available. A second category contains the switches, which should be able to connect G_{in}, while its voltage level is near G_+ or G_-. To provide sufficient overdrive voltage in both the situations, these switches have been implemented as transmission gates. Finally, the switches operating for mid-range G_{in} and the ones connected to the internal nodes T_2/T_3 have been implemented with two devices in parallel, of which the second one is four times wider. Depending on the iVCR, being a measure for the actual G_{in}, either one or both switches are activated. As such, a simple buffer chain between G_+ and G_- is sufficient to drive the gates of all the power switches in the input converter, avoiding an area-consuming bootstrap capacitor or complex gate driveControl circuitry.

The third circuit in the MIS is the 2-bit quantizer. As explained earlier, the actual value of V_{in} determines in which configuration the DVDS system should operate. Therefore, four clocked comparators quantize the input, as shown in Fig. 13. Although this simple quantizer only reveals a 2-bit resolution, it can accurately track V_{in} across the wide ΔV_{in} because it benefits from the zoom approach. Likewise the iVCRs of the input converter, the initially limited resolution is reused in each of the N voltage domains. Within each voltage domain, the four $V_{dd}/4$-separated reference levels correspond to the four configurations of the input switch and the converter: a direct connection, or an iVCR of 3/4, 1/2, or 1/4. Therefore, the output of this quantizer is directly used in the MIS to set the configuration of the input switch and converter, before being shifted down to the logic voltage domain where it triggers the FSM. To limit the current through the resistive dividers in the quantizer, switches have been added in series, while the duty cycle of the applied clock signal (f_{FSM}) is limited to only 1 μs, being 0.1% of the clock period.

V. Control

The presented DVDS system integrates three clocked closed-loop controls: two to control the switching frequency of each converter (f_{gear} and f_{ladder}), and a third one to manage the states of all the different blocks (f_{FSM}).

A. Frequency Control

As discussed earlier, both V_{stack} and the voltage of each voltage domain have to be within margins. Therefore, the switching frequency of the input and imbalance converter is tuned to keep these voltages within their margins. For both the converters, an inherently stable pulse-skipping frequency controller is used in which a clocked comparator checks the respective levels against an upper and lower boundary [30].

On the one hand, the controller of the input converter regulates V_{stack} to be within its boundaries (3). But since V_{stack} is always discharged by the load, it only decreases and cannot exceed its

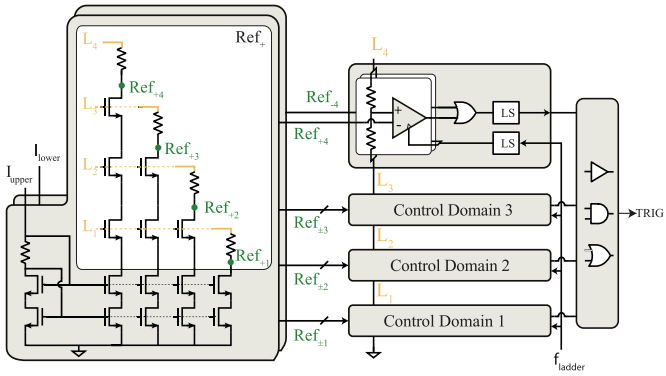

Fig. 14. Double-bound frequency controller of the imbalance converter in four domains with on-chip reference generation.

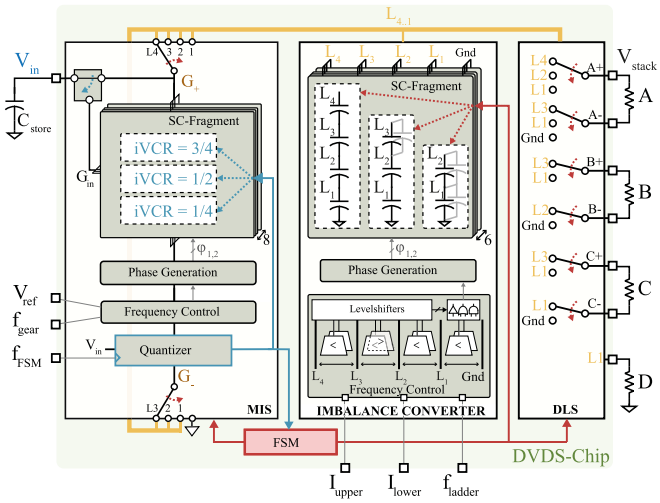

Fig. 15. System overview of the implemented DVDS system.

upper boundary. Therefore, a controller with a single reference, namely, the lower boundary of V_{stack} (V_{ref}), is sufficient. When the clocked comparator detects that V_{stack} has dropped below this boundary, it repeatedly toggles the input converter, transferring charge from V_{in} to V_{stack} until V_{stack} rises again above V_{ref}. The input converter has eight time-interleaved fragments to reduce the voltage ripple. Since the fragments are designed for a maximal switching frequency of 62.5 MHz, the comparator operates at 1 GHz.

On the other hand, the frequency controller of the imbalance converter regulates the four voltage domains to be within $V_{dd} \pm V_{\text{margin}}$. Contrary to V_{stack}, each domain may rise above or drop below its boundaries due to imbalance. Therefore, a frequency controller is required, which compares each of the four voltage domains to both the upper and lower boundaries, resulting in 4×2 references and comparators. With the same 1-GHz clock, the switching frequency of the six time-interleaved fragments may reach up to 83.3 MHz.

Fig. 14 shows the resulting frequency controller for the imbalance converter with two distinguishable parts. The right half of Fig. 14 illustrates how, in each voltage domain, two clocked comparators (f_{ladder}) check whether the domain is still within margins: one comparator for the upper boundary (Ref_+) and one for the lower boundary (Ref_-). When at least one of the eight comparators toggles, the combined TRIG signal repeatedly triggers the imbalance converter, redistributing the charge imbalance until all the voltage domains are again balanced and within margins.

The left half of Fig. 14 shows the circuit generating the eight references: four upper (Ref_+) and four lower boundaries (Ref_-). For each reference, a current mirror forces a current to flow from the supply of the stacked domain ($L_{1..4}$) through a resistor. The voltage across this resistor can be tuned with I_{upper} or I_{lower} and is a metric for $V_{dd} \pm V_{\text{margin}}$. As a result, the bottom terminals of the resistors, Ref_+ or Ref_-, can be used as references for the comparators.

B. State Control

Fig. 15 overviews the implemented DVDS system with the three major blocks: the MIS, the imbalance converter, and the DLS. The dotted arrows indicate the different configurations within each block. Besides the three load configurations of the DLS, both the imbalance and input converters also have three states determining the number of dc nodes and the iVCR, respectively. In addition, the MIS has four possible connections to the global levels for its supply rails (G_+/G_-). The input switch, finally, has two states: either connecting V_{in} directly to the global levels or to the input of converter (G_{in}).

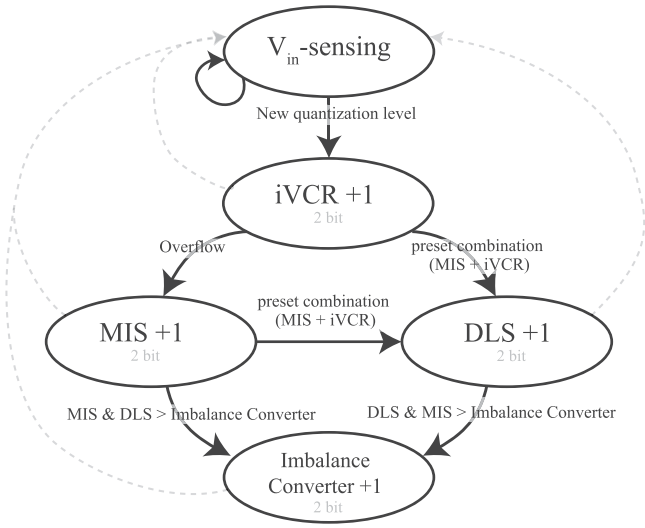

Fig. 16. Decision tree of the FSM, which is implemented with four 2-bit counters.

To prevent breakdown due to unacceptable state combinations and to guarantee proper functionality, a central autonomous FSM sets the states of each block. Therefore, the FSM implements four 2-bit counters which may trigger each other, as indicated in Fig. 16. Any counter update is initiated from the default state, in which V_{in} is periodically quantized. Once the quantization level changes, the FSM updates the iVCR of the input converter to efficiently convert V_{in} to G_+. When this iVCR counter overflows, the input converter cannot bridge the gap anymore. Therefore,

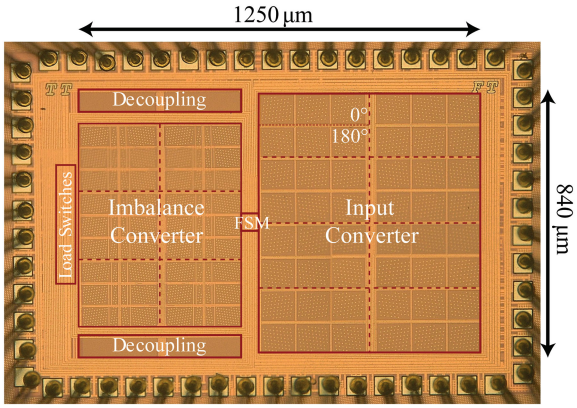

Fig. 17. Chip micrograph of the 40-nm CMOS DVDS implementation with 1.05-mm^2 active area.

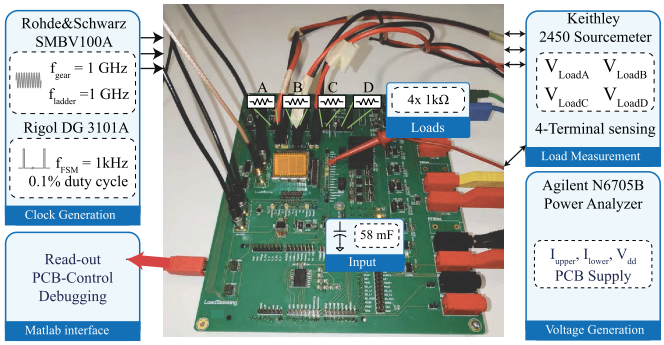

Fig. 18. Measurement setup.

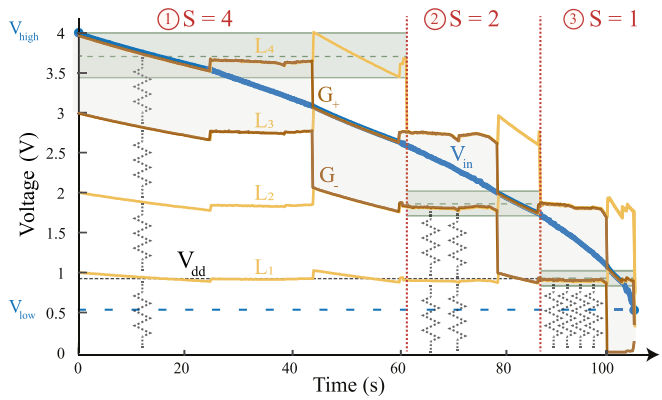

Fig. 19. Measured global voltages ($L_{1..4}$) and MIS supply rails (G_+/G_-) over a 4-V-to-0.55-V V_{in} from a discharging C_{store}.

the overflow signal triggers the MIS counter in order to reconnect G_+ and G_- to another voltage domain. As such, V_{in} is continuously kept between both the supply rails, accommodating the zoom approach.

Whereas the quantizer only reveals the value of V_{in} relative to G_-, the absolute value of V_{in} can be determined by combining its output (fine conversion) with the state of the MIS (coarse conversion). As such, this combination decides upon the optimal configuration for the DLS. Finally, the counter of the imbalance converter is triggered when neither the MIS nor the DLS use one of the global levels ($L_{1,\ldots,4}$) to continuously optimize its flying capacitor allocation. After every counter update, the FSM resets to the default state.

The applied clock to the quantizer (f_{FSM}) determines how fast the FSM may track fluctuations on V_{in}. Although the quantizer and the FSM can easily cope with higher frequencies than the current 1 kHz to allow faster input variations, in terms of efficiency, it is not preferable to increase this frequency. First, any reconfiguration of the MIS, DLS, or imbalance converter induces losses due to the (dis)charging of parasitic capacitance between the DNW of the respective block and substrate. Furthermore, a proper and efficient working of SC converters requires steady-state operation. This means that topology changes, induced by the FSM, should be rare relatively to the switching frequency. Therefore, the frequency of f_{FSM} should be kept orders of magnitude lower than the frequency controller of the input converter. Conclusively, the intended operation regime of DVDS demands a low f_{FSM} to make the reconfiguration losses marginal over the wide ΔV_{in} compared to the losses of the power converters. Nevertheless, input variations at frequencies higher than f_{FSM} can still be tackled by the frequency controller, as long as they occur within the voltage range of a single iVCR and, therefore, do not require an FSM update.

VI. Measurements

The presented DVDS system is realized in a 40-nm CMOS process. In the chip micrograph in Fig. 17, one can distinguish the two converters with their interleaved fragments. The flying capacitors have been implemented with a stack of MOM and MOS capacitors, while high-impedance DNW biasing reduced the parasitic coupling [31]. Their capacitance equals 3.3 and 2.2 nF for the input and imbalance converters, respectively. Fig. 18 shows the testing board, the used equipment, and the applied signals for the transient and efficiency measurements discussed below.

A. Transient Performance

To verify operation, four external 1 k Ω $\pm$ 5% loads were attached to the chip, which is supplied by a 4-V precharged external C_{store} of 58 mF. The nominal supply (V_{dd}) for the loads is set to 925 mV with a V_{margin} of 75 mV. Owing to the voltage-dependent load current of the resistors, V_{margin} mimics loads with dynamic voltage scaling and will inherently introduce current imbalance. Fig. 19 plots the measured global levels $L_{1..4}$ and the supply rails of the MIS (G_+/G_-) over a full discharge cycle. As intended, the MIS keeps V_{in} within its supply rails, enabling the beneficial zoom approach. Furthermore, one can see how the global levels, L_4, L_3, and later also L_2, coincide with lowering V_{in}, optimizing the flying capacitor allocation in the imbalance converter.

For the same measurement, Fig. 20 details the voltages across the loads of which the terminals are connected to the global levels $L_{1..4}$ by the DLS. As can be seen, the imbalance converter controls all the loads to be continuously within margins, down to the point where V_{in} reaches 0.55 V. The large deviation of V_{loadA}

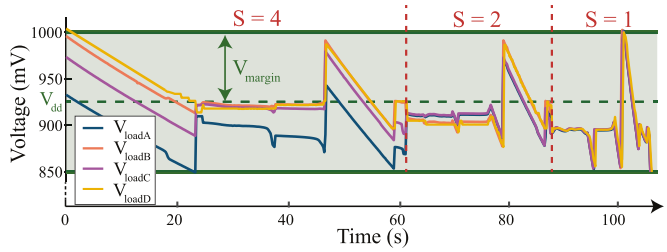

Fig. 20. Measured load voltages over a 4-V-to-0.55-V V_{in} from a discharging C_{store} with the annotation of the load configurations.

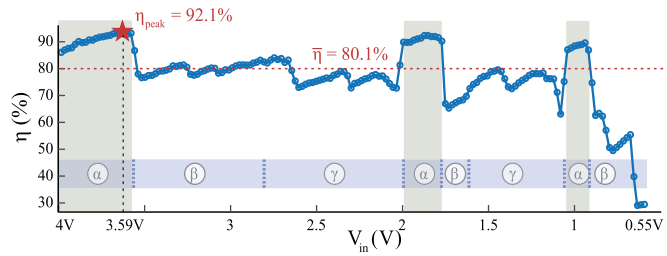

Fig. 21. Measured efficiency versus V_{in} with four 1-kΩ loads, all the power sources included and conversion states annotated (α–γ). The direct connection (α) is highlighted in green.

is due to the configuration switches. Because the terminals of load$_A$ experience a wider voltage range than the ones of the other loads, the configuration switches in between V_{in} and load$_A$ have to block higher voltages as well. As seen earlier, a higher blocking voltage requires more cascading, which results in a higher R_{on}. This increased series resistance induces a larger voltage drop and, therefore, a lower $V_{\text{load}A}$.

B. Efficiency

Fig. 21 plots the measured efficiency for the full operation range, again with four external 1-kΩ loads, which results in a total load power of 3.4 mW. The two states of the input switch can be distinguished. First, when the input switch directly connects V_{in} and V_{stack} (α), the DVDS system achieves high efficiencies, as highlighted in green. Thanks to the DLS, there are three such direct connections, significantly boosting the average efficiency. Second, when the input switch connects V_{in} to the input converter, a typical efficiency curve for gearbox converters emerges in which the various iVCRs can be distinguished. This is as expected since the input converter, containing three different iVCRs, is the loss determining component.

It is noticeable that the efficiency curve degrades with lower V_{in}, whereas one might expect that the zoom approach enables a similar converter operation in each voltage domain. However, because the DLS places the loads more in parallel with lower V_{in}, less charge can be recycled in the load stack. To compensate this, the input converter has to deliver more current. Because of the increased current, the total losses in the converter increase with lower V_{in}, despite the similar converter efficiency in each voltage domain. Since the total load power remains constant ($4V_{dd}^2/R_{\text{load}}$) over ΔV_{in}, the system efficiency degrades accordingly with lower V_{in}.

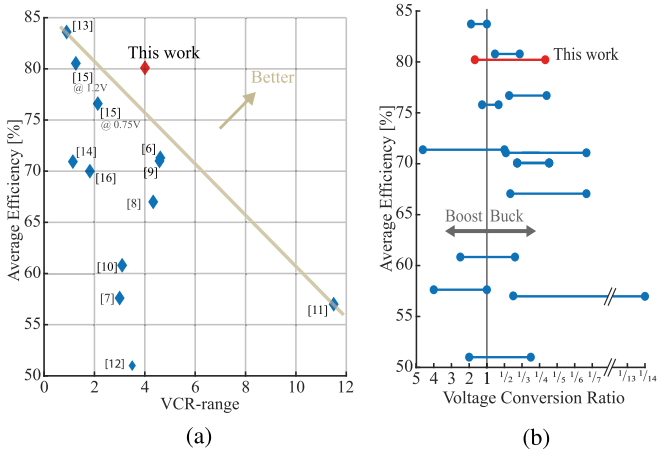

Fig. 22. (a) State-of-the-art comparison of fully integrated wide-input range converters. (b) Details on the reported VCR range of these converters. Both the figures have the same y-axis.

Overall, the DVDS system achieves an average efficiency of 80.1% with a peak efficiency of 92.1% across the wide ΔV_{in} from 4 to 0.55 V. For the reported measurements, V_{margin} was chosen to correspond to the four-level stacked design in [23]. More margin would allow a longer direct connection, resulting in a higher $\overline{\eta}$ and vice versa.

C. Comparison

Table II compares the presented measurements to state-of-the-art VDS and ΔV_{in} converters. On the one hand, the conventional VDS-enabling converters achieve a high η_{peak} but lack a ΔV_{in} [21]–[24]. Although an input range is reported in [22], it can only be achied by varying V_{load} proportionaly and is therefore not an independent V_{in} The converter in [21] also allows an input range with two preliminary load configurations, but it lacks a closed-loop controller and only reports efficiencies of the two direct connections. This work with dynamic VDS, on the contrary, enables a true wide ΔV_{in} with stable V_{load}'s over the whole operation range. The reconfigurable DVDS system, however, does come at the expense of a reduced η_{peak} due to the losses in the configuration switches. Moreover, the power density is rather limited which is due to two reasons. First, DVDS requires two area-consuming converters instead of only one. Second, as mentioned earlier, the maximal current is limited by the input converter when all the loads are in parallel. Conventional VDS converters, instead, always benefit from charge recycling, which is advantageous for the power density.

On the other hand, the conventional ΔV_{in} converters in Table II [9]–[13] reveal the earlier discussed tradeoff between $\overline{\eta}$ and ΔV_{in}. This tradeoff is even more pronounced in Fig. 22(a), which visually compares an extended range of fully integrated designs. Fig. 22(b) provides more detailed information on the reported VCR ranges in (a) which includes both buck, boost, and buck–boost converters. The presented work achieves a similar $\overline{\eta}$ to the one reported in [15] but with a three times wider VCR range, while for a similar VCR range [6], a 9% higher $\overline{\eta}$ has been achieved.

TABLE II
COMPARISON WITH STATE-OF-THE-ART VDS [21]–[24] AND ΔV_{IN} [9]–[13] CONVERTERS

	This article	[21] TCAS19	[22] CICC18	[23] JSSCC16	[24] JSSC17	[13] TCAS20	[9] ASSC15	[10] ISSCC16	[11] JSSC20	[12] CICC15
Technology [nm]	40	130	40	40	40	180	90	350	350	65
# Stacked loads	4/2/1	3/2	2	4	2	1	1	1	1	1
V_{in} [V]	**0.55–4**	2.35–3.65	0.9–1.8	3.6	2.2	0.95–1.8	2.5–8	2–13	7.5–42	0.5–3.5
V_{load} [V]	0.85–1	1.08–1.35	0.45–0.9	0.85–1	1.1	1.8	1.2	5	3	1
Integrated Control	yes	no	yes	yes	yes	yes	yes	yes	yes	yes
$\overline{\eta}$ [%]	**80.1**	N/A	/	/	/	83.6	71	60.8*	57*	51*
η_{peak} [%]	92.1	99	98.2	96	96	85.3	75	81.5	68.3	70.4
P_{dense} [mW/mm^2]**	3.07	2.7	74.28	21.1	21	0.668	13.3	0.96	0.4	0.007

*Calculated based on results in paper. **For reported $\overline{\eta}$.

To show the possibilities of DVDS, one could compare with the converter in [12], which has a similar voltage range to the proposed DVDS converter but discharges a storage capacitor conventionally with a single load and a gearbox converter. They achieve an average efficiency of only 51%, while the proposed DVDS system achieved 80.1%, which reveals a 4× reduction of the normalized losses.

VII. CONCLUSION

This article first discussed the need for converters with both a high $\overline{\eta}$ and a wide ΔV_{in}. The presented DVDS topology enabled a wide input range to the highly efficient VDS topology by adding an input converter and input switch. Then, the performance was enhance twofold. First, the zoom approach reduced the input range with a factor N, and second, the DLS minimized the conversion step. Furthermore, the DLS also unlocked multiple highly efficient direct connections, even bypassing the input converter with associated losses. In addition, the reconfigurable ladder converter optimized the flying capacitor allocation. Finally, dynamic VDS was demonstrated with measurements on a 40-nm prototype. Across an input voltage ranging from 4 V down to 0.55 V, a state-of-the-art average efficiency of 80.1% was measured together with a peak efficiency of 92.1%.

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