Active Gate Driver With Turn-off Delay Control for Voltage Balancing of Series–Connected SiC MOSFETs

Myeongsu Son, *Member, IEEE*, Younghoon Cho, *Senior Member, IEEE*, and Seunghoon Baek, *Member, IEEE*

***Abstract*—Connecting semiconductor switches in series is a way to increase the voltage rating of a power electronic converter. However, if two switches are directly connected without any special effort, an uneven voltage between the switches can occur due to non-identical characteristics of them. A significant voltage imbalance may destroy the switches, and both thermal and loss imbalance also lead to the unstable system. Since a silicon carbide (SiC) metal–oxide–semiconductor field–effect transistor (MOSFET) has a faster switching speed and higher voltage blocking capability than silicon (Si) devices, existing voltage balancing methods for Si devices may not be suitable. This article proposes a voltage balancing method that controls turn-OFF delay time of the switch by adding one bipolar junction transistor (BJT) on a gate turn-OFF path. Depending on the base voltage of the BJT, turn-OFF resistance and delay time are actively changed which mitigates the imbalance problem. The theoretical analysis of the proposed method has been discussed in detail based on the classical MOSFET model. Both the simulations and experiments have been performed to verify the theory and the validity of the proposed method where the voltage imbalance is reduced from 22.4% to 3.2% as well as reducing the switching loss at the entire voltage and load conditions.**

***Index Terms*—Silicon carbide (SiC), series-connection, semiconductor device modeling, time delay control, voltage balancing.**

I. Introduction

Over the last decade, the growth of semiconductor devices has led to having better properties such as higher voltage blocking capability, lower switching loss, and faster switching speed [1]. The development of these semiconductor materials such as silicon carbide (SiC) and gallium nitride has improved the efficiency of power conversion systems. Some semiconductor devices with lateral structures may not have high blocking voltage capability, but silicon (Si) or SiC devices with vertical structures can have higher blocking voltage capability [2], [3]. It is reported that the voltage rating limit of Si devices is 6.5 kV due to their intrinsic properties. Meanwhile, SiC devices have higher voltage ratings than Si devices due to higher band–gap energy. SiC modules with 15 kV voltage ratings have also been reported in [4] and [5].

Although the maximum voltage range of SiC devices has been reported to be 15 kV, the maximum voltage range of commercially available SiC metal–oxide–semiconductor field–effect transistor (MOSFET) is 1.7 kV. In this respect, there are two effective ways to increase the voltage rating of the system. One method is stacking the topology modules such as a modular multilevel converter (MMC). Another is connecting semiconductors in series. The MMC structure offers low voltage stress (dv/dt) applied to switches, and has low common mode voltage [6]–[8]. However, comparing the two methods, the series–connected structure will have higher efficiency and lower cost. Furthermore, in [9], a series–connected structure has higher current density, lower ON-state resistance, and stronger terrestrial cosmic radiation immunity than a single higher-voltage semiconductor.

However, in a series–connected structure, the parasitic capacitors are essentially existing in the devices and the circuit layout, and this leads to unequal voltage sharing [10]. This parasitic capacitor is structurally inherent in circuit and isolation components [11]. It causes a voltage inequality, and this results in a switching loss imbalance. In addition, a voltage imbalance can drive switches failure or damage by exceeding voltage rating. To reduce this voltage imbalance, following techniques had been studied in Si–based insulated gate bipolar transistor: *RC* or RCD snubber [12], active clamping [13], and active gate drive [14] techniques. Although these methods demonstrate meaningful improvement on voltage balancing in series-connected Si devices, they may increase switching loss, and deteriorate switching performance in SiC devices which are faster and more sensitive than Si devices.

To overcome these limitations, voltage balancing methods for SiC MOSFETs have been actively studied. These are classified into four main categories, and given in Table I. The easiest and most common way to reduce the voltage inequality is the *RC* snubber method using a resistor and capacitor. In [15]–[17], a suitable snubber value for stacked 1.7 kV SiC MOSFETs was suggested. According to [15], the snubber capacitance should

Manuscript received 13 July 2021; revised 24 February 2022 and 24 April 2022; accepted 22 June 2022. Date of publication 6 July 2022; date of current version 6 September 2022. This work was supported by Konkuk University, in 2017. Recommended for publication by Associate Editor G. Konstantinou. *(Corresponding author: Younghoon Cho.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3188747.

Digital Object Identifier 10.1109/TPEL.2022.3188747

TABLE I
VOLTAGE BALANCING TECHNIQUES FOR SERIES-CONNECTED SIC MOSFETS

Method	Technique	Circuit structure for	Rating	Capabilities	Refs.	Similar works
RC snubber	Select proper RC snubber	DPT circuit	1800 V 100–300 A	Increased switch current and Different frequency condition	[15]	[17]
		Half-bridge	1800 V 48–111 A_{rms}	Different current condition and Different frequency condition	[16]	
Super-cascode structure	Compact balancing circuit with ten passive components	DPT circuit	1200 V 4.5 A	Static DC voltage	[18]	[20]
	Limiting snubber circuits	DPT circuit	1300 V 10 A	Static DC voltage and Static switching frequency	[19]	
Passive gate driver with MOSFET (Hybrid gate type)	Dynamic voltage balancing control	DPT circuit with R	600 – 1200 V 1.5–3 A	Variable DC voltage and Static switching frequency	[21]	
	Energy recovery and snubber capacitor self–balancing	Half-bridge	3000V 15.6 A_{rms}	Different current condition and Different frequency condition	[22]	
Active gate driver	Adjusting driving signal time delay	DPT circuit with R	400 V 3–10 A	Variable drain current and Static switching frequency	[23]	[24]–[28]
	dv/dt control for dynamic voltage balancing	DPT circuit	1200 V 200 A	Increased switch current and Different frequency condition	[10]	[29]– [30]

be selected at least five times more than the MOSFET's output capacitance $C_{\rm oss}$ to reduce voltage imbalance. Moreover, it is suggested that the capacitance should be 10–20 times more than $C_{\rm oss}$ to reduce the imbalance within 5% compared to dc voltage in [17]. Apparently, a large capacitance increases the switching speed and loss.

Another approach is adopting the supercascode structure [18]–[20]. This method uses one gate driver and several passive components to achieve voltage balancing, and the single gate driver controls multiple switches simultaneously. In [18], the supercascode method operates with only ten passive components. In [19], with a limited snubber circuit, the voltage balancing was attained. Nevertheless, it is not possible to operate more than three switches at the same time due to the limitations of the powering capability. Furthermore, the additional gate path in the circuit layout may cause extreme voltage and current oscillations during transients.

To overcome the functional limitations of the supercascode, the hybrid-cascode structure where an MOSFET is added to the circuit is proposed in [21] and [22]. Yang *et al.*, [21] proposed the dynamic voltage balancing control which can work even under dc voltage changing conditions. The energy recovery technique with a snubber is proposed in [22] to balance out the voltages of the four series–connected switches as well as reducing the losses incurred in the snubber.

The last is the active gate driver (AGD) method. In [23], a field programmable gate array (FPGA) generates time delays on the gate signals to compensate for the signal leading caused by the parasitic capacitor. Since this technique has been actively studied in Si devices, many similar studies have been also conducted for SiC devices [24]–[28]. However, the computational burden is a major concern which limits the switching frequency. In [23]–[29], the maximum switching frequency is limited less than several tens kilo hertz. Moreover, the maximum operating voltage of the system is restricted by the insulation strength of the voltage sensor circuitry. Meanwhile, Marzoughi *et al.* [10], Zhou *et al.* [29], and Raszmann *et al.* [30] propose a current driven gate driver with a current mirror circuit to change the *dv/dt* of SiC MOSFETs. This method does not limit on voltage measurement, because a control unit is placed in each gate driver circuit. However, this method is relatively complicated than other approaches.

This article proposes an AGD for device voltage balancing in series-connected SiC MOSFETs. The proposed AGD controls a turn-OFF impedance of a MOSFET by using a bipolar junction transistor (BJT) which is placed in the gate turn-OFF path. To address the operating principles of the proposed method, a series-connected MOSFET model is suggested based on the classical equivalent MOSFET model. Then, the specific design procedure is explained. With the proposed method, it is possible to control turn-OFF time delay for voltage balancing in various switching frequency and current condition. In addition, unlike the traditional methods which have been mentioned previously, the proposed method is simply implemented, and has less issues on the insulation.

In Section II, a series–connected MOSFET model is proposed and analyzed. By using the model, it is explained how the turn-OFF procedure is affected by the parasitic capacitance in the circuit layout and the device gate terminal. Then, the change of turn-OFF process by the gate driver parameters is discussed. After that, in Section III, the AGD is proposed, and its operating principle is presented. In this section, the voltage balancing mechanism with the proposed AGD is explained in deep. The specific design procedure is also suggested. In Section IV and V, the simulation and experimental results are provided to validate the proposed AGD, respectively. Finally, Section VI concludes this article.

II. ANALYSIS OF TURN-OFF CHARACTERISTIC FOR MOSFETS

In this section, the MOSFET turn-OFF process is analyzed in detail. All the symbols used in this section are given in Table II. Since voltage imbalance mainly occurs in the turn-OFF sequence [14], turn-ON states are not considered in this article as in [23]. A classical equivalent MOSFET model, used in this section, only considers the gate-source capacitance $C_{\rm GS}$ and the gate-drain capacitance $C_{\rm GD}$ which are parts of its parasitic capacitors [31]. The drain-source capacitance $C_{\rm DS}$ does not consider, because it is trivial compared to $C_{\rm GS}$ in SiC devices. Although this model does not fully reflect the nonlinearities of $C_{\rm GS}$ and $G_{\rm GD}$ during

TABLE II
SYMBOLS FOR MODELING EQUATION.

Symbol	Description	Symbol	Description
v_{DS}	Drain–source voltage	i_{DS}	Drain–source current
v_{GS}	Gate–source voltage	i_G	Gate current
v_{GD}	Gate–drain voltage	i_{ch}	MOSFET channel current
v_{GO}	Gate–ground voltage	I_L	Load current
v_{SO}	Source–ground voltage	g_m	Transconductance
v_{GG}	Gate driver voltage	C_{GS}	Gate–source capacitance
V_{nn}	Gate negative voltage	C_{GD}	Gate–drain capacitance
V_{pp}	Gate positive voltage	C_{iss}	Input capacitance
V_{DC}	DC link voltage	C_p	Gate–ground capacitance
V_{TH}	Gate threshold voltage	$r_{DS(ON)}$	On-state resistance
V_{miller}	Miller plateau voltage	R_G	Gate resistance
τ	Time constant	L	Load inductance

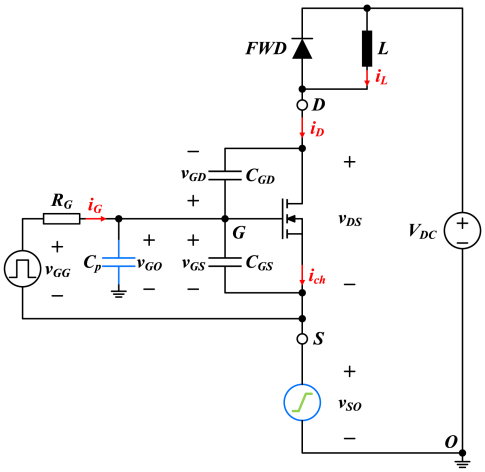

Fig. 1. DPT circuit with equivalent model of MOSFET and parasitic capacitor.

transients, it provides an insight into its turn-OFF process by the modeling equation. To organize turn-OFF transient properties of stacked MOSFETs, the gate-ground parasitic capacitance C_p should be taken into account. Fig. 1 shows an equivalence of a double pulse test (DPT) circuit including C_p. To simplify the models, the lower MOSFET is modeled as a ramp voltage source with a constant slew rate, dv_{SO}/dt. Figs. 2 and 3 presents MOSFET models and waveforms at each stage, respectively. When $t < t_0$, it is assumed that the MOSFET is under a turn-ON state. Thus, at $t = t_0$, the following initial conditions can be established

$$v_{\mathrm{DS}}(t_0) = I_L r_{\mathrm{DS(ON)}} \tag{1}$$

$$i_{\mathrm{DS}}(t_0) = I_L \tag{2}$$

$$i_g(t_0) = 0 \tag{3}$$

$$v_{\mathrm{GS}}(t_0) = V_{\mathrm{pp}} \tag{4}$$

$$v_{\mathrm{GD}}(t_0) = V_{\mathrm{pp}} - I_L r_{\mathrm{DS(ON)}} \tag{5}$$

$$v_{\mathrm{SO}}(t_0) = 0. \tag{6}$$

Stage 1 (Δt_{10}, $t_0 \le t < t_1$): At $t = t_0$, $v_{\mathrm{GG}}(t)$ becomes V_{nn}. Since the device operates in the linear region, the equivalent circuit at this stage is shown in Fig. 2(a). If it assumes that the v_{DS} and v_{SO} remain constant, then C_{GS}, C_{GD}, and C_p discharge

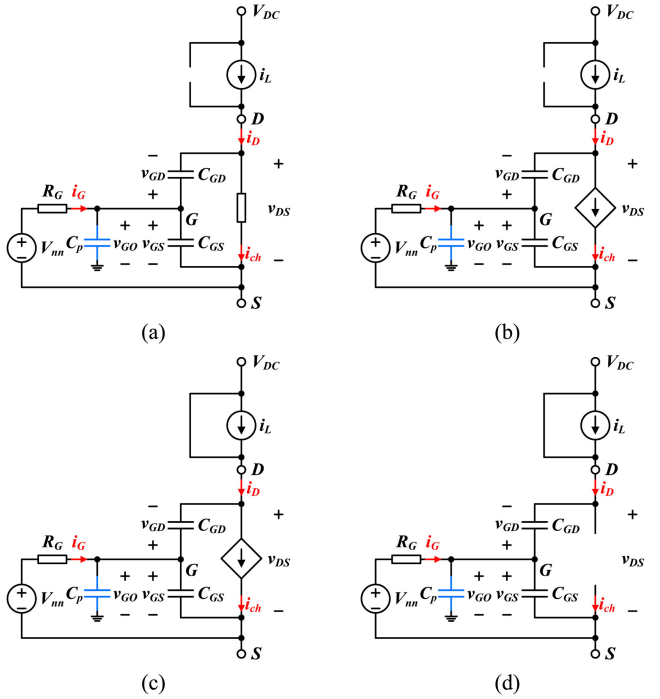

Fig. 2. Equivalent MOSFET circuits. (a) $t_0 \le t < t_1$. (b) $t_1 \le t < t_2$. (c) $t_2 \le t < t_3$. (d) $t_3 \le t < t_4$.

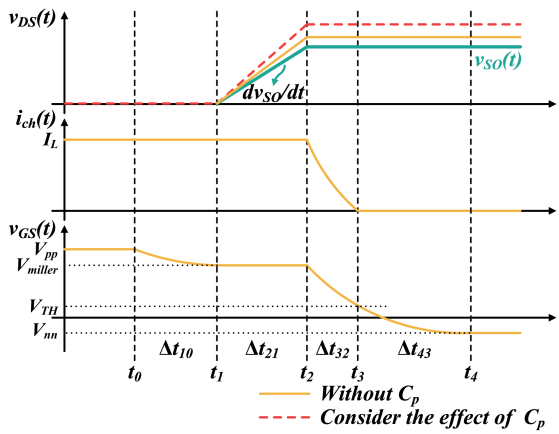

Fig. 3. Equivalent MOSFET model in turn-OFF transient.

through R_G as governed by the following relations:

$$i_G = \frac{V_{nn} - v_{\mathrm{GS}}}{R_G} = C_p \frac{dv_{\mathrm{GO}}}{dt} + C_{\mathrm{GS}} \frac{dv_{\mathrm{GS}}}{dt} + C_{\mathrm{GD}} \frac{dv_{\mathrm{GD}}}{dt}. \tag{7}$$

Since v_{DS} and v_{SO} are assumed as constant values, i_G becomes

$$i_G = \frac{V_{nn} - v_{\mathrm{GS}}}{R_G} = (C_p + C_{\mathrm{iss}}) \frac{dv_{\mathrm{GS}}}{dt} \tag{8}$$

where C_{iss} represents the input capacitance which is the sum of C_{GD} and C_{GS}. Thus, from (8), v_{GS} and i_G for $t \ge t_0$ can be acquired as

$$v_{\mathrm{GS}}(t) = V_{nn} - (V_{nn} - V_{\mathrm{pp}})\, e^{\frac{-(t-t_0)}{R_G(C_p + C_{\mathrm{iss}})}} \tag{9}$$

$$i_G(t) = ((V_{nn} - V_{pp})/R_G)\, e^{\frac{-(t-t_0)}{R_G(C_p+C_{iss})}}. \quad (10)$$

From (9), v_{GS} continues to decrease exponentially. At $t = t_1$, v_{GS} reaches to the miller plateau voltage V_{miller}. From transconductance g_m characteristics, V_{miller} is given by

$$v_{GS}(t_1) = V_{miller} = (I_L/g_m) + V_{TH}. \quad (11)$$

The time interval $\Delta t_{10} = t_1 - t_0$ can be drawn easily by substituting (9) into (11) at $t = t_1$

$$\Delta t_{10} = t_1 - t_0 = R_G(C_p + C_{iss}) \ln\left(\frac{V_{pp} - V_{nn}}{(I_L/g_m) + V_{TH} - V_{nn}}\right) \quad (12)$$

However, in [10], it is reported that C_p is commonly about tens of pico farads in real systems. This is relatively much smaller than C_{iss} whose value is normally thousands of pico farads. Thus, the effect of C_p is very limited in this interval.

Stage 2 (Δt_{21}, $t_1 \le t < t_2$): Since v_{GS} is constant and equal to V_{miller}, the current flow through C_{GD} is divided into i_G and C_p in this stage. Moreover, v_{DS} is increased due to the discharging of C_{GD}

$$i_G = \frac{V_{nn} - ((I_L/g_m) + V_{TH})}{R_G} = C_p\frac{dv_{GO}}{dt} + C_{GD}\frac{dv_{GD}}{dt}. \quad (13)$$

At this stage Δt_{21}, the lower switch is modeled as a ramp voltage source. The slew rate of this voltage source causes the charging current flow into C_p, which increases the current flowing of C_{GD}. The discharge of C_{GD} induces rapid increases of v_{DS}. Thus, by using (13) and V_{miller}, dv_{DS}/dt can be summarized as

$$\frac{dv_{DS}}{dt} = \frac{C_p}{C_{GD}}\frac{dv_{SO}}{dt} - \frac{V_{nn} - ((I_L/g_m) + V_{TH})}{C_{GD}\cdot R_G}. \quad (14)$$

In SiC MOSFETs, C_{GD} is generally several pico farads, and a large C_p and dv_{SO}/dt which is the switching speed of the lower MOSFET cause significant dv_{DS}/dt. Hence, voltage imbalance is getting larger.

Stage 3 (Δt_{32}, $t_2 \le t < t_3$): At $t = t_2$, the sum of v_{DS} and v_{SO} is equal to V_{DC}. At the same time, the free-wheeling diode (FWD) is forced to be turned ON as shown in Fig. 2(c). Here, i_{ch} is determined from g_m and given by

$$i_{ch}(t) = g_m(v_{GS}(t) - V_{TH}). \quad (15)$$

Since v_{DS} and v_{SO} are assumed to be constant, i_G can be expressed the same as (8). From (8) and g_m, di_{ch}/dt and v_{GS} can be defined as following relations:

$$\frac{di_{ch}}{dt} = \frac{g_m}{C_p + C_{iss}}\cdot\frac{V_{nn} - v_{GS}}{R_G} \quad (16)$$

$$v_{GS}(t) = V_{nn} - (V_{nn} - V_{miller})\, e^{\frac{-(t-t_2)}{R_G(C_p+C_{iss})}}. \quad (17)$$

Again, C_p is much trivial compared to C_{iss}, so it does not significantly affect di_{ch}/dt. In addition, i_{ch} shown in (18) can be drawn easily by substituting (17) for (15)

$$i_{ch}(t) = g_m(V_{TH} - V_{nn})\left(e^{-(t-t_2)/\tau} - 1\right) + I_L e^{-(t-t_2)/\tau} \quad (18)$$

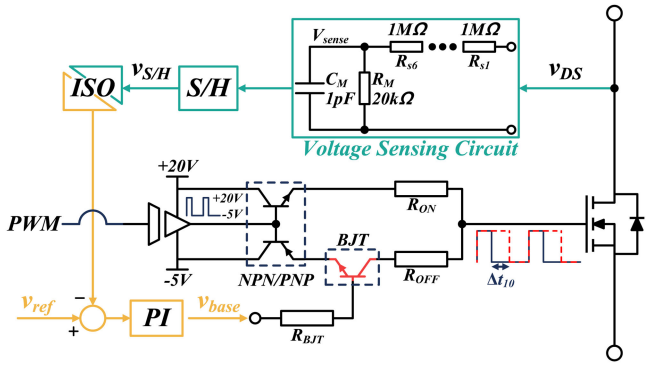

Fig. 4. Simplified composition of the proposed AGD.

where τ is $R_G(C_p+C_{iss})$. Time interval Δt_{32} is obtained by setting (17) to V_{TH} at $t = t_3$.

$$\Delta t_{32} = t_3 - t_2 = R_G(C_p + C_{iss}) \ln\left(1 + \frac{I_L}{g_m(V_{TH} - V_{nn})}\right). \quad (19)$$

Hence, there is little effect by C_p on this section as well.

Stage 4 (Δt_{43}, $t_3 \le t < t_4$): For $t > t_3$, as the gate current approaches zero, v_{GS} decreases exponentially to reach V_{nn}. Between t_3 and t_4, i_{ch} is discharged to zero as shown in Fig. 3.

III. Proposed Active Gate Driver

Fig. 4 shows the conceptual diagram of the proposed AGD. The NPN/PNP transistors in the figure are employed to implement complementary operation. As can be seen in Fig. 4, one BJT which is the key component in the proposed scheme is connected in series with the gate turn-OFF resistor R_{OFF}. Generally, BJTs are used as amplifiers for small signals. This is because the base current determines a current flowing through the collector. In the same way, when the collector–emitter voltage remains constant, the base current controls the collector–emitter impedance Z_{ce} of the BJT. The base current is adjusted by v_{base}, and the voltage applied to gate-OFF path through Z_{ce} and R_{OFF} at $t = t_0$ has always a constant value, V_{pp}–V_{nn}. Thus, v_{base} determines the total gate turn-off resistance, Z_{ce}+R_{OFF}. When the BJT operates in a linear area, the collector current is proportional to the base current which is restricted by R_{BJT}, so that Z_{ce} is inversely proportioned to v_{base}.

In the previous section, it was confirmed that the voltage imbalance mainly occurs in Δt_{21}. From (12), (16), and (19), C_p has little effect on Δt_{10}, Δt_{32}, and di_{ch}/dt. Conversely, dv_{DS}/dt is changed drastically by C_p in (14). By the way, the most prominent factor in Section II is a gate resistance R_G. Fig. 5 shows the turn-OFF characteristics by changes of R_G using (12) and (14). The datasheet of SiC MOSFET C2M0080170P from Wolfspeed was used for this calculation. In this process, nonlinear factors, g_m and C_{iss}, whose values are changed by voltage and temperature conditions, were considered as constant values for simplicity. As R_G changes from 3 to 20 Ω, the turn-OFF time delay Δt_{10} varies linearly from 6.5 to 43.2 ns. Meanwhile,

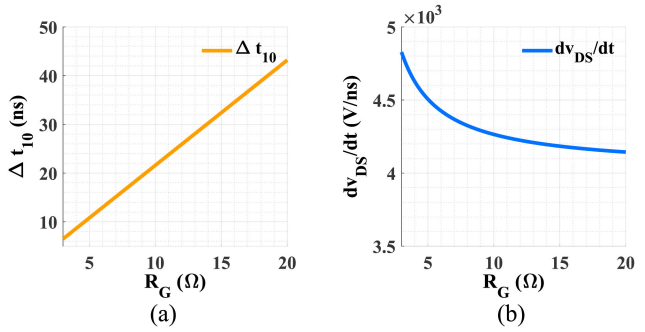

Fig. 5. Impact of gate resistance on turn-OFF parameters. (a) Turn-OFF delay time (Δt_{10}). (b) Drain-source voltage change rate ($dv_{\rm DS}/dt$).

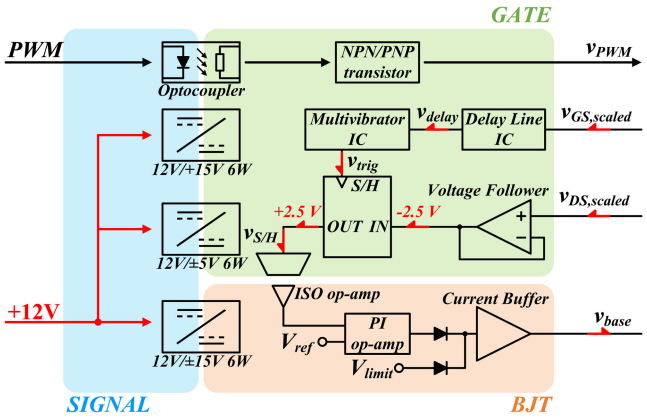

Fig. 6. Detailed AGD design schematic diagram.

$dv_{\rm DS}/dt$ varies inversely in small areas depending on R_G. The decrease of $dv_{\rm DS}/dt$ by R_G is not significant, so that Z_{ce} mainly adjusts Δt_{10}. In [32], the switch turn-OFF time is changed by R_G in actual SiC MOSFET systems. In other words, the proposed method will change the turn-OFF delay time by changing $v_{\rm base}$, so that voltage balancing between the devices can be attained.

For adjusting Z_{ce} appropriately, $v_{\rm base}$ must be correctly controlled. The proposed AGD is functionally divided into three parts. The first is a pulsewidth modulation (PWM) signal part, the second is a sample and hold (S/H) part for $v_{\rm DS}$ measurement, and the last is a proportional–integral (PI) control part. The detailed diagram of the proposed AGD is shown in Fig. 6. The PWM signal part composed of the optocoupler ACPL–W349–000E and the NPN/PNP transistors. The optocoupler isolates the pulse signal generated from a microcontroller unit (MCU). The output of the optocoupler passes to the NPN/PNP transistor. The transistor applies a gate driver voltage to the switch according to the PWM signal.

The S/H part has several chips and circuits. First, there is a voltage divider which reduces $v_{\rm DS}$ by 1/300 as shown in Fig. 4. In this article, R_s, R_M, and C_M are selected as 1 MΩ, 20 kΩ, and 1 pF, respectively. The reduced $v_{\rm DS}$ which is denoted $v_{\rm DS.scaled}$ in Fig. 6 is passed to the S/H chip through a voltage follower LMH6628. Among various choices for S/H function, AD783 from analog devices is selected because of its very short sampling time compared to other candidates. The input range of

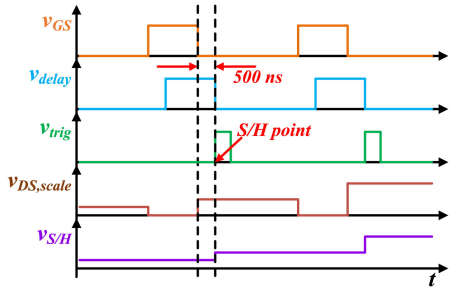

Fig. 7. Signals for S/H operation.

the S/H chip is –2.5 to +2.5 V, but the range of $v_{\rm DS.scaled}$ is 0 to 5 V when $v_{\rm DS}$ varies from 0 to 1500 V. Hence, 2.5 V must be subtracted from $v_{\rm DS.scaled}$ by an op-amp circuit. After the S/H phase, another op–amp is existing to get it back to its original range.

The timing sequence of the S/H process is shown in Fig. 7. Since $v_{\rm base}$ adjusts the turn-OFF voltage, the S/H chip should measure the turn-OFF state of $v_{\rm DS}$. In general, the turn-OFF wave form of *vDS* is oscillatory due to a stray inductance. Hence, the measurement of $v_{\rm DS}$ is taken place after at least 300 ns in empirical when the gate turn-OFF sequence is finished which is right after t_2 in Fig. 3. The delay line chip DS1100Z–500+ was used for implementing 500 ns of time delay. The scaled-down $v_{\rm GS}$ which is denoted $v_{\rm GS,scaled}$ is implemented using a diode and a resistor to bias 5 and 0 V, and it is fed to the delay line chip. The output signal of the delay chip is connected to the retriggerable IC 74LVC1G123DP. For the next, $v_{\rm trig}$ which triggers the S/H operation is generated at the falling edge of $v_{\rm delay}$ as shown in Fig. 7.

Since the emitter node of the BJT is not put on the MOSFET's source, $v_{\rm base}$ and PI part are needed to be isolated. Here, $v_{\rm S/H}$ which measures $v_{\rm DS}$ with the time delay is directly fed to the PI controller through an isolation amplifier ISO124U. The PI controller is implemented with inverting amplifier and integrator using op-amp LM6172. Its proportional gain and time constant are set to 0.1 and 50 ns, respectively. The controller generates $v_{\rm base}$ based on reference voltage $V_{\rm ref}$. When the voltage balancing is achieved, $v_{\rm DS}$ is 900 V in this article, so that $V_{\rm ref}$ is set to be 3 V. If $v_{\rm S/H}$ is less than $V_{\rm ref}$, *i.e.*, less than 900 V, $v_{\rm base}$ is increased by the operation of the PI controller. The increased $v_{\rm base}$ reduces Z_{ce} and Δt_{10}. This reduction brings a fast switch turn-OFF for voltage balancing. In the opposite case, the voltage balancing is achieved by increasing Z_{ce} and Δt_{10}. On the other hand, it should be mentioned that when $v_{\rm base}$ is 0 V, the gate off current path will be disconnected, because Z_{ce} is almost infinite. Hence, the turn-OFF operation of the switch is not guaranteed. This situation may cause serious accidents in the entire system, so that a minimum voltage limit $V_{\rm limit}$ should be guaranteed. In this article, $V_{\rm limit}$ was set to be 1.4 V. By $V_{\rm limit}$ and op–amp output limitation property, the range of $v_{\rm base}$ is limited from 1.4 to 13 V. Finally, the current buffer BUF634 was placed to ensure the stability of the BJT drive.

In addition, as can be seen in Fig. 6, the gate voltage applied to the switch is –5 and +20 V. The voltage is produced through an

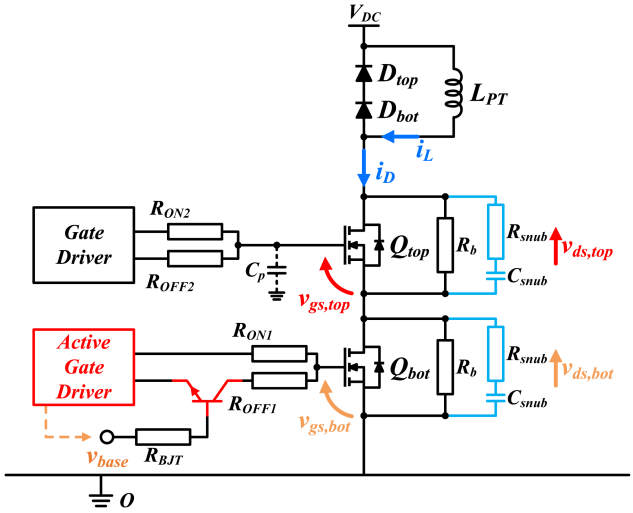

Fig. 8. Series-connected SiC MOSFETs simulation circuit.

TABLE III
SIMULATION PARAMETERS.

f_{sw}	100 kHz	*Duty*	0.2
L_{PT}	9 mH	V_{DC}	1800 V
R_{ON}	5 Ω	R_{OFF}	2.5 Ω
C_p	40 pF	R_b	750 kΩ
Q_{top}, Q_{bot}	C2M0080170P		

isolated dc–dc converter that outputs ±5 and +15 V. Here, ±5 V work as the power sources for the S/H circuit. Meanwhile, an isolated dc–dc converter with ±15 V outputs supplies all other parts of the PI controller.

IV. SIMULATION

The simulations using LTspice software from Linear Technology were conducted to verify the effectiveness of the proposed AGD. Fig. 8 illustrates a simulation circuit diagram. In this simulation, the diodes and the inductor are assumed to be ideal, and the spice model of C2M0080170P provided from Wolfspeed is employed. The parasitic capacitor C_p existing in gate drivers was added to verify the voltage imbalance and AGD performance. Detailed parameters for the simulation are given in Table III. Multiple pulse tests (MPT) with 100 kHz with 0.2 of duty cycle were performed as shown in Fig. 9.

The waveform of the series–connected SiC MOSFETs without C_p is shown in Fig. 9(a). Since there is no factor causing voltage imbalance, perfect voltage balancing is achieved in Fig. 9(a). However, a parasitic capacitor inevitably exists in a real system. Fig. 9(b) shows the simulation results when C_p is set to 40 pF. In this case, extreme voltage imbalance occurs in the low current area. As I_L increase, the $dv_{\rm DS}/dt$ speed of the lower switch is increased by (14) without v_{SO} term, and then voltage imbalance is also enlarged. When I_L reaches 20 A, voltage imbalance is up to 260 V which corresponds to 14.4% of $V_{\rm DC}$.

A common way to achieve voltage balancing is connecting RC snubbers in parallel along with the switches. According to [15], the *RC* snubber capacitance $C_{\rm snub}$ should be at least five

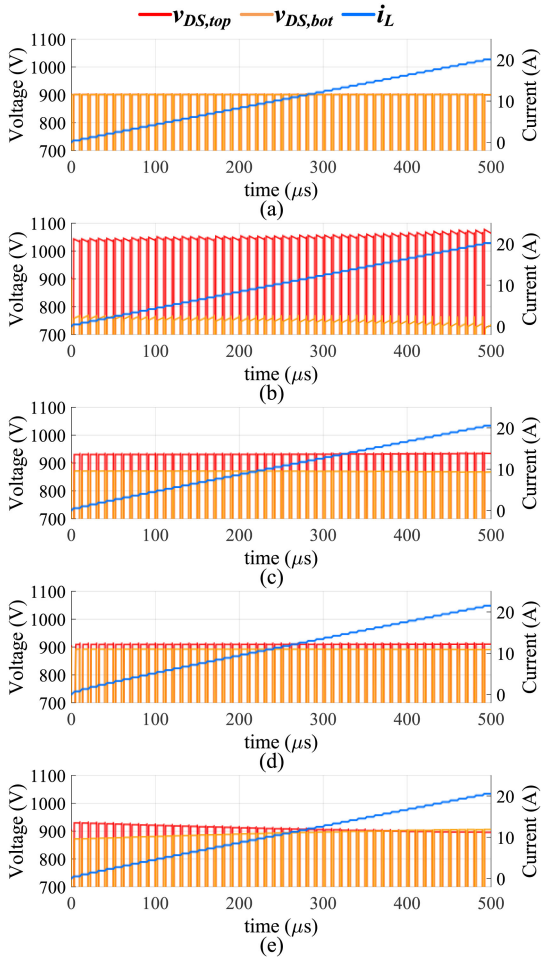

Fig. 9. Series-connected SiC MOSFETs simulation result waveforms under different condition. (a) Ideal case; (b) Parasitic capacitors C_p is considered. (c) Add minimum *RC* snubber. (d) Add maximum *RC* snubber. (e) Increase gate resistance of top switch with minimum RC snubber.

times of $C_{\rm oss}$ for mitigating voltage inequality. In addition, for voltage imbalance within 5% of $V_{\rm DC}$, $C_{\rm snub}$ is selected to be 10 to 30 times of $C_{\rm oss}$. In this article, $C_{\rm oss}$ is 105 pF, so the simulation was carried out under the conditions that when $C_{\rm snub}$ has the minimum and the maximum values. For the minimum case, the parameters are set to $R_{\rm snub} = 2\ \Omega$, $C_{\rm snub} = 470$ pF, and $\tau_{\rm snub} = 0.94$ ns. For the maximum value, they are selected to be $R_{\rm snub} = 5\ \Omega$, $C_{\rm snub} = 2.2$ nF, and $\tau_{\rm snub} = 11$ ns. Fig. 9(c) and (d) compare the MPT results with the *RC* snubbers at each condition. In Fig. 9(c) where the minimum value is employed for the snubber, the voltage imbalance is measured as 66 V which is about 3.6% of $V_{\rm DC}$. On the other hand, it is measured as 22 V which corresponds to 1.2% of $V_{\rm DC}$. In fact, the maximum *RC* snubber values can reduce voltage imbalance, but large switching losses also be occurred. On the other hand, one main reason of voltage imbalance is a different discharge speed of $C_{\rm GD}$ caused by C_p during turn-OFF process. This difference can be mitigated by increasing gate resistance of the upper switch by (13) and (14). In Fig. 9(e), $R_{\rm OFF2}$ is increased from 2.5 to 4 Ω, and the *RC* snubber is set to the minimum. In this case, the

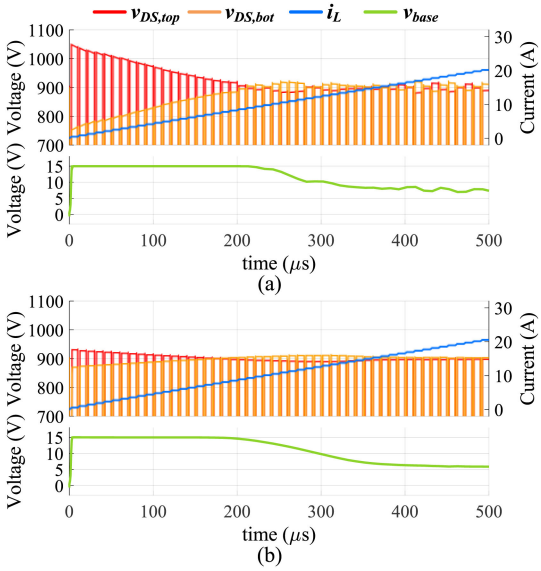

Fig. 10. Series-connected SiC MOSFETs simulation waveforms with AGD. (a) Performance of AGD without RC snubber. (b) Performance of AGD with minimum RC snubber.

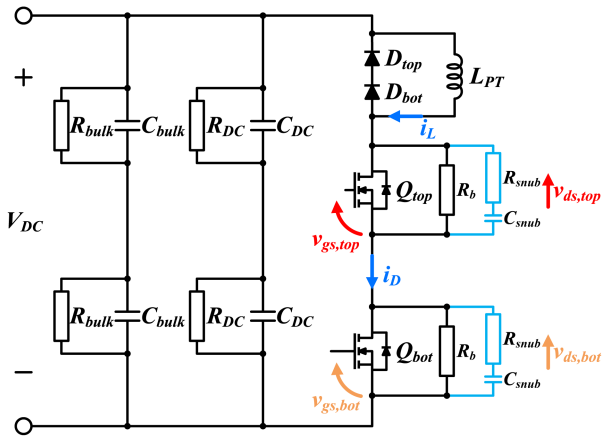

Fig. 11. Series-connected SiC MOSFETs circuit scheme for MPT.

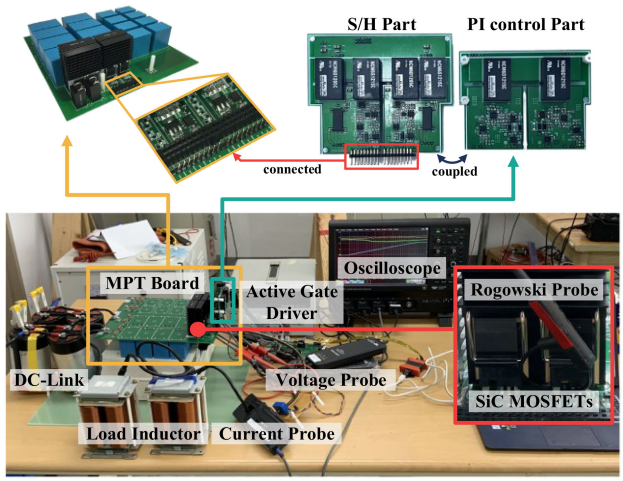

Fig. 12. Populated AGD boards and experimental setup. .

voltage imbalance is measured as 61V which is 3.3% of V_{DC} at 0 A. In a certain current range around 10 A, the voltage balancing is perfectly achieved, but again voltage imbalance enlarges as I_L increases. This is because dv_{DS}/dt is changed by I_L can be seen in (14). Now, the proposed AGD has been implemented in this simulation in Fig. 10. The S/H, op–amp, and delay parts are considered as ideal by using the standard library model. The isolated op-amp is constructed using an ideal op-amp and a voltage dependent voltage source. The BJT is implemented with the spice model of PBSS4041SPN provided from Nexperia. Meanwhile, if R_{OFF1} and R_{OFF2} are the same, the upper switch is turn-OFF earlier than the lower switch due to C_p. In this article, the gate turn-OFF resistance of the lower switch is changed to control the turn-OFF delay as shown in Fig. 8. Thus, to achieve voltage balancing with the AGD operation, R_{OFF2} is increased by 1.5 Ω higher than R_{OFF1}. So, the AGD simulation is operated when $R_{\mathrm{OFF2}} = 4\ \Omega$ and $R_{\mathrm{OFF1}} = 2.5\ \Omega$. Fig. 10(a) shows the MPT results with AGD operation. In the low current area, extreme voltage imbalance, 291 V and 16.2% of V_{DC}, occurs. When I_L is larger than 10 A, the maximum voltage imbalance decreases to 37.7 V which corresponds to 2.1% of V_{DC} by proper operation of the proposed AGD.

To reduce the voltage imbalance occurring in the low current area and increase control stability, the minimum *RC* snubber is added. Hence, the proposed AGD can be considered as a hybrid AGD (HAGD) because passive snubber is combined. Fig. 10(b) shows the HAGD operating waveform with the minimum *RC* snubber. In this condition, a small voltage imbalance of around 60.7 V occurs in the low current area. As I_L increases, the voltage balancing is almost perfectly achieved. When I_L is 20 A, the voltage imbalance is only 6 V which is 0.3% of V_{DC}. In conclusion, a minimum *RC* snubber is exceptionally prominent to achieve voltage balancing in various current conditions. Moreover, it may prevent an accidental voltage imbalance in the low current area as well as minimizing the additional snubber losses.

V. Experiments

A. Experimental Setup

The gate driver and the MPT setup were configured to verify the proposed AGD concept. The circuit diagram and the test bench for experiments are shown in Figs. 11 and 12. Fig. 11 shows the configuration of the series–connected SiC MOSFETs and FWDs. These are selected as C2M0080170P from Wolfspeed and GB25MPS17–247 from GeneSiC, respectively. In general, *RC* snubbers are connected in parallel with FWDs to mitigate diode voltage imbalance. In [33], the origin of this diode imbalance is reported as parasitic capacitors in circuit structure. When *RC* snubbers are added to the diodes, the charging and discharging of the diode junction capacitor is affected by the snubber parameter. Since this effect changes a transient state of SiC MOSFET, the *RC* snubber for FWD is not placed after confirming that the voltage imbalance of diodes does not exceed the voltage rating.

TABLE IV
PARAMETERS FOR EXPERIMENTS

f_{sw}	100kHz/200kHz	*Duty*	0.5
L_{PT}	6mH	V_{DC}	1800V
C_{DC}	80μF	C_{bulk}	500μF
R_{DC}	360kΩ	R_{bulk}	400kΩ
R_{ON}	5Ω	R_b	750kΩ
R_{OFF1}	2.7Ω	R_{OFF2}	3.3Ω
Q_{top}, Q_{bot}	C2M0080170P	D_{top}, D_{bot}	GB25MPS17-247

TABLE V
EXPERIMENT CONDITIONS

Cases	RC snubber parameters	AGD operation	Figures
Case 1	No snubber (τ_{snub} = 0 ns)	No AGD	Fig. 13(a)
Case 2	τ_{snub} = 0.94 ns	No AGD	Fig. 13(b)
Case 3	τ_{snub} = 11 ns	No AGD	Fig. 13(c)
Case 4	τ_{snub} = 0.94 ns	AGD operated	Figs. 13(d), (e) Fig. 14(b)
Case 5	τ_{snub} = 0.94 ns	AGD not operated	Fig. 14(a)

On the other hand, in [18], the balancing resistor R_b for promoting the static voltage balancing of the switches is typically selected less than 1/10 of the OFF-state equivalent resistance $R_{\rm off}$ of the switch. According to [34], the nominal $R_{\rm off}$ of SiC MOSFET is about 17 MΩ, so that R_b was selected as 750 kΩ. The dc-link capacitors are composed of $C_{\rm DC}$ and $C_{\rm bulk}$. The film capacitor $C_{\rm DC}$ is placed on the closest as possible in the vicinity of the devices. This placement reduces the oscillation by reducing the stray inductance. $C_{\rm bulk}$ is a capacitor for supplying instantaneous current required for MPT. Both $C_{\rm DC}$ and $C_{\rm bulk}$ are connected in series considering the maximum voltage rating, and the balancing resistors, $R_{\rm DC}$ and $R_{\rm bulk}$, are connected in parallel with each capacitor to support capacitor voltage balancing.

The pulse signals for MPT are generated from TMS320F28335 MCU from Texas Instruments. The pulses of 200 and 100 kHz with 0.5 duty are applied to the switches during the tests. A bench power supply is employed for the proposed AGD and the control circuits. All other detailed parameters for the experiments are given in Table IV.

Commonly, a high voltage rating passive probe PPE2KV from Teledyne LeCroy with 300 MHz bandwidth or more may be used for voltage measurements of SiC MOSFETs' transient analyses as [35]. However, since the passive probe is not electrically isolated, it is impossible to measure the voltage of $Q_{\rm top}$ and $Q_{\rm bot}$ simultaneously shown in Fig. 11. Therefore, a differential probe is vital for the measurement in here. In addition, the purpose of this article is not to analyze the transient state in detail, but to analyze the voltage imbalance by C_p and the performance of the AGD. Hence, a probe bandwidth of 300-MHz or more is not required. For this reason, HVD3106A from Teledyne LeCroy was utilized for the measurements. The probe has 1.5 kV voltage rating and 120 MHz bandwidth. The inductor current measurements are performed by using the closed-loop type current probe CP150 with 10 MHz bandwidth from Teledyne LeCroy.

The switch current i_D is measured by a Rogowski current probe CTW3 from PEM. This current probe has a 600 A current rating and 30 MHz bandwidth.

B. Test Results

To examine the voltage balancing performance of the *RC* snubbers and the AGD operation, the five cases are considered as in Table V. In all cases, $R_{\rm OFF2}$ is set to 3.3 Ω. Two facts were confirmed in Section IV: A voltage imbalance increases with I_L when $R_{\rm OFF2}$ is equal to $R_{\rm OFF1}$, and $R_{\rm OFF2}$ increment is inevitable for AGD operation. From these facts, it is clear that the above conditions are more appropriate for comparing voltage inequality.

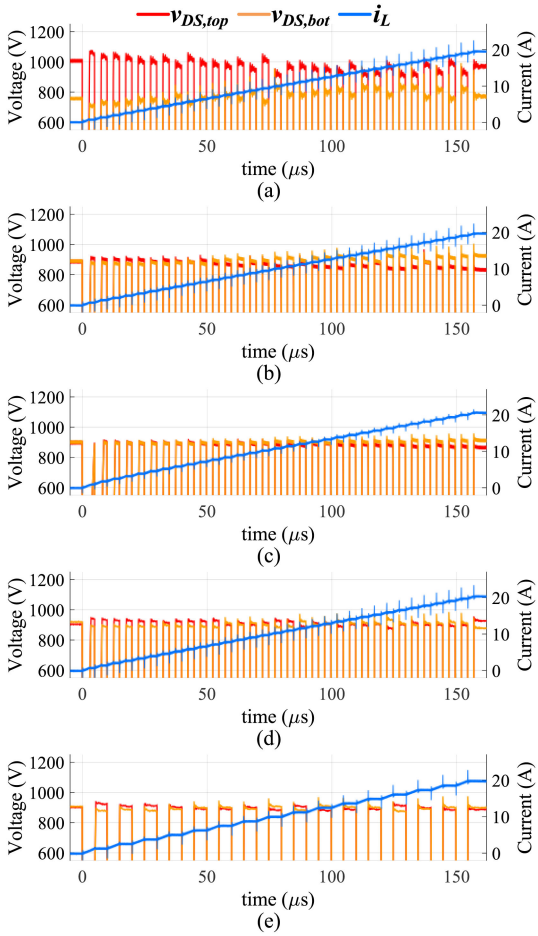

Fig. 13. Series-connected SiC MOSFETs experiment result waveforms under different condition. (a) Without RC snubber and AGD. (b) With minimum RC snubber value. (c) With maximum *RC* snubber value. (d) With AGD and minimum *RC* snubber in 200 kHz switching frequency. (e) With AGD and minimum *RC* snubber in 100 kHz switching frequency.

Fig. 13 compares the MPT experimental waveform under different conditions. Fig. 13(a) shows the experimental waveforms when neither *RC* snubbers nor the proposed AGD is not employed. In this case, the extreme voltage imbalance is observed in all current areas, and the maximum voltage imbalance is up to 404 V which is 22.4% of $V_{\rm DC}$. Figs. 13(b) and (c) show the waveforms with only the snubber circuits, cases 2 and 3 in Table V. Here, the voltage imbalance also occurs up to 101 and 51 V which are 5.6% and 2.8% of $V_{\rm DC}$, respectively. Apparently,

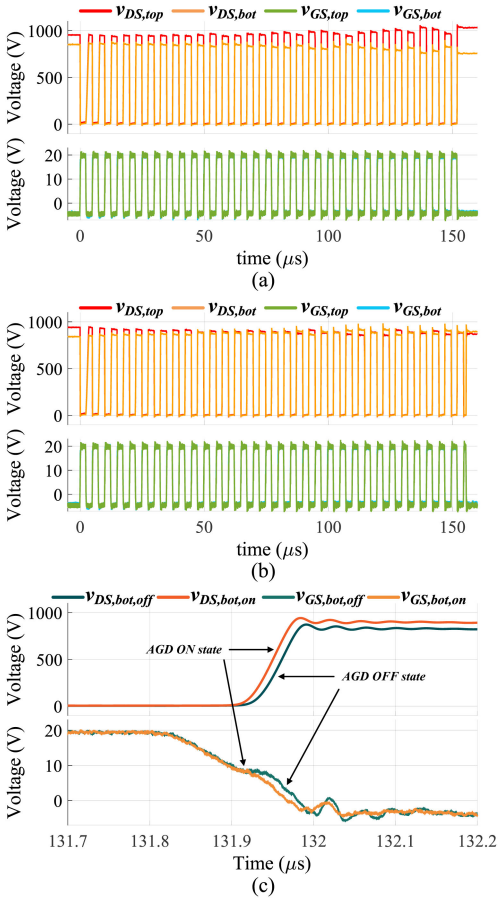

Fig. 14. Waveform of the SiC MOSFETs connected in series depending on AGD operation. (a) When AGD is not operating state. (b) When AGD is operating state. (c) Comparison of the bottom switch voltage waveforms depending on AGD operation.

the larger snubber in case 3 can successfully reduce the voltage imbalance as well as decreasing $dv_{\mathrm{DS,bot}}/dt$ which equals to dv_{SO}/dt as in (14). However, still the voltage imbalance exists in most current areas except for a particular current range, as shown in Fig. 9(e). Moreover, in these cases, higher switching loss is expected.

Figs. 13(d) and (e) are the experimental results of case 4. The AGD was tested at 200 and 100 kHz switching frequency conditions. In the result, the voltage balancing is not only achieved under different switching frequency conditions, but also performed very well under various load current conditions. The voltage imbalance with the AGD is up to 60.7 V for 200-kHz and 43 V for 100 kHz conditions. These values correspond to 3.4% and 2.5% of V_{DC}, respectively. Obviously, the voltage balancing performance is significantly improved compared to in case 3.

Fig. 14 compares the turn-OFF transient waveforms with and without the proposed AGD. Here, cases 4 and 5 are considered. When the AGD is not working so that v_{base} is holding at 1.4 V as in Fig. 6, the voltage imbalance occurs up to 292.3 V which is 16.2% of V_{DC}. In contrast, when the proposed AGD operates, the appropriate v_{base} is applied to the BJT. Accordingly, voltage

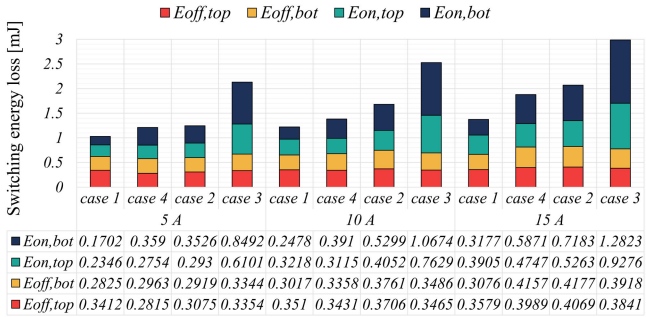

Fig. 15. Switching energy loss of the series-connected SiC MOSFETs for each case.

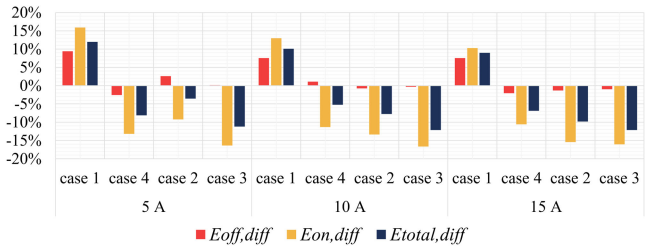

Fig. 16. Difference ratio of the series-connected SiC MOSFETs for each case.

balancing is achieved in almost all current areas as shown in Fig. 14(b). In this figure, the maximum voltage difference is evaluated as 57.3 V in the low current region. This value is merely 3.2% of V_{DC} and trivial in practice. When I_L is larger than 10 A, the voltage imbalance appears up to 40.1 V which is 2.2% of V_{DC}. Fig. 14(c) compares the waveforms of $v_{\mathrm{GS,bot}}$ and $v_{\mathrm{DS,bot}}$ according to the AGD operation at the same time interval. When the proposed AGD operates, the BJT impedance is decreased by v_{base} resulting in a fast turn-OFF of Q_{bot}. This result corresponds with the previous analysis where the turn-off delay Δt_{10} and dv_{DS}/dt of the switch are changed by R_G. In Fig. 14(c), $dv_{\mathrm{DS,bot}}/dt$ increases with 0.7 V/ns, and Δt_{10} is decreased by 8.8 ns when the AGD is operated.

C. Switching Loss Analysis

Fig. 15 analyzes the switching losses including snubber losses in each case, and Fig. 16 shows the loss imbalance ratio. Table VI gives the switching speed at each switch and voltage imbalance with ΔV which is $v_{\mathrm{DS,top}} - v_{\mathrm{DS,bot}}$. Although the voltage imbalance is significant, case 1 has the lowest switching loss, because there is no snubber circuit. Conversely, case 3 where the snubber constant is the longest shows the highest switching loss.

As given in Table VI, the switching speed of upper switch in case 1 is always faster than the lower one, so both $E_{\mathrm{off,top}}$ and $V_{\mathrm{ds,top}}$ are larger than others. At the turn-ON process, $E_{\mathrm{on,top}}$ is higher than $E_{\mathrm{on,bot}}$, because the top switch starts at a higher voltage despite its faster turn-ON speed. This trend is alleviated as the current increases.

Let us compare the loss distribution in cases 2–4. As shown in Fig. 16, for 5 A condition, case 2 loss imbalance is not that

TABLE VI
SWITCHING STATE COMPARISON

		dv_{DS}/dt (V/ns)				Switching energy loss (mJ)				ΔV (V)
		ON state		OFF state		ON state		OFF state		
		TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
5A	case 1	-35.78	-18.99	15.14	12.70	0.235	0.170	0.341	0.283	285.06
	case 4	-24.10	-17.64	6.40	6.20	0.275	0.359	0.282	0.296	-31.30
	case 2	-24.97	-17.36	6.74	6.40	0.293	0.353	0.307	0.292	18.58
	case 3	-16.17	-12.84	2.51	2.49	0.610	0.849	0.335	0.334	18.84
10A	case 1	-38.05	-18.05	27.37	20.12	0.322	0.248	0.351	0.302	404.24
	case 4	-24.80	-17.60	11.61	11.09	0.312	0.391	0.343	0.336	26.82
	case 2	-25.57	-17.84	12.31	11.54	0.405	0.530	0.371	0.376	-67.23
	case 3	-16.28	-12.98	4.41	4.33	0.763	1.067	0.346	0.349	-31.34
15A	case 1	-37.23	-19.94	33.24	26.59	0.390	0.318	0.358	0.308	199.37
	case 4	-25.02	-17.91	16.29	15.32	0.475	0.587	0.399	0.416	-25.44
	case 2	-25.58	-18.07	17.28	15.95	0.526	0.718	0.407	0.418	-97.83
	case 3	-16.45	-12.80	6.31	6.18	0.928	1.282	0.384	0.392	-30.96

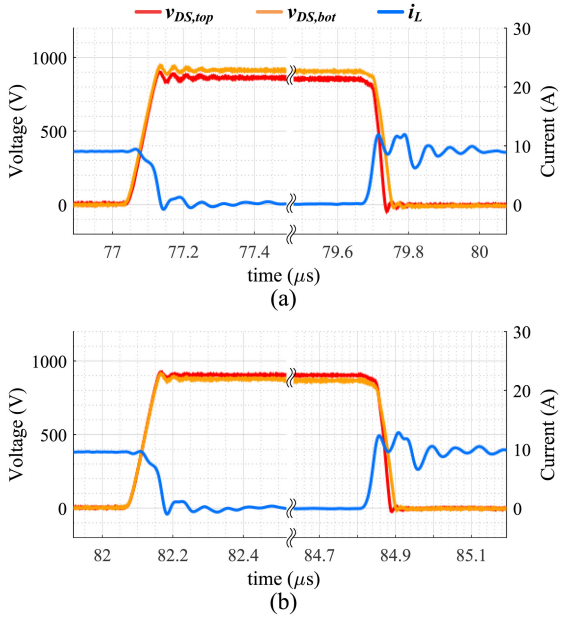

Fig. 17. Switching transient waveform at 10 A under different case. (a) With minimum *RC* snubber value, case 2. (b) With AGD and minimum *RC* snubber, case 4.

much serious. However, the loss imbalance in case 2 is getting severe as increasing the load current. This trend is the same in case 3. Meanwhile, case 4 with the proposed AGD shows even loss distributions in the series-connected devices.

For comparing cases 2 and 4 where same *RC* snubber constant is employed, the total losses of case 4 is lower than the ones of case 2. It means that the voltage imbalance between series-connected switches increases the switching loss. It is supposed that this is mainly caused by the discharging energies of the parasitic and snubber capacitors which are proportional to the square of the drain-source voltage of the semiconductor switch. When the voltages in the switches are well balanced, the discharging energies are minimized, so that lower switching loss can be obtained. On the other hand, in Table VI and Fig. 17, in both cases 2 and 4, the turn-OFF speeds of the upper and lower switches are very similar, but a loss imbalance occurs due to the slow turn-ON speed of the lower switch. This phenomenon strengthens as the turn-OFF voltage of the lower switch increases. Loss inequality due to the turn-ON rate difference occurs more intensely in case 3, where the snubber constant is the longest.

In cases 1 and 2 with $I_D = 15$ A, the loss inequality is evaluated as 9.0% and 9.8%, but it decreased to 6.9% in case 4.

D. Limitation

The proposed AGD enables the following functional improvements through several circuit modifications.

1. *Voltage Equilibrium in Various $V_{\rm DC}$ Ranges*: If a reference voltage is generated according to a $V_{\rm DC}$ instead of a fixed $V_{\rm ref}$ shown in Fig. 6, it can operate in various $V_{\rm DC}$ ranges.
2. *Extension of Devices in Series*: If the issues discussed below are improved, stable AGD control is possible on the ground disconnection switch using voltage sensing circuits that reduce switching noise [30].
3. *Duty Limit*: The S/H delay of the proposed method requires at least 500 ns of a turn-OFF time. This delay limits a maximum duty to 0.9 under the experimental conditions of this article. By reducing the switching frequency or delay length, this constraint can be relaxed.

However, overcoming the following fundamental problems is a priority.

1. *Performance limitation of PI Controller*: In (12), Δt_{10} is proportional to R_G, so the relationship between the time delay and the voltage imbalance is proportional to the gate turn-OFF resistance. In [23], since the proper delay time for voltage equilibrium is inversely proportional to the current, increasing current can lead to a large voltage imbalance even in small delay time errors. That is, the control sensitivity increases with the load current. Due to these inverse characteristics, the PI controller is not suitable for systems with varying currents. This article reduced control sensitivity and increased stability by lowering the switching speed with snubber. Fig. 10 shows this trend. Therefore, to remove the snubber or control it in

all switches connected in series, the limit of the controller must be improved.

2. *Snubber*: The method proposed in this article is a kind of hybrid AGD because a passive snubber is combined. This causes additional losses as shown in Fig. 15. If the control problem discussed above is solved, then snubber removal might be possible.
3. *Turn-OFF Voltage Control*: Meanwhile, it can be seen from the experimental results of this article that all AGDs controlling the turn-OFF sequence have limitations. Even if the turn-OFF voltage is absolutely controlled, loss inequality will inevitably occur in the turn-ON process, so it is difficult to industrialize it in terms of life and heat dissipation. In order to make serial switches practical in the future, we need to study how to eliminate loss inequality even if a small voltage inequality is allowed.

E. Discussion

The above analysis and experimental verification show the excellence of the proposed method. The proposed method has voltage balancing performance within 3.4% as in Fig. 13. As can be seen in Fig. 15, the loss imbalance is also reduced from 9.0% and 9.8% in cases 1 and 2, respectively, to 6.9% with the proposed method. The proposed AGD has the benefits of not being constrained by voltage isolation limits due to the single switch's gate change and applying to higher switching frequency compared to previous studies. Furthermore, the proposed AGD operates independently on each switch, which does not impose a computational burden on MCU.

In terms of the circuit realization, the proposed method is simply implemented with commercially available low-cost chips. It also does not require an extensive space in the circuit board. However, the proposed method may not be free from the tradition of the analog circuit implementation such as the circuit layout and component aging issues.

VI. Conclusion

In this article, the turn-OFF time delay control method was proposed for series–connected SiC MOSFETs. First, the turn-OFF characteristics with the parasitic gate-ground capacitor of stacked MOSFETs were explained using modeling equations. Then, by uses the properties of the BJT, the gate turn-OFF resistance is adjusted to modify the turn-OFF delay time for voltage balancing. The proposed method was verified through simulation and experiment. Through the simulation, the effects of the parasitic capacitor and *RC* snubber were discussed, and the minimum *RC* snubber value for the stable operation without system failure was selected. The experimental results have shown that the proposed method improves voltage sharing and loss balancing in series-connected SiC MOSFETs. With the proposed AGD, the maximum voltage imbalance ratio was reduced from 22.4% to 3.2% at the full voltage and entire load conditions. The switching loss imbalance was also lowered from 9.0% to 6.9% at the full load condition. In sum, the proposed method can successfully achieve the voltage and loss balancing in the series-connected SiC MOSFET structure.

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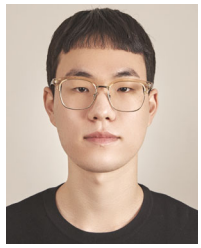

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