A Practical Digital Implementation of Completely Decentralized Ripple Minimization in Parallel-Connected DC–DC Converters

Soham Dutta, *Student Member, IEEE*, and Brian Johnson, *Member, IEEE*

***Abstract*—Parallel dc–dc converters are commonplace in applications such as computing power supplies, point of load systems, and dc microgrids. The presence of multiple converters in such systems allows for switch interleaving and ripple cancellation. One class of existing ripple reduction methods depends on central controllers that require communication among the converters. These approaches compromise system scalability and reliability. When it comes to decentralized methods, the state-of-the-art is limited to uniform conditions and cannot handle mismatches in physical parameters and operating points among converters. In this article, we address these shortcomings with fully decentralized controller that robustly drives the pulsewidth modulation carriers of a collection of heterogeneous converters to the phase-shifts that give minimized ripple. More precisely, the proposed controller eliminates the dominant fundamental switching harmonic from the output current and voltage using only local voltage feedback. After outlining a comprehensive analytical model, we experimentally validate our approach on a system of five parallel-connected buck converters under a variety of parametric and operational mismatches. Measurements show ripple reduction of more than $4\times$ in the output voltage and the fundamental switching frequency harmonic is attenuated by more than 30 dB compared to conventional symmetric interleaving.**

***Index Terms*—Dc microgrids, decentralized control, electric vehicles, interleaving, modular converters, multiphase converters, parallel dc–dc converters, ripple minimization.**

I. Introduction

SYSTEMS of parallel-connected dc–dc converters are ubiquitous across a variety of applications. Architectures with parallel-connections on both the inputs and outputs [see Fig. 1(a)] are generally referred to as *multiphase* converter systems and are often seen in computing applications [2]. Setups with independent inputs (outputs) and parallelized output (input) interconnections, as shown in Fig. 1(b), appear in many applications from dc microgrids to mobile devices [3], [4], [5]. For low power mobile or computing applications this configuration is often called a *point-of-load* system. Furthermore, with advances in electric vehicles and their charging systems, efforts are being made to reduce charging time by use of extreme fast charging (XFC) systems that utilize series-stacked ac–dc converters to draw power from the medium voltage grid [6], [7]. As depicted in Fig. 1(c), the dc-sides of these isolated ac–dc converters are connected in parallel and fed to the vehicle battery in order to increase current-carrying capacity and reduce battery current ripple. Although current ripple is unavoidable in any power electronic system with pulsewidth modulation (PWM), the presence of multiple parallel converters allows for the use of switch interleaving to obtain ripple cancellation [8].

However, the fact that interleaving may require control of the relative switch timing among many converters creates challenges. For instance, as the number of converters goes up we are eventually impeded by finite PWM and analog to digital conversion (ADC) channel counts as well as computational resource limitations on any given digital controller. Distributed methods with multiple digital controllers dispersed across converters necessitate high bandwidth communication channels for the exchange of PWM-related data in real-time. Hence, centralized and distributed control architectures, as found in [8], [9], [10], [11], [12], [13], [14], [15], [16], cannot be extended to systems with arbitrarily large converter counts. Furthermore, any source of asymmetry among converters obscures what phase shifts are needed between converter switch signals for ideal ripple cancellation [16], [17]. A solution that can minimize ripple under operating point asymmetries and is scalable to arbitrary converter counts is lacking in prior literature.

Multiphase systems as shown in Fig. 1 offer several key performance advantages that make them the default choice for high current applications. Advantages include relaxed input and output capacitance requirements, dispersed heat dissipation, improved efficiency at high currents, and enhanced dynamic performance [18]. These benefits are compounded as the number of paralleled units increases. In general, when N identical converters operate under uniform conditions at their inputs and outputs, then evenly dispersed phase shifts of $360^\circ/N$ between their PWM signals yields minimum net ripple. This condition, which is known as *symmetric interleaving*, yields minimized net ripple only under this ideal setting and is mainly practiced in

Manuscript received 23 March 2022; revised 14 June 2022; accepted 24 July 2022. Date of publication 10 August 2022; date of current version 6 September 2022. Funding provided by the U.S. Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office under Grant DE-EE0008346. The work of Brian Johnson was supported by the Washington Research Foundation. This paper is an extension of a conference paper that was presented at the 13th Annual Energy Conversion Congress and Exposition on October 12th, 2021 [1]. Recommended for publication by Associate Editor J. Liu. *(Corresponding author: Soham Dutta.)*

The authors are with the Department of Electrical and Computer Engineering, University of Washington, Seattle, WA 98195 USA (e-mail: sdutta@uw.edu; brianbj@uw.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3197674.

Digital Object Identifier 10.1109/TPEL.2022.3197674

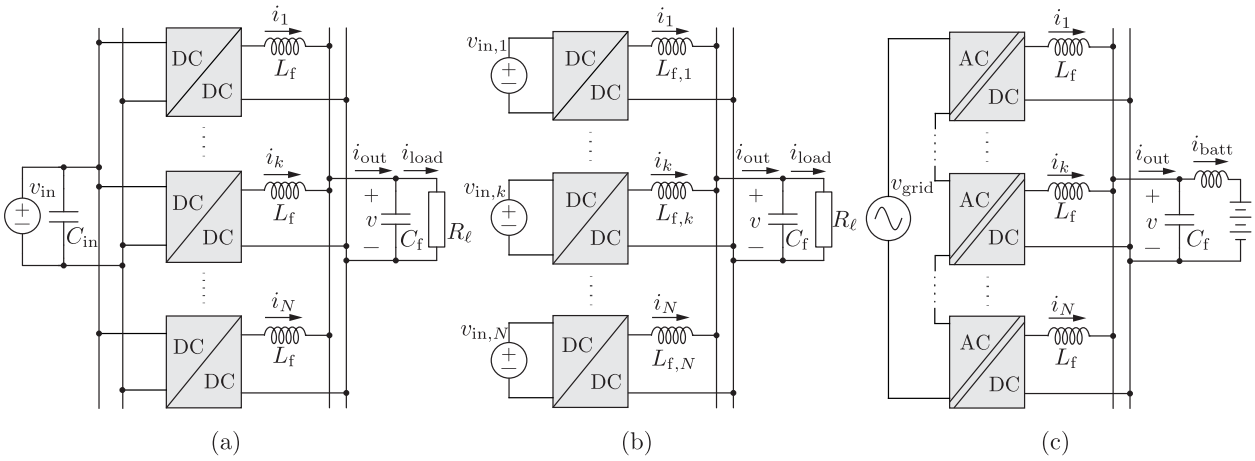

Fig. 1. System architecture of parallel-connected DC–DC converters: (a) Parallel-input parallel-output multiphase system. (b) Parallel-output converter system with nonuniform decoupled input sources (c) Electric Vehicle charger with series connected isolated ac–dc modules on the grid side and paralleled dc outputs on the battery side.

multiphase dc–dc systems with a central controller controlling a modest numbers of converters [18].

Generally speaking, any source of nonuniformity degrades ripple cancellation if symmetric interleaving is maintained. For instance, unavoidable parametric mismatches among filter inductances reduces ripple cancellation [17], [19]. Going one step further and looking at systems with nonuniformly rated modules and decoupled inputs, such as dc microgrids that mirror Fig. 1(b), the extent of nonuniformity only goes up. In such scenarios, mismatches among the input-side voltages or filter inductances naturally lead to nonuniform inductor current ripples among the converters. Therefore, it becomes necessary to determine the optimal set of phase shifts among the converter waveforms so that the overall output current ripple is minimized. Reduction in current ripple can be used to minimize the size and current rating of the filter capacitance and improve power density. Hence, we seek for a control strategy that gives us a high degree of ripple cancellation under asymmetries, and is also amenable to a decentralized control implementation such that arbitrarily sized systems can be assembled.

Considering the discussion above, it should no wonder that ripple cancellation in asymmetric systems has been a focus of recent investigations. Previous work on this front has mostly been centered on centralized controllers [10], [11], [12], [13], [14], [15], [16] that require global knowledge of the network and control parameters, and, hence, lack scalability. In [12] and [13], three different algorithms were proposed for solving the optimal phase shifts that minimize total harmonic distortion. However, two of these algorithms require a centralized controller with real-time knowledge of the system parameters. Moreover, the remaining decentralized algorithm gives slow convergence due to its high computational burden. The methods in [15] and [16] break the dependence on system-level knowledge and reduce online computations through the use of look-up tables that store the optimal phase shifts that minimize the fundamental harmonic in the current ripple. However, the system under consideration and optimization result in [15] and [16] are limited to only three modules and uses a central controller. Decentralized control methods for ripple minimization in various multiconverter systems can be found in [20], [21], [22], [23], [24], [25]. The approach in [20] gives a decentralized solution based on dynamics of coupled nonlinear oscillators. However, it only handles identical converters and relies on a high measurement sample rate that prevents its use at high switching frequencies. Recently, the work in [21] shows an optimization technique for decentralized asymmetric dc–ac inverters.

In this article, we propose and experimentally validate a novel controller that addresses several of the aforementioned drawbacks of existing approaches and whose advantages can be summarized as follows.

1) Implementation is fully decentralized and requires only local voltage measurements.
2) The proposed method can be robustly applied in both symmetric and asymmetric converter setups.
3) The control law takes the form of a simple proportional controller and does not require any complex time-consuming optimization algorithm or look-up tables.
4) The sample rate of the sensed voltage is equal to the converter switching frequency (or integer multiples) such that oversampling is unnecessary and implementations at high switching frequencies are feasible.
5) Our method resides only in the PWM logic and can be seamlessly integrated alongside any existing current or voltage controller without affecting their performance.
6) Clock drift among multiple digital controllers [26] is addressed by the proposed method, since it operates operates at a much faster rate and corrects the phases of the carriers in each switch cycle.

The key innovation needed to uncover this simple implementation lies in the timing of the sampling instant of the locally available voltage measurement. In summary, we show that a measurement taken at a precisely chosen time-instant captures all information needed for decentralized feedback control and convergence to the PWM phase shifts, which minimize the switching ripple. In particular, output ripple is reduced by minimization of the fundamental harmonic in the output voltage

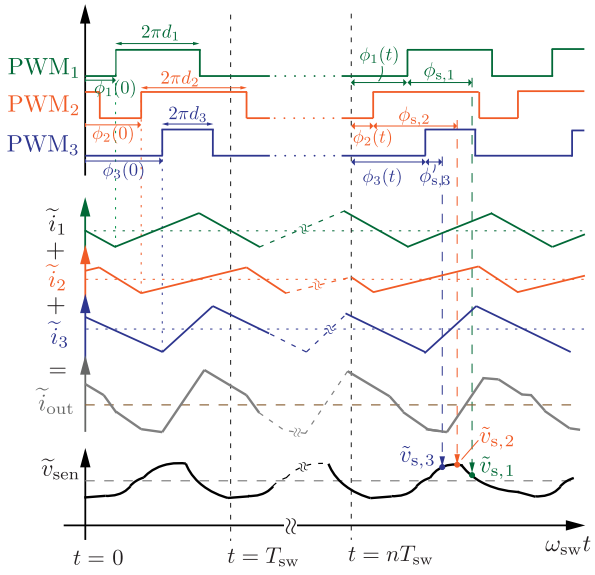

Fig. 2. Representative switch-level waveforms for a system of three parallel converters. The ripple currents sum and yield the load capacitor voltage. This signal is processed by a sensor and analog filter network to yield $\widetilde{v}_{\text{sen}}$, which appears at the ADC terminals. This signal is sampled by the ADC at the indicated instances in time by each respective converter.

and current. Since the fundamental harmonic dominates, this in turn yields low distortion at the output.

Hereafter, this article is organized as follows: Section II outlines notation and establishes foundational analysis for the quantification of ripple harmonics. Next, the controller is formulated in Section III and its hardware implementation is provided. Experimental results follow in Section IV. Finally Section V concludes this article.

II. Fourier Analysis of Voltage Ripple

For the sake of generality, we analyze systems with asymmetry in both input voltages as well as filter inductances. As shown in Fig. 1(b), we consider N dc–dc converters connected in parallel at their output and delivering power to a common load with resistance R_ℓ across filter capacitance C_{f}. The set $\mathcal{N}$ is defined as $\mathcal{N} := \{1, 2, \ldots, N\}$. $v_{\text{in},k}$ and $L_{\text{f},k}$ are the input voltage and the filter inductance of the kth converter, respectively. The kth converter operates with duty ratio d_k that is produced by any arbitrary controller.

Now, we aim to uncover the dependence of the net output current and voltage ripple on the converter PWM phase shifts. For a generic system of N converters, the kth unit has duty ratio and PWM phase-shift d_k and $\phi_k(t)$, respectively. The phase $\phi_k(t)$ is defined with respect to a reference frame synchronously rotating at angular velocity ω_{sw}. In the following analysis, we assume the output voltage has small ripple and that the inductor currents are triangular waveforms. A triangular waveform for the kth converter inductor current is denoted as i_k and its ac ripple component is $\widetilde{i}_k$. Waveforms for an example system of three converters are shown in Fig. 2. The Fourier series for the

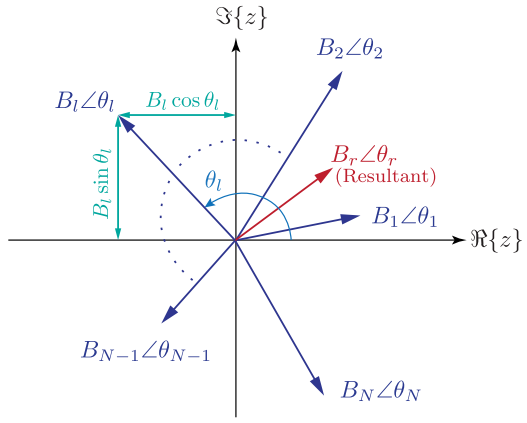

Fig. 3. Phasor decomposition of the fundamental component in capacitor voltage ripple denoted as $B_r\angle\theta_r$.

ripple current $\widetilde{i}_k$ is given by

$$\widetilde{i}_k = \sum_{m=1}^{\infty} A_{k,m} \cos(m(\omega_{\text{sw}}t - \phi_k(t) - \pi d_k)) \tag{1}$$

where $A_{k,m}$ denotes the magnitude of the mth harmonic of the kth converter current ripple and is given by

$$A_{k,m} = -\frac{2V_{\text{out}}(-1)^m \sin(m(1-d_k)\pi)}{m^2\pi\omega_{\text{sw}}L_{\text{f},k}d_k}. \tag{2}$$

The total ripple current, $\widetilde{i}_{\text{out}}$, which flows into the filter capacitance is given by the summation

$$\widetilde{i}_{\text{out}} = \sum_{k=1}^{N}\widetilde{i}_k = \sum_{k=1}^{N}\sum_{m=1}^{\infty} A_{k,m}\cos(m(\omega_{\text{sw}}t - \phi_k(t) - \pi d_k)). \tag{3}$$

Hereafter, we focus on the fundamental harmonic in $\widetilde{i}_{\text{out}}$, since it dominates the ripple absorbed by the filter capacitor. Moreover, this component largely determines the capacitor size. Since we focus exclusively on the first harmonic from here forward, we will drop the use of the harmonic subscript m in subsequent analysis. The fundamental harmonic in the capacitor voltage ripple can be found by integrating the fundamental harmonic in (3) as follows:

$$\widetilde{v}^1 = \frac{1}{C_{\text{out}}}\int \sum_{k=1}^{N} A_k \cos(\omega_{\text{sw}}t - \phi_k(t) - \pi d_k)\, dt \tag{4}$$

$$= \sum_{k=1}^{N} B_k \cos(\omega_{\text{sw}}t + \theta_k(t)) \tag{5}$$

where $B_k = A_k/(\omega_{\text{sw}}C_{\text{out}})$ and $\theta_k(t) = \pi\bar{d}_k - \phi_k(t)$. The complement of d_k is $\bar{d}_k = 1 - d_k$. Expressing (5) in polar form gives

$$\vec{v}^1 = \sum_{k=1}^{N} B_k e^{j\theta_k} = B_r e^{j\theta_r} \tag{6}$$

which is pictorially depicted in Fig. 3. Using phasors to assist visual intuition, the contribution of the kth converter to the net

TABLE I
SYSTEM PARAMETERS IN NUMERICAL SIMULATIONS

Symbol	Description	Value	Units
V_{out}	Steady state output voltage	12	V
f_{sw}	Nominal switching frequency	20	kHz
L_{f}	Filter inductance per module	230	μH
C_{f}	Output filter Capacitance	25	μF
R_ℓ	Load resistance	5	Ω

voltage ripple is represented by a phasor with amplitude B_k and phase θ_k. The summation of all N phasors has amplitude B_r and phase θ_r. This gives the net 1st harmonic component present in the capacitor voltage ripple. The magnitude of B_r can be obtained from inspection of Fig. 3 and use of basic vector addition methods as follows:

$$B_r^2 = \left(\sum_{k=1}^{N} B_k \cos\theta_k\right)^2 + \left(\sum_{k=1}^{N} B_k \sin\theta_k\right)^2. \quad (7)$$

Eq. (7) can be simplified as

$$B_r^2 = \sum_{k=1}^{N}\sum_{l=1}^{N} B_k B_l \cos(\theta_k - \theta_l). \quad (8)$$

III. PROPOSED DECENTRALIZED PHASE-SHIFT CONTROL

In essence, B_r represents the RMS of the fundamental harmonic present in the capacitor voltage ripple. Note that the fundamental harmonic is completely eliminated iff, $B_r = 0$. However, if system asymmetries are such that the differences between the converter-generated component contributions B_k, $(k \in \mathcal{N})$ are too large, there may not exist any set of angles, $\{\theta_1, \ldots, \theta_N\}$, that give complete first harmonic cancellation. Given an example system of three converters, this could be visualized as phasors that cannot form a closed triangle or satisfy the triangle inequality

$$\|a+b\| \le \|a\| + \|b\|, \quad \forall a, b \in \{B_1, B_2, B_3\}. \quad (9)$$

Therefore, our objective is to minimize B_r for any possible scenario. Since B_r is non-negative, B_r^2 has the same minima as B_r. Hence, for ease of analysis we seek to minimize the cost function

$$U(\phi) = B_r^2. \quad (10)$$

In other words, we seek to obtain the vector of PWM phase shifts $\phi = [\phi_1, \ldots, \phi_N]^\top$, that minimize the unconstrained optimization problem whose cost function is $U(\phi)$. However, since $U(\phi)$ is a nonconvex function of ϕ, it can have multiple local minima. To illustrate the nature of $U(\phi)$ in asymmetric conditions, we simulate a system of $N = 3$ converters connected in parallel. The component parameters and operating conditions for these simulations are in Table I. We show the following two cases:

Case 1: Here, we study the shape of $U(\phi)$ as a function of PWM phase shifts. To induce asymmetry, the three input voltages are chosen as $v_{\text{in},1} = 36$ V, $v_{\text{in},2} = 24$ V, and $v_{\text{in},3} = 48$ V. All remaining parameters are identical and their output voltage is $V_{\text{out}} = 12$ V. We sweep ϕ_2 and ϕ_3 independently from 0 to 2π while fixing $\phi_1 = 0$ and plot the magnitude of $U(\phi)/U_{\text{symm}}$ in Fig. 4, where U_{symm} is the value of $U(\phi)$ at symmetric interleaving (i.e., when $\phi_1 = 0$, $\phi_2 = 120°$ and $\phi_3 = 240°$). Evidently $U(\phi)$ has 2 local minima where the fundamental harmonic can be reduced by more that 20 dB in comparison to the value at symmetric interleaved state. These minima are obtained at $\phi_2 \approx 72°, \phi_3 \approx 234°$, and $\phi_2 \approx 224°, \phi_3 \approx 150°$. ■

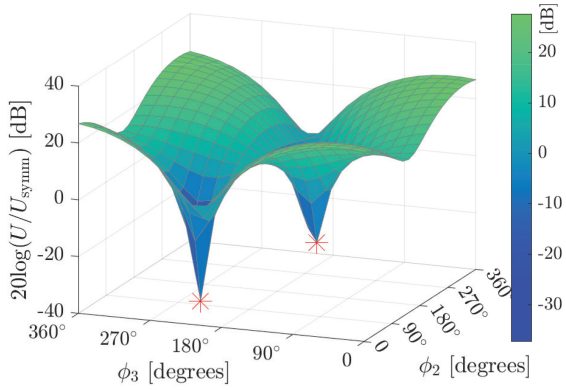

Fig. 4. Cost function $U(\phi)$ normalized with respect to its value at symmetric interleaved state while ϕ_2 and ϕ_3 are varied as described in Case 1.

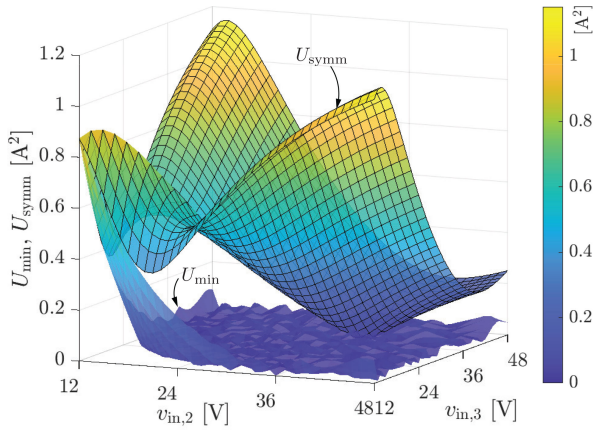

Fig. 5. Surfaces traced out by local minima of $U(\phi)$, denoted as U_{min}, and value of $U(\phi)$ at symmetric interleaving as the input voltages are varied as described in Case 2.

Case 2: Next, we investigate whether the local minima obtained for $U(\phi)$ provides enhanced ripple reduction compared to the symmetric interleaved state for any arbitrary input voltages. We independently sweep the input voltages $v_{\text{in},2}$ and $v_{\text{in},3}$ of the 2nd and 3rd converter, respectively, from 12 to 48 V while fixing $v_{\text{in},1} = 36$ V and $V_{\text{out}} = 12$ V. The results are in Fig. 5, where the meshed surface represents the values of $U(\phi)$ at symmetric interleaving, denoted as U_{symm}, and the unmeshed surface represents the values of the local minima of $U(\phi)$, denoted as U_{min}. It can be seen that U_{min} is much lower than U_{symm} across every operating point in the sweep except one. U_{symm} equals U_{min} only when the system operating conditions are uniform (i.e., $v_{\text{in},1} = v_{\text{in},2} = v_{\text{in},3} = 36$ V). Therefore, we can infer that for any condition of asymmetry, operating the system at the local minima of $U(\phi)$ provides much better

ripple reduction which in turn allows for passive filter size reduction. ■

Now, we seek a controller that drives the PWM phases, ϕ_k, $(k \in \mathcal{N})$, toward a local minimum of $U(\phi)$ from any initial condition. We do this by construction of a gradient-descent-based control law that asymptotically drives $U(\phi)$ toward a local minimum [27], [28]. In particular, the phase of the kth PWM signal has the dynamics

$$\dot{\phi}_k = -K\frac{\partial U(\phi)}{\partial \phi_k}, \quad \forall\, k \in \mathcal{N} \tag{11}$$

where K is the controller gain applied across all units.

A. Controller Derivation

Now, we derive an implementable form of (11). Since $\theta_k = \pi \bar{d}_k - \phi_k$ and $\bar{d}_k$ is a constant, we can write

$$\frac{\partial U(\phi)}{\partial \phi_k} = -\frac{\partial U(\theta)}{\partial \theta_k}, \quad \forall\, k \in \mathcal{N}. \tag{12}$$

Taking the partial derivative of (8) with respect to θ_k gives

$$\frac{\partial U(\phi)}{\partial \phi_k} = -2\sum_{l=1}^{N} B_k B_l \sin(\theta_{kl}) \tag{13}$$

where $\theta_{kl} = \theta_k - \theta_l$. Hence, (11) becomes

$$\dot{\phi}_k = 2K\sum_{l=1}^{N} B_k B_l \sin(\theta_{kl}), \quad \forall\, k \in \mathcal{N}. \tag{14}$$

Note that the phase-shift dynamics in (14) takes the form of coupled Kuramoto oscillators [29], which can either synchronize or repel if K is negative or positive, respectively. In our setting, it turns out that the converter units with Kuramoto dynamics minimize the net RMS ripple. Discretizing (14) gives the following PWM phase shift update rule at the $[n+1]$th time step

$$\phi_k[n+1] = \phi_k[n] + 2T_{\text{sw}}K\sum_{l=1}^{N} B_k B_l \sin(\theta_{kl}[n]). \tag{15}$$

To illustrate performance of the control law in (15), we now apply it to the system described in Case 1. Referring to Fig. 7, the vector field shows that the system will reach one of minima irrespective of the initial condition. Convergence to either one of the particular minima depends on the initial phase shifts, denoted as $(\phi_{2\text{o}}, \phi_{3\text{o}})$ in Fig. 7.

B. Decentralization of Control

The controller in (15) requires global knowledge of the parameters and operating points such as inductances, filter capacitance, output voltage, duty ratios d_k, and phase shift angles $\phi_k, \forall\, k \in \mathcal{N}$. In this section, we will show how this information is encoded within the locally sampled capacitor voltage and enables decentralized feedback loops.

Our implementation in Fig. 6 collectively includes sensing, analog signal filtering, ADC, digital control, and digital PWM. The capacitor voltage, v, is measurable at every set of converter terminals. An analog high-pass RC filter is installed at each converter output and removes the dc component from the sensed voltage to yield the ripple component denoted as $\widetilde{v}$. An op-amp, isolation amplifier, or generic sensor processes this signal which is also low-pass filtered to attenuate frequencies above the nominal switching frequency. This signal chain structure deliberately contains cascaded high-pass and low-pass operations so that the fundamental switching harmonic is preserved with a sufficiently high amplitude. This signal produced by the aforementioned signal chain is denoted as $\widetilde{v}_{\text{sen}}$ and is available at the ADC inputs for each converter-level digital controller.

The aforementioned analog signal chain collectively imparts a gain and phase shift to the fundamental switching component. In real applications with manufacturing tolerances and parasitics, the gain and the phase shift will not be exactly the same among converters. For instance, the gain tolerance of a typical isolation amplifier for voltage sensing is typically $\pm 0.05\%$. This small variation has minimal effect on controller performance. For the sake of completeness, we consider this variation by denoting the gain as G_k and phase shift as ψ_k for the kth converter. Recalling that the fundamental switching component of the output voltage is given by (5), it follows that the sensor output for the kth unit is

$$\widetilde{v}_{\text{sen},k} \approx \sum_{l=1}^{N} G_k B_l \cos(\omega_{\text{sw}} t + \theta_l - \psi_k). \tag{16}$$

To sample the above voltage in each switching period, we trigger the ADC of the kth converter at an angle $\phi_{\text{s},k}$ relative to the start of the switch period. Referring to Fig. 2, this translates to sampling the sensed voltage waveform at an angle $\omega_{\text{sw}} t = 2n\pi + \phi_{\text{s},k} + \phi_k$ in the nth cycle. From (16), the kth sampled voltage is

$$\widetilde{v}_{\text{s},k} \approx \sum_{l=1}^{N} G_k B_l \cos((\phi_{\text{s},k} + \phi_k) + \theta_l - \psi_k). \tag{17}$$

Recalling that $\theta_k = \pi \bar{d}_k - \phi_k$, we get

$$\widetilde{v}_{\text{s},k} \approx \sum_{l=1}^{N} G_k B_l \cos(\phi_{\text{s},k} + \pi \bar{d}_k - \theta_k + \theta_l - \psi_k). \tag{18}$$

Comparison of (18) with (13)–(14), we see that if the sampling instant is chosen as $\phi_{\text{s},k} = \frac{\pi}{2} - \pi \bar{d}_k + \psi_k$, then (18) becomes

$$\widetilde{v}_{\text{s},k} \approx \sum_{l=1}^{N} G_k B_l \sin(\theta_{kl}) \tag{19}$$

which matches the form of the proposed gradient-descent controller given in (14). In discrete time (19) is $\widetilde{v}_{\text{s},k}[n] \approx \sum_{l=1}^{N} G_k B_l \sin(\theta_{kl}[n])$. Therefore, the phase-shift update rule in (15) is now

$$\phi_k[n+1] = \phi_k[n] + (T_{\text{sw}} K_{\text{p},k}) \times \widetilde{v}_{\text{s},k}[n] \tag{20}$$

where $K_{\text{p},k}$ is the feedback gain of the k'th converter controller and is $K_{\text{p},k} = (2KB_k)/G_k$. Therefore, we show that using the locally sampled capacitor voltage value as feedback, we can implement the proposed gradient-descent control at each converter in a decentralized fashion.

The key parameter that lies at the crux of this controller is the selection of the sampling instant. As can be seen in Fig. 6,

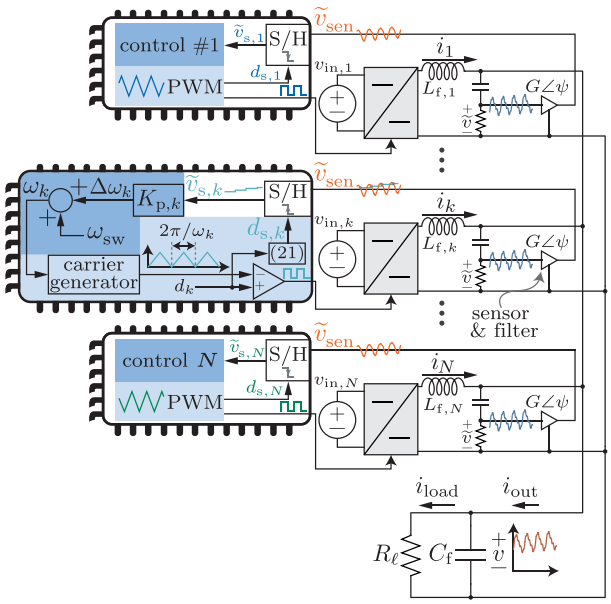

Fig. 6. Practical implementation of the proposed control. A voltage v appears across the load. Each converter has a high-pass filter that removes the dc-component of v and yields $\widetilde{v}$. A sensor and filter network imparts gain and phase shift G and ψ, respectively, and produces $\widetilde{v}_{\text{sen}}$ appears at the ADC terminals. The aforementioned voltage signals are globally available to each converter. Each converter has an independent control loop that dictates the sampling instant and adjust the local switching frequency. The system collectively drives the ripple in v to a minimum.

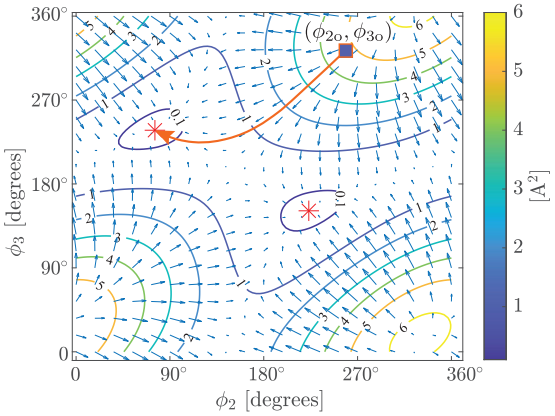

Fig. 7. Simulation of the proposed gradient-descent law showing convergence to one of the local minima.

the filtered signal is sampled at a particular time instant in each switching cycle as characterized by duty ratio

$$d_{\text{s},k} = \frac{\phi_{\text{s},k}}{2\pi} = \frac{1}{4}\left(2d_k - 1\right) + \frac{\psi_k}{2\pi} \tag{21}$$

where this expression follows from the prior definition of $\phi_{\text{s},k}$. Also note that this implies the need for a reasonable estimate of the phase-lag, ψ_k, introduced by the analog signal-chain. This can be obtained by using a signal generator to feed the sensor circuitry and measuring the phase lag of the sensor output with respect to the input. Each converter-level digital controller carries out the PWM phase shift update in (20) via incremental adjustments of the switching frequency as follows:

$$\Delta\omega_k = \frac{\phi_k[n+1] - \phi_k[n]}{T_{\text{sw}}} \tag{22}$$

$$= K_{\text{p},k} \times \widetilde{v}_{\text{s},k}[n] \tag{23}$$

where $\omega_k = \omega_{\text{sw}} + \Delta\omega_k$ is computed in each switch cycle and ω_{sw} is the nominal switching frequency (see Fig. 6). In other words, the sampled voltage is multiplied by $K_{\text{p},k}$ and added to the nominal switching frequency. In effect, a perturbation in the switching frequency allows us to indirectly adjust the PWM phase shift angle. This method of adjusting phase by changing the frequency is similar to the operation of a phase-locked loop (PLL) an example of which is the synchronous reference frame (SRF) PLL used for control of grid-connected power converters [30].

The switching frequency will come back to the nominal ω_{sw} once the converters have reached the desired phase in steady state. This can be inferred from (20), which in continuous time gives

$$\dot{\phi_k} = K_{\text{p},k} \times \widetilde{v}_{\text{s},k}[n]. \tag{24}$$

Since in steady state $\dot{\phi}_k = 0$, hence, the sampled voltage is $\widetilde{v}_{\text{s},k}[n] = 0$, which implies that in steady state $\Delta\omega_k = K_{\text{p},k} \times \widetilde{v}_{\text{s},k}[n] = 0$. This observation allows us to infer the physical meaning of the controller as follows: The proposed controller uses an integrator, which adjusts the phase shift of the PWM carrier to regulate the magnitude of the voltage ripple at a specific point on the waveform and drive it toward zero. Since every unit tries to achieve this, the number of zeros in the capacitor voltage waveform increases, which implies that the amplitude of the voltage ripple decreases.

The choice of $K_{\text{p},k}$ entails a tradeoff between convergence speed and stability. A large value of $K_{\text{p},k}$ will give faster convergence but compromises numerical stability of the algorithm. To guarantee convergence to a local minima, $K_{\text{p},k}$ must be chosen in the following interval:

$$0 < K_{\text{p},k} < \frac{2B_k f_{\text{sw}}}{(2N-1)B_{\max}^2 G_k} \tag{25}$$

where $B_{\max} = \max\{B_\ell\}$ for $\ell \in \mathcal{N}$. The derivation of this result is given in the Appendix.

C. Effect of Sampling Point Timing Error

Here, we analyze the impact of unintended or unmodeled variations in the ADC sample timing on controller performance. The ideal sampling instant should occur at $\phi_{\text{s},k} = \frac{\pi}{2} - \pi\bar{d}_k + \psi_k$. Note that sample timing can be straightforwardly manipulated in modern digital controllers and, hence, are of negligible concern here. The more likely source of error stems from the measurement of the phase lag ψ_k contributed by the sensor and filter network. We denote the difference between the measured phase lag and its actual value as $\Delta_k = \psi_k - \psi_{k,\text{meas}}$. This error quantity can be distinct among converters. We make two assumptions on this error. First, we assume that the tolerances of the passive components used in the low-pass filter are small (approximately $0.5\% - 1\%$) so that ψ_k varies within a small

range. And second, the phase lag measurements are consistent enough to have a small standard deviation. With these two assumptions, we approximate this error as an angle Δ for all the units (i.e., $\Delta_k \approx \Delta$ for $k \in \mathcal{N}$). This implies that the sampling actually occurs at $\phi'_{\mathrm{s},k} = \phi_{\mathrm{s},k} + \Delta$. It follows that (19) becomes:

$$\widetilde{v}_{\mathrm{s},k} \approx \sum_{l=1}^{N} G_k B_l \sin\left(\theta_{lk} + \Delta\right) \tag{26}$$

which alters the gradient descent in (15) into

$$\dot{\phi}_k = 2K \sum_{l=1}^{N} B_k B_l \sin\left(\theta_{lk} + \Delta\right), \quad \forall\, k \in \mathcal{N}. \tag{27}$$

Using (12)–(13) allows us to rewrite (27) as

$$\dot{\phi}_k = -K \frac{\partial}{\partial \phi_k} \left(U \cos\Delta + \frac{\partial U}{\partial \theta_k} \sin\Delta \right) = -K \frac{\partial U_k}{\partial \phi_k} \tag{28}$$

where U_k is the modified cost function for the kth unit. With the assumption $\cos\Delta \approx 1$ for small Δ, U_k takes the form

$$U_k = \left(\sum_{l=1}^{N} B_l \cos\left(\theta_l + \Delta_l\right) \right)^2 + \left(\sum_{l=1}^{N} B_l \sin\left(\theta_l + \Delta_l\right) \right)^2 \tag{29}$$

where $\Delta_l = \Delta$ only if $l = k$ and is zero otherwise. Comparing (29) with (7), we see that U_k for $k \in \mathcal{N}$ resembles the original cost function U, except that the voltage phasor corresponding to the kth converter has an additional phase shift of Δ (see Fig. 3). This phase translation does not alter the shape of the cost function. As a result, the gradient descent law converges to a solution $\phi_k^\star + \Delta$ for the kth unit where, $\phi_k^\star$ is the solution obtained in the ideal case. Since this happens for all $k \in \mathcal{N}$, the system eventually converges to the same local minimum for ripple. This is because if $\phi^\star = [\phi_1^\star, \ldots, \phi_N^\star]^\top$ is a local minimum, then so is $\phi^\star + \Delta$ as the relative angles between the units do not change. However, the discussion above holds only when $\cos\Delta \approx 1$. Fortunately, the value of $\cos\Delta$ stays within 3% of unity for values of Δ within $\pm 14^\circ$. This observation highlights the robustness of our controller to parametric uncertainties.

IV. Experimental Validation

A. Hardware Description

To experimentally validate the proposed controller, a hardware setup consisting five parallel-connected dc–dc converters was built. An annotated photograph of the experiment is in Fig. 8. In this setup, each converter unit has a front-end dc–dc dual active bridge (DAB) stage followed by an output-side buck converter. The outputs of all buck stages are in parallel across a common filter capacitor and resistive load as shown in Fig. 1(b). Each buck output has a filter inductor and voltage sensing circuitry that aligns with Fig. 6.

As shown in Fig. 9, the first stage of this analog signal chain contains a high-pass filter at the output of each converter to filter out the ripple component ($\widetilde{v}$) from the output voltage v. The high-pass filter is made of R_h and C_h in series and the output is

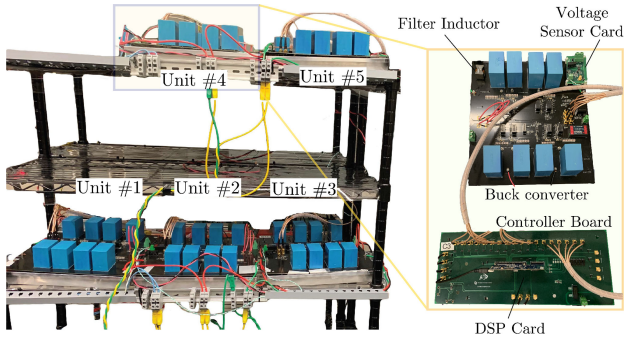

Fig. 8. Experimental setup of five parallel connected dc–dc converters.

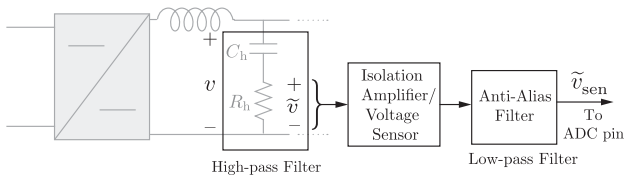

Fig. 9. Block diagram of the analog signal chain.

taken across R_h. The corner frequency of the filter, ω_hp, should be at least 10 times less than the switching frequency in order to filter the ripple part. Accordingly, $\omega_\mathrm{hp} = 1/(R_\mathrm{h} C_\mathrm{h}) \leq 0.1\omega_\mathrm{sw}$. In our case, as the switching frequency is 10 kHz, the corner frequency must be less than 1 kHz.

Moreover, we do not want to filter the load branch current. Hence, the current through the high-pass shunt branch should be negligibly small at all frequencies. This implies that the impedance of the filter is should be much higher than the impedance of the main output capacitor or $Z_\mathrm{hp} = R_\mathbf{h} + 1/sC_\mathrm{h} >> 1/sC_\mathrm{f}$. To ensure this is satisfied we choose a fairly large $R_\mathrm{h} = 100\ \mathrm{k}\,\Omega$. Then from the corner frequency constraint we choose $C_\mathrm{h} = 0.1\ \mu\ \mathrm{F}$ to get a corner frequency of 16 Hz. The output of the high-pass branch, $\widetilde{v}$, now contains only the switching frequency harmonics. This signal is now fed to the isolation amplifier or voltage sensor, which has a -3 dB cut-off frequency of 275 kHz. The voltage sensor is followed by a low-pass antialias filter. The corner frequency of this filter should be chosen so that it allows only the fundamental harmonic and attenuates higher order harmonics. In our case, this is kept at 20 kHz.

The proposed method was implemented in closed-loop around each buck stage such that the net current ripple fed to the output filter capacitor was minimized. Each buck was fed by a DAB to provide a controllable voltage, which can be modulated to emulate asymmetric input voltage sources. A single dc supply connects to the inputs of all five DABs. Each converter unit was controlled by a dedicated TMS320F28379D digital signal processor, which executes the proposed method. Current sharing among the parallel buck converters was achieved with conventional droop control [31], which provides the output voltage reference as well as the buck duty ratio. The droop controller functions independently from the proposed method and was mainly used to facilitate power sharing.

TABLE II
EXPERIMENTAL PARAMETERS

Parameter	Description	Value
V_{in}	DC supply/DAB input voltage	100 V
v_{in}	Nominal buck input voltage	50 V
f_{sw}	Switching frequency	10 kHz
C_{f}	Output capacitance	25 μF
R_{ℓ}	Load resistance	5 Ω
L_{f}	Buck filter inductance	230 μH
K_{P}	Controller gain	50 Hz/V
ψ	Filter phase lag at f_{sw}	44°
G	Filter gain at f_{sw}	0.9 V/V
	High-pass filter cut-off frequency	16 Hz
	Voltage Sensor bandwidth	275 kHz
	Low-pass filter bandwidth	20 kHz
Description	Part Number	Manufacturer
Voltage Sensor	ISO224BDWVR	Texas Instr.
Control Card	Delfino F28379D	Texas Instr.

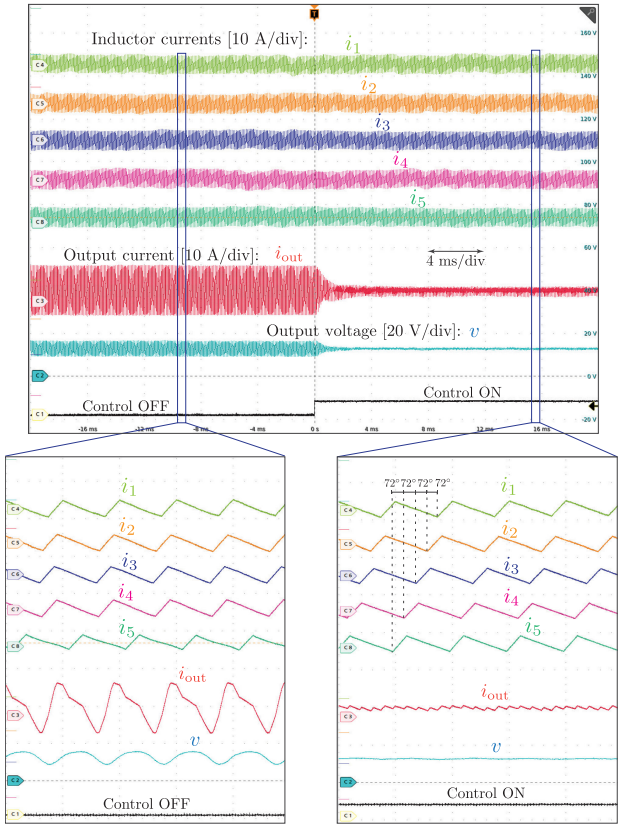

Fig. 10. Measured waveforms of phase currents, load current, and load voltage during operation with uniform power stage voltage inputs and average current delivery.

The experimental hardware and control parameters are in Table II.

B. Experimental Results

1) Uniform Hardware and Operating Conditions: Fig. 10 shows system performance when the converters operate with uniform input voltages and filter inductances while regulating 12 V across the load. In this case, minimum ripple is obtained with symmetric interleaving. Convergence to the symmetric interleaved state occurs in around 4 ms, where the inductor currents are phase shifted $360°/5 = 72°$ with respect to each other. The transient response of the system is depicted before and after the controller is turned ON. Evidently, the peak-to-peak ripple in i_{out} was reduced from 12 to 2 A giving a 6× reduction compared to the uncontrolled state. Worst case current ripple, which occurs with phase-synchronized PWM carriers, is larger than 12 A. Hence, the ripple reduction factor can be larger than what is described in this particular case.

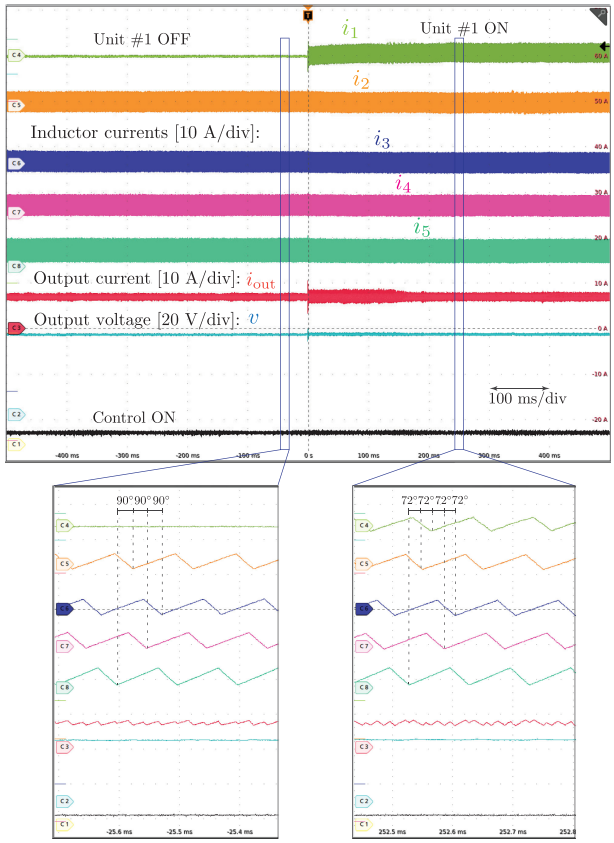

Fig. 11. Measured waveforms of phase currents, load current, and load voltage before and after addition of the 5th unit. The controller maintains the interleaved state irrespective of the number of units in the system.

2) Unit Addition: Next, we show results when an additional converter unit is added to the system. As seen in Fig. 11, the system initially had four converters with interleaved currents having $360°/4 = 90°$ phase shifts. Once the additional fifth unit is energized, the controller adjusts PWM phase shifts such that the inductor currents become $360°/5 = 72°$ out of phase. Convergence to the new interleaved state occurs in approximately 200 ms. This demonstrates plug-and-play capabilities of the proposed approach.

3) Nonuniform Input Voltages: Next, we apply nonuniform input voltages to the buck stages and compare the measured ripple with the proposed control against symmetric interleaving.

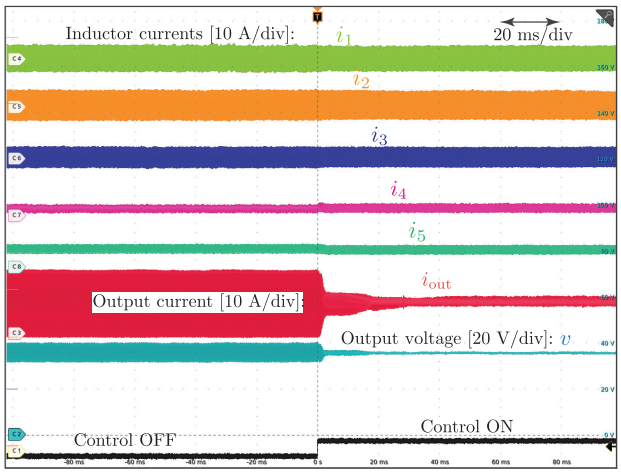

Fig. 12. Measurements with non-uniform input voltages. Convergence to the minimized ripple state from arbitrary initial conditions is obtained within 40 ms.

The inputs are randomly chosen as $v_{\text{in},1} = 56\,V$, $v_{\text{in},2} = 60\,V$, $v_{\text{in},3} = 50\,V$, $v_{\text{in},4} = 40\,V$, and $v_{\text{in},5} = 40\,V$ while the output voltage is regulated at $v = 36\,V$. Fig. 12 shows the transient response of the system when the controller is turned ON from an uncontrolled state of operation. Here, the closed-loop system converges to the minimum ripple operating point in 40 ms. Fig. 13(a) and (b) shows the steady-state waveforms of inductor currents i_1 through i_5, output current i_{out}, output voltage v, as well as the harmonic spectrum of i_{out}, under both the proposed control and conventional symmetric interleaving, respectively. The sum of the first 10 harmonics in i_{out} is reduced by $4.5\times$ as it falls from 5.4 to 1.2 A. Also note that the 1st harmonic component is attenuated from 4 to 0.1 A for a -32 dB reduction compared to symmetric interleaving.

4) Output Voltage Step Change: To validate control robustness under varying output voltages, we now adjust the output voltage reference from 36 V$\rightarrow$ 30 V$\rightarrow$ 24 V. As seen in Fig. 15, the droop controller tracks the output voltage reference and maintains current sharing while the decentralized phase-shift controller simultaneously tracks the ripple minima and maintains the minimum ripple operation in each operating point.

5) Load Step Change: The performance of the controller during load transitions in experimentally verified in Fig. 14. Fig. 14(a) shows the response of the system currents and voltages when the load is stepped up by 300% from 2.5 to 7.5 A while maintaining the output voltage at 36 V. Fig. 14(b) shows a zoomed view of the load transient, where it can be seen that the system continues to operate with the optimal current ripple even during the transient. This is because the minima of the RMS of fundamental ripple component, B_r, does not depend on the average value of the load current. This can be inferred from (2) and (8). Hence, the optimal phase shifts $\phi^\star$ do not change during load transients provided the output voltage is well regulated. In this case, the controller remains unaffected by the system dynamics and continues to operate the system at the ripple minima.

6) Nonuniform Filter Inductances: Finally, we consider a system with nonuniform filter inductances at the converter outputs. Nonuniform inductances naturally occur due to manufacturing tolerances and are commonplace in systems having converters with nonuniform ratings. We selected buck filter inductances as $L_{\text{f},1} = 460\,\mu$H, $L_{\text{f},2} = 230\,\mu$H, $L_{\text{f},3} = 115\,\mu$H, $L_{\text{f},4} = 345\,\mu$H, and $L_{\text{f},5} = 230\,\mu$H while the output voltage was regulated at 36 V. The transient response of the system after the controller is turned ON is illustrated in Fig. 17. The output current and voltage converge to the minimized ripple state within approximately 10 ms. Fig. 16(a) and (b) compares the steady-state waveforms and harmonic spectrum of i_{out} for the proposed control and symmetric interleaving, respectively. Superior performance of the proposed controller is evident despite the challenges brought on by asymmetries. Note that harmonics in i_{out} went from 4.2 to 2.1 A for a $2\times$ reduction. Compared to symmetric interleaving, the proposed controller reduced the fundamental harmonic amplitude from 2.5 to 0.3 A for a -18 dB reduction.

Note that in this implementation, the required sampling frequency of the sensed and filtered output voltage is equal to the switching frequency of the dc–dc converter. Even though the experimental results are presented at a relatively low switching frequency, the controller can be used at much higher switching frequencies in the range of 100 kHz to 1 MHz. The main advantage of this controller over the controller proposed in previous works is that it does not require oversampling of the output voltage. Only one sample at a specific point in the switching cycle is required for the controller to take action. For very high switching frequencies, samples may even be taken at integer multiples of switch cycle (i.e., the controller is executed at integer fractions of the switching frequency). The main challenge for applications with switching frequencies above 500 kHz is voltage sensor bandwidth. In these settings, differential amplifiers with sufficiently high bandwidth can be used.

V. Conclusion

In this article, we address and solve two key challenges of ripple minimization in systems of parallel dc–dc converters. Existing ripple minimization techniques largely depended on centralized control frameworks that requires global information when computing the PWM phase shifts for ripple reduction. These methods compromise system scalability and reliability. Recent advances in decentralized mainly deal with uniform hardware and operating conditions, which does not apply to practical systems with tolerances and nonuniformity.

In this work, we solve the aforementioned issues by proposing a fully decentralized controller that works for both uniform and nonuniform parallel-connected dc–dc systems. The proposed controller uses a gradient-descent algorithm to minimize the fundamental switching harmonic in the current and voltage ripple, which generally dominates and dictates output filter design. This algorithm is implemented at each converter by sampling the local terminal voltage each switch cycle and perturbing the switching frequency to give PWM phase shift adjustment. Compared to prior methods, this approach provides a greatly

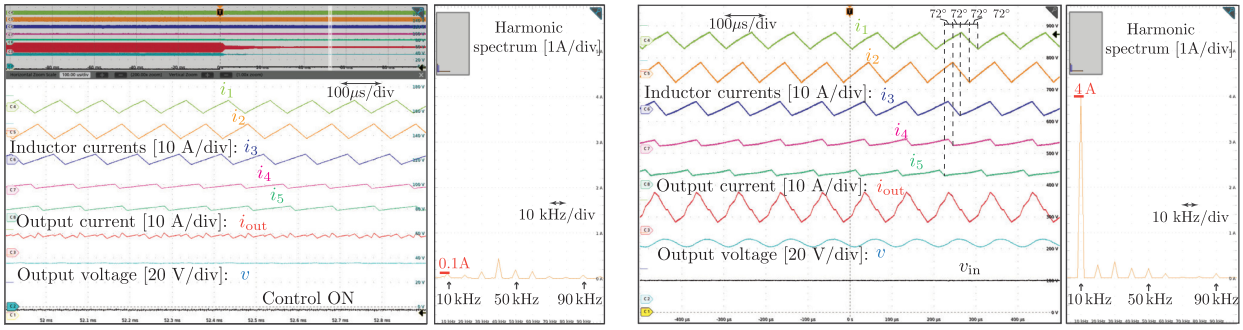

Fig. 13. Comparison of ripple reduction achieved with proposed controller versus symmetric interleaving for nonuniform input voltages. A 4.5× net reduction in the output current ripple is obtained in (a) compared to symmetric interleaving in (b), while the fundamental harmonic is reduced by 32 dB. (a) Proposed Decentralized Control. (b) Symmetric Interleaving.

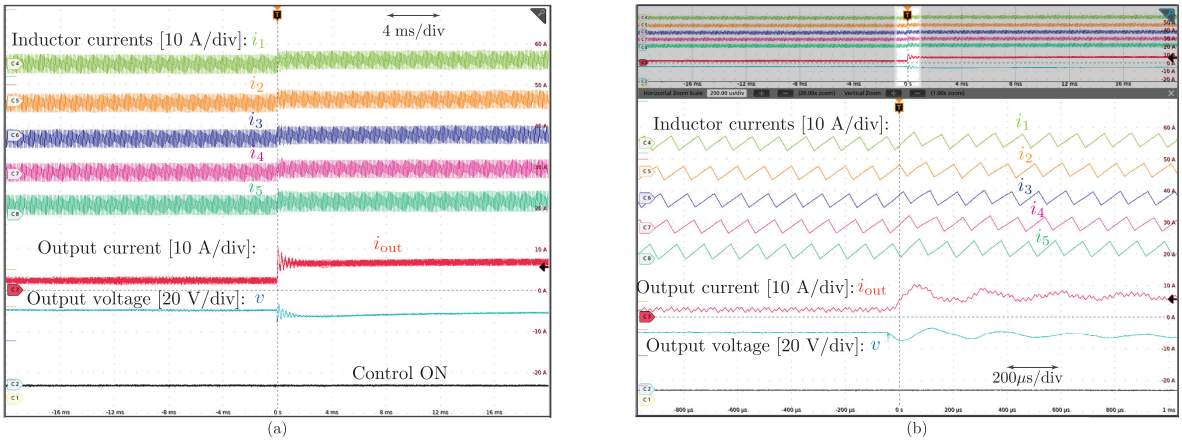

Fig. 14. Experimental results showing the performance of the controller when the load is stepped up by 300% from 2.5 A to 7.5 A in (a). Zoomed view of the load transient in (b) shows that the controller maintains the optimal ripple state even during the transient. (a) Load step change. (b) Zoomed view of load transient.

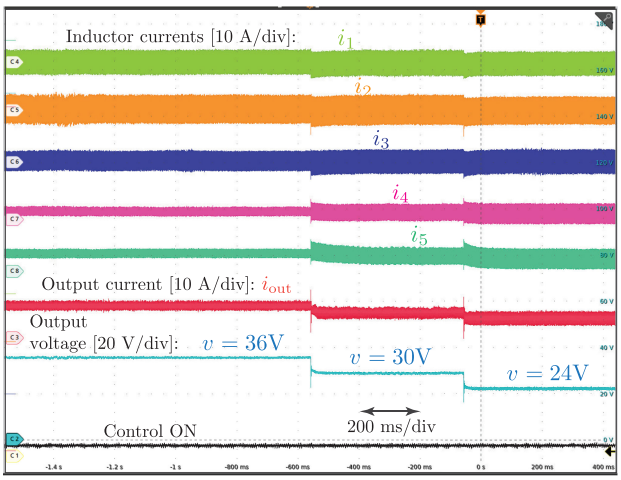

Fig. 15. Waveforms with nonuniform input voltages while output voltage reference changed from 36 V→ 30 V→ 24 V. Controller maintains the minimized ripple state despite output changes.

simplified digital implementation as it does not require complex optimization algorithms, look-up tables, high-fidelity sensing, or measurement oversampling. Finally, performance gains offered by the proposed controller were experimentally validated on a parallel-connected setup of five dc–dc converters.

APPENDIX

A. *Convergence Analysis and Selection of Parameter* $K_{\mathrm{p},k}$

To demonstrate convergence of the gradient descent algorithm with the objective function

$$U(\theta) = B_r^2 = \sum_{k=1}^{N}\sum_{l=1}^{N} B_k B_l \cos(\theta_k - \theta_l) \tag{30}$$

we use the regularity conditions for convergence as prescribed in [32]. This article deals with the gradient descent of nonconvex functions and requires the function to satisfy two conditions which are: (a) it has to be twice differentiable, and (b) the gradient of the function, ∇U, has to be Lipschitz continuous. The latter is the main regularity condition which means that for any θ_1, θ_2 there exists a finite constant $L > 0$ such that

$$\frac{\|\nabla U(\theta_1) - \nabla U(\theta_2)\|_2}{\|\theta_1 - \theta_2\|_2} \leq L \tag{31}$$

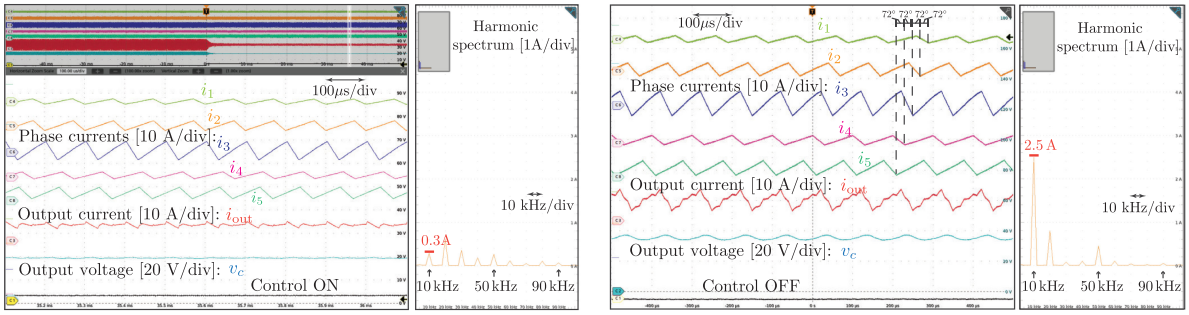

Fig. 16. Performance comparison of proposed method with symmetric interleaving for asymmetric filter inductances. A 2× net reduction in output current ripple is obtained in (a) compared to symmetric interleaving in (b). The fundamental switching harmonic is attenuated by −18 dB. (a) Proposed Decentralized Control. (b) Symmetric Interleaving.

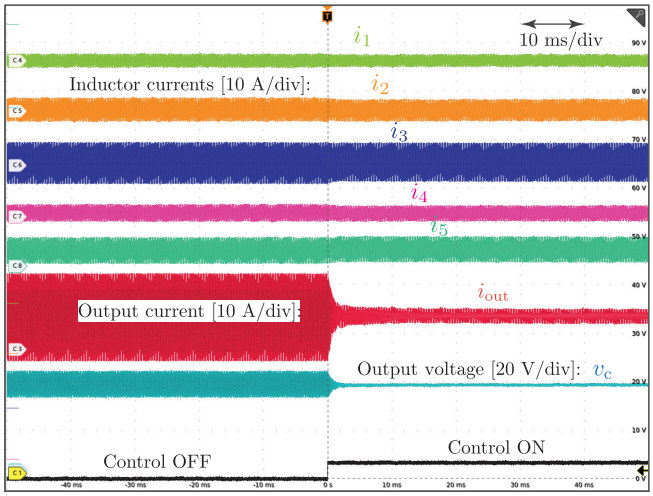

Fig. 17. Measurements with asymmetric filter inductances. Convergence to the minimized ripple state occurs within 10 ms.

where $\|\cdot\|_2$ is the $\mathcal{L}^2$ norm of a vector. If we then apply gradient descent with fixed step size $\tau \leq 1/L$, after κ iterations it will yield a solution $U(\theta[\kappa])$, which satisfies

$$U(\theta[\kappa]) - U(\theta^\star) \leq \frac{\|\theta[0] - \theta^\star\|_2^2}{2\tau\kappa} \tag{32}$$

where $\theta^\star$ is the optimal solution and $\theta[0]$ is the initial value of θ. This shows that the algorithm is guaranteed to converge and it converges with rate $O(1/k)$.

Since, the objective function $U(\theta)$ considered here is a sum of cosines of angle differences, it is indeed twice differentiable and satisfies condition (a). The Lipschitz continuity of the gradient in (31) physically means that the gradient can not change too rapidly anywhere in the domain. (31) implies that the Hessian of $U(\theta)$ should satisfy

$$\nabla^2 U(\theta) \preceq LI \tag{33}$$

or $\nabla^2 U(\theta) - LI$ is a negative semidefinite matrix, where I is a $N \times N$ identity matrix. Eq. (33) further implies that the eigenvalues of the Hessian are bounded above by L. Therefore, to fulfill the Lipschitz continuity condition in (b), we need to show that there exists a positive upper bound L on the eigenvalues of $\nabla^2 U$. Using (10), the Hessian of U is

$$\nabla^2 U = 2\begin{bmatrix} -\sum_{l=1}^{N} b_{1\,l} & b_{12} & \cdots & b_{1\,N} \\ b_{12} & -\sum_{l=1}^{N} b_{2\,l} & \cdots & b_{2\,N} \\ \vdots & \vdots & \ddots & \vdots \\ b_{1\,N} & b_{2\,N} & \cdots & -\sum_{l=1}^{N} b_{Nl} \end{bmatrix} \tag{34}$$

where $b_{ij} = B_i B_j \cos\theta_{ij}$, $\forall\, i, j \in \mathcal{N}$. The above matrix is a symmetric and diagonally dominant matrix where the absolute value of the diagonal entries are larger than the sum of the magnitudes of all other (nondiagonal) entries in each row. Applying Gershgorin circle theorem [33], the bound on any eigenvalue of the matrix is

$$\lambda - |\sum_{l=1}^{N} B_i B_l \cos\theta_{il}| \leq \sum_{\substack{j=1 \\ j\neq i}}^{N} |B_i B_j \cos\theta_{ij}| \tag{35}$$

The tightest gap occurs when $\theta_{ij} = 0$ or π for any $i, j \in \{1, \ldots, N\}$. In this case, it follows that:

$$\lambda \leq |\sum_{l=1}^{N} B_i B_l| + \sum_{\substack{j=1 \\ j\neq i}}^{N} |B_i B_j|, \qquad \text{for any } i \in \mathcal{N} \tag{36}$$

If $B_{\max} = \max\{B_i\}$ for $i \in \mathcal{N}$, then (36) gives $\lambda \leq (2N-1)B_{\max}^2$. It follows that the upper bound on the eigenvalues of $\nabla^2 U$ for any case is given as $L = (2N-1)B_{\max}^2$. Therefore, from condition (b) the gradient step size must satisfy $\tau \leq 1/L$ or $\tau \leq 1/((2N-1)B_{\max}^2)$. For convenience, we repeat our form of the gradient descent algorithm here

$$\phi_k[n+1] = \phi_k[n] - T_{\text{sw}} K \frac{\partial U(\phi)}{\partial \phi_k} \tag{37}$$

where the step size in each iteration is $\tau = KT_{\text{sw}}$. To guarantee convergence, $K \leq \frac{f_{\text{sw}}}{(2N-1)B_{\max}^2}$. Since $K_{\text{p},k} = (2KB_k)/G$, it follows that $K_{\text{p},k}$ should be chosen within the following range

to ensure convergence:

$$0 < K_{\mathrm{p},k} < \frac{2B_k f_{\mathrm{sw}}}{(2N-1)B_{\max}^2\, G}. \tag{38}$$

ACKNOWLEDGMENT

The authors would like to thank Branko Majmunovic and Satyaki Mukherjee from the University of Colorado, Boulder for their help in designing the hardware used for the experiments shown in this article.

REFERENCES

[1] S. Dutta, M. Lu, and B. Johnson, "Decentralized PWM interleaving for ripple minimization in both symmetric and asymmetric parallel-connected DC-DC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 2894–2901.
[2] E. A. Burton et al., "Five–fully integrated voltage regulators on 4th generation intel core SoCs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 432–439.
[3] H. Kakigano, Y. Miura, and T. Ise, "Low-voltage bipolar-type DC microgrid for super high quality distribution," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3066–3075, Dec. 2010.
[4] M. Su et al., "Stability analysis and stabilization methods of DC microgrid with multiple parallel-connected dc-dc converters loaded by CPLs," *IEEE Trans. Smart Grid*, vol. 9, no. 1, pp. 132–142, Jan. 2018.
[5] G. Buticchi, L. Costa, and M. Liserre, "Improving system efficiency for the more electric aircraft: A look at DC-DC converters for the avionic onboard AC microgrid," *IEEE Ind. Electron. Mag.*, vol. 11, no. 3, pp. 26–36, Sep. 2017.
[6] H. Tu et al., "Extreme fast charging of electric vehicles: A technology overview," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 4, pp. 861–878, Dec. 2019.
[7] D. Sha, G. Xu, and Y. Xu, "Utility direct interfaced charger/discharger employing unified voltage balance control for cascaded H-bridge units and decentralized control for CF-DAB modules," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7831–7841, Oct. 2017.
[8] D. J. Perreault and J. G. Kassakian, "Distributed interleaving of paralleled power converters," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 44, no. 8, pp. 728–734, Aug. 1997.
[9] J. Holtz and B. Beyer, "The trajectory tracking approach: A new method for minimum distortion PWM in dynamic high-power drives," *IEEE Trans. Ind. Appl.*, vol. 30, no. 4, pp. 1048–1057, Jul./Aug. 1994.
[10] T. Beechner and J. Sun, "Asymmetric interleaving: A new approach to operating parallel converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 99–105.
[11] M. Caris, H. Huisman, and J. Duarte, "Harmonic elimination by adaptive phase-shift optimization in interleaved converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 763–768.
[12] J. Poon et al., "Minimum distortion point tracking: Optimal phase shifting for input-or output-parallel connected DC-DC converters," in *Proc. IEEE Workshop Control Model. Power Electron.*, 2018, pp. 1–6.
[13] J. Poon et al., "Minimum distortion point tracking," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11013–11025, Oct. 2020.
[14] S. Waffler, J. Biela, and J. W. Kolar, "Output ripple reduction of an automotive multi-phase bi-directional DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 2184–2190.
[15] M. Schuck and R. C. Pilawa-Podgurski, "Ripple minimization through harmonic elimination in asymmetric interleaved multiphase DC-DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7202–7214, Dec. 2015.
[16] M. Schuck, A. D. Ho, and R. C. Pilawa-Podgurski, "Asymmetric interleaving in low-voltage CMOS power management with multiple supply rails," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 715–722, Jan. 2017.
[17] O. Garcia et al., "Effect of the tolerances in multi-phase DC-DC converters," in *Proc. IEEE 36th Power Electron. Specialists Conf.*, 2005, pp. 1452–1457.
[18] C. Parisi, "Multiphase buck design from start to finish (Part 1)," Texas Instruments, Application Report SLVA882, 2017.
[19] H. Liu, D. Zhang, and D. Wang, "Design considerations for output capacitance under inductance mismatches in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5004–5015, Jul. 2017.
[20] M. Sinha et al., "Decentralized interleaving of parallel-connected buck converters," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4993–5006, May 2019.
[21] J. Poon et al., "Decentralized carrier phase shifting for optimal harmonic minimization in asymmetric parallel-connected inverters," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5915–5925, May 2021.
[22] M. Cousineau et al., "Triangular carrier self-alignment using modular approach for interleaved converter control," in *Proc. IEEE Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
[23] S. Dutta et al., "Decentralized carrier interleaving in cascaded multilevel DC-AC converters," in *Proc. IEEE 20th Workshop Control Model. Power Electron.*, 2019, pp. 1–6.
[24] D. F. Frost and D. A. Howey, "Completely decentralized active balancing battery management system," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 729–738, Jan. 2018.
[25] S. Dutta et al., "A novel decentralized PWM interleaving technique for ripple minimization in series-stacked DC-DC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 487–493.
[26] T. Xu and F. Gao, "Global synchronous pulse width modulation of distributed inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6237–6253, Sep. 2016.
[27] D. A. Paley, N. E. Leonard, and R. Sepulchre, "Oscillator models and collective motion: Splay state stabilization of self-propelled particles," in *Proc. IEEE Conf. Decis. Control*, 2005, pp. 3935–3940.
[28] R. Sepulchre, D. A. Paley, and N. E. Leonard, "Stabilization of planar collective motion: All-to-all communication," *IEEE Trans. Autom. Control*, vol. 52, no. 5, pp. 811–824, May 2007.
[29] Y. Kuramoto, "Self-entrainment of a population of coupled non-linear oscillators," in *Proc. Int. Symp. Math. Problems Theor. Phys.*, 1975, pp. 420–422.
[30] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017.
[31] J. M. Guerrero et al., "Hierarchical control of droop-controlled AC and DC microgrids: A general approach toward standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, Jan. 2011.
[32] J. D. Lee et al., "Gradient descent only converges to minimizers," in *Proc. Conf. Learn. theory*, 2016, pp. 1246–1257.
[33] E. W. Weisstein, "Gershgorin circle theorem," 2003. [Online]. Available: https://mathworld.wolfram.com/

Soham Dutta (Student Member, IEEE) received the B.E. degree in electrical engineering from Jadavpur University, Kolkata, India, in 2015, and the M.E. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2017. He is currently working toward the Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, USA.

His current research interests include design, modeling and control of isolated, bi-directional cascaded dc–ac converters for medium voltage-level ultra-fast electric vehicle chargers, decentralized control of multiconverter systems, and grid-forming converters.

Brian Johnson (Member, IEEE) obtained the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, USA, in 2010 and 2013, respectively.

He is the Washington Research Foundation Innovation Assistant Professor within the Department of Electrical and Computer Engineering, University of Washington. Prior to joining the University of Washington in 2018, he was an Engineer with the National Renewable Energy Laboratory in Golden, CO, USA. His research interests are in renewable energy systems, power electronics, and control systems.

Prof. Johnson currently serves as an Associate Editor for the IEEE TRANSACTIONS ON ENERGY CONVERSION.