A Highly Adaptive and Flipping-Time Optimized Piezoelectric Energy Harvesting Interface IC With Synchronized Triple Bias-Flip

Yanhang Chen, *Student Member, IEEE*, Chuhui Wang, and Jianping Guo, *Senior Member, IEEE*

***Abstract*—This article presents a piezoelectric energy harvesting interface circuit with high adaptability to external inductors, transducer types, and vibration frequencies. High output power can be obtained with the help of triple bias-flip and optimal flipping time control. The triple bias-flip enables both higher efficiency and the use of an inductor with lower volume compared to conventional bias-flip topologies. Besides, owing to the highly adaptive circuit design and reverse current reduction in the *LC* resonant loop, the proposed interface circuit not only automatically adjusts flipping time according to external inductance and piezoelectric transducer, but also reduces the reverse current of the inductor effectively. Also, an active rectifier that can reduce conduction loss of the diode-based rectifier has been implemented. The prototype integrated circuit has been fabricated in 180-nm CMOS technology and the chip area is 0.646 mm^2. The measurement results show that the proposed circuit achieves cold start-up without any external power supply, and can work with high efficiency when the external inductor is varying from 0 to 10 mH, transducer capacitance is changing from 20 to 90 nF, and vibration frequency is ranging from 35 to 200 Hz. The measured maximum output power of the proposed design can achieve as high as 473% enhancement to the full-bridge rectifier.**

***Index Terms*—Adaptive control, bias-flip, CMOS, cold start-up, interface circuit, piezoelectric energy harvesting.**

I. Introduction

THE energy harvesting circuits used in wireless sensor nodes (WSN), which enable prompt monitoring of many unreachable locations, can effectively prolong the battery life and avoid bulky power equipment, or even achieve fully autonomous operation without any external power supply [1]. The energy harvesting technology can obtain power supply from ambience such as solar, thermal, or vibrational energy. Among different energy sources, the vibrational energy harvested by piezoelectric sensors benefits from high output voltage [2], high energy density [3], and universal distribution [4]. As a result, the piezoelectric energy harvesting technique becomes a popular choice for many WSN systems [1]–[4]. In a typical piezoelectric energy harvesting system, a rectifier is usually required to convert the energy to the dc output since the excitations of the mechanical systems are generally not dc. The full-bridge rectifier (FBR) is the simplest and most widely-used circuit to perform ac–dc conversion [5]. Unfortunately, FBR suffers from large energy loss when charging the internal capacitor C_P of the piezoelectric transducer. The use of inductive bias-flip technology, or parallel synchronized switch harvesting on inductor (P-SSHI) technique [6]–[10], which uses an off-chip inductor to transfer the residual charge in the internal capacitor of a piezoelectric sensor, significantly reduces the energy loss to charge C_P to increase the harvesting efficiency. The bias-flip with capacitors can also complete the same charge-transferring process, namely synchronized switch harvesting on capacitor (SSHC) [5] or flipping-capacitor rectifier [11]. Capacitive bias-flip circuits generally need more flipping steps with complicated control to achieve comparable performance with P-SSHI circuits due to charge redistribution loss when charge-sharing. Synchronous electric charge extraction (SECE) is also a promising technique with load-independent characteristics [12], [13], but the extracted power from SECE is suffering from the maximum output power limit and usually less than using the SSHI technique. The input voltage under strong excitation is usually higher than the upper limits of the maximum voltage allowed by modern CMOS technology [14].

Nonetheless, there are still many problems when implementing the P-SSHI circuits. First of all, the flipping process, which is based on the *LC* resonance loop, needs to be finished precisely at half of the flipping period, or it will result in harmful timing errors. Off-chip calibration, such as digital control [6] or variable resistor [7], can partly address the timing errors. To achieve optimal timing control instead of external trimming, some on-chip flipping control methods for bias-flip rectifiers have been proposed. For example, the active on-chip *RC* time constant control is proposed to avoid timing error in [3], the flipping time is controlled with the help of the active diodes in the *LC* resonant loop in [8], and flipping detectors are adapted to monitor the flipping status to end flipping on time in [15]. However, the

Manuscript received 22 March 2022; revised 1 June 2022; accepted 8 July 2022. Date of publication 13 July 2022; date of current version 6 September 2022. This work was supported by the National Natural Science Foundation of China under Grant 61874143. Recommended for publication by Associate Editor H. Hofmann. *(Corresponding author: Jianping Guo.)*

Yanhang Chen was with the School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou 510006, China, and is currently with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China (e-mail: ychenj n@connect.ust.hk).

Chuhui Wang and Jianping Guo are with the School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou 510006, China (e-mail: wangchh36@mail2.sysu.edu.cn; guojp3@mail.sysu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3190433.

Digital Object Identifier 10.1109/TPEL.2022.3190433

method used in [3] fails to entirely cancel the reverse current introduced by the inductor, and this current may still be as high as 5 mA (according to [3], Fig. 14). Besides, the active diodes in [8] must have sufficient static current as well as sufficient bandwidth to monitor the voltage flipping, which may cause high power dissipation. The parasitic resistance of additional diodes in the *LC* resonant loop should also be paid attention to. Additionally, the external capacitor in [15] is required to be equal to C_P, which is difficult to realize in real applications. More importantly, most of the existing piezoelectric energy harvesting interface circuits cannot well realize adaptive control. In [8], two comparators and switches are adapted as active diodes to achieve an optimal flipping time so that off-chip tuning is not required. However, only one LC_P setup is tested, whereas the flipping time is greatly varied under different external inductances and transducer capacitances. Meanwhile, as the active diode in [8] is a closed-loop system, the loop stability should be carefully considered since external LC_P varies. All measurement results provided in [3], [8], and [15] are under a fixed or narrow range of external inductance and C_P, and the circuit performance when applying different external inductances and C_P are not experimentally verified, which would limit the real application of these circuits when external inductance changes or different transducers are used.

Another problem associated with P-SSHI circuits is the parasitic resistance in the *LC* resonant loop, which causes energy loss. This can be addressed by using a large inductor (e.g., $L = 3.4$ mH in [7]) at the cost of larger system volume, or by adopting a multistep bias-flip (e.g., triple bias-flip [16], [17] or 5-step bias-flip [3]) that can reduce the peak flipping current value, to reduce energy loss at the cost of longer flipping time and more complicated control circuits. The parasitic resistance of additional diodes in the *LC* resonant loop should also be paid attention to. Other issues, such as cold start-up and fully integrated control circuits, also increase the design complexity. Additionally, the large volume of inductors also becomes an important drawback in some size-limited applications [9], [11], where capacitive bias-flip circuit becomes more attractive.

Based on the above discussions, this article proposed a synchronized triple bias-flip (S3BF) rectifier for piezoelectric energy harvesting with self-powered (i.e., all the circuit modules are powered by the energy obtained from the ambience) and cold start-up (i.e., the circuit can start-up from zero-state without external power supply) features. The triple bias-flip technique significantly reduces the effect of parasitic resistance and hence improves the harvesting efficiency. In [16], the prototype S3BF rectifier is verified with the micro control unit with a constant voltage supply and a velocity sensor for synchronized switch control. In the proposed design, all control circuits, voltage generation, and detection are on-chip even though supply voltage has a large variation. Moreover, in the previously reported flipping-time optimized interface circuits [3], [8], [12], [15], only one or a few external setups are verified. To better accomplish different L, C_P, and f_P setups in practical applications, the proposed interface circuit guarantees high-efficiency energy extraction from piezoelectric sensors even though different transducers and external inductors are utilized. To overcome the problem of large size introduced by inductive elements, the proposed interface circuit can be configured automatically to the capacitive bias-flip circuit if there is no external inductor. Meanwhile, the flipping time, as well as the reverse current of external inductors, is optimally controlled by the proposed adaptive flipping time and switch control.

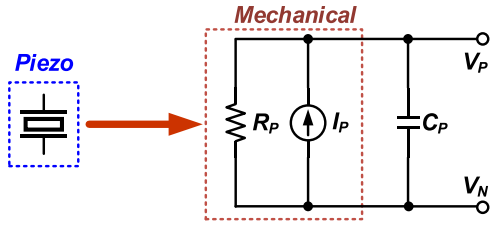

Fig. 1. Equivalent model of piezoelectric transducer.

The rest of this article is organized as follows. Section II introduces the theoretical analysis of the existing bias-flip rectifier and the proposed S3BF rectifier. Section III describes the circuit implementation of the proposed interface circuits. Section IV provides measurement results of the prototype circuit fabricated in 180-nm CMOS technology and makes a comparison with state-of-the-art research. Finally, Section V concludes this article.

II. Analysis of Existing Bias-Flip Rectifiers and Proposed Adaptive S3BF Rectifier

A. Electrical Model of Piezoelectric Transducer

Before the discussion of the detailed operation of interface circuits, it is of great benefit to introduce the equivalent electrical model of piezoelectric transducer instead of its complicated mechanical representation for simplicity.

Fig. 1 shows that the piezoelectric transducer can be modeled as a current source I_P shunted with a resistor R_P, which represents the resistance of the transducer, and a capacitor C_P, which stands for the transducer's internal capacitance as mentioned earlier [4]. Assuming the current source is sinusoidal with a frequency of f_P and an amplitude of I_{Peak}, I_P can be modeled as

$$I_P = I_{\text{Peak}} \sin(2\pi f_P t). \tag{1}$$

The peak open-circuit voltage V_{OC} of the piezoelectric transducer (neglecting the R_P) can be given by [8]

$$V_{\text{OC}} = \frac{I_{\text{Peak}}}{2\pi f_P C_P}. \tag{2}$$

B. Analysis of Bias-Flip Circuits With Voltage Rebuilt Factor

Fig. 2 illustrates the circuit diagram of a typical bias-flip rectifier and its operating waveform [11], where R_P, I_P, and C_P stand for the piezoelectric transducer discussed earlier and C_S and R_L are storage capacitor and loading resistance, respectively. V_S is the voltage across C_S and $\pm V_r$ is the voltage across C_P when the bias-flip operation is just finished. As shown in Fig. 2(b) where I_P is modeled as a sinusoidal current source,

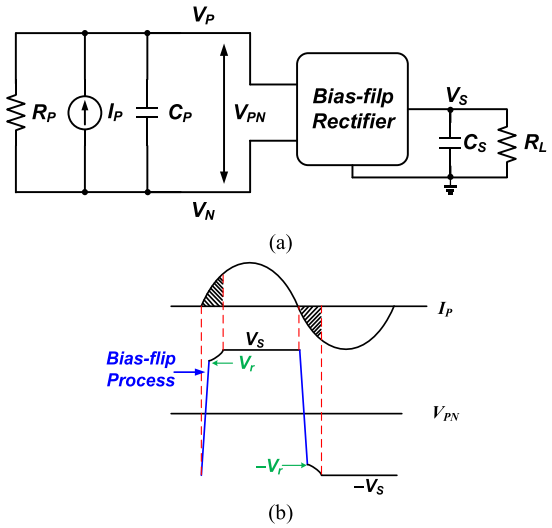

Fig. 2. Typical bias-flip rectifier: (a) block diagram and (b) operating waveform.

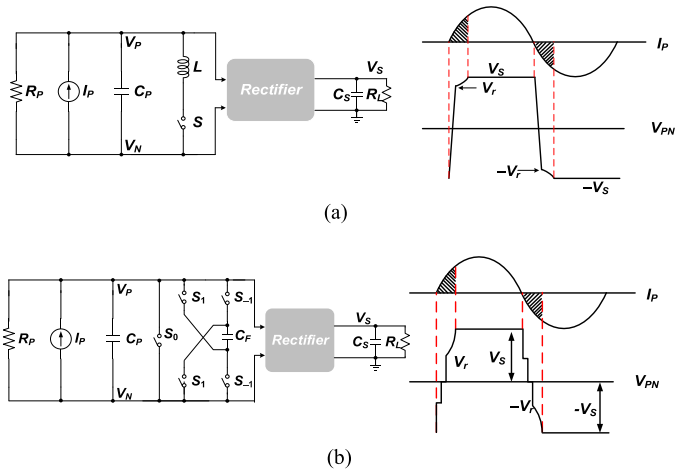

Fig. 3. Circuit diagrams and operating waveforms of (a) P-SSHI and (b) SSHC rectifiers.

the bias-flip process (shown as blue line) takes place when the I_P crosses the zero-current point to flip the voltage across C_P. In this way, the charge loss due to charging C_P is significantly reduced. These wasted charges in each period are given by

$$Q_{\text{loss,bias-flip}} = 2C_P\ (V_S - V_r)\,. \tag{3}$$

The charge loss of FBR with ideal diode assumption in each sinusoidal period can be modeled as [18]

$$Q_{\text{loss,FBR}} = 2C_P V_S. \tag{4}$$

It is obvious that the charge loss of the bias-flip circuit is much less than that of FBR. Also, according to (3), to achieve low charge loss, V_r should be fairly close to V_S. This can also be represented by the voltage rebuilt factor k [11], which is given by (assuming the falling edge and rising edge of V_{PN} are equal)

$$k = \frac{V_r}{V_S}. \tag{5}$$

Hence, the output power of a bias-flip rectifier (without conduction loss) can be given by [11]

$$P_{\text{OUT}} = 2C_P V_S f_P\,[2V_{\text{OC}} - (1-k)\,V_S] \tag{6}$$

and its maximum output power can also be given by [4]

$$P_{\text{OUT,max}} = \frac{2C_P V_{\text{OC}}^2 f_P}{1-k}. \tag{7}$$

Equation (7) shows that k ought to be as close as 1 to achieve a higher maximum output power. In other words, the bias-flip circuit with higher V_r will have higher harvesting efficiency.

C. Output Power Analysis of P-SSHI and SSHC Rectifiers

Fig. 3 illustrates the circuit diagrams and operating waveforms of P-SSHI [9]–[13] and SSHC circuits [5], [11]. The P-SSHI circuit forms an LC resonant loop to flip the voltage across C_P during the zero-crossing of I_P, and the ideal flipping lasts for half of the resonant period. It can be obtained that [8]

$$V_r = |-V_r| = V_S\ \exp\left(-\frac{\pi}{\sqrt{\frac{4L}{C_P R^2} - 1}}\right) \tag{8}$$

where L and R are external inductance and parasitic resistance in the resonant loop, respectively. Hence, the voltage rebuilt factor of P-SSHI circuits can be given by

$$k_{\text{SSHI}} = \exp\left(-\frac{\pi}{\sqrt{\frac{4L}{C_P R^2} - 1}}\right). \tag{9}$$

Ideally, the parasitic resistance R is 0, so k_{SSHI} is 1. In other words, the theoretical bias-flip process of P-SSHI is lossless. In practical cases, k_{SSHI} can be enlarged by reducing the parasitic resistance (mostly enlarging the aspect ratios of power switches) or using larger off-chip inductance.

As for the SSHC circuit, however, the bias-flip process is relatively complicated. The residual charge of C_P will be first transferred to an extra capacitor C_F (can be on-chip [11] or off-chip [5]), then C_P will be shorted. Finally, the charge in C_F will be transferred back to C_P. The voltage rebuilt factor of SSHC circuits can be given by [11]

$$k_{\text{SSHC}} = \frac{1}{2 + \frac{C_P}{C_F}} < \lim_{C_F \to \infty} \frac{1}{2 + \frac{C_P}{C_F}} = \frac{1}{2}. \tag{10}$$

It is obvious that the theoretical maximum voltage rebuilt factor of SSHC circuits is less than 0.5, which limits this circuit to achieve comparable output power with P-SSHI. Nonetheless, the capacitive bias-flip technology benefits from a lower volume than the inductive one, and the relatively low efficiency can be improved by multistep capacitive bias-flip, e.g., 7-step [11], 17-step [5], or even 21-step [19] capacitive bias-flip.

In conclusion, both the P-SSHI and SSHC bias-flip rectifiers discussed earlier have some drawbacks. P-SSHI circuits are generally more efficient than SSHC circuits, but they require accurate timing control and careful design for switches. The large volume of inductors also limits its application. The SSHC topology benefits from the compact capacitive components with severe energy loss. The proposed S3BF rectifier, on the other

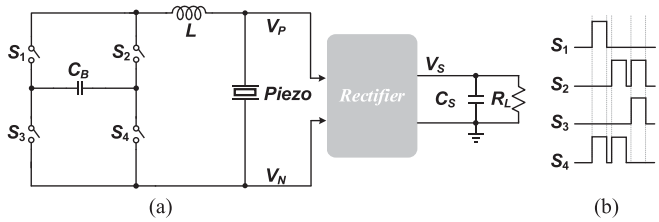

Fig. 4. (a) Conceptual circuit diagram of proposed S3BF rectifier. (b) Control waveform of switches S_{1-4} for falling edge.

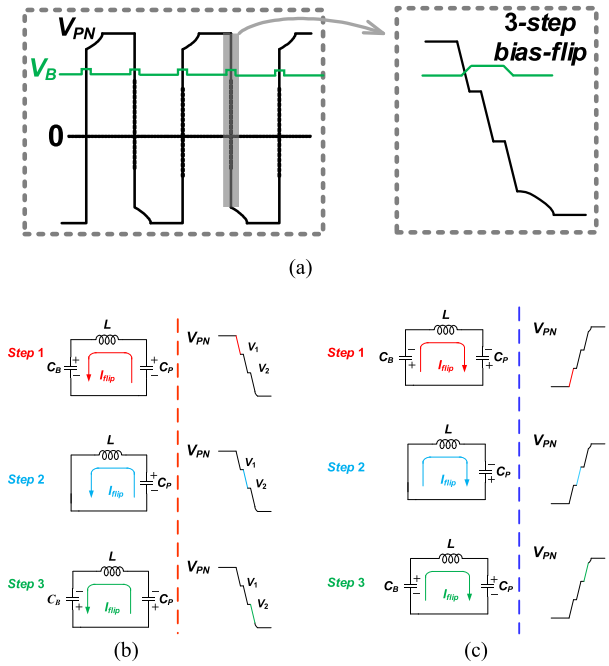

Fig. 5. Operating waveforms of $V_{\rm PN}$ in S3BF circuit. (a) Steady-state waveform. (b) Equivalent circuit model and waveform for falling edge. (c) Equivalent circuit model and waveform for rising edge.

hand, can reduce the effect of parasitic resistance to increase the voltage rebuilt factor and automatically configure to SSHC topology without the presence of an inductor when the system's size becomes limited.

D. Output Power Analysis of Proposed S3BF Rectifier

The operation principle of S3BF has been derived precisely in previous work [16], [17]. To analyze the performance and output power using the voltage rebuilt factor k as SSHI and SSHC, the derivations have been modified from [16]. As shown in Fig. 4(a), the proposed S3BF circuit utilizes an external inductor L and an external capacitor C_B to perform a triple-step bias-flip while all of the control circuits are integrated. Taking the falling step (i.e., V_P is positive and V_N is negative), for example, in Fig. 4(b), switches S_1 and S_4 are closed for the first-step operation. Switches S_2 and S_4 are closed for the second-step operation. The last step operates when S_2 and S_3 are close. The equivalent circuit configuration and relevant conceptual waveforms at different steps are illustrated in Fig. 5. Fig. 5(a) shows the steady-state waveform of $V_{\rm PN}$ across the piezoelectric transducer (PEH) and V_B across C_B. V_B first increases and then decreases in every triple bias-flip, which always maintains dynamic balance. The circuit implementations of each step for falling and rising edges are shown in Fig. 5(b) and (c), respectively. The voltages V_1 and V_2 in Fig. 5(b) are the voltage across C_P after the first and second step of bias-flip, respectively. During the bias-flip, first, the residual charge in C_P will be transferred to C_B through L, then L will connect to C_P to form an LC resonant loop. Finally, the charge will be transferred back to C_P through L. The theoretical analysis based on the voltage rebuilt factor is as follows. For simplicity, the analysis will mainly focus on the falling edge of $V_{\rm PN}$, and C_B is modeled as a constant voltage source V_B during a steady state because its capacitance is large (typically $> 10C_P$). The differential equation of the first, second, and third steps can be given by the following equations:

$$u_{C_P}(t) + RC_P\frac{\mathbf{d}u_{C_P}(t)}{\mathbf{d}t} + LC_P\frac{\mathbf{d}^2u_{C_P}(t)}{\mathbf{d}t^2} = V_B \tag{11}$$

$$u_{C_P}(t) + RC_P\frac{\mathbf{d}u_{C_P}(t)}{\mathbf{d}t} + LC_P\frac{\mathbf{d}^2u_{C_P}(t)}{\mathbf{d}t^2} = 0 \tag{12}$$

$$u_{C_P}(t) + RC_P\frac{\mathbf{d}u_{C_P}(t)}{\mathbf{d}t} + LC_P\frac{\mathbf{d}^2u_{C_P}(t)}{\mathbf{d}t^2} = -V_B \tag{13}$$

where R is the parasitic resistance in the LC loop and u_{C_P} is the voltage across C_P. Meanwhile, the initial condition of the first, second, and third steps can also be given by the following equations:

$$\begin{cases} u_{C_P}(0) = V_S \\ i_L(0) = 0 \end{cases} \tag{14}$$

$$\begin{cases} u_{C_P}(0) = V_1 \\ i_L(0) = 0 \end{cases} \tag{15}$$

$$\begin{cases} u_{C_P}(0) = V_2 \\ i_L(0) = 0 \end{cases}. \tag{16}$$

Solving (11)–(13) with (14)–(16) and assuming that each step lasts for half of the LC period, it can be obtained that

$$V_r = V_B + \left\{\left[V_B - (V_S - V_B)\,e^{-\frac{\delta\pi}{\omega}}\right]e^{-\frac{\delta\pi}{\omega}}\right\}e^{-\frac{\delta\pi}{\omega}} \tag{17}$$

where $\delta = \frac{R}{2L}$ and $\omega = \sqrt{\frac{1}{LC_P} - \frac{R^2}{4L^2}}$. Finally, during the steady state, the voltage V_B will be constant. Hence, the charge of C_B remains constant in each bias-flip process. For example, the transferred charges of Step 1 and Step 3 are the same during the falling edge of $V_{\rm PN}$. This can be given by

$$(V_S - V_1)\,C_B = [V_2 - (-V_r)]\,C_B. \tag{18}$$

Combining (17) and (18), V_B can be expressed as

$$V_B = \frac{1 + e^{-\frac{\delta\pi}{\omega}} - e^{-\frac{2\delta\pi}{\omega}} + e^{-\frac{3\delta\pi}{\omega}}}{2 + e^{-\frac{3\delta\pi}{\omega}}}\,V_S. \tag{19}$$

Subsisting (19) into (17), V_r can be given by

$$V_r = V_S\,\frac{1 + e^{-\frac{\delta\pi}{\omega}} + e^{-\frac{3\delta\pi}{\omega}}}{2 + e^{-\frac{3\delta\pi}{\omega}}}. \tag{20}$$

Combining (5) and (20), the voltage rebuilt factor of the S3BF rectifier can be given by

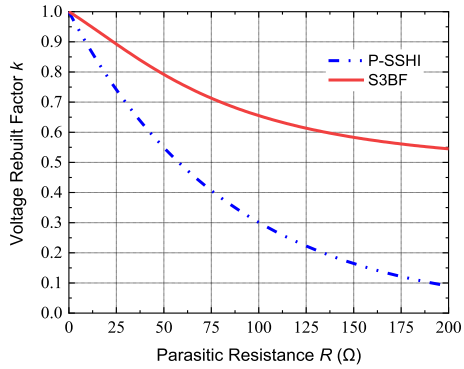

Fig. 6. Theoretically calculated voltage rebuilt factor of P-SSHI and S3BF circuits versus parasitic resistance.

$$k_{\mathrm{S3BF}} = \frac{1 + e^{-\frac{\delta\pi}{\omega}} + e^{-\frac{3\delta\pi}{\omega}}}{2 + e^{-\frac{3\delta\pi}{\omega}}}. \tag{21}$$

To compare the performance of P-SSHI and S3BF, (9) can be rewritten as the following equation, assuming the parasitic resistance R, excitation frequency, and external inductor are the same for these two circuits:

$$K_{\mathrm{SSHI}} = e^{-\frac{\delta\pi}{\omega}}. \tag{22}$$

With the assumption that $L = 470\ \mu$H and $C_P = 32$ nF, Fig. 6 shows the theoretical calculation of voltage rebuilt factor k under different parasitic resistance R for P-SSHI and the proposed S3BF circuit. It can be seen that k_{SSHI} drops quickly as R increases, but k_{S3BF} still remains at a relatively high quantity. This indicates that S3BF circuits have higher harvesting efficiency compared to P-SSHI circuits, especially when the parasitic resistance R is large. As a result, the S3BF control not only boosts the output power capability but also enables the use of smaller external inductance.

More importantly, other inductive bias-flip circuits cannot exhibit bias-flip when the external inductance is zero. The proposed S3BF rectifier, on the other hand, can realize bias-flip without any external inductor, which is not reported in [16]. Assuming that the inductor is shorted (i.e., the inductance of L is 0) in Fig. 4, the bias-flip operation of the proposed circuit will automatically configure to SSHC operation, where the residual charge of C_P will be transferred to C_B, then C_P will be shorted by S_1 and S_3, or by S_2 and S_4, and, finally, the charge will be transferred to C_P. The automatic SSHC operation helps the proposed circuit perform high-efficiency energy harvesting when no inductor is available, which makes the proposed circuit more advantageous in the volume-limited application than other inductive bias-flip rectifiers.

E. Analysis of the Proposed Flipping Time Control Scheme

The inductive bias-flip technology can achieve the lossless flipping process theoretically as discussed earlier. However, the time-domain expression of the flipping process, taking the falling edge of P-SSHI circuits as an example, can be given by [8]

$$u_{C_P}(t) = \frac{\omega_0}{\omega} \exp(-\delta t) \cos(\omega t - \beta) \tag{23}$$

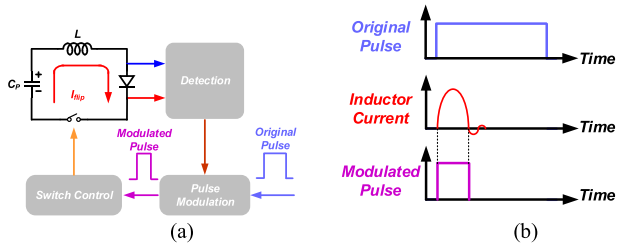

Fig. 7. (a) Diagram and (b) operating waveforms of the proposed adaptive control scheme.

where $\omega_0 = \sqrt{\frac{1}{LC_P}}$, $\omega = \sqrt{\frac{1}{LC_P} - \frac{R^2}{4L^2}}$, $\delta = \frac{R}{2L}$, and $\beta = \arctan(\frac{\delta}{\omega})$. It can be seen from (23) that the inductive bias-flip should be ended exactly at half of the flipping period, or the flipped voltage cannot reach its optimal value. In the practical implementation, it is difficult to well control the flipping time to be exactly half of the flipping period due to the variations of the process, voltage, and temperature (PVT), or different configurations of transducers and inductors. In previous studies, this problem can be addressed by off-chip calibration or adaptive circuit design. The off-chip calibration, namely digital control [6] or variable resistor [7], is hard to implement in practical applications and only suitable for fixed transducers and inductors. On the other hand, the flipping time optimized designs in [3], [8], and [15], which can adjust the flipping time or the flipping process accordingly, are more attractive than their off-chip counterparts. Nonetheless, those designs are only verified under fixed LC_P configurations, whereas in practical applications, a wide range of external components can be applied.

Considering this background, this article proposes the adaptive control scheme based on diode and reverse current detection. As shown in Fig. 7, the proposed adaptive control scheme first generates a pulse signal ("original pulse" in Fig. 7) that is long enough. When bias-flip completes, the inductor current will generate the reverse current from C_P back to L (if L is 0 for SSHC operation or is too small, the reverse current is negligible and the pulse will remain in the original pulse). During this time, this current will be detected via the voltage drop across the diode so that the switch control signal ("modulated pulse" in Fig. 7) can go to a low level to end the flipping process. In this way, not only the flipping time is well adjusted to the optimal flipping time but also the energy loss caused by the inductor's reverse current is reduced significantly by both the diode and the adaptive switch control. Hence, the bias-flip processes with a wide range of external components can be achieved.

In the proposed S3BF circuit, the conduction loss of diodes in the LC resonant loop is minimized by using an on-chip Schottky barrier diode. Meanwhile, the original pulses are designed to be around 100 μs (i.e., about 300 μs for the entire three-step bias-flip), which guarantees both the operation for large LC_P and enough vibrating frequencies range (according to the criterion that the flipping time should be less than 10% of the vibration period [11] and the theoretical vibrating frequency for the proposed circuit can be up to around 300 Hz).

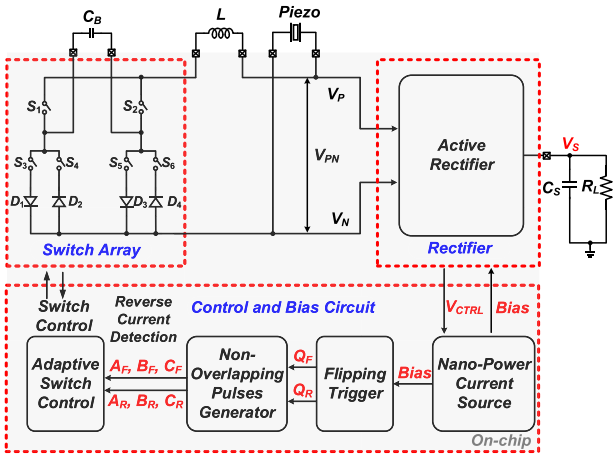

Fig. 8. System diagram of proposed S3BF interface circuit.

III. Circuit Implementation of the Proposed Interface Circuit

The circuit diagram of the proposed S3BF interface circuit can be found in Fig. 8, where the piezo element, loading resistance R_L, storage capacitor C_S, inductor L, and capacitor C_B are off-chip, and other circuits (i.e., the active rectifier (AR), the switch array, the control, and bias circuit) are integrated on chip. The ac input of the piezoelectric transducer is rectified by the AR, where the diodes have been replaced by MOSFETs controlled by a comparator to reduce the conduction loss. The harvested energy that is stored in C_S powers the remaining circuits and the loading. If the control signals from control circuits trigger the bias-flip operation, then the trigger signal will start the pulse generator to generate two groups of identical pulses (three pulses, i.e., A_F, B_F, and C_F, for $V_{\rm PN}$'s falling edge, and three pulses, i.e., A_R, B_R, and C_R, for $V_{\rm PN}$'s rising edge, respectively). The pulses and the diode's voltage that help to detect the inductor's reverse current are processed in the adaptive switch control unit, where the control signals of switches S_{1-6} are generated. The operation and implementation of each block will be discussed in detail as follows.

A. Active Rectifier (AR)

As described earlier, the AR helps to reduce the conduction loss of rectification while providing a signal to trigger the bias-flip operation. Fig. 9 shows that the AR used in this circuit consists of a negative voltage converter (NVC), an active diode, and a diode-connected MOSFET $\rm M_{P1}$ [3], [12], [20], [21]. The NVC can convert the negative voltage of V_P or V_N to a positive value so that one diode drop can be saved compared to FBR [20]. The active diode is formed by a comparator-controlled MOSFET $\rm M_{P2}$. The bulk control circuit, formed by $\rm M_{B1}$ and $\rm M_{B2}$, keeps the bulk terminals of $\rm M_{P1-2}$ at the highest value between $V_{\rm IN}$ and V_S. Also, to guarantee cold start-up, when V_S is relatively low and the comparator cannot well control $\rm M_{P2}$, $\rm M_{P1}$ will harvest the energy until V_S is high enough to allow rectification through $\rm M_{P2}$.

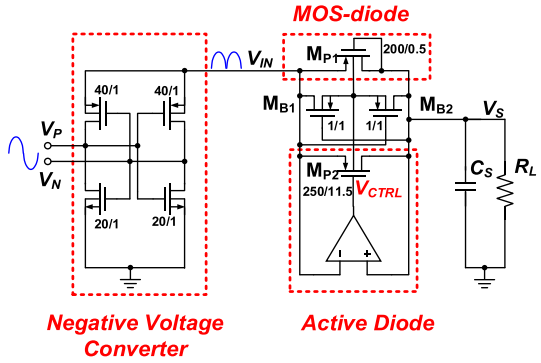

Fig. 9. Schematic of the proposed active rectifier circuit.

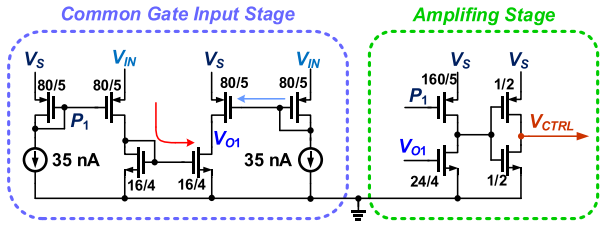

Fig. 10. Schematic of the comparator of the active rectifier circuit.

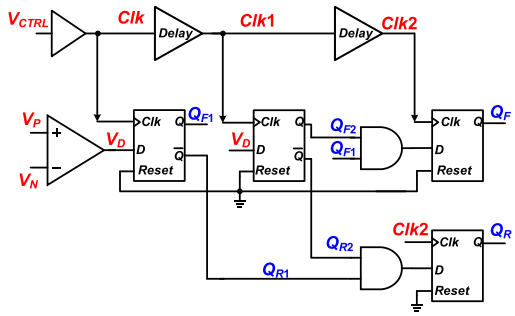

Fig. 11. Schematic of the proposed flipping trigger with noise suppression.

The schematic of the comparator, including a two-stage common-gate-input amplifier and an inverter, is shown in Fig. 10. Owing to common-gate configuration and subthreshold operation, the comparator can achieve low-voltage operation (around 1.4 V), low static power dissipation (about 130 nA quiescent current) and acceptable bandwidth. The simulated dropout voltage can be lower than 20 mV, whereas that of the on-chip diode is at least 100 mV.

B. Flipping Trigger With Noise Suppression

The bias-flip operation should take place during the zero-crossing of current source I_P. When I_P approaches 0, $\rm M_{P2}$ in the AR is about to close, so that the control signal $V_{\rm CTRL}$ in Figs. 10 and 11 will change from low level to high level. By detecting this rising edge, the zero-crossing of I_P can be recognized. Unfortunately, the control signal of the active diode may contain substantial noise, either from the circuit itself or from nonideal mechanical vibration, that will cause erroneous results. The

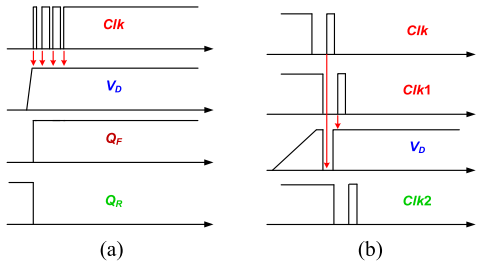

Fig. 12. Operating waveform of flipping trigger (a) before flipping and (b) during flipping.

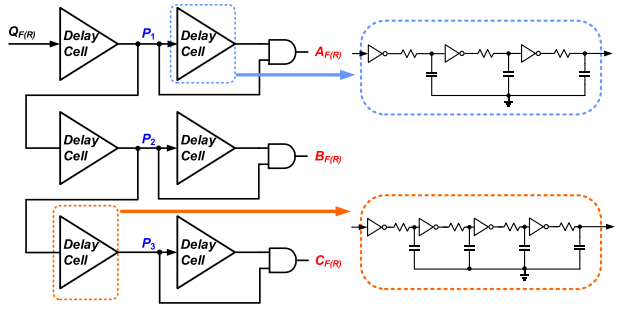

Fig. 13. Implementation of nonoverlapping pulses generator.

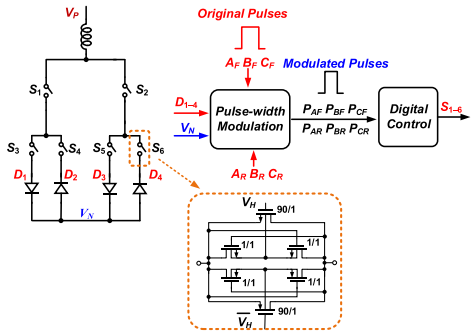

Fig. 14. System diagram of the switch control unit.

Schmitt trigger can be utilized to suppress this noise [5], [22]. Nonetheless, the hysteresis of the Schmitt triggers in [5] and [22] are hard to control since it is directly determined by the devices' parameters that are affected significantly by PVT variations. Hence, this article proposes a double-detection scheme to reduce the effect of noise with better PVT immunity. As shown in Fig. 11, the buffered V_{CTRL}, *Clk*, serves as the edge-trigger signal for D flip-flop. When zero-crossing happened, the *Clk* will rise from low level to high level so that the D flip-flop will be triggered. The flipping direction is determined by the signal V_D. When $V_P > V_N$ and vice versa, the comparator (formed by a classic five-transitor OTA) will generate an output of a high level so that signal Q_F will be pushed to a high level to start the falling operation of V_{PN}. The delay modules are based on *RC* delay.

Meanwhile, the error caused by *Clk* when triggering bias-flip operation (i.e., the operation right before flipping) will be canceled by the detection scheme. As shown in Fig. 12(a), the signal *Clk* contains some glitches and generates multiple rising edges that will trigger the D flip-flop. However, since signal V_D remains at a high level, Q_F and Q_R will remain unchanged after the first flipping edge and will not be affected by the subsequent rising edges of *Clk*.

During the flipping process, the situation will be much more complicated as the flipping will change the polarity of both V_P and V_N, which changes the logic level of V_D. In other words, the noise of both V_D and *Clk* will cause an error. As a result, the double-detection circuits consisting of delay cells, three extra D flip-flops and two AND gates are adopted to address the problem of noise. As shown in Fig. 12(b), during the flipping, the magnitudes of V_P and V_N are gradually changing, which causes V_D also begin to change. During this transition, there may be some glitches generated at both V_D and *Clk*. Fig. 12(b) shows an example of these glitches, where V_D generate an erroneous low level and will be detected by *Clk*. Fortunately, after *Clk* triggers the first detection signal, the *Clk*1 that is *Clk* after short delays will trigger the next detection operation and only if both the first and second detection signals are activated (controlled by the AND gates as shown in Fig. 11), the final detection output will be high and trigger the flipping process. Hence, the error illustrated in Fig. 12(b) will be hard to cause an erroneous flipping process thanks to the double-detection scheme. As a result, the glitches of both signal V_D and *Clk* can be effectively suppressed at the cost of negligible delay (the simulated delay is less than 30 μs and is also lower than the detection delay of 50 μs in [23]).

C. Nonoverlapping Pulse Generator

After zero-crossing detection, three pulses are required to perform a three-step bias-flip. As shown in Fig. 13, the pulse generator is triggered by the signal Q_F or Q_R generated by the flipping trigger circuit. The pulse cell is based on *RC* delay and AND gate [19], and the nonoverlapping property is guaranteed by the delay cell that is of the same structure as the pulse cell.

There are two identical pulse generators in the proposed interface circuits since the trigger signals for V_{PN}'s rising and falling edges, i.e., Q_F as well as Q_R, are processed separately.

D. Adaptive Switch Control

The pulses generated by the pulse generator discussed earlier cannot directly control the switches as different switches need different digital control signals. Meanwhile, the pulses' widths are also not controlled, which indicates that timing errors will occur if they are used to drive the switches directly. Hence, the pulses must be processed digitally, and the pulses' widths should be tuned according to the transducer and inductor, i.e., time constant $2\pi\sqrt{LC_P}$.

Fig. 14 shows the systematic implementation of a switch control circuit. The pulses from the pulse generator will be processed first by the pulsewidth control circuit with the help of diode voltage detections, and then sent to the digital control circuit to generate the control signals. The switches are composed of transmission gates with bulk regulation to prevent current leakage [19]. The pulsewidth control unit can tune the pulsewidth to be half of *LC* resonant period, and its schematic is shown in Fig. 15(a). To illustrate the operating principle of

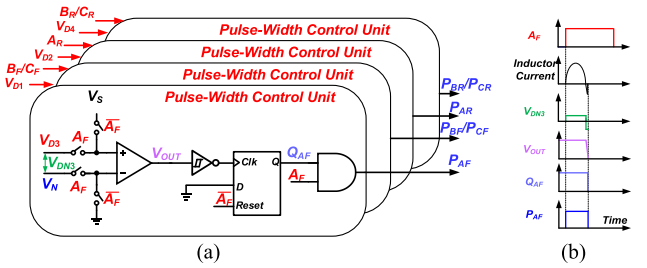

Fig. 15. (a) Schematic of pulsewidth control unit. (b) Operating waveform of A_F-to-P_{AF}.

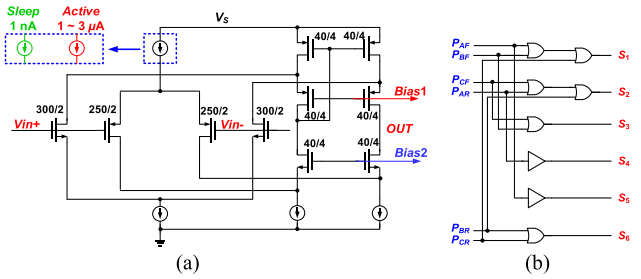

Fig. 16. Schematic of (a) rail-to-rail comparator with active bias and (b) digital control circuit.

a pulsewidth control unit, its operating waveform (taking A_F and P_{AF} as an example) is also shown in Fig. 15(b). During the flipping period, the flipping current passes through the diode D_3 and keeps V_{DN3} (i.e., $V_{D3} - V_N$) positive. When bias-flip is finished, the inductor will generate a reverse current and hence a negative V_D, which is detected by a comparator. As a result, $V_{\rm OUT}$ will change to a low level, and trigger the D flip flop to output a low-level signal Q_{AF}. Finally, P_{AF} is obtained by AND operation of both A_F and Q_{AF}, and then the flipping process is ended. The operation of $P_{AF} \sim P_{CF}$ and $P_{AR} \sim P_{CR}$ are similar. In this way, the actual flipping phases ($P_{AF} \sim P_{CF}$ and $P_{AR} \sim P_{CR}$) are directly determined by $\sqrt{LC_P}$ rather than the RC delay. As a result, the proposed circuit can corporate with different external inductances and piezo elements.

Meanwhile, because the diode's voltage and V_N may vary from $-V_S$ to $+V_S$, the comparators in Fig. 15 must have a rail-to-rail input common-mode range. Besides, the comparator also needs to have sufficient bandwidth to detect the reverse voltage and prevent the inductor from drawing too much current. Hence, this article adopts a rail-to-rail input and output comparator, as shown in Fig. 16(a). The comparator uses both nMOSFET and pMOSFET input pairs to achieve rail-to-rail operation, and the active bias technique [12], [15] is also adopted to increase the bandwidth and reduce power consumption. The bias current is only 1 nA during normal operation and is increased to 1–3 μA (which is affected by PVT) during flipping. The digital control circuit of switches is also depicted in Fig. 16(b) where combinational logic control is applied.

The adaptive switch control also helps to reduce the reverse current of the inductor. Although the diode can sufficiently reduce the reverse current, this current will still be significant due to PVT variations, or especially, when a large external inductor

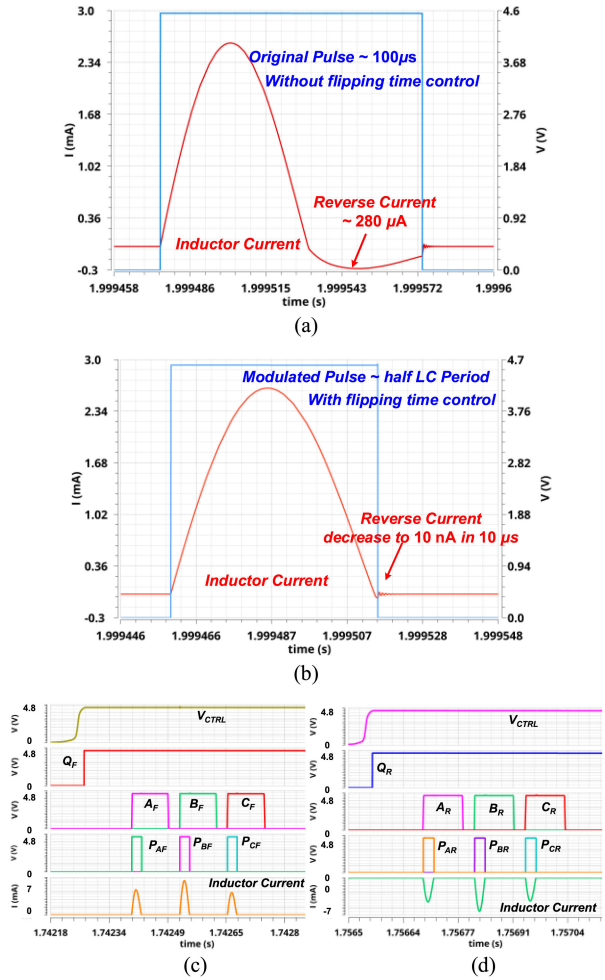

Fig. 17. Simulation results when C_P= 32 nF and L = 10 mH of (a) inductor's current without adaptive switch control, (b) inductor's current with adaptive switch control, (c) control sequences for $V_{\rm PN}$'s falling edge, and (d) control sequences for $V_{\rm PN}$'s falling edge.

is applied. Fig. 17(a) and (b) shows that when a 10 mH inductor with 10-Ω dc resistance is used, the reverse current remains in the order of 100 μA without flipping control, whereas it is attenuated to the range of nA in 10 μs with the proposed flipping time control. Although the reverse current is small by comparing with the forward current, the forward current only shows the charge transformation of the charge of C_P, whereas the reverse current will directly reduce the output current since it comes directly from the input current I_P. The simulated power loss due to the reverse current is 12 μW when V_S = 4.4 V. This power loss is still significant as the output power is only in the unit of 10–100 μW. As a result, this feature also helps the proposed circuit remain high efficiency when the external inductance is large. The simulated time sequences of flipping trigger, pulse generator, and adapative pulses are depicted in Fig. 17(c) and (d). It can be seen that the adaptive pulses change from high-level to low-level when flipping ends so that the flipping time is well controlled according to the external inductance L and the internal capacitance of the piezoelectric transducer, i.e., C_P.

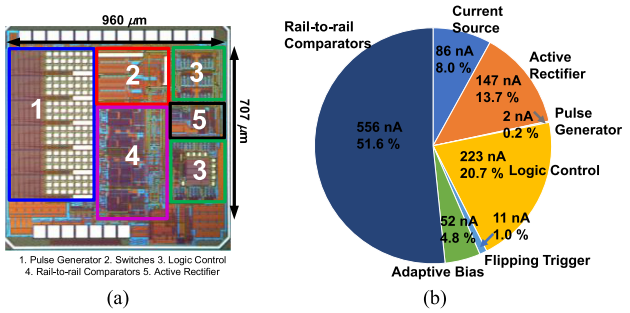

Fig. 18. (a) Chip micrograph. (b) Simulated current breakdown.

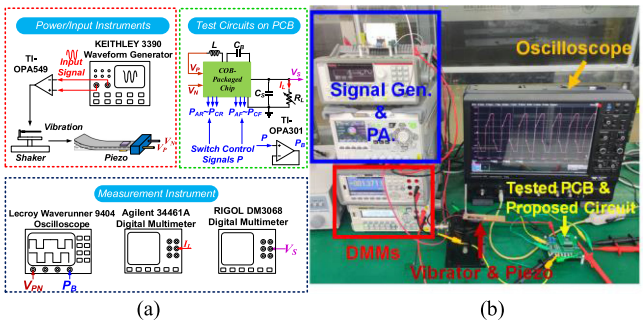

Fig. 19. Measurement setup: (a) conceptual diagram and (b) photograph.

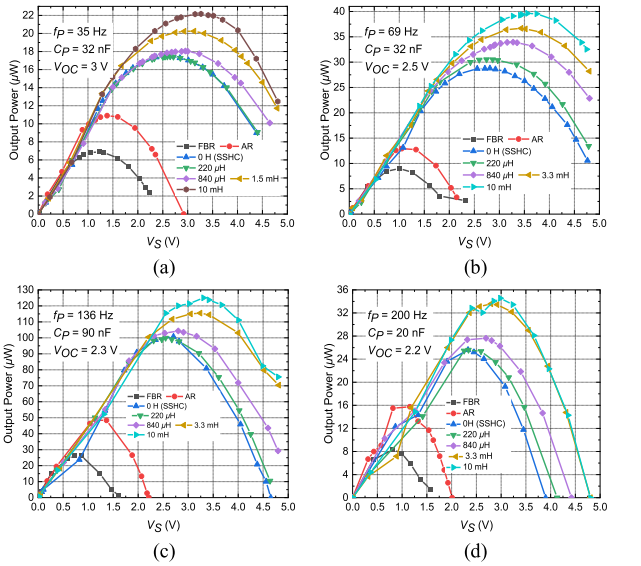

Fig. 20. Measured output power versus V_S under different conditions: (a) $f_P = 35$ Hz and $C_P = 32$ nF, (b) $f_P = 69$ Hz and $C_P = 32$ nF, (c) $f_P = 136$ Hz and $C_P = 90$ nF, and (d) $f_P = 200$ Hz and $C_P = 20$ nF.

IV. Experimental Results

The proposed interface circuit has been designed and fabricated in 180-nm CMOS technology and its chip micrograph can be found in Fig. 18(a). The whole chip area is 0.679 mm^2, where the pulse generator and rail-to-rail comparators occupy the majority of the chip area (i.e., 0.229 mm^2 and 0.125 mm^2, respectively). The area of AR is 0.024 mm^2. The switches and logic control circuit cover the remaining area of 0.301 mm^2. As shown in Fig. 18(b), the simulated total current breakdown of the interface circuit is 1.08 μA and the highest current dissipation (556 nA, 51.6%) is from rail-to-rail comparators, which are used to produce precise switch conduction pulses.

The measurement setup can be found in Fig. 19. The signal generated by the waveform generator will be amplified by Texas Instrument's power amplifier OPA549 to drive the shaker (Wuxi Shiao SA-JZ002). Excited by the vibration, the piezoelectric transducer generates the electrical output harvested by the proposed circuit packaged on a printed circuit board. The pulsewidths of switch control signals ($P_{AF} \sim P_{CF}$ and $P_{AR} \sim P_{CR}$) and the output power are mainly measured. The pulsewidth is measured by an oscilloscope, and the output power is measured by recording the output voltage V_S, which is also the voltage across the storage capacitor C_S, and the output current I_L. The relationship between V_S and the output power is obtained by changing the load resistance R_L [8]. C_B and C_S are with 0805 package (i.e., 2 mm×1.2 mm), the capacitances of which are 680 nF and 10 μF, respectively.

To evaluate the adaptability of the proposed circuits, different external inductance L (ranging from 0 to 10 mH) and different internal capacitance C_P of piezoelectric transducers (varying from 20 nF to 90 nF) is used during measurement. The volumes of the used inductors are 3.13 and 87.9 mm^3, respectively (i.e., the volume is 3.13 mm^3 when the inductance is less than 1 mH, and the volume is 87.9 mm^3 when the inductance is larger than 1 mH). Three types of piezoelectric transducers with 20 nF, 32 nF, and 90 nF capacitance were used in the measurement, whose sizes are 23×20×1, 50×7.2×0.84, and 25×12×0.13 mm^3, respectively. Fig. 20 shows the relationship between output power and V_S. The maximum output power in Fig. 20(c) is the largest even though its V_{OC} is only 2.3 V. The reason is that in Fig. 20(c), C_P is the largest and f_P is relatively high. According to (7), maximum output power grows rapidly as C_P and f_P increase. Meanwhile, the measured V_S only goes up to around 4.8 V to avoid device breakdown. The functions of the proposed circuit are verified under 45 groups of different L and C_P configurations, which are measured under different vibration frequencies. The output power of FBR (1N4148, $V_D = 0.5$ V @ 100 μA) and the proposed stand-alone AR ($V_D = 0.014$ V @ 100 μA) [3], [7], [12], have also been measured to evaluate the maximum output power improving rate (MOPIR) [6], [11], i.e., the maximum output power improvement compared to FBR, or other effective rectifiers. The FBR is used to show the effectiveness of AR, and the performance of bias-flip is shown by the comparison of the proposed S3BF and the standalone AR. The measurement results of output power suggest that the proposed AR can effectively eliminate the effect of conduction loss since the output power of which is much higher than FBR. Besides, thanks to the proposed S3BF technique, the highest MOPIRs for Fig. 20(a)–(d) are 321%, 441%, 473%, and 415% compared to FBR, and 203%, 307%, 258%, and 220% compared to proposed stand-alone AR, respectively. As stated earlier in this article, when the external inductance is 0, the proposed circuit can automatically configure to SSHC topology that can still perform high-efficiency energy harvesting. In this configuration, the MOPIRs for Fig. 20(a)–(d)

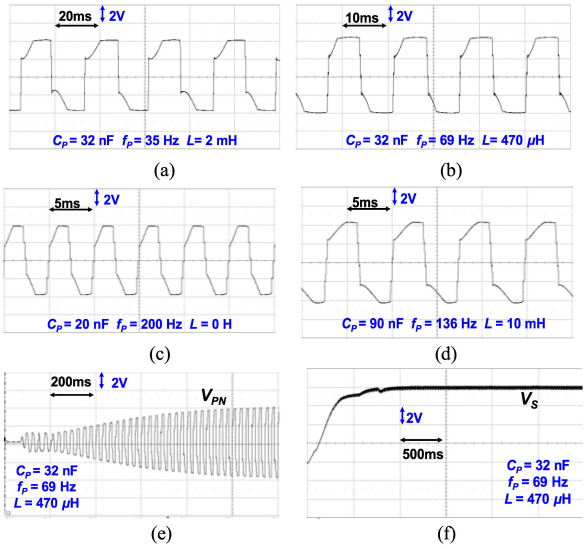

Fig. 21. Measured steady-state waveforms of $V_{\rm PN}$ when (a) $C_P = 32$ nF, $f_P = 35$ Hz, and $L = 2$ mH, (b) $C_P = 32$ nF, $f_P = 69$ Hz, and $L = 470$ μH, (c) $C_P = 20$ nF, $f_P = 200$ Hz, and $L = 0$ H, (d) $C_P = 90$ nF, $f_P = 136$ Hz, $L = 10$ mH, and cold start-up waveforms of (e) $V_{\rm PN}$, and (f) V_S when $C_P = 32$ nF, $f_P = 69$ Hz, and $L = 470$ μH.

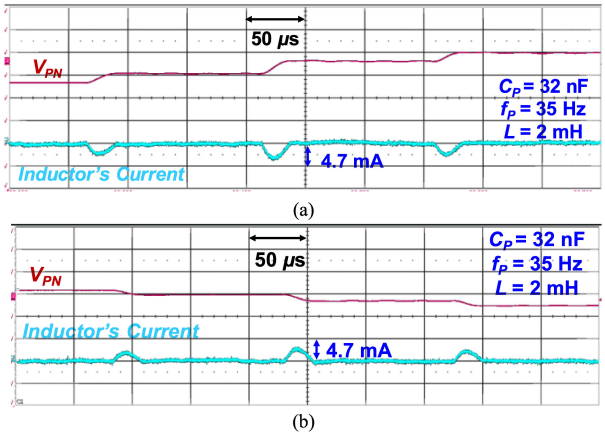

Fig. 22. Measured waveforms of inductor's current during (a) $V_{\rm PN}$'s rising edge and (b) $V_{\rm PN}$'s falling edge when C_P =32 nF, f_P=35 Hz, and L=2 mH.

are 254, 320, 382, and 307% compared to FBR, and 161, 223, 208, and 163% compared to AR.

The operating waveforms of the proposed circuit under different external configurations are also shown in Fig. 21. Fig. 21(a)–(d) indicates the proposed circuit can achieve a three-step bias-flip under different inductors, parasitic capacitors, and vibration frequencies. Besides, the proposed circuit can be configured as SSHC mode when $L = 0$. During a steady state, the flipping efficiency can be as high as 86.6% with a 3.3 mH inductor. As shown in Fig. 21(e) and (f), the waveform of $V_{\rm PN}$ shows that the circuit operates as AR first, and then the S3BF mode operates when the control circuits start to work. The waveform of V_S also shows the storage capacitor is charged from zero to steady state. The start-up waveform also indicates that the proposed circuit can realize a cold start-up.

Fig. 22 illustrates the measured inductor current during bias-flip events. The charge-transferring process and the inductor

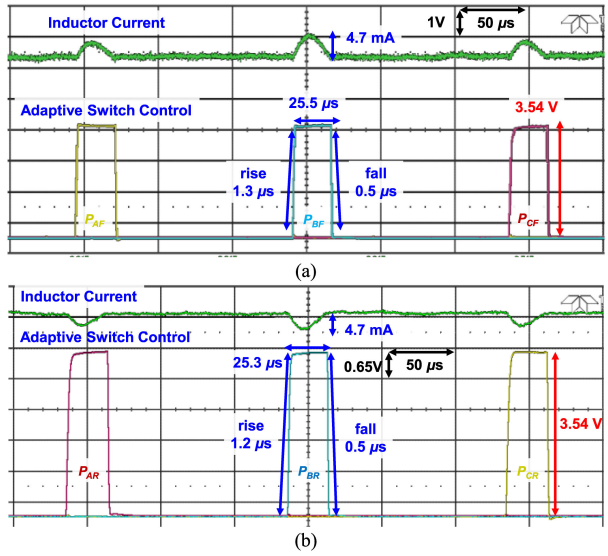

Fig. 23. Measured inductor current versus adaptive switch control signal during (a) $V_{\rm PN}$'s falling edge and (b) $V_{\rm PN}$'s rising edge.

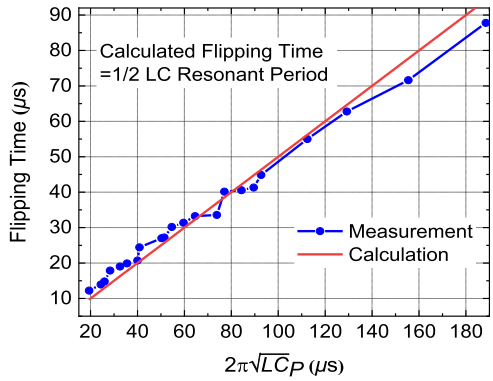

Fig. 24. Measured and theoretically calculated flipping time under different external inductances and piezoelectric transducers.

current are divided into three steps to reduce the peak flipping current as stated in Section III . The measured adaptive flipping time (i.e., the pulsewidth of modulated pulse $P_{AF} \sim P_{CF}$ and $P_{AR} \sim P_{CR}$) during bias-flip is also presented in Fig. 23, where the measured control signals can adjust the pulsewidth according to the transient inductor current. The measured and theoretically calculated (assume flipping time right equal to $\frac{1}{2}\sqrt{LC_P}$) optimal flipping time is illustrated in Fig. 24. It clearly shows that the proposed circuit can adjust the flipping time according to the external inductances and the internal capacitances of piezoelectric transducers, so as to guarantee optimal bias-flip under different LC_P configurations, and the flipping time is very close to half of the ideal LC period.

Table I summarizes the performance of the proposed S3BF rectifier and compares it with other state-of-the-art piezoelectric energy harvesting interface circuits. It is noted that all the works in Table I have a cold start-up capability. Although many researchers succeed in achieving flipping time optimization, those designs are only verified under fixed LC_P configurations and hence may not be able to realize adaptive control. The proposed design, on the other hand, can realize

TABLE I
PERFORMANCE COMPARISON

	This Work	[12] JSSC'12	[7] JSSC'16	[8] TCAS-I'17	[5] JSSC'17	[3] JSSC'19	[19] JSSC'20	[15] TCAS-I'21
Process (nm)	**180**	350	350	250	350	130	180	180
Area (mm^2)	**0.646**	1.25	1.2	0.745	2.9	0.53	0.2	1.23
C_P (nF)	**20~90**	19.5	9.6~27.5	19	45	14/22	22	2
f_P (Hz)	**35~200**	173	134.6~229.6	144	92	432/441	200	415
Off-chjp Components	**1 Cap. 1 or 0 Ind.**	1 Ind.	1 Ind.	1 Ind.	1 ~ 8 Cap.	1 Ind.	4 Cap.	1 Cap. 1 Ind.
Harvesting Scheme	**S3BF**	PSCE	SSHI	SSHI	SSHC	SSHI	SPFCR	SSHCI
Inductor (μH) Volume (mm^3)	**0 ~ 10000 (3.13, 87.9)**	2200~10000 (348.2, 8478) *	3400 (16445.6) *	220 (N/A)	0	47/33 (49)	0	68~100 (18)
Flipping Time	**Self Adj.**	Self Adj.	External Adj.	Self Adj.	External Adj.	Self Adj.	External Adj.	Self Adj.
Adaptive Control	**Yes**	Yes	No	No	No	No	No	Yes
Flipping Step(s)	**3**	3	1	1	3 ~ 17	5	21	3
Flipping Efficiency	**70% @ 0 mH 86.6% @ 3.3 mH**	N/A	89%~94%	75%	66%~89.8 %	89.5%	84%	83.8%~87.1%
MOPIR	**251%~473% (FBR) 161%~307% (AR)**	123%~206% (AR)	269%~681% (AR)	207% (FBR)	270%~970% (FBR)	428%/448% (AR)	590%~930% (FBR)	350%~544% (Ideal FBR)
$FoM_{Adaptive}$ (10^{-3})	**37.70**	8.06	N/A	N/A	N/A	N/A	N/A	0.20

*Calculated from article.

adaptive control under the widest range of L and C_P, which covers the most commonly used inductance and piezoelectric transducers. Meanwhile, the method presented in [3] achieved good output power enhancement with a small inductance of 47 μH, but its inductor's reverse current is not completely eliminated, this current may still reach the order of mA. The $\sqrt{LC_P}$ values in [3] are also limited to 0.811–0.852 μs. If the LC_P setups are modified, the circuit performance of [3] may be degraded. The method presented in [15] also achieves large MOPIR while realizing adaptive control, but the off-chip capacitor in this article is required to be equal to C_P, which is less practical in real applications. The LC_P range for [15] is also relatively narrow. To evaluate the adaptivity (i.e., adaptivity to different inductances, parasitic capacitances of piezoelectric transducers, and vibration frequency), a figure-of-merit, $\mathrm{FoM_{Adaptive}}$, which can be expressed as $f_{P,\max} \times 2\pi \times (\sqrt{LC_P}_{\max} - \sqrt{LC_P}_{\min})$ has been defined in this article. Compared to adaptive designs presented in [12] and [15], the proposed circuit achieves the highest FoM, indicating that the proposed circuit is compatible with more different external configurations and hence more versatile in real applications. The capacitive bias-flip rectifiers in [5] and [19] achieve excellent MOPIRs by applying the multistep bias-flip. Nonetheless, the flipping pulses in these works require off-chip calibration, and more off-chip components are required. Also, these circuits may need many flipping phases like 17 in [5] or 21 in [19], requiring more complicated control circuits and stricter flipping time limitations.

V. CONCLUSION

This article proposes a highly adaptive piezoelectric energy harvesting circuit fabricated in 180-nm CMOS technology. With the help of the proposed S3BF technique together with adaptive control, the proposed circuit can perform efficient energy harvesting under a wide range of inductors and piezoelectric transducers without timing errors. Besides, the proposed circuit can automatically configure to SSHC rectifier to retain the bias-flip operation. The proposed circuit also adopts AR to reduce the conduction loss. Measurement results indicate that the output power enhancement of the proposed circuit can be as high as 473% compared to FBR, and the circuits can extract energy effectively when external inductance changes from 0 to 10 mH and the transducer's internal capacitance varies from 20 to 90 nF. In theory, the proposed interface circuit can also work with transducer capacitance less than 20 nF, which has been proved through simulation. However, this has not been verified from measurement as we cannot get the proper transducer with such small capacitance. Meanwhile, thanks to the flipping time optimization, the proposed circuit can adjust the flipping time according to the external inductances and transducers and reduce the reverse current of the inductor. All these figures of merit reveal that the proposed interface circuit is suitable for most existing piezoelectric transducers and inductors to perform high-efficiency energy harvesting without any off-chip calibration. Nevertheless, the proposed circuit cannot achieve load-independent output power, which can be improved by including maximum power point tracking technology in future work.

ACKNOWLEDGMENT

The authors would like to thank Mr. L. Teng and Prof. J. Liang for useful discussions and helpful advice about measurement setup. They would also like to thank Prof. Shengxi Zhou and Dr. X. Mei for support of piezoelectric transducers, and Mr. W. Li, Mr. S. Xi, and Miss Z. Huang for useful discussions.

REFERENCES

[1] S. Sudevalayam and P. Kulkarni, "Energy harvesting sensor nodes: Survey and implications," *IEEE Commun. Surv. Tut.*, vol. 13, no. 3, pp. 443–461, Jul. 2011.

[2] S. Chamanian, H. Uluşan, A. Koyuncuoğlu, A. Muhtaroğlu, and H. Külah, "An adaptable interface circuit with multistage energy extraction for low-power piezoelectric energy harvesting MEMS," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2739–2747, Mar. 2019.

[3] S. Javvaji, V. Singhal, V. Menezes, R. Chauhan, and S. Pavan, "Analysis and design of a multi-step bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2590–2600, Sep. 2019.

[4] K. Yoon, S. Hong, and G. Cho, "Double pile-up resonance energy harvesting circuit for piezoelectric and thermoelectric materials," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1049–1060, Apr. 2018.

[5] S. Du and A. A. Seshia, "An inductorless bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2746–2757, Oct. 2017.

[6] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.

[7] D. A. Sanchez, J. Leicht, F. Hagedorn, E. Jodka, E. Fazel, and Y. Manoli, "A parallel-SSHI rectifier for piezoelectric energy harvesting of periodic and shock excitations," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2867–2879, Dec. 2016.

[8] L. Wu, X.-D. Do, S.-G. Lee, and D. S. Ha, "A self-powered and optimal SSHI circuit integrated with an active rectifier for piezoelectric energy harvesting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 3, pp. 537–549, Mar. 2017.

[9] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A nail-size piezoelectric energy harvesting system integrating a MEMS transducer and a CMOS SSHI circuit," *IEEE Sensors J.,* vol. 20, no. 1, pp. 277–285, Jan. 2020.

[10] E. E. Aktakka and K. Najafi, "A micro inertial energy harvesting platform with self-supplied power management circuit for autonomous wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 2017–2029, Sep. 2014.

[11] Z. Chen, M.-K. Law, P.-I. Mak, W.-H. Ki, and R. P. Martins, "Fully integrated inductor-less flipping-capacitor rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3168–3180, Dec. 2017.

[12] T. Hehn et al., "A fully autonomous integrated interface circuit for piezoelectric harvesters," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2185–2198, Sep. 2012.

[13] S. Chamanian, H. Uluşan, A. Koyuncuoğlu, A. Muhtaroğlu, and H. Külah, "An adaptable interface circuit with multistage energy extraction for low-power piezoelectric energy harvesting MEMS," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2739–2747, Mar. 2019.

[14] M. B. Khan, H. Saif, and Y. Lee, "A piezoelectric energy harvesting interface for irregular high voltage input with partial electric charge extraction with 3.9× extraction improvement," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2019, pp. 181–184.

[15] B. Çiftci, S. Chamanian, A. Koyuncuoğlu, A. Muhtaroğlu, and H. Külah, "A low-profile autonomous interface circuit for piezoelectric micro-power generators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 4, pp. 1458–1471, Apr. 2021.

[16] J. Liang, Y. Zhao, and K. Zhao, "Synchronized triple bias-flip interface circuit for piezoelectric energy harvesting enhancement," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 275–286, Jan. 2019.

[17] B. Zhao, K. Zhao, X. Wang, J. Liang, and Z. Chen, "Series synchronized triple bias-flip circuit: Maximizing the usage of a single storage capacitor for piezoelectric energy harvesting enhancement," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6787–6796, Jun. 2021.

[18] Y. K. Ramadass, "Energy processing circuits for low-power applications," Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., Massachusetts Inst. Technol., Cambridge, MA, USA, Jun. 2009.

[19] Z. Chen, M.-K. Law, P.-I. Mak, X. Zeng, and R. P. Martins, "Piezoelectric energy-harvesting interface using split-phase flipping-capacitor rectifier with capacitor reuse for input power adaptation," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2106–2117, Aug. 2020.

[20] S. Xi, W. Li, J. Guo, and J. Liang, "A self-powered piezoelectric energy harvesting interface circuit based on adaptive SSHI with fully integrated switch control," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2020, pp. 1–4.

[21] S. Li, A. Roy, and B. H. Calhoun, "A piezoelectric energy-harvesting system with parallel-SSHI rectifier and integrated maximum-power-point tracking," *IEEE Solid-State Circuits Lett,* vol. 2, no. 12, pp. 301–304, Dec. 2019.

[22] M. Meng, D. Wang, B. D. Truong, S. Trolier-McKinstry, S. Roundy, and M. Kiani, "A multi-beam shared-inductor reconfigurable voltage/SECE mode piezoelectric energy harvesting interface circuit," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1277–1287, Dec. 2019.

[23] P. Gasnier et al., "An autonomous piezoelectric energy harvesting IC based on a synchronous multi-shot technique," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1561–1570, Jul. 2014.

Yanhang Chen (Student Member, IEEE) received the B.Eng. degree from the School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou, China, in 2021. He is currently working toward the Ph.D. degree in electronic and computer engineering from the Department of Electrical and Computer Engineering, The Hong Kong University of Science and Technology (HKUST), Hong Kong SAR, China.

His current research interests include the design and calibration of high-resolution ADCs.

Chuhui Wang received the B.Sc. degree in safety engineering from the School of Mechanical and Automotive Engineering, South China University of Technology, Guangzhou, China, in 2020. He is currently working toward the M.Sc. degree in microelectronics and solid-state electronics from the School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou, China.

His current research interests include the design of energy harvesting interface circuits and low-power analog integrated circuits.

Jianping Guo (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electronic engineering from Xidian University, Xi'an, China, in 2003 and 2006, respectively, and the Ph.D. degree in electronic engineering from The Chinese University of Hong Kong (CUHK), Hong Kong SAR, China, in 2011.

From 2004 to 2007, he was an IC Designer with Xi'an Deheng Microelectronics, Inc. From 2011 to 2012, he was a postdoctoral research fellow with the Department of Electronic Engineering, CUHK. In July 2012, he joined the Sun Yat-sen University, Guangzhou, China, where he is currently an Associate Professor with the School of Electronics and Information Technology. His current research interests include the design of analog and mixed-signal ICs for Lidar and IoT applications.

Dr. Guo has been a member of The Power and Energy Circuits and Systems Technical Committee of the IEEE Circuits and Systems Society since 2019 and the Technical Program Committee of the IEEE International Conference on Integrated Circuits, Technologies and Applications since 2018. He is also the Vice Chairperson of the IEEE Solid-State Circuits Society Guangzhou Chapter.