A High-Efficiency Protection Circuit Integrating Semi-Soft Switching and Voltage Limiting Functions for Solid-State Switch Applications

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***Abstract*—Despite the high performance of high-voltage direct current circuit breaker (CB) technology, its high cost restricts its further development. Thus, this article proposes a high-efficiency protection circuit for solid-state switches (SSs) that integrates semisoft switching and voltage limiting functions. The protection circuit also does not resonate with the system inductance which in turn does not affect the reclosing operation of the CB. The novel SS scheme reduces the cost and simplifies the layout of the SS. The special constraints for the parameter design of power electronics, gaps, and metal oxide varistors (MOVs) are proposed in this article for the first time, and a parameters design method that solves the transient power shock and voltage spike problems during the large current breaking process under multiple constraints is formed. Finally, an SS prototype is developed to verify the feasibility and the strong surge and turn-OFF ability of the novel SS and to test the robustness of the series-connected gapped-MOV circuits.**

***Index Terms*—DC circuit breaker (CB), gap, MOV, residual voltage ratio, robustness, solid-state switch (SS).**

I. Introduction

THE VSC-high voltage direct current (HVdc) technology has been rapidly developed to meet the demand for large-scale grid connection of new energy in recent years. HVdc circuit breakers (CBs) can quickly clear the fault current in the dc power grid rapidly to maintain the reliable operation of the VSC-HVdc system [1], [2].

As a result of the development of power electronics, solid-state CBs and hybrid CBs (HCBs)have developed rapidly over the years and become the popular solutions for HVdc CBs in recent years because of their short interruption time [2], [3].

Fig. 1 shows the topologies of one of the solid-state CBs [2] and the HCBs [4]. Their common feature is that they all have a unit composed of semiconductor devices, snubber circuits, and MOVs. We define such a unit as a solid-state switch (SS). When the fault occurs, the fault current is forced to impact the MOVs, generating overvoltage, and causing the high fault current to drop.

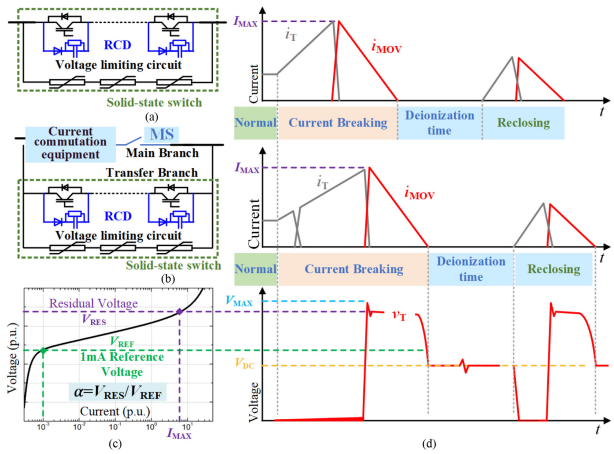

Fig. 1. Topologies of the CBs and their current breaking process. (a) Topology of one of the solid-state circuit breakers. (b) Topology of one of the HCBs. (c) *V–I* curve of the MOV device. (d) Current breaking process.

Overvoltage suppression and high fault current withstand abilities are major considerations when designing an SS. As the most critical component in CBs, a very strong protection circuit is required to cooperate with the SS. Generally, a protection circuit in the SS needs to have the following requirements.

1) Withstand rated voltage and limit overvoltage.
2) Reduce switching losses.
3) Avoid the oscillation after the current is broken.

At present, the mainstream protection circuit is composed of an resistor-capacitor-diode (RCD) snubber circuit and a voltage limiting circuit composed of MOVs. The RCD snubber circuit is used to reduce *dv/dt,* and the MOV is used to limit overvoltage and absorb fault energy.

RC snubber circuit is a low-cost snubber circuit that is widely used in converter valves. However, for the *RC* snubber circuit, the voltage drop across the snubber resistor R_S will increase the overvoltage during the current breaking process. Furthermore, when used with a medium-capacity insulated gate bipolar transistor (IGBT), the *RC* snubber causes the collector current of the

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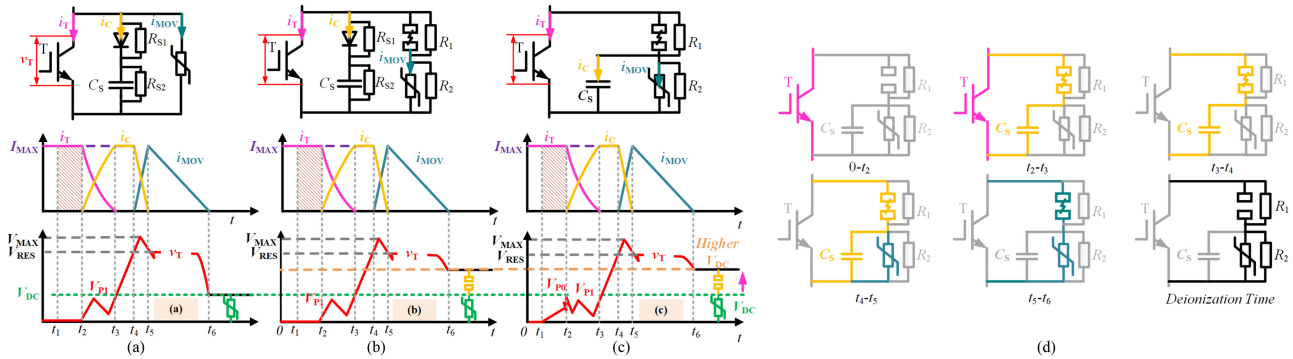

Fig. 2. Development of solid-state switches. (a) Traditional solid-state switch with MOV-RCD. (b) Solid-state switch with gapped-MOV-RCD. (c) Solid-state switch with gapped-MOV-C. (d). operating mode of the solid-state switch.

IGBT to increase, and C_S may oscillate with the system inductance for hundreds of milliseconds, thereby affecting the system reclosing operation. These demerits make the *RC* snubber circuit an inappropriate topology for CBs application [5]–[8]. Only the RCD circuit is applied in 500 kV CBs in the Zhangbei flexible dc transmission project, but the cost of the RCD circuit is high.

In terms of the voltage limiting circuit, although MOVs have voltage-limiting abilities, their limited nonlinearity degrades the SS's static available voltage. In Fig. 1(c), the definition of voltage utilization efficiency $\alpha = V_{\rm DC}/V_{\rm MAX}$ is given. $V_{\rm MAX}$ is the maximum withstand-voltage of the SS. $V_{\rm DC}$ is the SS's static available voltage in deionization time. A SS's $V_{\rm DC}$ is often far lower than its $V_{\rm MAX}$ because of the limited nonlinearity of MOV, thereby resulting in waste in the SS's voltage capacity.

The nonlinearity of a MOV is expressed by the ratio of its residual voltage ($V_{\rm RES}$) for a certain impulse current to its 1 mA/cm^2 reference voltage ($V_{\rm REF}$). $V_{\rm RES}/V_{\rm REF}$ of a MOV is approximately 1.4–1.6 [9], [10], indicating that the voltage utilization efficiency of the SS with parallel MOVs is destined to be lower than 70%. As shown in Fig. 1(b) and (c), MOVs' $V_{\rm RES}$ is generally designed to be lower than the $V_{\rm MAX}$ of the power electronics for the safety margin. Also, MOVs' $V_{\rm REF}$ must be higher than the $V_{\rm DC}$ of the SS, otherwise, the MOV will be damaged in the long-term voltage withstanding. Therefore, the voltage utilization efficiency of the SS in actual projects is often extremely low. The voltage utilization efficiency of the 200 kV CBs in the Zhoushan flexible dc power grid project and the 500 kV CBs in the Zhangbei flexible dc power grid project are approximately 40% [3], [4], [11], thereby greatly increasing the cost of CBs.

To solve this problem, inspired by the gapped-MOVs for lightning protection [10], we proposed a gapped-MOV-based SS [12]. The voltage utilization efficiency is increased from 44.4% to 72.0%. The residual voltage ratio of the gapped-MOV circuit is reduced to 1.1, and the number of series-connected devices is reduced by 31%.

For the SS using an RCD-gapped-MOV circuit as the protection circuit, this article integrates its soft-switching function and voltage-limiting function and then proposes a high-efficiency gapped-MOV-C protection circuit that integrates semisoft switching and voltage limiting functions for SS applications. The gapped-MOV-C circuit, such as the gapped-MOV-RCD, satisfies the standard of a high-efficiency protection circuit and also has the advantages of low cost, small size, and small loop stray inductance. And, the gap's robustness, breakdown characteristic, and regulation method are also discussed for the first time in this article.

The remainder of this article is organized as follows: Section II proposes the integrated gapped-MOV-C protection circuit and introduces its working mechanism. Section III discusses the parameters' design constraints and selection method for the SS. Section IV determines the special design constraints such as the power electronics' transient power tolerance and the gap's breakdown voltage experimentally. Section V discusses the robustness of series modular gapped-MOV-C circuits. Finally, Section VI concludes this article.

II. Proposed Integrated Modular Gapped-MOV-C Protection Circuit

A. Integrated Scheme and Its Working Process

Fig. 2(a)–(c) shows the development of SSs. Fig. 2(a) presents a traditional SS with a MOV-RCD protection circuit [4], [13]. On this basis, as shown in Fig. 2(b), the gap is introduced into the voltage-limiting circuit, and a gapped-MOV-RCD-based SS is proposed [12]. In deionization time (about a few hundred milliseconds), the breakable gap can easily increase the static available voltage $V_{\rm DC}$ of the SS. By configuring appropriate resistors (e.g., R_1 and R_2), the voltage across the MOV is less than its reference voltage, and the leakage current is small, which will not damage the MOV. When the gap is broken down and maintained at a low resistance, it does not affect the overvoltage suppression and decouples $V_{\rm DC}$ and overvoltage.

Instead of adding a separate RCD snubber circuit, in this article, a snubber capacitor is integrated into the voltage-limiting circuit that forms an integrated gapped-MOV-C protection circuit in this article, as shown in Fig. 2(c). The high-efficiency protection circuit integrates semisoft switching and voltage limiting functions. The operating process of the integrated gapped-MOV-C based SS is shown in Fig. 2(d).

1) 0-t_2: The device T starts to turn OFF at time 0, the partial capacitance of the gap is approximately a few picofarads, and the junction capacitance of the MOV device is about several nanofarads. Initially, the gap shares almost all the voltage during this period because of the high *dv/dt*. When

the collector voltage exceeds the gap's breakdown voltage $V_{\rm gpb}$ ($=V_{\rm P0}$), the gap breaks down, and current flows into C_S. The device T operates in a semisoft-switching mode.

2) t_2-t_3: The current flows into the C_S. In this period, a voltage spike $V_{\rm P1}$ appears due to *di/dt* and stray inductance (e.g., busbar inductance). Then, the *di/dt* becomes smaller, and the v_T decreases.
3) t_3-t_4: The current is wholly transferred to the C_S, and the collector voltage v_T gradually rises.
4) t_4-t_5: When v_T exceeds the MOV's reference voltage $V_{\rm REF}$, the current transfers to the MOV circuit.
5) t_5-t_6: The current is wholly transferred to the MOV circuit, the MOV absorbs energy and limits the overvoltage, and the fault current $i_{\rm fault}$ gradually drops to zero. In this period, a voltage spike $V_{\rm MAX}$ appears because of the high *di/dt*, stray loop inductance, and the MOV's steep front effect.

As the fault current $i_{\rm fault}$ gradually drops to zero at t_6, the insulation of the gap is restored, Hence, C_S will not oscillate with system inductance.

Deionization Time: By configuring appropriate resistors (e.g., R_1 and R_2), the gap and the MOV each share part of the dc-bus voltage, the voltage across the MOV is less than its reference voltage, and the leakage current will not damage the MOV. To distinguish the gapped-MOV from MOV devices, the gapped-MOV's 1 mA/cm^2 reference voltage is represented by $V_{\rm REF}{}'$. The residual voltage ratio of the gapped-MOV circuit is represented by α'.

Compared with the SS with the gapped-MOV-RCD circuit, the novel scheme uses one less high-power diode and its press-fit structural parts. The integrated scheme is simpler, and the commutation loop between the MOV and the snubber circuit is small. This feature reduces the complexity of the SS structure design and reduces the volume of the high-voltage CBs.

In t_1-t_3, the device T in the integrated scheme operates in a semisoft-switching mode, aside from V_{P1} (in t_2-t_3) and $V_{\rm MAX}$ (in t_4-t_5), an additional voltage spike $V_{\rm P0}$ exists at t_2. The voltage spike V_{P0} and the transient power shock will be discussed later.

B. Dynamic Threshold Effect of Modular Solid-State Switch

During the large current breaking process, passive dynamic voltage balance measures cannot eliminate series devices' inconsistent turn-OFF process. Moreover, the gap's breakdown $V_{\rm gpb}$ fluctuates, and the turn-OFF inconsistency will be more pronounced for SSs using gapped-MOV circuits. To solve this problem, discrete gapped-MOV-C protection circuits are connected in parallel with each power electronic device. Even if the turn-OFF time of the series devices and the breakdown voltages of the gaps are inconsistent, in Fig. 3 the overvoltage across the device will be clamped by each discrete MOV.

III. Parameters' Design Constraints and Selection of the Novel Solid-State Switch

For SSs that used the gapped-MOV-C protection circuit, special and mutually interacting constraints are observed in the parametric design. Specifically, the gapped-MOV circuit reduces the overvoltage across the CBs and the number of series-connected SSs, which reduces the cost of CBs significantly. However, the lower overvoltage slows down the current interruption process and increases the energy dissipated in the MOVs. Conversely, in order to reduce the residual voltage ratio, the gap needs to share more dc-bus voltage, that is, at t_2, the device will withstand a higher transient power shock.

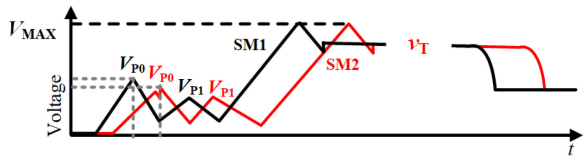

Fig. 3. Dynamic threshold effect of series-connected SSs.

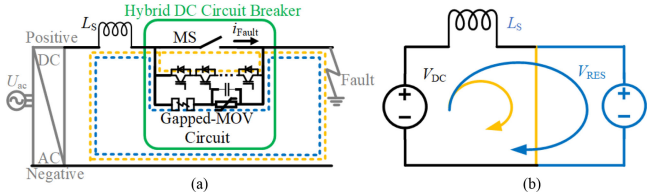

Fig. 4. Simplified DC power system circuit. (a) Simplified dc power system circuit. (b) Equivalent circuit.

A. Effect of Low Residual Voltage Ratio

A flexible dc power system is shown in Fig. 4(a). During the current breaking process in 0-t_r, the current rises from the system rated current $I_{\rm rate}$ to $I_{\rm max}$ (represented by the yellow line in the figure). The voltage limiting circuit has not yet limited the voltage and dissipated energy at this stage, and the CB is in a low resistance state. The equivalent circuit in this process is shown as the yellow loop in Fig. 4(b), where L_S is the system loop inductance.

The fault current rise time t_r can be calculated

$$t_r = (I_{\rm max} - I_{\rm rate})L_S/V_{\rm DC}. \tag{1}$$

Thus, as the voltage limiting circuit in the CBs, the gapped-MOV circuit does not affect the fault current rise time t_r.

In the t_r-t_f stage, v_T exceeds the supply voltage $V_{\rm DC}$. Hence, the fault current gradually decreases to 0 (represented by the blue line in the figure). During this process, v_T decays slowly, and the MOV can be approximated as a voltage supply. The equivalent circuit is shown as the blue loop in Fig. 4(b).

The fault current fall time (t_f-t_r) and the energy dissipated in the MOVs can be calculated as

$$t_f - t_r = \frac{I_{\rm max}L_S}{V_{\rm RES} - V_{\rm DC}},\ \text{where}\ V_{\rm RES} = \alpha' V'_{\rm REF} = \alpha'\beta V_{\rm DC}$$
$$E_{\rm dis} = \frac{\alpha' I^2 L_S}{2(\alpha' - \beta)} \tag{2}$$

where β is related to the system voltage, generally 1.05-1.1. $E_{\rm dis}$ is the energy dissipated in the MOVs.

As shown in Fig. 5, the main contribution of the gapped-MOV circuit is to reduce series-connected power electronic devices by

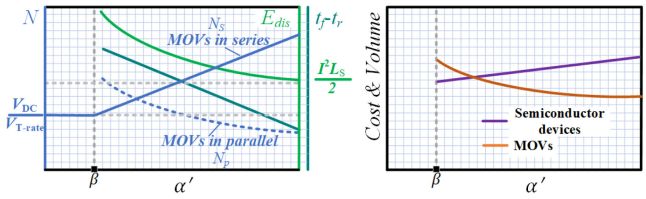

Fig. 5. Effect of the low residual voltage ratio.

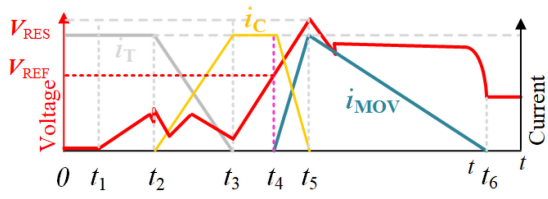

Fig. 6. Process of current transfer to the MOV circuit.

reducing residual voltage ratio α'. However, the reduced ratio slows down the current interruption process and increases the energy dissipated in the MOVs. Therefore, when designing a CB with the gapped-MOV circuit, an appropriate overvoltage of the power system or the breaking time of the CBs must be determined. Reducing α' blindly may increase the cost of MOVs significantly.

B. Parameter Selection of the Modular Gapped-MOV

After setting the overvoltage of the system, we determine the parameters of the modular SS. Generally, a suitable semiconductor device is selected first, and then the parameters of the snubber capacitor and the voltage limiting circuit are determined.

1) Residual Voltage of MOV-V_{RES}*:* The overvoltage peak $V_{\max}$ will be slightly higher than the V_{RES} provided by the manufacturer because of the stray loop inductance. To facilitate the selection of parameters, this article no longer distinguishes V_{RES} and V_{MAX}. V_{RES} depends on the I_{MAX} and the front time t_f, generally

$$V_{\mathrm{RES}}(I_{\mathrm{MAX}}/N_p, t_f) \le k_s V_{T-\mathrm{rate}} \tag{3}$$

where k_s is the device's voltage safety factor, usually 0.8–0.9. $V_{T\text{-rate}}$ is the device's rated voltage. N_p is the number of MOVs connected in parallel, which depends on the energy that needs to be dissipated. Providing enormous energy in the laboratory is difficult. This article selects N_p from the perspective of overvoltage protection.

2) Reference Voltage of MOV-V_{REF}*:* To reduce the MOV's leakage current, the MOV's continuous operating voltage $V_{\mathrm{MOV\text{-}DC}}$ is lower than its reference voltage

$$V_{\mathrm{MOV-DC}} = V_{\mathrm{REF}}/\beta = V_{\mathrm{RES}}/\alpha\beta. \tag{4}$$

3) Breakdown Voltage of Gap-V_{gsb} *and* V_{gpb}*:* In the deionization time, $V_{\mathrm{MOV}} = V_{\mathrm{MOV\text{-}DC}}$, the MOV is in high resistance, and its resistance value is in the megaohm level. As the voltage decreases, its resistance increases largely. To reduce the influence of individual differences on voltage balancing issues, a resistor of several hundred kilohms is connected in parallel with the MOV. The gap and MOV are connected in parallel with resistors R_1 and R_2

$$\begin{aligned} V_{\mathrm{gap-DC}} + V_{\mathrm{MOV-DC}} &= V_{\mathrm{DC}} = V_{\mathrm{RES}}/\alpha'\beta \\ V_{\mathrm{gap-DC}}/V_{\mathrm{MOV-DC}} &= R_1/R_2 \end{aligned} \tag{5}$$

where $V_{\mathrm{gap\text{-}DC}}$ is the gap voltage in MS opened stage.

According to the volt-second characteristics of the gap

$$V_{gpb} = k_{V-T} V_{gsb} \text{ and } V_{\mathrm{gap-DC}} < V_{gsb} \tag{6}$$

where $k_{V\text{-}T}$ (>1) is the volt-second characteristic coefficient of the gap, which can be obtained through experiments. V_{gpb} is the gap's pulse breakdown voltage. V_{gsb} is the gap's static-state breakdown voltage.

As mentioned above, the *dv/dt* across the semiconductor device is high, and the gap shares almost all of the voltage in t_1-t_2

$$V_{gpb} \le k_s V_{\mathrm{T-rate}} \text{and} V_{gpb} \le k_P P_{\mathrm{T-MAX}}/I_{\mathrm{MAX}} \tag{7}$$

where $P_{T\text{-MAX}}$ is the semiconductor device's maximum transient power tolerance at t_2. k_P is the power shock safety factor.

To reduce the residual voltage ratio α', according to Eq. (5), a higher $V_{\mathrm{gap\text{-}DC}}$ must be set to reduce the reference voltage of the MOVs. According to (7), the gap's breakdown voltage determines the transient power P_0, indicating that at t_2, the device will withstand a higher transient power shock. Thus, an appropriate gap breakdown voltage needs to be set to balance the transient power shock and the residual voltage ratio.

C. Parameter Selection of the Modular Gapped-MOV

The snubber capacitor affects the device's turn-OFF process in t_2-t_3 period and the current transfer process to the MOV in t_4-t_5. The appropriate parameters are usually obtained through simulation by establishing a detailed model.

This article proposes a simplified method for determining snubber capacitor C_S. As shown in Fig. 6, at time t_4, the current is transferred from the capacitor to the MOV, that is, V_{MOV} at this moment exceeds V_{REF}.

Due to stray loop inductance and *di/dt,* the capacitor voltage will be greater than the MOV voltage. To simplify the calculation, the effect of stray loop inductance, $V_{\mathrm{Cs}} = V_{\mathrm{MOV}}$, is ignored. At t_5, V_{MOV} can be approximated to V_{RES}. In t_4-t_5, i_{fault} continues to charge the C_{S}, and its voltage increases from V_{REF} to V_{RES}. This process can be described as

$$C_S \cdot (V_{\mathrm{RES}} - V_{\mathrm{REF}}) = 0.5 \cdot I_{\mathrm{MAX}} \cdot \Delta t \tag{8}$$

where Δt is the commutation time, which is t_f.

Based on (8), we can obtain an initial value of the snubber capacitor. On this basis, the loop inductance and the device turn-OFF period (t_2-t_3) are considered to determine the snubber capacitance instead of starting from $C_S = 0$.

D. Modeling and Simulation of the Solid-State Switch

Taking the gap breakdown time as the boundary, the current breaking process of the SS can be divided into two stages. Fig. 7(a) and (b) illustrate the model of the SS before and

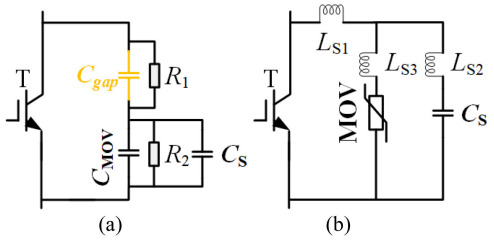

Fig. 7. Dynamic model of the solid-state switch. (a) Model before the gap breakdown. (b) Model after the gap breakdown.

after the gap breakdown, respectively. $C_{\rm gap}$ is the gap's partial capacitance, $C_{\rm MOV}$ is the MOV's junction capacitance, and L_{S1} is the bus inductance between the device *T* and the gapped MOV circuit. L_{S2} is the bus inductance in the snubber circuit, and L_{S3} is the bus inductance in the voltage limiting circuit. The experimental results show that the voltage across the gap after the gap breakdown is about tens of volts, which is negligible compared with the overvoltage. $C_{\rm gap}$ is several pF, and $C_{\rm MOV}$ is several nanofarads to tens of nanofarads.

After the gap breakdown, v_T can be expressed as

$$\begin{cases} v_T = (L_{S1}+L_{S2})\frac{di_{\rm CS}}{dt} + \frac{1}{C_S}\int_{t_2}^{t_4} i_{\rm CS}dt(t_2-t_4) \\ v_T = L_{S1}\frac{di_{\rm fault}}{dt} + L_{S2}\frac{di_{\rm CS}}{dt} + \frac{1}{C_S}\int_{t_2}^{t_5} i_{\rm CS}dt(t_4-t_5) \\ \quad = L_{S1}\frac{di_{\rm fault}}{dt} + L_{S3}\frac{di_{\rm MOV}}{dt} + v_{\rm MOV} \end{cases} . \quad (9)$$

The SS's component parameters are generally determined before its layout design. To facilitate layout design, engineers generally set a lower device operating voltage $V_{\rm RES}$; as such, the difficulty of layout design and design iterations are reduced. This design process is relatively quick but uneconomical. When designing the 500 kV CBs in the Zhangbei flexible dc project, the safety factor of the device k_S was 0.8, and C_S is set to 300 μF [13].

In [14], we proposed a low inductance SS layout, and the loop inductance is significantly lower than those reported in other literature. When designing parameters based on this premise, the device operating voltage set in the existing project can be increased appropriately. In this article, the operating voltage of a 4.5 kV device is raised from 3.6 to 4.0 kV. In engineering, $V_{\rm MAX}$ exceeds 4.0 kV [11].

The diode full-bridge submodule is applied in the 500 kV CBs in the Zhangbei flexible dc project. Based on the layout in [13], the gapped-MOV circuit is introduced into the diode full-bridge sub-module. The "+" layout for the gapped-MOV-C-based SS is shown in Fig. 8(a), and the "+" layout for the gapped-MOV-RCD-based SS is shown in Fig. 8(b). From left to right are *T*, diodes, gap, snubber capacitor, and MOVs. In terms of size, for Gapped-MOV-C based SS, its length is reduced by 27% from 1370 to 1000 mm. Table I gives the stray bus inductance and size parameters of the two SSs. In terms of loop bus inductance, for the gapped-MOV-C based SS, during t_2-t_3, the loop inductance is reduced by 40.2% from 86.9 to 52 nH, and during t_3-t_4, the loop inductance is reduced by 66.4% from 138.1 to 46.4 nH.

In this article, the rated voltage of the device is 4500 V, and the rated current is 2100 A. This device is designed to turn OFF five times its rated current, which is 10.5 kA. The device model

TABLE I
INDUCTANCES IN THE SOLID-STATE SWITCH OBTAINED BY Q3-D (NH)

	L_{S1}			L_{S2}	L_{S3}	*Size* (mm^3)
	L_{B1}	L_{B2}	L_{B3}			
Gapped-MOV-RCD-based SS	12.4	8.4	5.6	25.6	20.8	1370×350×440
Gapped-MOV-C-based SS	12.4	8.4	5.6	60.5	77.6	1000×350×440

for the MOV is YH7W-2.4/3.6, its 1 mA/cm^2 reference voltage is 2.4 kV, under 5 kA-8/20 μs pulse current, and the residual voltage is 3.6 kV. Therefore, the number of MOVs connected in parallel is $N_{\rm p} = 2$. By using (8), the initial value $C_S = 25$ μF.

Based on the dynamic model, we analyzed the influence of $C_{\rm S}$ and loop inductance on voltage spike (V_{P1} and$V_{\rm MAX}$). Fig. 9(a) shows the $V_{\rm MAX}$ under different fault currents ($C_S = 25$ μF, $L_{\rm equ} = 0$ nH). Fig. 9(b) shows the influence of loop inductance on $V_{\rm MAX}$ ($C_S = 25$ μF). Fig. 9(c) shows the influence of C_S on $V_{\rm MAX}$ ($L_{\rm equ} = 0$ nH). Fig. 9(d) shows the influence of C_S on V_{P1}.

The results show that when $C_{\rm S} = 25$ μF, the overvoltage can be controlled within 4 kV. Moreover, the voltage spike increases approximately linearly with the increase in loop inductance. Increasing the snubber capacitance within a specific range can reduce the voltage spike. After exceeding this range, the effect is significantly reduced. Combining low-inductance design with theoretical analysis (8) to determine the snubber capacitor is an economy design method.

IV. Determination of the Transient Power Tolerance and the Gap Breakdown Voltage

During the large current breaking process, the semiconductor devices in the transfer branch are first turned ON for a few milliseconds and then turned OFF. As mentioned above, a transient power shock occurred during the turn-OFF process (at t_2), $P_0 = I_{\rm MAX}V_{gpb}$. As discussed in Section III, the stress on the semiconductor device increases as the residual voltage ratio decreases. A constraint, which is the semiconductor device's transient power tolerance-$P_{T\text{-MAX}}$, must be obtained first, and then the boundary of the gap breakdown voltage should be determined to guide the design of the gap. Evaluating the devices' transient power tolerance $P_{T\text{-MAX}}$ after a surge current flow period is difficult, especially in CBs operating mode.

A. Determination of the Device's Transient Power Tolerance

Referring to the HCBs' current breaking process in Zhangbei 500 kV Flexible dc Project, the contacts in the MS take 1–3 ms to separate to a sufficient insulation distance, after which the semiconductor devices in the transfer branch can be turned OFF. The fault current flows through the semiconductor devices for 1–3 ms. The device's junction temperature rises and can be calculated using the thermal network model, such as the Foster model. In the device's turn-OFF process, the turn-OFF time (t_1-t_3) ranges from a few μs to a dozen μs, which is much smaller than

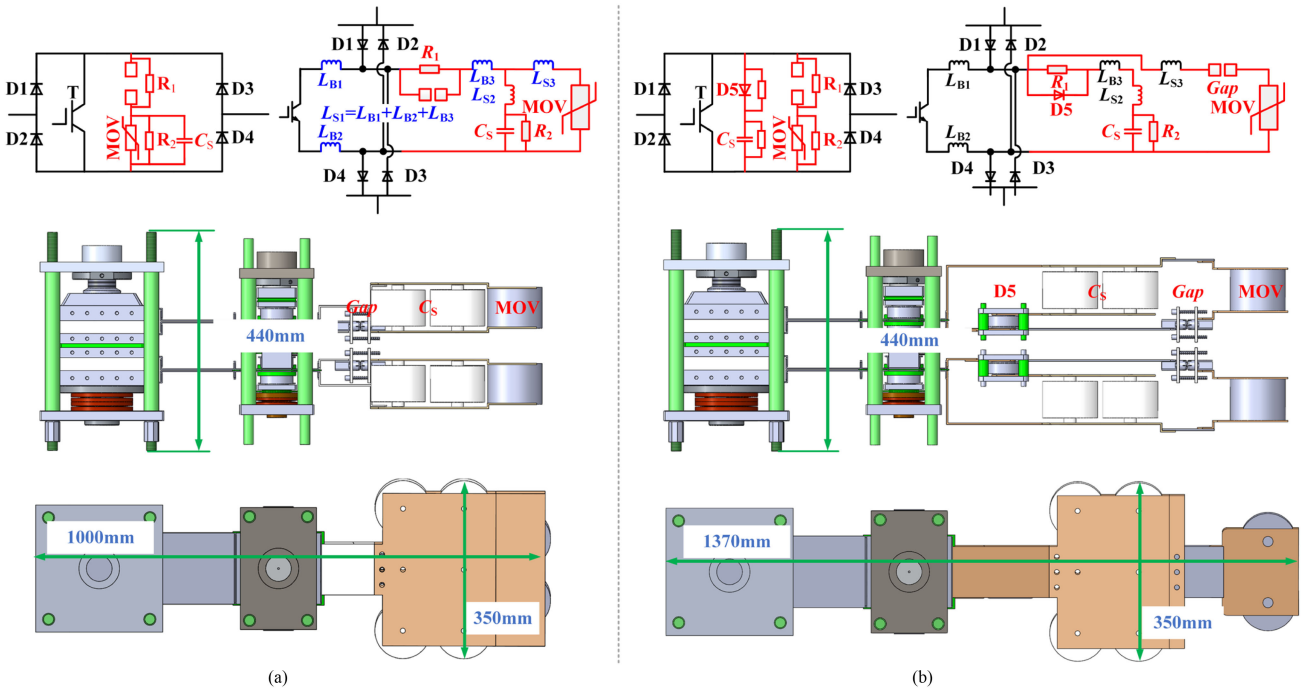

Fig. 8. "+" layout for the integrated design scheme. (a) "+" layout for the gapped-MOV-C-based SS. (b) "+" layout for the gapped-MOV-RCD-based SS.

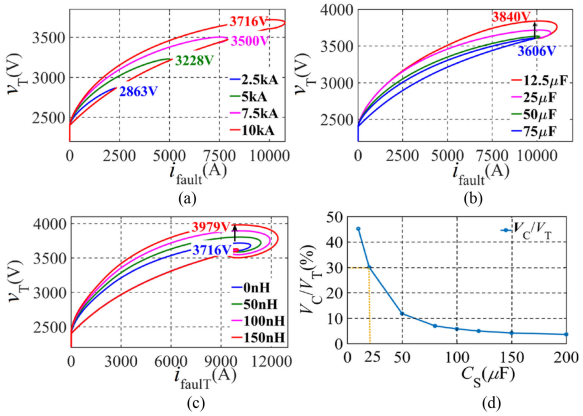

Fig. 9. Influence of capacitor capacitance and loop inductance on voltage spike. (a) V_{MAX} under different fault currents. (b) Loop inductance influence on V_{MAX}. (c) Influence of C_{S} on V_{MAX}. (d) Influence of C_S on V_{P1}.

the thermal network's time constant ($\geq$1 ms), and the device's junction temperature cannot be calculated.

The device's surge and turn-OFF ability are involved in this operating mode. This problem is very complex and has not yet been fully solved. Few scholars have explored this area, and there are significant differences between different products, so most of the current research is based on tests [15]. In this article, the device's surge and turn-OFF ability is investigated through experiments. Like in the project, after the fault current rises for 3 ms, the semiconductor device is turned OFF to test its transient power tolerance $P_{T\text{-MAX}}$ and V_{gpb} at t_2.

The high-power semiconductor devices are expensive, and the destructive test is dangerous. In this article, we test the transient power of one chip over a period of current flow to infer the device's maximum transient power tolerance. We connect a good device in series with a chip to protect the test circuit, as shown in Fig. 10(a). The *LC* oscillator circuit generates the required pulse current, and then the device and the chip are turned OFF. In this article, the rated current of a single chip is 50 A.

The current breaking result is shown in Fig. 10(b), and the chip is not damaged. A single chip can turn OFF the pulse current seven times its rated current in 3 ms, which is 365 A; V_{gpb} is 3714 V. In this operating mode, the transient power tolerance of a single chip is above 1.35 MW.

We assume that the current of each chip is the same, and the transient power tolerance of a single device is above 56.9 MW (42 parallel chips in a single device). Considering the difference between the chips and the uneven current distribution [16], [17], this article refers to the injection enhanced gate transistor (IEGT) device's current breaking test results in [11] and [18], and consults the manufacturer, about the safety of the device. P_T is limited to less than 25 MW. V_{gpb} cannot exceed 2.5 kV ($i_{\mathrm{fault}} = 10$ kA).

B. Gap Design and Its Breakdown Voltage Regulation

The gap's breakdown voltage is affected by many factors, such as the structure of the gap, the dielectric, the environment, and the volt-second characteristics.

Many scholars have conducted in-depth research by optimizing the contact structure to adjust gap's the breakdown voltage [19], [20], and a similar research process will not be repeated here. This process requires constant adjustment of the

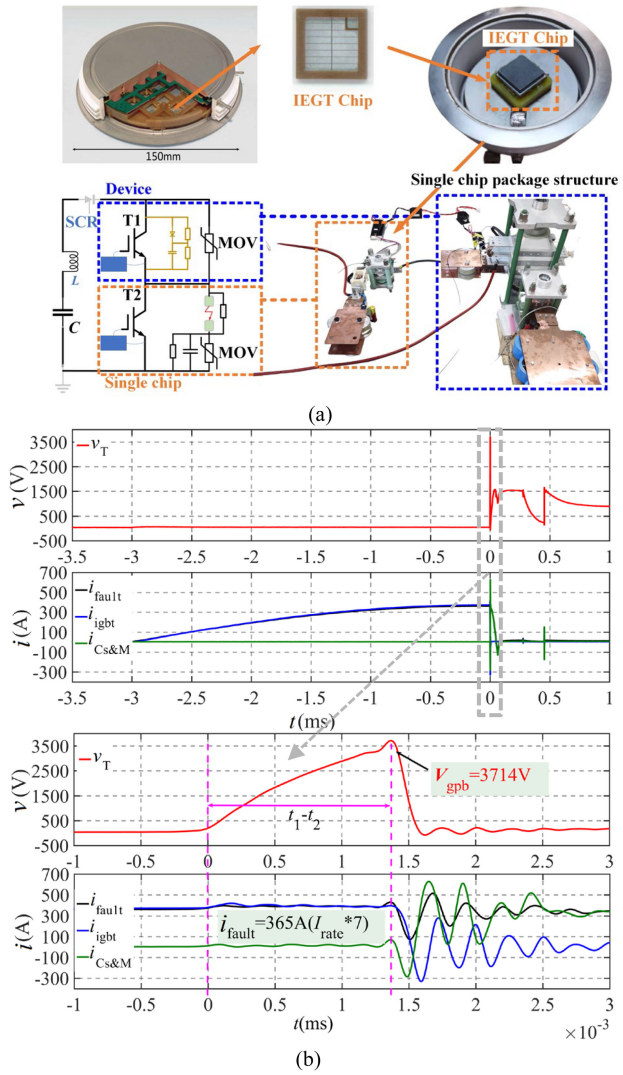

Fig. 10. Large current breaking result of a single chip. (a) Test circuit. (b) Single-chip large current breaking result.

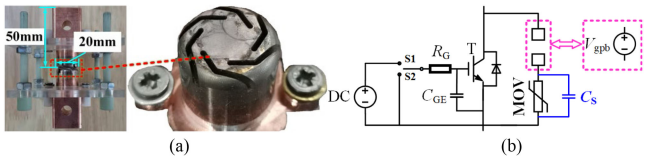

Fig. 11. Transverse magnetic contact. (a) Transverse magnetic contact. (b) Equivalent circuit.

structure and materials of the contact, which is costly and has a long lead time.

We designed a transverse magnetic contact and applied it to SSs, as shown in Fig. 11. This contact is only a prototype. For easy viewing of the contacts, the contacts have no encapsulation structure and are exposed to air. To minimize the influence of environmental factors, such as temperature and humidity, tests are carried out rapidly.

After continuously optimizing the contact structures, when the gap spacing is 0.33 mm, in the air, when the static breakdown

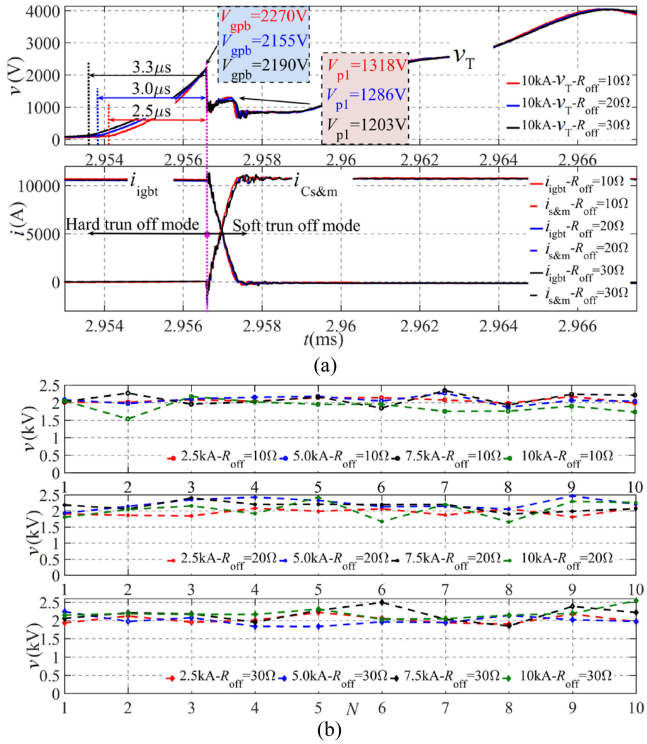

Fig. 12. Module-level tests of 0–10 kA. (a) R_{off} increases from 10 to 30 cΩ. (b) Effect of R_{off} on the V_{gpb} under different fault currents.

voltage -V_{gsb} does not exceed 2.0 kV, the pulse breakdown voltage of the gap -V_{gpb} does not exceed 2.5 kV. Until now, the gap has broken down nearly 1000 times, the single arcing time is nearly 1 ms, and the contact is still in good condition.

In addition to optimizing the contact structures, we attempted to change the volt-second characteristics of the gap to regulate its breakdown voltage. IEGTs are fully controlled semiconductor devices, and we can adjust their turn-OFF processes by changing the gate resistance. As introduced in Section II, in 0-t_2, the device operates in hard turn-OFF mode, and v_T increases rapidly to the gap's breakdown voltage. During this period, the turn-OFF process of the device is the same as the device in the half-bridge modular multilevel converter (MMC) submodule. Before the gap breakdown, the gap can be equivalent to a voltage source, as shown in Fig. 12(b). Refer to [21] to obtain

$$t_2 - t_1 = R_{\text{off}} C_{\text{GE}} \frac{V_{gpb}}{V_{\text{GP}}} \rightarrow \frac{V_{gpb}}{t_2 - t_1} = \frac{V_{\text{GP}}}{R_{\text{off}} C_{\text{GE}}} \tag{10}$$

where R_{off} is the gate-emitter resistor, and C_{GE} is the gate-emitter capacitor. V_{GP} is the miller platform voltage.

Therefore, the volt-second characteristics of the gap can be changed by adjusting $R_{\text{off}}C_{\text{GE}}$. This article attempts to regulate the gap's breakdown voltage by adjusting R_{off} to a few ohms. Module-level tests of 0–10 kA are carried out.

In Fig. 12(a), when R_{off} increases from 10 to 30 Ω, (t_2-t_1) is increased from 2.5 to 3.3 μs, and V_{P1} is reduced from 1318 to 1203 V. Fig. 12(b) shows the effect of R_{off} on the V_{gpb}. Under different breaking currents and different R_{off}, the gap breakdown voltage has no obvious difference but fluctuates within a specific

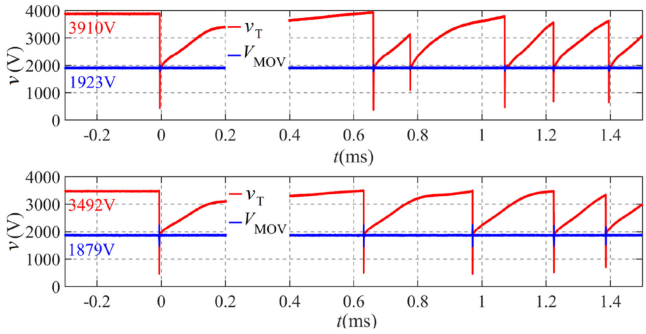

Fig. 13. Gap static breakdown voltage.

TABLE II
COMPARISON OF POWER LOSS AND TRANSIENT POWER SHOCK

R_{off} (Ω)	Hard (J)	P_{MAX} (MW)	V_{gpb} (V)	Δt (μs)	Soft (J)	P_{MAX} (MW)	V_{P1} (V)	Δt (μs)
10	22.45	23.37	2270	2.5	4.68	12.12	1318	0.86
20	25.39	22.61	2155	3.0	4.83	12.39	1286	0.86
30	28.34	23.09	2190	3.3	4.78	12.23	1203	0.86

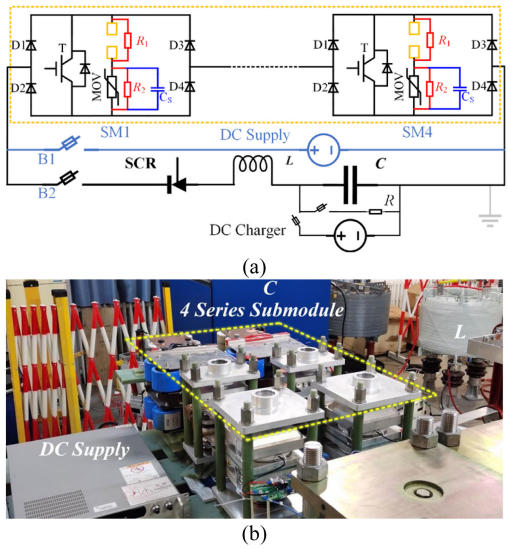

Fig. 14. Experimental Platform. (a) Solid-state switch prototype. (b) The experiment circuit.

range (between 1.5–2.5 kV). The fluctuation of gap breakdown voltage offsets the regulation of R_{off}; that is, under the current contact structure, when breaking large currents, the gap breakdown voltage is not sensitive to R_{off}. After each large current breaking test, we test its static breakdown voltage. In Fig. 13, the maximum static breakdown voltage of the gapped-MOV is 3910 V, and the minimum is 3492 V. The voltage across the MOV is around 1.9 kV. The leakage current could not overheat the MOV.

Each time an SS breaks a large current, the arc will ablate the contact, and various small burrs will be generated on the contact's surface, thereby causing the breakdown voltage to fluctuate. Therefore, when designing a high-voltage SS and determining the required series submodules, the fluctuation of the gap breakdown voltage must be considered, and an appropriate voltage must be selected. In the future, we will cooperate with the manufacturer to put the contact in a vacuum interrupter and continue to optimize it to meet the engineering application standards.

Although the gap breakdown voltage is not sensitive to R_{off}, in this article, we compared the power loss and transient power between 0-t_2 and t_2-t_3 as given in Table II. When the gap breakdown voltage is the same, the power loss during 0-t_2 increases significantly with R_{off}. Considering that the stray inductance of the submodule is very low, during t_2-t_3, the power loss is unchanged, and the voltage spike is only reduced by 115 V. Based on the above analysis, in this article, we can select a smaller turn-OFF resistance, R_{off}, to minimize the loss in t_1-t_2.

In addition, based on the SS module-level testing, as shown in Fig. 13(a), the overvoltage is limited to 4 kV, indicating that C_S and MOV are well-matched. The novel SS's strong surge and turn-OFF ability are also verified. Moreover, the voltage limiting circuit's residual voltage ratio α' is approximately 1.15, which is very low. In engineering applications, α' can be appropriately increased to reduce the current breaking time and the cost of MOVs. The stress on semiconductor devices will also be reduced, thereby further improving turn-OFF reliability.

C. Gap's Lifetime Issue

The lifetime of a gap is the discharge time at a certain current without replacement, such as 1 s/10 kA. In this article and in [7], we show nearly 500 discharge experiment results (0.5–1 ms each). In the laboratory, these gaps have been discharged almost 1000 times, and the performance of these gaps is still good. Nevertheless, we are still exploring the lifetime of these gaps.

Discussing the lifetime of the gaps only is not enough, the lifetime of MSs, the semiconductor devices, and the MOVs together determine CB's lifetime. DC breakers are system protection equipment for breaking pulse fault current; hence, they do not operate frequently. Only based on the power system's needs can the appropriate lifetime be set, but no literature is available for reference. We consulted with several MS manufacturers, and they estimated that in CB operating mode, MSs' discharging lifetime is about hundreds of times (a few milliseconds each).

V. ROBUSTNESS ANALYSIS OF SERIES-CONNECTED GAPPED MOV-C PROTECTION CIRCUITS

The high-voltage SS consists of multiple series-connected submodules. As introduced in Section IV, the gap's breakdown voltage fluctuates. Thus, the robustness of series-connected gapped-MOV-C protection circuits matters.

A. Comprehensive Experimental Platform

Fig. 14(a) presents an SS prototype with four diode bridge submodules. The diode bridge submodule used has been introduced in Section III. Without a sufficient dc power supply system, reproducing the whole current breaking process in the laboratory is difficult. We have to carry out the dc voltage

TABLE III
CIRCUIT PARAMETER DESIGN

MOV	V_{REF}/V_{DC}	2.4 kV/2.0 kV	R_1/R_2	400 k/500 k	
	t_f, I_{pulse}, V_{RES}	8 μs,10 kA, 3.6 kV	C_S	25 μF	
	N_p	2	IEGT	Rated	4.5 kV/2 kA
Gap	V_{gsb}	1.3–2.0 kV		$P_{T\text{-MAX}}$	25 MW
	V_{gpb}	1.5–2.5 kV		k_S/V_{MAX}	0.85/4 kV
LC oscillating circuit		*C*	20.2 mF	*L*	0.2 mH

withstand experiment and large current breaking experiment step by step. The test circuit is shown in Fig. 14(b).

When carrying out the dc voltage withstand experiment, B1 is closed, B2 is opened, and the voltage is slowly increased until the gap breaks down. When carrying out the large-current breaking experiment, B1 is opened, B2 is closed, the capacitor is charged through a dc power supply, and then the thyristor is triggered, causing the fault current to rise. When the current peak is reached, the SS is turned OFF. The circuit parameters are given in Table III.

B. Comprehensive Experimental Platform

When producing a high-voltage CB, instead of connecting all the submodules to form a complete CB and then donging the comprehensive test, some submodules are connected in series to form a medium-voltage unit as 10, 20, or 50 kV. After testing each unit, they are assembled into a high-voltage CB. We only need to discuss the robustness of a medium voltage unit. We tested the robustness of an SS unit that consists of four submodules in the laboratory.

Fig. 15(a) shows the experiment result of the gapped-MOV-RCD-based SS breaking a 10 kA current, and Fig. 15(b) shows the experiment result of the gapped-MOV-C-based SS breaking a 10 kA current. The gap breakdown voltage and breakdown time of the four gaps are different, but the breaking process of the SS remains unaffected.

As mentioned in Section III-C, the loop inductance of the gapped-MOV-RCD-based SS is greater than that of the gapped-MOV-C-based SS. As shown in Fig. 15, the overvoltage of the gapped-MOV-RCD-based SS is higher than that of the gapped-MOV-C-based SS, but the overvoltage is also within the safe range. For large-capacity SS, it needs to turn OFF the pulse current of tens of kA [3], [4], [22]. In this operating condition, the volume of the SS itself is significantly increased. The larger loop stray inductance and larger *di/dt* will cause the SS's overvoltage issue to be very prominent. The advantages of the gapped-MOV-C-based SS with small size and small loop inductance are more obvious in large-capacity SS applications.

For the gapped-MOV-C-based SS, we performed about 200 large current-breaking experiments in the laboratory. After each large current breaking experiment, the dc voltage withstand experiment is carried out. Fig. 15(c) shows that the maximum measured V_{DC} is 15.35 kV, and the voltage utilization efficiency ($V_{DC}/V_{T\text{-rate}}$) increases from 44.4% is 91.8%. Fig. 15(d) shows that the lowest measured V_{DC} is 13.72 kV, and the voltage utilization efficiency is 76.2%. The fluctuation of the static breakdown voltage of the gap is significantly smaller than its transient breakdown voltage. More detailed data are given in Table IV.

TABLE IV
FAULT CURRENT BREAKING EXPERIMENT RESULTS

Static-State Operating Experiment					
(kV)	Total	V_{SM1}	V_{SM2}	V_{SM3}	V_{SM4}
Highest V_{DC}	15.35	4.08	3.71	3.81	3.75
Lowest V_{DC}	13.72	3.47	3.32	3.44	3.39

Large Current Breaking Experiment								
kV / kA	V_{MAX} /Each	$V_{P0\text{-}Vall}$	$V_{P1\text{-}Vall}$	V_{gpb1}	V_{gpb2}	V_{gpb3}	V_{gpb4}	Δt
2.5	12.09/3.02	4.10	3.07	1.72	1.71	2.27	1.69	2.0μs
5	13.53/3.38	4.12	3.27	1.89	1.71	1.60	1.58	3.0μs
10	15.10/3.78	5.96	4.05	1.69	1.51	2.05	1.71	3.0μs

Based on these experiment results, for a four series-connected SS unit, each gap's transient breakdown voltage and static breakdown voltage are different and fluctuate. Still, the range of fluctuation is limited, the voltage utilization efficiency of the device remains above 75%, and the residual voltage ratio α' is 1.15.

Referring to the configuration method in the project, increasing the number of series-connected submodules by 10% and setting a safety factor (e.g., 0.8–0.9) based on the measured lowest dc withstand voltage, the robustness can be improved further. So, series-connected modular gapped MOV circuits have good robustness in high-voltage SSs.

Moreover, we measured some oscillations in the waveform, as shown in Fig. 15(a) and (b). When the gap breaks down, the arc in the gap will cause electromagnetic disturbance to other devices. During testing, relatively fragile and sensitive devices, such as drive boards, power supply systems, and semiconductor devices, work fine with electromagnetic shielding measures. The arc in the gap does not cause electromagnetic interference (EMI) to the devices.

TABLE V
COST AND SIZE ISSUES

Items	Cost (p.u.)	
	Integrated gapped-MOV-C based SS	Gapped-MOV-RCD based SS
Cost of IGBT	1	1
Cost of diodes	0.25×4	0.25×5
Cost of C_S	0.045	0.045
Cost of MOV	0.02	0.02
Cost of gap	0.01	-
Cost of the structure	0.50	0.65
Total cost	2.575	2.965
Size(mm^3)	1000×350×440	1370×350×440

C. Cost and Size Issues

In Table V, compared with the SS with the RCD snubber circuit, the novel scheme uses one less diode and its structural parts. As shown in Figs. 8 and 11, the installation structure of the gap can only use some cheap acrylic insulation structure, which

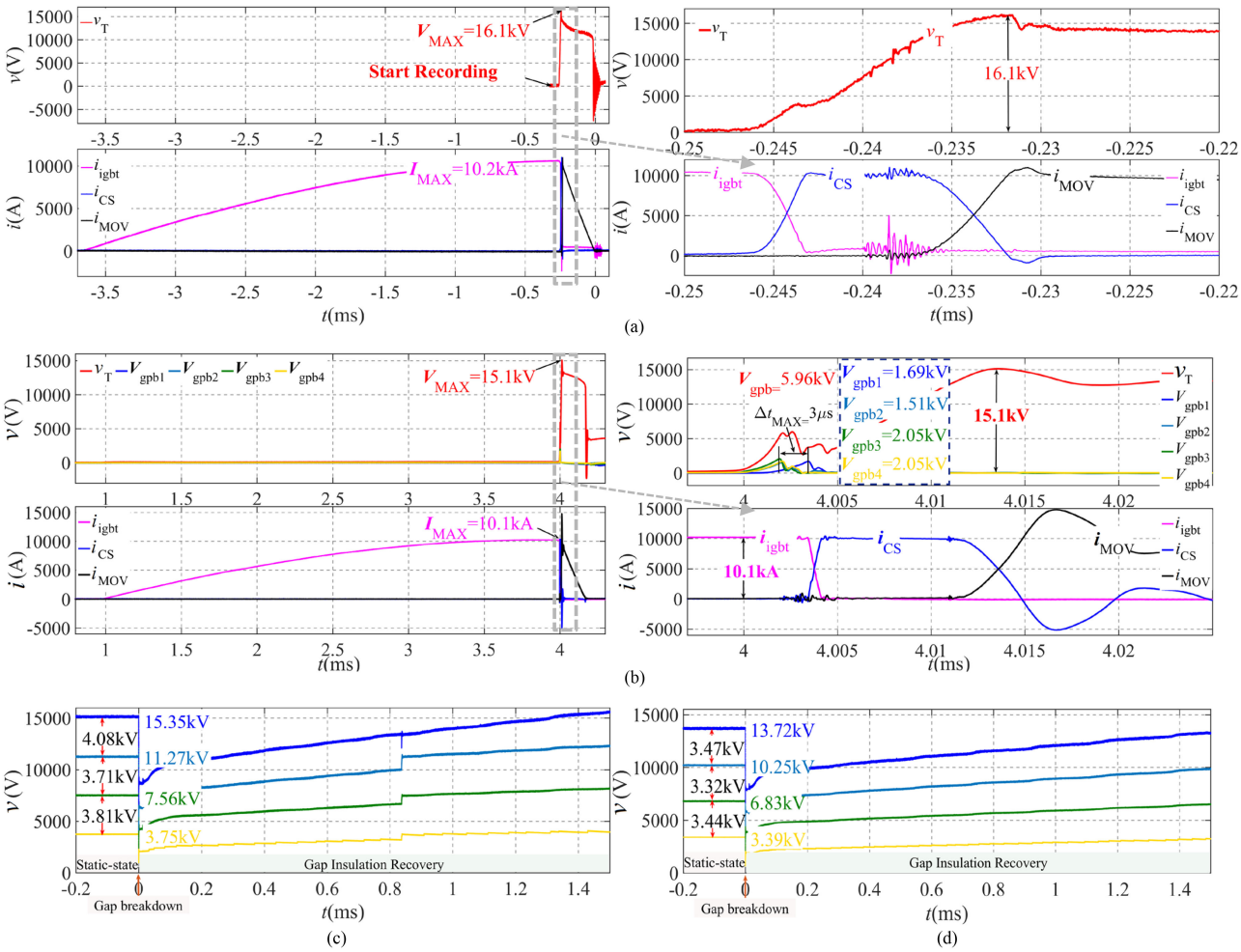

Fig. 15. Experiment results. (a) Experiment result of the gapped-MOV-RCD-based SS breaking a 10 kA current. (b) Experiment result of the gapped-MOV-C-based SS breaking a 10 kA current. (c) The highest measured V_{DC}. (d) Lowest measured V_{DC}.

is much cheaper compared to the high-strength installation structure of the press-fit diode. The gap itself is extremely cheap. In our lab, for the SS prototype, the cost of a single submodule has dropped by 15.1%. In terms of size, the layout length is reduced by 27.0%.

It is not enough to discuss the cost and size of a single submodule. For high-voltage and large-capacity CBs, its SS consists of hundreds of submodules connected in series. The gapped-MOV-C-based SS with small size and small loop inductance, so the effect of reducing the overall cost and size of the CBs will be more significant.

VI. Conclusion

This article proposes a high-efficiency protection circuit that integrates semisoft switching and voltage limiting functions for SSs. After the high fault current is turned OFF, the protection circuit will not resonate with the system, which is convenient for fast reclosing. Compared with the SS with the gapped-MOV-RCD protection circuit, the cost is reduced by 15.1%, and the layout length is reduced by 27.0%. The advantages of the gapped-MOV-C-based SS with small size and small loop inductance are more obvious in large-capacity SS applications. The special and mutually interacting constraints in parameter designs are discussed and obtained experimentally. The parameter design method and the novel SS's strong surge and turn-OFF ability are verified by module-level testing. A SS unit that consists of four series-connected submodules was built, and its robustness is tested for the first time. Experimental results show that series-connected modular gapped MOV circuits have good robustness in high-voltage SSs. Its voltage utilization efficiency remains above 75%, and the residual voltage ratio α' is about 1.15.

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