A Dual-Current-Fed Dual-Active-Bridge DC/DC Converter With High-Frequency Current-Ripple-Friendly Ports

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***Abstract*—The current-fed isolated dc/dc converters are suitable solutions for applications requiring low high-frequency current ripple and convenient current control, such as fuel cells and Li-ion batteries. The existing current-fed isolated dc/dc converters are combined with a current-fed bridge-type terminal and a voltage-fed bridge-type terminal, which can only partially obtain the merits of the current-fed terminals. In this article, a dual-current-fed dual-active-bridge dc/dc converter is proposed with the inductor connection on both terminals. Hence, low high-frequency current ripple and convenient current control can be realized on both sides. Besides, it can also realize the voltage spike suppression without snubber circuits and has the inherent soft-switching operation and voltage boost function. Then, the operation principle, design process, and loss analysis of the proposed converter are presented in detail. The experimental results based on a proof-of-concept laboratory prototype are given to verify the steady-state and dynamic performance of the proposed converter.**

***Index Terms*—Current ripple, current-fed, precharging, snubberless, soft-switching, voltage gain.**

I. Introduction

RENEWABLE energy sources such as fuel cells have operating characteristics, including low dc voltage and huge variability in port voltage. They cannot be integrated into the dc bus directly. To improve the reliability of the fuel cells and provide a constant voltage for the cascaded load, the fuel cells need to use a dc/dc converter with a high voltage gain as a medium to connect to the high-voltage dc bus [1], [2]. Hence, the high voltage gain dc/dc topologies are meaningful in the seamless interface of these renewable energy sources. Besides, since fuel cells lack satisfying dynamic performance, the electric vehicles (EVs) Li-ion batteries are usually utilized as energy buffering sets to recycle the braking/accelerating energy and support for vehicle auxiliary loads [3].

Nevertheless, the EVs Li-ion batteries and fuel cells constantly face troublesome current ripples during power transmission, induced from the interface converter in steady states and transient states, which are the main sources of ripple current [4], [5]. Moreover, the operation performance and the lifetime of fuel cells and Li-ion batteries are affected by high-frequency current ripples on the connected ports. Meanwhile, the high-frequency current ripple also results in the reduction of hydrogen utilization and increment of the mechanical stresses in fuel cells [6], [7]. In the long run, this may accelerate fuel cells degradation. Similarly, the high-frequency current ripple has negative impacts on the battery management system (BMS) of EVs Li-ion batteries and decreases the efficiency. The existing BMS protection mechanisms are ranged between 1 and 10 ms and are unable to achieve voltage protection through timely external blocking of transient overcharge at frequencies above 1 kHz [8]. In addition, many studies have shown that the high-frequency current ripple could trigger the deposition of lithium metal on the surface of the negative electrode and cause capacity degradation even generating an internal short circuit, especially in harsh low-temperature environments [9]. Hence, an interface converter with current-ripple-friendly ports and high voltage gain is meaningful to these renewable energy applications [10].

At present, the isolated dc/dc converters are usually utilized to produce a high step-up voltage by using the isolated transformer with a high turns ratio. The isolated transformer can also provide galvanic isolation for safety considerations [11]. However, increasing the turns ratio will increase the parasitic parameters such as inductance and capacitance, which may aggravate the problem of electromagnetic interference noise. The basic units that make up the isolated dc/dc converters can be classified as voltage-fed terminals and current-fed terminals. Fig. 1 shows the schematic of the single-phase voltage-fed bridge-type terminals and current-fed bridge-type terminals, including full-bridge, half-bridge, *L-L* type, push–pull, etc., [12]. The modulation principle of the voltage-fed terminals is totally different from the current-fed terminals, which results in different requirements of control designs [13]. For example, the short-circuit state must be avoided in the voltage-fed terminals, by contrast, the short-circuit state is necessary for the current-fed terminals and

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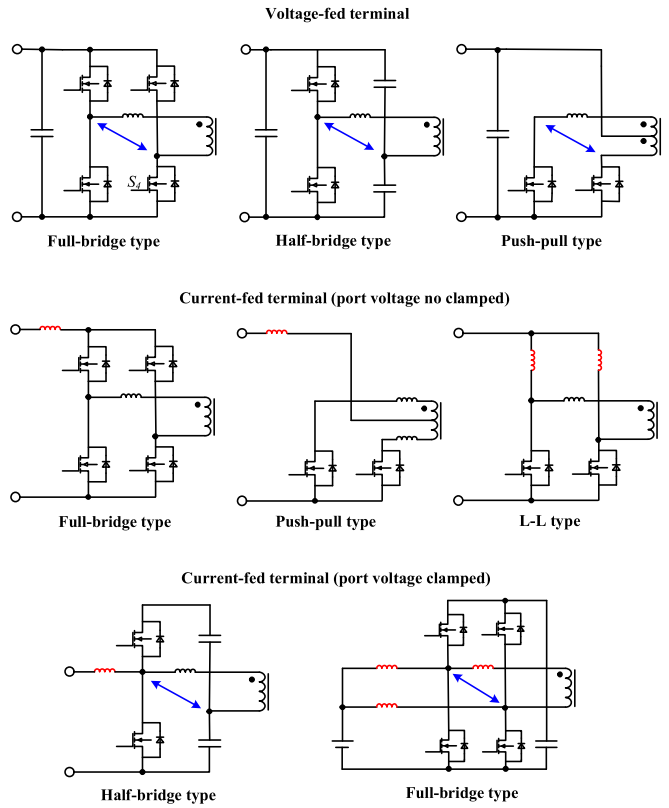


Fig. 1. Schematic of the single-phase voltage-fed bridge-type terminals and current-fed bridge-type terminals. (Blue line: transformer's port voltage is clamped.)

is named "overlap period." Besides, the current-fed terminals have direct input-current control capacity [14]. In contrast, the input current of the voltage-fed terminals is usually controlled indirectly. Note that there is a special case that the current-fed half-bridge terminal proposed in [15] does not need the overlap conduction time of the switches since its port voltage is clamped with the capacitors.

The voltage-fed terminals are not suitable for current-ripple-sensitive applications due to their large high-frequency current ripple. To reduce the current ripple, an additional *LC* filter is required in the voltage-fed terminals, and the power efficiency will be lowered [16], [17]. Besides, the conventional voltage-fed isolated dc/dc converters are not suitable for fuel cell systems since the voltage conversion gain range is limited. Otherwise, zero-voltage-switching (ZVS) may be lost or the nonactive current [18]–[20]. To reduce the current ripple, current-fed isolated dc/dc converters can be good solutions [21]. As boost-type derived topologies, the current-fed configurations can achieve high voltage gain with low transformer turns ratio [22]. In addition, current-fed configurations have several other merits, such as low input-current ripple, inherent short-circuit protection, and direct current control capability [23]. Hence, the current-fed isolated dc/dc converters are promising solutions to renewable energy sources interface converters. At present, the voltage spike suppression and wide soft-switching operation range are two major research focuses of the current-fed bridge-type terminals, limiting the wide applications of the current-fed isolated converters [24]. According to the instantaneous model analysis, the current mismatching between the input-inductor and leakage-inductor will introduce high voltage spikes upon semiconductor devices during turn OFF actions [25]. It is worth mentioning that the current-fed half-bridge terminal has different features. Since its port voltage is clamped to the capacitors, the current-fed half-bridge terminal will not face the voltage spike issue [26]. Another major challenge to the current-fed bridge-type terminals is to increase soft-switching operation range in wide load variation. A variable load may lead to hard switching of the switches and reduce the conversion efficiency [27].

Recently, several new topologies and innovative modulation techniques have been reported in the literature to eliminate the need for traditional snubber circuits. The core concepts of these methods are employed to force the leakage-inductor current to match with the input current for subsequent switching actions by the reflected output voltage [28], [29] or resonance [30]. The current-fed resonant configurations attract lots of investigations. Other than pulsewidth modulation (PWM) converters, current-fed resonant converters utilize transformer nonidealities, circuit parasitic, and resonance tanks to achieve soft-switching of semiconductor devices [31]. In the resonance-pulse current commutation method, the voltage of the switches is clamped through a resonance tank during the overlap period, where resonance occurs for a short duration at turn-OFF causing device current to reduce to zero naturally. Then, the high voltage spike on switching devices can be avoided. However, the resonance-pulse current commutation method will suffer from high-frequency variation under small port voltage fluctuations. The resonance-pulse soft-switching methods, such as quasi-resonant mode, can achieve zero-current-switching (ZCS) of the switching devices [32]. The basic concepts of these methods are all through utilizing the resonance between leakage inductance of the high-frequency transformer (HFTR) and parasitic capacitance of switching devices. Resonance pulse is maintained through a series resonance tank during the overlap conduction time of the switches to facilitate ZCS turn-OFF [33], [34]. However, the above methods realize ZCS in wide load variation at the cost of high voltage stress on switches and duty cycle loss.

Other than the resonant converters, current-fed PWM converters do not need additional resonant circuits. Previously, passive auxiliary circuits, such as inductor snubber, resistor–capacitor–diode snubber, and flyback snubber, are feasible approaches for mitigating voltage spikes [35]. However, passive auxiliary circuits dissipate power through the resistor and compromise the conversion efficiency. Usually, active clamping circuits are easy alternatives to suppress the voltage spike, such as auxiliary inductor snubber, flyback snubber, and active clamping snubber [36]. Nevertheless, additional hardware requires additional floating active devices and hence complex control strategies. Besides, additional hardware may reduce the converter's boost capability or increase the current stress. Hence, modulation-oriented current commutation approaches and modulation-oriented soft-switching approaches avoiding additional hardware or resonance tank attract more attention [37]. The concept of current commutation modulations has been developed to solve the

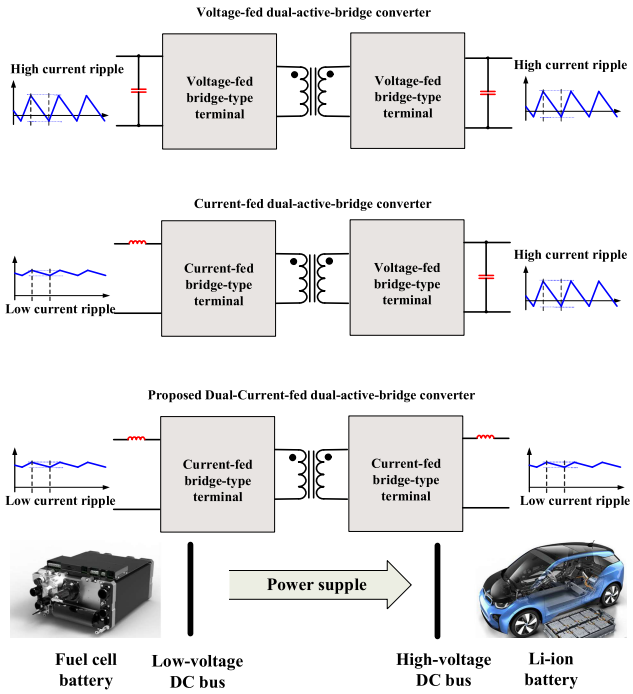


Fig. 2. Schematic of different feed-type DAB converters.

voltage spike issue without auxiliary circuits, such as single-PWM modulation [29] and phase-shift (PS) plus PWM modulation [38]. Meanwhile, some improved soft-switching modulation schemes have been developed by adding additional degrees of freedom, including extended PS, PWM plus PS, and dual-PS. The duty cycles or inner PS angles are controlled by PWM or inner PS operation within the same bridge. Their optimized objectives are to achieve a compromise between low conduction loss and soft-switching operation range under variable port-voltage conditions or different load conditions [39]–[41].

As shown in Fig. 2, the existing current-fed dual-active-bridge (CF-DAB) converters are mainly composed of one current-fed bridge-type terminal and one voltage-fed bridge-type terminal, in which only one port achieves low high-frequency current ripples. To achieve minimum current ripple on both ports, a dual-current-fed dual-active-bridge (DCF-DAB) dc/dc converter is proposed in this article. The DCF-DAB converter has one more inductor-connected port than the conventional CF-DAB converter and provides two current-ripple-friendly ports. This current-ripple-friendly feature is quite important in some current-ripple-sensitive applications. Besides, the inherent boost function makes the topology suitable for high voltage gain applications. Moreover, the voltage spike suppression and wide soft-switching operation range are also realized in the proposed DCF-DAB converter. A precharging technique is utilized to prevent voltage spike at device turn-OFF with low drain–source voltage, and therefore, the use of over-rated components can be avoided. Meanwhile, the proposed converter can realize soft-switching operation even if the input voltage or load is fluctuating while maintaining high efficiency to respect the benefits of low cost, volume, and weight.

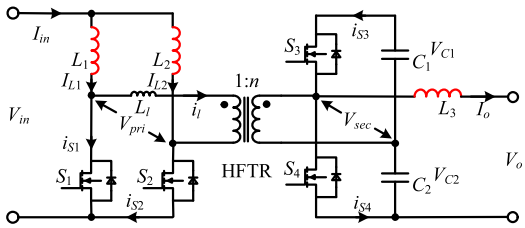


Fig. 3. Schematic of the proposed DCF-DAB dc/dc converter.

The rest of this article is organized as follows. The configuration and brief operation principle of the proposed DCF-DAB dc/dc converter are elaborated in Section II. The precharging technique and soft-switching operations are presented in Section III. The detailed converter analysis following the desired objectives, power loss analysis, and control strategy is given in Section IV. Then, the experimental results of a proof-of-concept laboratory prototype are given in Section V. Finally, conclusions are drawn in Section VI.

II. Configuration and Basic Operation Principle

A. Configuration

Fig. 3 shows the schematic of the proposed DCF-DAB dc/dc converter. $V_{\rm in}$ and V_o are the input voltage and the output voltage. L_1 and L_2 are the input inductors of the current-fed L-L terminal. L_3 and $C_{1\sim2}$ are output-inductor and output capacitors of the current-fed half-bridge terminal, respectively. V_{c1} and V_{c2} are the voltage on the capacitors $C_{1\sim2}$. The HFTR is with a turns ratio of n and leakage inductor L_l. $V_{\rm pri}$ and $V_{\rm sec}$ are the voltages across the primary side and secondary side of the HFTR. $I_{\rm in}$ is the input current. I_{L1}, I_{L2}, I_o, and i_l are the currents through the input inductors L_1 and L_2, output inductor L_3, and leakage inductor L_l, respectively. $i_{\rm s1}$–$i_{\rm s4}$ are the currents through the corresponding switches, and the forward conduction direction is defined as the positive value. The switching frequency, cycle, and equivalent load resistor of the converter are f_s, T_s, and R. This simple topology uses a low count of switching devices $\rm S_1$–$\rm S_4$, and the common ground switches $\rm S_1$–$\rm S_2$ can simplify the driver circuits. The inherent boost function of the current-fed L-L terminal enables the proposed converter to achieve high voltage gain without using a high turns-ratio transformer. Moreover, half-cycle interleaving of the input currents I_{L1} and I_{L2} further reduces the high-frequency current ripple.

B. Basic Operation Principles

Fig. 4 shows the operation principle of the current-fed L-L terminal. The input inductor L_1 works with the diagonal switch $\rm S_2$, while the input inductor L_2 works with the diagonal switch $\rm S_1$, transmitting the energy from the primary side to the secondary side through the HFTR. To avoid a sudden open circuit of the inductor current I_{L1}, the switch $\rm S_1$ should turn ON before the turn-OFF action of the switch $\rm S_2$, providing a fly-wheel loop for the current, and vice versa. The gating signals of $\rm S_1$ and $\rm S_2$ are

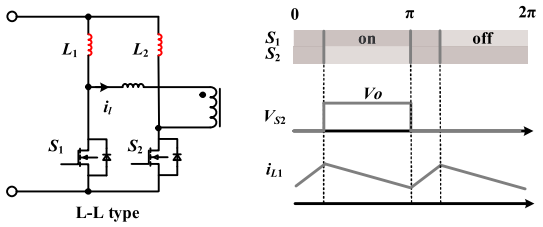


Fig. 4. Operation principle of the current-fed *L-L* terminal.

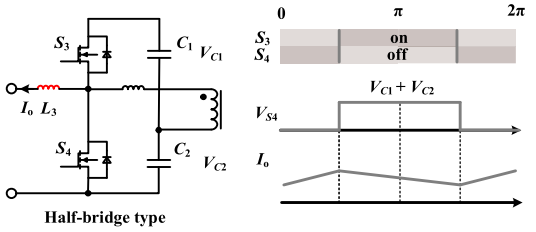


Fig. 5. Operation principle of the current-fed half-bridge terminal.

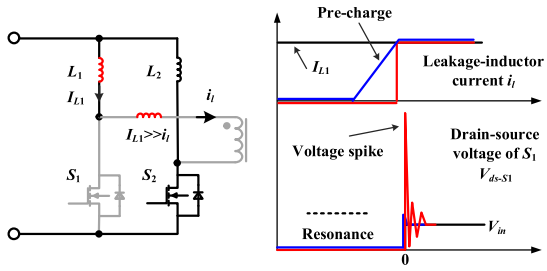


Fig. 6. Generation mechanism of voltage spikes.

phase-shifted by 180° with the same duty cycle *d*, which should be above 0.5.

Fig. 5 shows the operation principle of the current-fed half-bridge terminal, constituting a coupled buck–boost circuit. The duty cycles of the switches S_3–S_4 are the same, defined as d_2. In the proposed DCF-DAB converter, the duty cycle is kept at 0.49, considering the dead time issue. The output capacitors $C_{1\sim2}$ constitute the dc bus of the current-fed half-bridge terminal. The drain–source voltage of the switches is equal to the dc bus voltage during the OFF state.

III. Precharge Technique and Operation Schemes

A. Precharge Technique

When one switch of the current-fed *L-L* terminal turns OFF, there are two kinds of voltage oscillations: resonance $V_{\rm osc}$ and voltage spike $V_{\rm spi}$, as shown in the red line in Fig. 6 [37], [39]. The resonance is related to the inductors (L_1, L_2, and L_l) and the parasitic capacitors of the switches S_1–S_2. The time constant ω of voltage oscillations is presented in (1). The amplitude of resonance can be calculated, as shown in (2). Since the input inductors L_1 and L_2 are far greater than L_l, the maximum voltage caused by resonance is below $2{\cdot}V_{\rm in}$. Since there is usually enough margin of breakdown voltage in the selection of switches, this resonance is tolerable. By contrast, the high voltage spike will damage the switches. Voltage spikes $V_{\rm spi}$ will be caused by the current mismatching between the input inductor and the leakage inductor. The amplitude of voltage spikes is decided by the values of leakage-inductor, parasitic capacitors C_{oss}, time constant ω, and initial currents [I_{L1} (0) and i_l (0)], as presented in (3). It can be observed that the value can be decreased effectively only if the i_l matches I_{L1} at the initial instant. Hence, the key of current matching is to precharge the leakage inductor and commute the i_l to the current I_{L1} in advance, as shown in the blue line in Fig. 6. The major merit of the precharge technique is to eliminate the traditional requirement of a snubber circuit to clamp the device voltage at the turn-OFF moment.

$$\omega = \frac{\sqrt{L_l + L_1}}{\sqrt{2 \cdot C_{oss} \cdot L_l \cdot L_1}} \tag{1}$$

$$V_{\rm spi}|^{I_{L1}(0)=0}_{i_l(0)=0} = \frac{L_1 \cdot V_{\rm in} + \frac{L_l \cdot V_{C1}}{n}}{L_l + L_1} \cdot (1 - \cos(\omega \cdot t)) = V_{\rm in} \cdot (1 - \cos(\omega \cdot t)) \tag{2}$$

$$V_{\rm spi}|^{I_{L1}(0)>0}_{i_l(0)>0} = \frac{(I_{L1}(0) - i_l(0)) \cdot \frac{\sqrt{L_l^3 \cdot L_1} + \sqrt{L_l \cdot L_1^3}}{\sqrt{2 \cdot C_{oss} \cdot (L_l + L_1)}}}{L_l + L_1} \cdot \sin(\omega \cdot t). \tag{3}$$

B. Operation Schemes

Fig. 7 shows the steady-state operation waveforms of the DCF-DAB converter in half-switching cycle. Fig. 8 shows the corresponding equivalent circuits of the DCF-DAB converter. A half-switching cycle contains six states (*a--f*) (t_0–t_6), corresponding to Fig. 7. For the next half-switching cycle, the states are repeated in the same sequence with other symmetrical devices conducting. The state equations are obtained as well as to evaluate the performance of the proposed converter analytically.

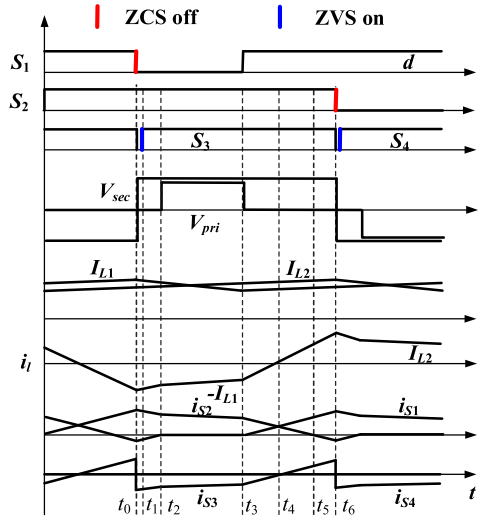


Fig. 7. Steady-state operating waveforms of the proposed DCF-DAB converter.

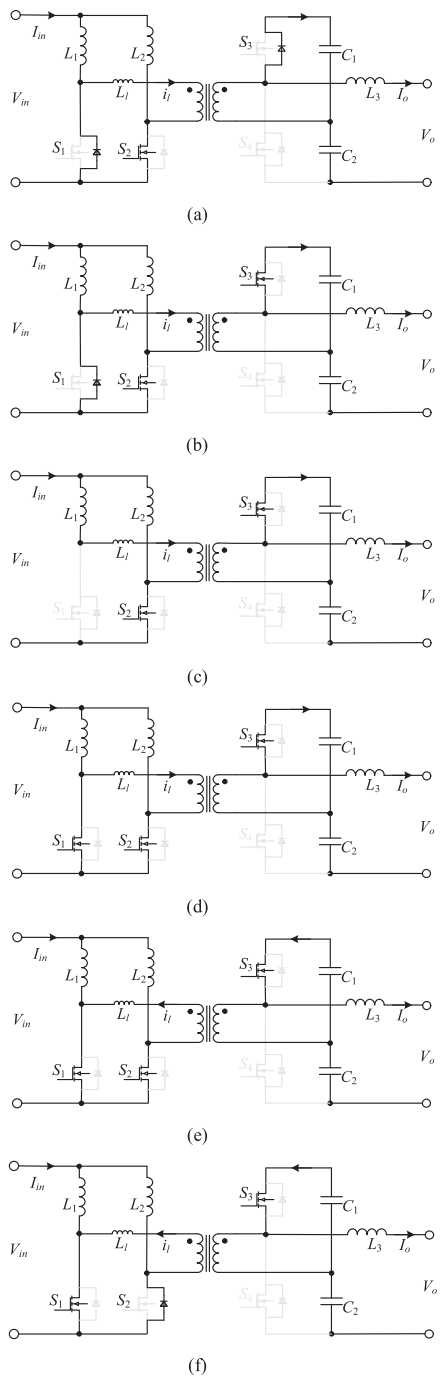


Fig. 8. Operation modes. (a) t_0–t_1. (b) t_1–t_2. (c) t_2–t_3. (d) t_3–t_4. (e) t_4–t_5. (f) t_5–t_6.

For simplifying subsequent analysis, all active components and passive components in the circuits are assumed to be ideal. The power switches, passive components, and voltage sources are nearly ideal without parasitic parameters. The uppercase *I* and lowercase *i* of the current symbol are used to indicate dc and ac, respectively.

State *a* (t_0–t_1): At the instant t_0, the switch S1 turns OFF with ZCS due to the conduction of body diode, and the switch S4 turns OFF with ZVS by its parasitic capacitor. During this state, the switch S3 and the switch S4 both keep a turn-OFF state for the dead time. The secondary-side current flows through the body diode of switch S3. Equation (4) presents the rule for ZCS-OFF of the primary-side switches S1∼2 and ZVS-ON of the secondary-side switches S3∼4. The leakage-inductor current $i_{l,}$ should be greater than the corresponding input current to ensure the conduction of body diodes of primary-side switches S1 and S2 at the turn-OFF moment.

$$\begin{cases} i_l(t_0) > I_{L1}(t_0) \;\; S_1\,\mathrm{ZCS-off}\;\; S_3\,\mathrm{ZVS-on} \\ i_l(t_6) > I_{L2}(t_6) \;\; S_2\,\mathrm{ZCS-off}\;\; S_4\,\mathrm{ZVS-on} \end{cases}. \tag{4}$$

State *b* (t_1–t_2): At the instant t_1, the switch S3 turns ON with ZVS due to the conduction of the body diode and works in synchronous rectification mode. The input energy is transferred to the output side, and the capacitor C_1 is charged. The voltages applied on both sides of the transformer determine the flow direction and amplitude of the leakage-inductor current i_l collectively. Hence, the current through the body diode of the switch S1 decreases linearly. The state equations in this state are expressed as follows:

$$i_l = \left(V_{\mathrm{in}} - L_1 \cdot \frac{dI_{L1}}{dt} - \frac{L_3 \cdot \frac{dI_o}{dt} + V_o}{n}\right) \cdot \frac{(t-t_1)}{L_l} \tag{5}$$

$$I_{\mathrm{in}} = I_{L1} + I_{L2} \tag{6}$$

$$i_{\mathrm{S1}} = I_{L1} - i_l \tag{7}$$

$$i_{\mathrm{S2}} = I_{L2} + i_l. \tag{8}$$

State *c* (t_2–t_3): At the instant t_2, the current through the body diode of the switch S_1 reaches zero, and the current through the switch S_2 equals the input current I_{in} during this state. The current continuous path of the inductor L_1 changes from the switch S_1 to the switch S_2. The input energy is transferred to the output side. The state equations in this state are expressed as follows:

$$i_l = I_{L1} = V_{\mathrm{in}} - L_1 \cdot \frac{dI_{L1}}{dt} \tag{9}$$

$$i_{\mathrm{S3}} = \frac{i_l}{n} - I_o. \tag{10}$$

State *d* (t_3–t_4): At the instant t_3, the switch S_1 turns ON with ZCS due to the constant input current maintained by the inductors. Switches S_1–S_2 keep conducting to provide a continuous path for input current during this state. The leakage-inductor *Ll* transfers stored energy to the output side. The voltage on the capacitor C_1 is reflected on the leakage-inductor L_l. The leakage-inductor current i_l decreases linearly and reaches zero at the instant t_4. Meanwhile, the current through the switch S1 equals the current through the switch S2 at the instant t_4. The state equations in this state are expressed as follows:

$$i_l = I_{L1} - \left(\frac{L_3 \cdot \frac{dI_o}{dt} + V_o}{n}\right) \cdot \frac{(t-t_3)}{L_l} \tag{11}$$

$$i_{\mathrm{S1}} = I_{L1} - i_l \tag{12}$$

$$i_{\mathrm{S2}} = I_{L2} + i_l. \tag{13}$$

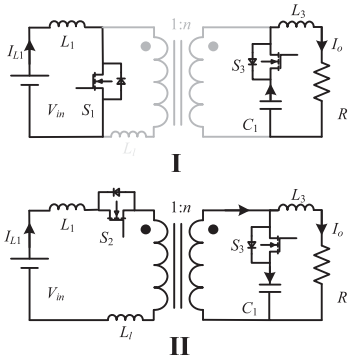


Fig. 9. Equivalent circuits of the proposed DCF-DAB dc/dc converter. (I) Power storage period ($t_n < t < T_s{}^*d$). (II) Power transmission period ($t_n + T_s{*}d < t < t_{n+1}$).

State *e* (t_4–t_5): The energy stored in the capacitor C_1 is utilized to precharge the leakage-inductor L_l. The leakage-inductor current i_l keeps increasing from zero with the same slope as State *d* and reaches the current I_{L2} at the instant t_5. The state equations in this state are expressed as follows:

$$i_l = \left(\frac{L_3 \cdot \frac{dI_o}{dt} + V_o}{n}\right) \cdot \frac{(t - t_4)}{L_l} \tag{14}$$

$$i_{s1} = I_{L1} + i_l \tag{15}$$

$$i_{s2} = I_{L2} - i_l. \tag{16}$$

State *f* (t_5–t_6): The leakage-inductor current i_l continues increasing and reaches the peak value at the instant t_6. The switch S_2 turns OFF with ZCS due to the conduction of the body diode, and the switch S_3 turns OFF with ZVS by its parasitic capacitor. Meanwhile, the secondary-side current changes its conducting path from the switch S_3 to the body diode of switch S_4. The state equations in this state are expressed as follows:

$$i_l = I_{L2} + \left(\frac{L_3 \cdot \frac{dI_o}{dt} + V_o}{n}\right) \cdot \frac{(t - t_5)}{L_l}. \tag{17}$$

IV. Converter Analysis

In this section, converter parameters are derived based on the design considerations. The converter analysis is done to obtain the design equations to determine or calculate the components' ratings and power losses as well as to obtain the converter's performance theoretically.

A. Voltage Gain and Power Range of the Proposed Converter

The proposed DCF-DAB dc/dc converter is a boost-type isolated dc/dc converter. Its equivalent circuit can be simplified as shown in Fig. 9 in a half-switching cycle. Fig. 10 presents the current variation ΔI of the input inductor L_1. The minimum value and maximum value of the current happen at the end of the transmission period and the storage period separately. The current variation ΔI is related to inductor value, voltage level, and load conditions. According to the equivalent circuits,

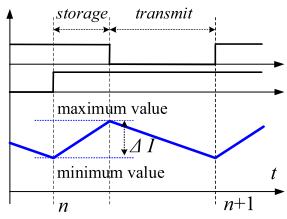


Fig. 10. Current variation ΔI of the input inductor L_1.

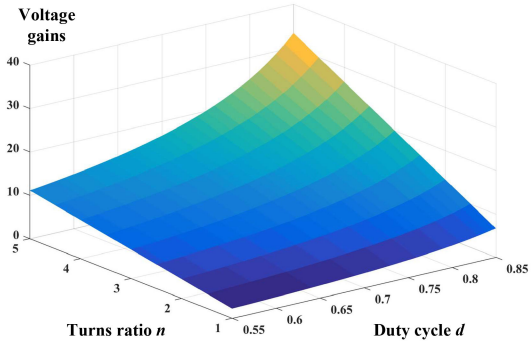


Fig. 11. Converter voltage gain variation for different turns ratio *n* of HFTR and duty cycle *d*.

the state equations and changes of inductor current I_{L1} can be presented as (18) and (19) during the *n*th switching cycle. t_n and $t_{(n+1)}$ are the start moments of *n*th and (*n*+1)th switching cycles, and $I_{L1}(n)$ and $I_{L1}(n+1)$ are the inductor currents at the corresponding moments, respectively. i_{L1} is the instantaneous inductor current. Equation (19) can further be derived into (20). When operating at steady state, the inductor current should be the same at the t_n and $t_{(n+1)}$ moments to avoid dc bias, as present in (21). Hence, combining (20) and (21), the voltage conversion ratio of the proposed DCF-DAB converter can be derived as (22). Fig. 11 presents the converter voltage gain variation of the proposed converter for different duty cycle *d* and turns ratio *n* of HFTR. The proposed converter demonstrates an excellent voltage-boost potential.

$$\begin{cases} L_1 \cdot \frac{di_{L1}}{dt} = V_{\text{in}} & t_n \le t \le t_n + T_s \cdot d \\ L_1 \cdot \frac{di_{L1}}{dt} = V_{\text{in}} - \frac{V_o}{n} & t_n + T_s \cdot d \le t \le t_{n+1} \end{cases} \tag{18}$$

$$\int_{I_{L1}(n)}^{I_{L1}(n+1)} di_{L1} = \frac{1}{L_1} \cdot \left(\int_{t_n}^{t_n + T_s \cdot d} V_{\text{in}} dt + \int_{t_n + T_s \cdot d}^{t_{n+1}} \left(V_{\text{in}} - \frac{V_o}{n} \right) dt \right) \tag{19}$$

$$\int_{I_{L1}(n)}^{I_{L1}(n+1)} di_{L1} = \frac{1}{L_1} \cdot \left(V_{\text{in}} \cdot d \cdot T_s + \left(V_{\text{in}} - \frac{V_o}{n} \right) \cdot \times (1 - d) \cdot T_s \right) \tag{20}$$

$$\int_{I_{L1}(n)}^{I_{L1}(n+1)} di_{L1} = I_{L1}(n+1) - I_{L1}(n) = 0 \tag{21}$$

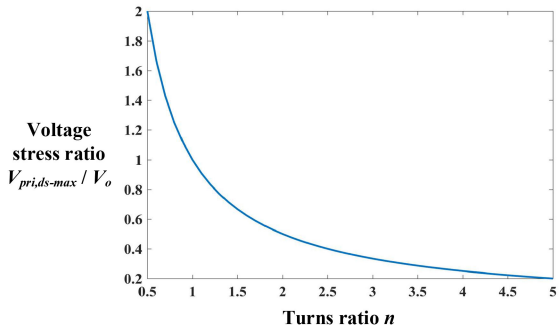


Fig. 12. Ratio variation of voltage across switches S_1–S_2 against output voltage for different turns ratio n of HFTR.

$$V_o = \frac{n \cdot V_{\text{in}}}{1-d}. \tag{22}$$

When the conduction time ($2{*}d^{*}{*}T_s$) of body diodes of switches $S_{1\sim2}$ is no longer negligible, the voltage gain will be coupled with output power P by the leakage inductor. The value of d^* is expressed in (23), and the equivalent duty cycle equals d plus d^*. Hence, a more accurate expression of output voltage can be given in (24), considering the leakage inductor. Fortunately, with a suitable design of leakage inductor, such as adding a series inductor, the duration of d^* can be ignored.

$$d* = d - 0.5 - \frac{n \cdot I_{L1} \cdot L_l}{V_o \cdot T_s} \tag{23}$$

$$V_o = \frac{n \cdot V_{\text{in}}}{1-(d+d^*)} = \frac{2 \cdot n \cdot (V_{\text{in}}^2 - L_l \cdot f_s \cdot P)}{(3-4 \cdot d) \cdot V_{\text{in}}}. \tag{24}$$

To ensure enough precharging time for the leakage-inductor current before the turn-OFF moment of switches $S_{1\sim2}$, (25) and (26) should be satisfied. The symbol P presents the output power. Meanwhile, the minimal value of the output capacitors C_1–C_2 for precharging the leakage inductor is given as (27) and (28). The symbol V_{ripple} presents the maximum allowable value of output voltage harmonics. Hence, the constraint of the maximum output power can be presented in (29).

$$\frac{L_l \cdot L_{L1}}{(d-0.5) \cdot T_s} \le \frac{V_o}{n} \tag{25}$$

$$P \le \frac{V_o \cdot (d-0.5) \cdot V_{\text{in}}}{n \cdot L_l \cdot f_s} \tag{26}$$

$$\frac{C_1 \cdot V_O^2}{2} - \frac{C_1 \cdot (V_o - V_{\text{ripple}})^2}{2} \ge P \cdot T_s \tag{27}$$

$$P \le C_1 \cdot f_s \cdot V_o \cdot V_{\text{ripple}} \tag{28}$$

$$P \le \min\left(C_1 \cdot f_s \cdot V_o \cdot V_{\text{ripple}}, \frac{V_o \cdot (d-0.5) \cdot V_m}{n \cdot L_l \cdot f_s}\right). \tag{29}$$

B. Component Stresses

1) Voltage Stress: The maximum voltages across the primary-side *L-L* bridge switches S_1–S_2, the secondary-side current-fed half-bridge bridge switches S_3–S_4, and capacitors C_1–C_2 are given in (30). Fig. 12 presents the ratio variation of voltage across switches S_1–S_2 against output voltage for different turns ratio n of HFTR.

$$\begin{aligned} V_{\text{pri},ds-\max} &= \frac{V_o}{n} \\ V_{\text{sec},ds-\max} &= 2 \cdot V_o \\ V_{\text{sec,cap}-\max} &= V_o. \end{aligned} \tag{30}$$

TABLE I
CURRENT EXPRESSIONS

Items	Expressions
$I_{l,RMS}$	$I_{in} \cdot \sqrt{\frac{5-4 \cdot d}{12}}$
$I_{Pri,RMS}$	$I_{in} \cdot \sqrt{\frac{2-d}{3}}$
$I_{Pri,peak}$	$\frac{4 \cdot V_{in} \cdot (d-0.5) - I_{in} \cdot L_l \cdot f_s}{4 \cdot L_l \cdot f_s}$
$I_{Sec,RMS}$	$\frac{I_{in}}{n} \cdot \sqrt{\frac{5-4 \cdot d}{24}}$
$I_{Sec,peak}$	$\frac{4 \cdot V_{in} \cdot (d-0.5) - I_{in} \cdot L_l \cdot f_s}{4 \cdot n \cdot L_l \cdot f_s}$

2) Current Stress: Current stresses on various switching devices and the transformer are determined by peak current and root-mean-square (RMS) current flowing through them which predominantly depends on various converter parameters as governed by the following expressions. Table I presents the expressions of RMS current through leakage-inductor $I_{l,\text{RMS}}$, RMS current through primary-side switches $I_{\text{Pri,RMS}}$ and secondary-side switches $I_{\text{Sec,RMS}}$, and peak current through primary-side switches $I_{\text{Pri,peak}}$ and secondary-side switches $I_{\text{Sec,peak}}$.

C. Passive Component Selection

The minimal value of the input inductors L_1–L_2 is given as (31). The symbol $i_{\text{in,ripple}}$ presents the maximum allowable value of input current ripples.

$$L_{1,\min} = \frac{d \cdot V_{\text{in}}}{i_{\text{in,ripple}} \cdot f_s}. \tag{31}$$

The minimal value of the output inductor L_3 is given as (32). The symbol $i_{\text{out,ripple}}$ presents the maximum allowable value of output current ripples.

$$L_{3,\min} = \frac{(1-d) \cdot V_o}{i_{\text{out,ripple}} \cdot f_s}. \tag{32}$$

The optimized value of the leakage inductor plus series inductor is given by

$$L_l = \frac{(d-0.5) \cdot V_o}{n \cdot f_s \cdot I_{\text{in}}}. \tag{33}$$

The minimal value of the output capacitors C_1–C_2 is given as

$$C_1 = \frac{P}{f_s \cdot V_o \cdot V_{\text{ripple}}}. \tag{34}$$

D. Power Losses

The total conduction losses including primary-side switches $P_{\text{Pri,con}}$ and secondary-side switches $P_{\text{Sec,con}}$ are presented in (35), where r_{Pri} and r_{Sec} are the corresponding ON-state resistances, respectively. The proportion of conduction loss of body diodes in $P_{\text{Sec,con}}$ can be ignored, owing to the synchronous rectification instead of body diodes.

$$P_{\text{con}} = P_{\text{Pri,con}} + P_{\text{Sec,con}} = r_{\text{Pri}} \cdot I^2_{\text{Pri},s,\text{RMS}} + r_{\text{Sec}} \cdot I^2_{\text{Sec},s,\text{RMS}}. \tag{35}$$

The switching losses of primary-side and secondary-side switches consist of turn-ON loss P_{on} and turn-OFF loss P_{off}, listed in (36) and (37). The turn-OFF loss of primary-side switches can be ignored owing to the realization of ZCS, and the turn-ON loss of secondary-side switches can be ignored benefitting from the realization of ZVS. $C_{\text{Pri},oss}$ and $C_{\text{Sec},oss}$ are the output capacitances of primary-side and secondary-side switches, respectively. t_f is the turn-OFF time of secondary-side switches. I_{off} is the current through secondary-side switches at the turn-OFF moment.

$$P_{\text{Pri,sw}} = P_{\text{on}} + P_{\text{off}} = \frac{C_{\text{Pri},oss} \cdot V_o^2 \cdot f_s}{n^2} + 0 \tag{36}$$

$$P_{\text{Sec,sw}} = P_{\text{on}} + P_{\text{off}} = 0 + \frac{I^2_{\text{off}} \cdot t_f^2 \cdot f_s}{24 \cdot C_{\text{Sec},oss}}. \tag{37}$$

The total conduction loss of input inductors $P_{L\text{in}}$ is given by (38), r_{L1} is the ON-state resistance of input inductors. The total loss of HFTR consists of copper loss P_{cop} and core loss P_{core}. R_{ac} and R_{dc} are the winding ac resistance and dc resistance, respectively. P_L, A_e, and L_e are the core loss density (W/mm^3), effective core cross-sectional area (mm^2), and effective core magnetic path length (mm), respectively [16].

$$P_{L\text{in}} = \frac{r_{L1} \cdot I^2_{\text{in}}}{2} \tag{38}$$

$$P_{\text{cop}} = I^2_{l,\text{RMS}} \cdot (R_{\text{dc}} + R_{\text{ac}}) \tag{39}$$

$$P_{\text{core}} = P_L \cdot A_e \cdot L_e. \tag{40}$$

E. Control Strategy and Small-Signal Analysis

The control block diagram for the proposed DCF-DAB converter is shown in Fig. 13. A dual closed-loop controller is employed to achieve excellent dynamic performance. It consists of an outer voltage loop and an inner current loop with the direct input-current control capacity. At the beginning of each sampling or control interval, the control system should sample the output voltage V_o, input current I_{in}, and the output current I_o. The control objection of the outer voltage loop is set as the desired output voltage $V_{o,\text{ref}}$. The reference input current $I_{\text{in,ref}}$ can be generated from the PI controller of the output voltage loop. Then, the suitable duty cycle d can be generated from the PI controller of the inner current loop. The driving signals

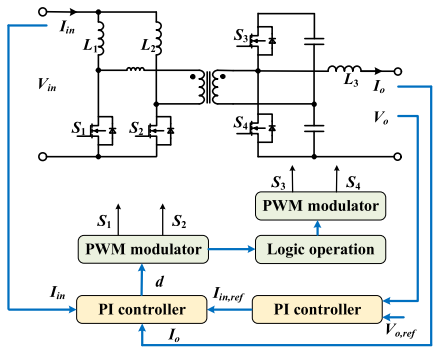


Fig. 13. Control structure of the proposed DCF-DAB converter.

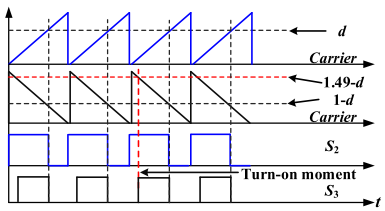


Fig. 14. Logic operation block.

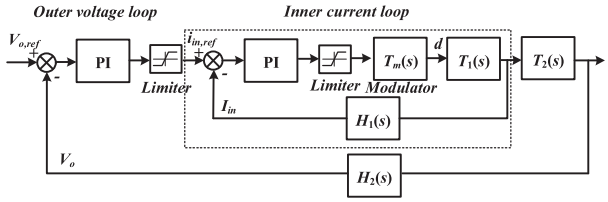


Fig. 15. Schematic diagram of a dual closed-loop controller.

of the switches $S_{3\sim4}$ can be derived from the logic operation block according to the duty cycle d, as shown in Fig. 14. The turn-OFF moment of the switch S_3 is the same as the switch S_2, and the duty cycle of the switches $S_{3\sim4}$ is fixed at 0.49. Hence, the turn-ON moments of the switches $S_{3\sim4}$ can be obtained.

The schematic diagram of dual closed-loop controller (outer voltage loop and inner current loop) is presented in Fig. 15. Since the gain and delay of the analog-to-digital conversion in the digital controller can be neglected, the current feedback gain $H_1(s)$ and voltage feedback gain $H_2(s)$ are set to 1. The PWM blocks serve as the modulator ($T_m(s) = 1$). Symbols K_{p1} and K_{p2} are the proportionality coefficients (1 and 10) of the inner current loop and outer voltage loop separately. Symbols K_{i1} and K_{i2} are the integration coefficients (500 and 500). The specific parameters of the model are the same as the prototype in the next section.

Due to the volt-second balance of the leakage inductor in the steady state, the average voltage value in one switching cycle is zero, as presented in (41). Therefore, the state variable i_{leak} can be omitted for the following analysis. The averaged state equations of input inductor L_1 and output capacitor C_1 in one

switching cycle are given in (42) based on Kirchhoff's law.

$$\int_0^{T_s}\left(L_l\cdot\frac{di_l}{dt}\right)\cdot dt=0 \tag{41}$$

$$\begin{cases}\int_0^{T_s}\left(L_1\cdot\frac{dI_{\text{in}}}{dt}\right)\cdot dt=\left(V_{\text{in}}-2\cdot(1-d)\cdot\frac{V_o}{2\cdot n}\right)\cdot T_s\\ \int_0^{T_s}\left(C_1\cdot\frac{dV_{C1}}{dt}\right)\cdot dt=\left(2\cdot(1-d)\cdot\frac{I_{\text{in}}}{2\cdot n}-\frac{V_o}{R}\right)\cdot T_s\end{cases}. \tag{42}$$

Perturbation is introduced into the variables around the steady-state point as shown in (43). High-order product and dc terms can be ignored for simplifying expression in (44).

$$\begin{cases}L_1\cdot\frac{d(I_{\text{in}}+\hat{I}_{\text{in}})}{dt}=(V_{\text{in}}+\hat{V}_{\text{in}})-2\cdot(1-(d+\hat{d}))\cdot\frac{(V_o+\hat{V}_o)}{2\cdot n}\\ C_1\cdot\frac{d(V_{C1}+\hat{V}_{C1})}{dt}=2\cdot(1-(d+\hat{d}))\cdot\frac{(I_{\text{in}}+\hat{I}_{\text{in}})}{2\cdot n}-\frac{(V_o+\hat{V}_o)}{R}\end{cases} \tag{43}$$

$$\begin{cases}L_1\cdot\frac{d(\widehat{I_{\text{in}}})}{dt}=\widehat{V_{\text{in}}}-2\cdot(1-d)\cdot\frac{\widehat{V_o}}{2\cdot n}-2\cdot(-\widehat{d})\cdot\frac{V_o}{2\cdot n}\\ C_1\cdot\frac{d(\widehat{V_{C1}})}{dt}=2\cdot(1-d)\cdot\frac{\widehat{I_{\text{in}}}}{2\cdot n}+2\cdot(-\widehat{d})\cdot\frac{I_{\text{in}}}{2\cdot n}-\frac{\widehat{V_o}}{R}\end{cases}. \tag{44}$$

Then, through the Laplace transform, (44) is transferred into the following:

$$\begin{cases}L_1\cdot s\cdot\widehat{I_{\text{in}}}(s)+\frac{(1-d)}{n}\cdot\widehat{V_o}(s)=\frac{V_o}{n}\cdot\widehat{d}(s)+\widehat{V_{\text{in}}}(s)\\ \frac{(1-d)}{n}\cdot\widehat{I_{\text{in}}}(s)-\left(\frac{C_1\cdot s}{2}+\frac{1}{R}\right)\cdot\widehat{V_o}(s)=\frac{I_{\text{in}}}{n}\cdot\widehat{d}(s)\end{cases}. \tag{45}$$

The state equations of the DCF-DAB dc/dc converter can also be rewritten to the matrix form as (46)–(50).

$$\begin{bmatrix}\widehat{I_{\text{in}}}(s)\\ \widehat{I_o}(s)\end{bmatrix}=[A(s)]\cdot\begin{bmatrix}b_1\\ b_2\end{bmatrix}\cdot\widehat{d}(s)+[A(s)]\begin{bmatrix}1\\ 0\end{bmatrix}\widehat{V_{\text{in}}}(s) \tag{46}$$

$$A(s)=\begin{bmatrix}L_1\cdot s & \frac{1-d}{n}\\ \frac{1-d}{n} & -\left(\frac{C_1\cdot s}{2}+\frac{1}{R}\right)\end{bmatrix}^{-1}=\frac{1}{|A(s)|}\cdot\begin{bmatrix}A_{11} & A_{12}\\ A_{21} & A_{22}\end{bmatrix} \tag{47}$$

$$\begin{cases}b_1=\frac{V_o}{n}\\ b_2=\frac{I_{\text{in}}}{n}\end{cases} \tag{48}$$

$$\begin{cases}A_{11}=-\left(\frac{C_1\cdot s}{2}+\frac{1}{R}\right)\\ A_{12}=-\frac{(1-d)}{n}\\ A_{21}=-\frac{(1-d)}{n}\\ A_{22}=L_1\cdot s\end{cases} \tag{49}$$

$$|A(s)|=-\frac{L_1\cdot C_1}{2}\cdot s^2-\frac{L_1}{R}\cdot s-\frac{(1-d)^2}{n^2}. \tag{50}$$

The control-to-current transfer function is given as (51) and (52) by setting the perturbation of input voltage to zero. Equation (53) gives the transfer function $T_{\text{inner}}(s)$ of the inner loop.

$$T_1(s)=\frac{\hat{I}_{\text{in}}(s)}{\hat{d}(s)}=\frac{1}{|A(s)|}\cdot\begin{bmatrix}A_{11} & A_{12}\end{bmatrix}\cdot\begin{bmatrix}b_1\\ b_2\end{bmatrix} \tag{51}$$

$$\frac{\hat{I}_{\text{in}}(s)}{\hat{d}(s)}=\frac{-\frac{C_1\cdot V_o}{2\cdot n}\cdot s-\frac{V_o}{R\cdot n}-\frac{(1-d)\cdot I_{\text{in}}}{n^2}}{-\frac{L_1\cdot C_1}{2}\cdot s^2-\frac{L_1}{R}\cdot s-\frac{(1-d)^2}{n^2}} \tag{52}$$

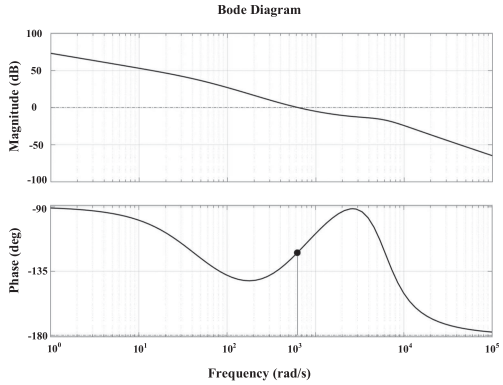


Fig. 16. Bode plot.

$$T_{\text{inner}}(s)=\left(K_{p1}+K_{i1}\cdot\frac{1}{s}\right)\cdot T_m(s)\cdot T_1(s)\cdot H_1(s). \tag{53}$$

The outer voltage loop enables the output voltage to track the reference value by adjusting the inner current reference. Since the inner current loop has faster dynamics, its dynamics can be neglected during the design of the outer voltage loop. The perturbation of the duty cycle can be neglected. Therefore, the current-to-voltage transfer function T_2(s) is obtained as (54) and (55) derived from (45). Equation (56) gives the transfer function $T_{\text{outer}}(s)$ of the outer voltage loop.

$$\frac{(1-d)=}{n}\cdot\hat{I}_{\text{in}}(s)-\left(\frac{C_1\cdot s}{2}+\frac{1}{R}\right)\cdot\hat{V}_o(s)=0 \tag{54}$$

$$T_2(s)=\frac{\hat{V}_o(s)}{\hat{I}_{\text{in}}(s)}=\frac{\frac{(1-d)}{n}}{\left(\frac{C_1\cdot s}{2}+\frac{1}{R}\right)} \tag{55}$$

$$T_{\text{outer}}(s)=\left(K_{p2}+K_{i2}\cdot\frac{1}{s}\right)\cdot T_2(s)\cdot H_2(s). \tag{56}$$

Then, the transfer function $T_{\text{system}}(s)$ of the dual closed-loop controller can be obtained as (57). The Bode plot of the converter can be drawn in Fig. 16. The dual closed-loop controller has a phase margin of 55° at the crossing frequency of 600 rad/s, introducing a fast-dynamic response and robust stability against input disturbances. Meanwhile, the limited steady-state error is realized by the high gain margin in the low-frequency range.

$$T_{\text{system}}(s)=\frac{\left(K_{p1}+K_{i1}\cdot\frac{1}{s}\right)\cdot T_m(s)\cdot T_1(s)}{1+T_{\text{inner}}(s)}\cdot T_{\text{outer}}(s). \tag{57}$$

V. Experimental Verification

A proof-of-concept laboratory prototype is developed, as shown in Fig. 17. The circuit parameters and components list of the laboratory prototype are listed in Tables II and III separately. Then, detailed experimental results are presented to demonstrate the performance of the proposed converter.

Fig. 18 shows the zoomed-in experimental waveforms to verify the effects of the precharging of the leakage-inductor under

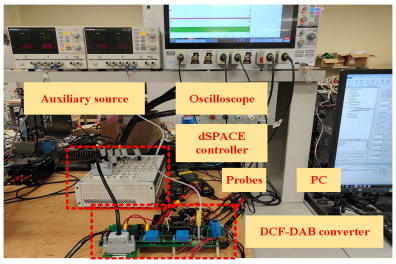


Fig. 17. Photograph of the proof-of-concept laboratory prototype.

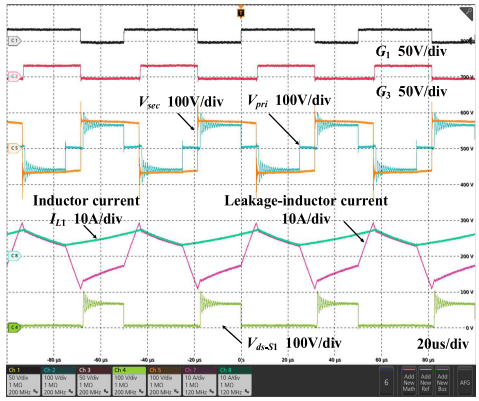
TABLE II
CIRCUIT PARAMETERS

Items	Value
Switching frequency f_s	20 kHz
Input voltage V_{in}	15–45 V
Output voltage V_o	65–100 V
Rating output power P	250 W
Input inductors $L_{1\sim2}$	250 μH
Output inductor L_3	2 mH
Capacitors $C_{1\sim2}$	220 μF
HFTR turns ratio n	1:1
Series leakage-inductor value L_l	30 μH

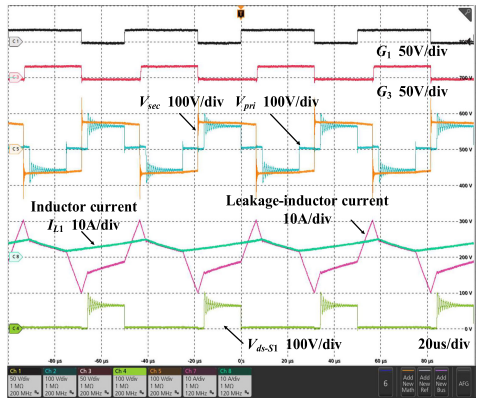
TABLE III
COMPONENTS LIST

Items	Value
MOSFETs S_1–S_4	S_1–S_2: Infineon IPP110N20NA S_3–S_4: Infineon IPP200N25N3
Digital controller	dSPACE MicroLabBox DS1202
Gate drivers	CREE CGD15SG00D2
Voltage/ Current sample devices	LEM LV25/LA25
HFTR	EE55 Ferrite material

different load conditions. When the converter works at full-load or half-load conditions, the experiment results can be shown in Fig. 18(a) and (b). G_1 and G_3 are the driving signals of S_1 and S_3. In Fig. 18(a), the leakage-inductor current is precharged to the value of input current at the turn-OFF moment of the switch S_1. Hence, when the output voltage is 70 V, the drain–source voltage $V_{\text{ds-S1}}$ of the switch S_1 is 70 V, and the maximum value is below 100 V. The same effect can also be achieved in Fig. 18(b). The precharging of the leakage-inductor can avoid the voltage spike on the switching devices under different load conditions. By this method, the primary-side switching devices will not suffer high temporary voltage spikes during the transition, ensuring the safe operation of switches. It allows for avoiding overrated switching devices and brings in higher conversion efficiency over the wide



(a)

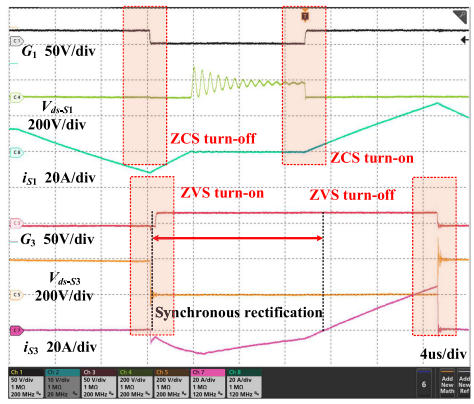


(b)

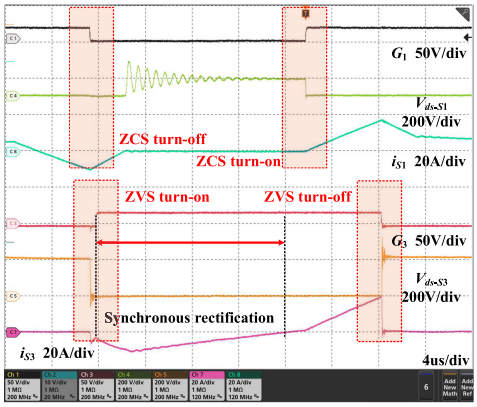
Fig. 18. Zoomed-in experimental waveforms for precharging of the leakage-inductor. (a) Full load. (b) Half load.

load range operation of the proposed topology. The experimental results are consistent with the principle in Section III-A.

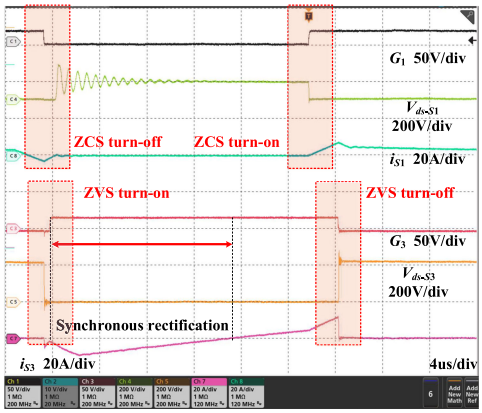
Fig. 19 shows the experimental waveforms of soft-switching and synchronous rectification under different voltage gain conditions (three times input-voltage fluctuation at full-load condition). When the converter works at the 15–100 V condition, the experiment results can be shown in Fig. 19(a), and the experiment results at 30–100 V and 45–100 V conditions are shown in Fig. 19(b)–(c). In Fig. 19(a), the soft-switching operations are highlighted in the red shaded area. It can be observed that the current i_{S1} through S_1 is negative at the falling edge of G_1, which means ZCS-OFF. Besides, the voltage $V_{\text{ds-S3}}$ upon the switch S_3 becomes zero in advance before the rising edge of G_3, which means ZVS-ON. Moreover, the synchronous rectification mode enables the current i_{S3} to flow through the switch S_3 instead of its body diode, decreasing the conduction losses. The same effects can also be achieved in the 30–100 V and 45–100 V conditions, as shown in Fig. 19(b)–(c). Hence, the switching losses and conduction loses can be lowered effectively under different voltage gain conditions. It benefits the proposed topology with high conversion efficiency in a wide input-voltage fluctuation range. Meanwhile, soft-switching and synchronous rectification can also be realized under different load conditions (30–100 V), as shown in Figs. 19(b) and 20, introducing low switching losses



(a)

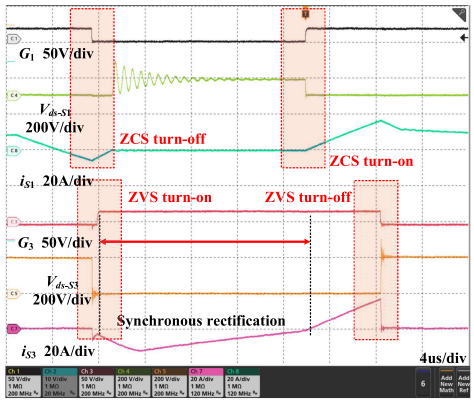


(b)

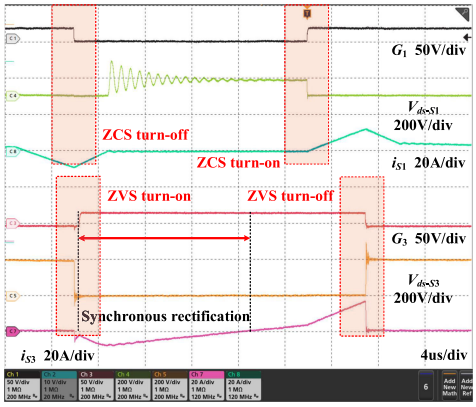


(c)

Fig. 19. Zoomed-in experimental waveforms of soft-switching and synchronous rectification under different voltage gain conditions (three times input-voltage fluctuation). (a) 15–100 V. (b) 30–100 V. (c) 45–100 V.



(a)



(b)

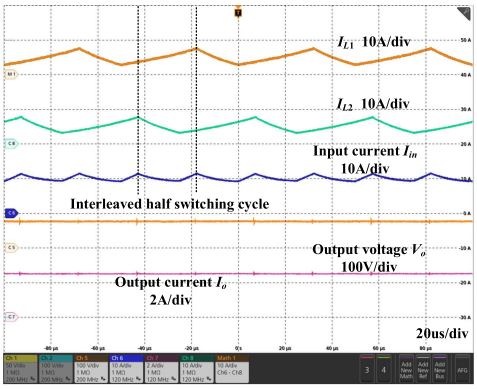
Fig. 20. Zoomed-in experimental waveforms of soft-switching and synchronous rectification under different load conditions. (a) 100% load. (b) 25% load.

and conduction losses. The experimental results are consistent with the operating principle in Section III-B.

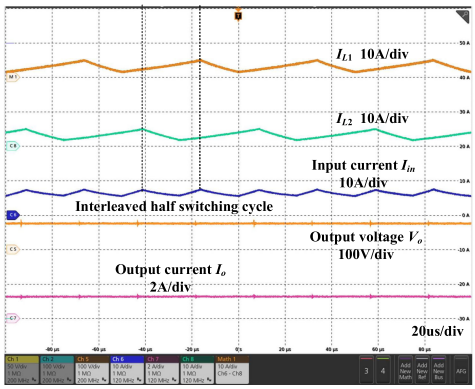
Fig. 21 shows the experimental wave of the measured high-frequency input-current ripples and output-current ripples of the laboratory prototype under different load conditions. The frequency of input-current ripple is twice the switching frequency f_s. It can be observed that the high-frequency input-current ripple is suppressed by the input inductors. Moreover, half-cycle interleaving of the input currents i_{L1} and i_{L2} further reduces the high-frequency input-current ripple injected into the current-fed L-L terminal. Meanwhile, the output current ripple is quite low benefitting from the output inductors L_3. The same effects can also be achieved in the half-load condition, as shown in Fig. 21(b). Hence, the low high-frequency current ripple can be achieved effectively despite the load variation, which is a vital feature of the proposed interface converter for the renewable energy system. The ratio of high-frequency current ripple to its average value can reach the desired standard through sufficient inductance values.

Fig. 22 shows the experimental waveforms under the input voltage change from 20 to 25 V in the left part and from 25 to 20 V in the right part. It can be found that the output voltage of the proposed DCF-DAB converter maintains at the reference value steadily, and the input current changes smoothly during input-voltage fluctuation. Low high-frequency current ripples flow through the input and output ports during steady states and port voltage fluctuation. The drain–source voltage $V_{\text{ds-S1}}$ is below 100 V in steady states and transient states.

Fig. 23 shows the experimental waveforms under the load step change from full load to half load in the left part and



(a)



(b)

Fig. 21. Zoomed-in experimental waveforms of low input-current and output-current ripples: input current I_{L1}, input current I_{L2}, total input current $I_{\rm in}$, output voltage V_o, and output current I_o. (a) Full load. (b) Half load.

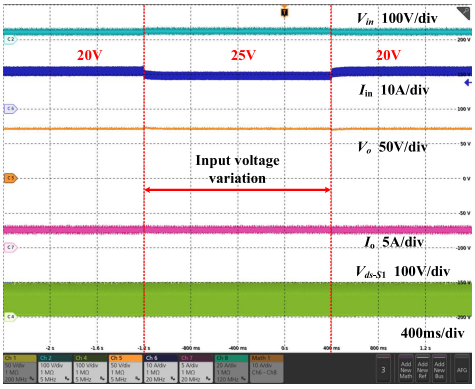


Fig. 22. Experimental waveforms of dynamic performance under input voltage variation conditions.

from full load to half load in the right part. It can be observed that the output voltage is unaffected, and the input current reduces by half or increases with negligible overshoot during load change. The variation of output current is also within safe limiting values. The drain–source voltage $V_{\rm ds\text{-}S1}$ keeps in safe range even if in step-load transient states. The proposed DCF-DAB converter has low high-frequency current ripples on

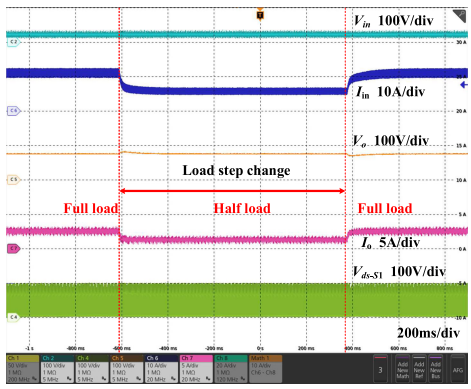


Fig. 23. Experimental waveforms of dynamic performance under load step change conditions.

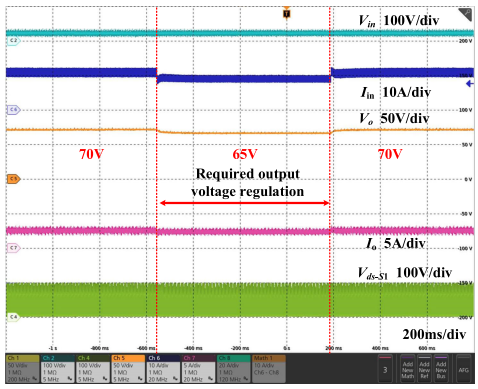


Fig. 24. Experimental waveforms of dynamic performance under required output voltage regulation conditions.

input and output ports in steady states and step-load transient states.

Fig. 24 shows the experimental waveforms required output voltage regulation from 70 to 65 V in the left part and from 65 to 70 V in the right part. It is obviously that the output voltage of the proposed DCF-DAB converter reaches the desired value fast and the input current changes smoothly during output-voltage change. Load current and input current waveforms are shown to be adjusted to their new steady-state values smoothly. The drain–source voltage $V_{\rm ds\text{-}S1}$ is still ensured low enough even if in transient states. In summary, there are low high-frequency current ripples through the input and output ports in steady states and transient states (port voltage fluctuation and load change).

To fully investigate the property of the proposed DCF-DAB converter, Table IV presents a comprehensive comparison of different DAB converters. As the proposed converter is a nonresonant PWM-controlled converter, the other comparison objects are also fixed-frequency nonresonant PWM-controlled DAB converters. The authors wish to point out that the relationship between the proposed DCF-DAB converter and conventional DAB converters is a supplement instead of a substitute. The readers will have another option for prioritizing different features at design time, such as current ripple, direct current control

TABLE IV
COMPREHENSIVE COMPARISON OF DIFFERENT DAB CONVERTERS

	VF-DAB	CF-DAB			DCF-DAB
Bridge type	Full bridge [41]	Voltage clamped full bridge [14]	Voltage clamped half bridge [26]	Voltage no-clamped half bridge [40]	Half bridge
Number of switching devices	8	8	4	6	4
Number of inductor/capacitors	2/4 (capacitive sources/loads)	5/6 (capacitive sources/loads)	4/5 (capacitive sources/loads)	3/4 (capacitive sources/loads)	5
Current ripple (capacitive sources/loads)	High ripple	Low ripple on current-fed port and high ripple on voltage-fed port			Low ripple on both ports
Convenient direct current control	No	One port			Both ports
Anti-short-circuit capability	No	One port			One port
Voltage gains	Medium	High			High
Suitable power level	High power	High power	Low power	Low power	Low power

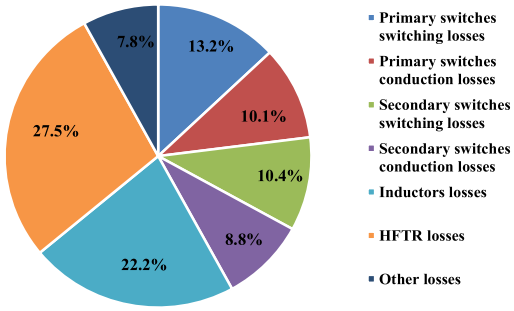


Fig. 25. Loss distribution of the experimental DCF-DAB prototype in full-load condition.

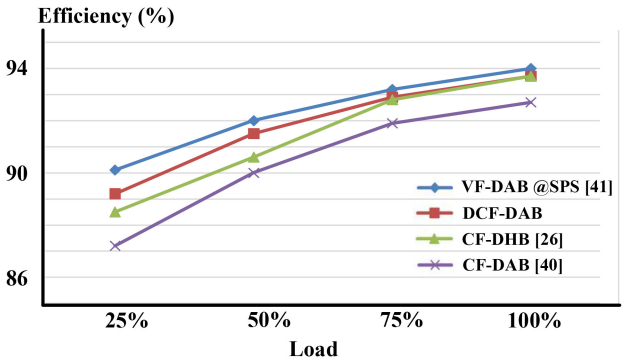


Fig. 26. Experimental efficiency comparison curve of different half-bridge DAB converters with load variation.

capability, and voltage gains. Fig. 25 shows the power loss distribution of the experimental DCF-DAB prototype in full-load condition. Due to measured errors, there exists a power loss difference. It can be obvious that the switches consist of large percentages of total loss. Fig. 26 shows the efficiency curves of the experimental DCF-DAB prototype compared with other DAB converters. The proposed DCF-DAB converter can achieve high efficiency in the rated operating condition. Besides, the efficiency of the proof-of-concept laboratory prototype can be further increased with a better printed-circuit-board design and selection of hardware including switching devices and passive components. Accurately, the proposed converter provides low high-frequency current ripple on both ports while ensuring an acceptable efficiency.

VI. CONCLUSION

In this article, a new isolated dc/dc converter is proposed and named DCF-DAB dc/dc converter. A detailed procedure to design the new converter is discussed for the given system specification. Experimental results demonstrate the proposed converter obtaining excellent dynamic performance under variable input-voltage, load resistor, and output-voltage conditions. When compared with existing similar topologies, the proposed DCF-DAB converter can provide the following advantages.

1) Low high-frequency current ripples on input and output ports in steady states and transient states (port voltage fluctuation and load change).
2) Boost operation offers natural voltage gain and makes the topology suitable for high voltage gain applications.
3) Soft-switching operation for both-side semiconductor devices.
4) Simple topology with low component count and simplified drivers.

In conclusion, the proposed DCF-DAB converter is a promising solution to high-frequency current-ripple-sensitive applications.

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