A Complementary Dual-Window DC Bus Interacting Method for Bipolar-Type DC Microgrids

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***Abstract*—Communication links, as a part of coordinated control in dc microgrids (MGs), play an essential role in achieving high operational performance. In this article, a bipolar topology based on series modular structure of dc MG is designed, and a complementary dual-window dc bus interacting (CDBI) method which combines droop control with antidroop control is proposed to improve the robustness of system and against communication failure. In the proposed CDBI method, distributed generations regard dc buses as common communication channels for information exchange, and the coordinated control within the dc MGs can be realized through predesigned sequences of voltage pulses without extra communication links. Finally, the proposed symmetrical bipolar structure and communication-free coordinated control scheme have been verified in various cases through rapid control prototype. The experimental results show that the bipolar-type dc MG controlled by the proposed CDBI method can supply high-quality power for a long time even in the case of communication failure.**

***Index Terms*—Antidroop control, bipolar-type dc microgrids (MGs), communication failure, coordinated control, dc bus interacting.**

I. Introduction

IN RECENT years, the emergence of dc microgrids (MGs) has provided a promising solution for efficiently integrating diverse distributed generations (DGs) into power systems [1]. On the one hand, the overwhelming majority of DGs have a dc nature. Hence, compared with the conventional ac MGs, dc MGs show higher efficiency due to the reduction of conversion steps, which favors the application of renewable energy sources (RESs). On the other hand, the absence of frequency and phase reduces the difficulty of controller design, enabling a more simplified control system [2], [3].

Nonetheless, a reasonable control and management scheme is still indispensable to the full play of the advantages of dc MGs. Droop control, as a local control method without communication links, is extremely functional for island mode dc MGs. However, droop control imposes a voltage variation on dc bus while realizing current sharing. The contradiction between voltage maintenance and current distribution prevents dc MGs from attaining satisfactory performance [4], [5]. The hierarchical control, in turn, aims to compensate for these errors and optimize the operation by introducing upper layers of control [6]. Therefore, dc MGs under hierarchical control generally have higher quality of power supply [7].

Hierarchical control presents clear superiority over other schemes, under which, however, the coordinated control of multiunits still assumes fairly complicacy due to the dense communication network. With the expectation of possibly extricating dc MGs from communication constraints, so as to further facilitate implementation, researchers begin to focus on some information exchange methods without communication links.

Power line communication (PLC) technology, which utilizes the existing power lines as information transmission medium, can offer great assistance for the mass information flow brought by DGs access. In typical PLC systems [8]–[10], high-frequency signals embedding abundant data are coupled to the power line through power amplifiers, coupling circuits, etc., for transmission. When high-frequency signals reach the terminal equipment, a similar reverse process is implemented to finally accomplish communication. This method can completely eliminate the communication links. However, independent circuits demanded in signal coupling still inevitably increase the cost and volume of the system, which hinders its applications in cost-first dc MGs [11], [12].

Another improved PLC approach raised by researchers draws support from intrinsic pulsewidth modulation (PWM) of the converters for both power conversion and signal transmission, which is also known as power/signal dual modulation with single carrier (PSDM-SC) [13], [14]. In a dc system [15], the frequency shift keying modulation is employed on the PWM carrier to embed the baseband data into the voltage ripples. Since the voltage ripples are inherently generated by switching activities, it can eliminate additional wires and couplers; however, the data demodulation is still complex due to the adjunction of extra analog peak detectors and envelope detectors. Based on this, Wu et al. [16] uses discrete Fourier transform algorithm to directly analyze the dc voltage spectrum, which shows better demodulation performance. In [17], a novel PSDM-SC method, allied with direct sequence spread spectrum technology and phase shift keying modulation is proposed for both communication and electromagnetic interference suppression purpose. Nevertheless, only dc MGs with limited number of switching converters are considered [18].

Exploratory attention has also turned toward the power/signal dual modulation in control loop (PSDM-CL) [19]–[25], recently.

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TABLE I
MAIN FEATURES OF INTEGRATED POWER/DATA COORDINATED CONTROL METHODS FOR DC MGS

Method	Type	In. inject	In. carrier	In. extract	Bandwidth	Signal strength	Dc voltage quality
PLC	ASST/DCT	Coupler	AC: F P R	Decoupler	Low	Medium	Low frequency disturbances
PSDM-SC	ASST/DCT	SM+PWM	AC: F P	Demodulation	High	Weak	High frequency harmonics
PSDM-CL	ASST/DCT	SM+CL	AC: F P R/dc: A	Demodulation	Medium	Medium	Low frequency disturbances
DBS	ASST	CL	Dc: A	Voltage detection	Low	Strong	Low frequency disturbances
CDBI	ASST	CL	Dc: A	Voltage detection	Low	Strong	No above-mentioned problems

In.: Information. ASST: Analog Signal Signaling Technology. DCT: Digital Communication Technology. SM: Signal Modulation. CL: Control Loop.
F: Frequency; P: Phase; R: Reactive power; A: Amplitude.

In [19], differential phase-shift keying technology is adopted to modulate digital signals into the voltage control loop of power optimizers, and a reliable data link with 2 kb/s bit is constructed. Zhang et al. [20] integrate the orthogonal frequency division multiplexing technology into the PSDM-CL method for a higher data rate. In other perturbation-based methods, low-frequency ac signals are superimposed on the control loop of the converters to carry out all-to-all communication through active [21] or reactive [22], [23] power. This method, however, demands synchronization between multiple signals to ensure the accuracy of current distribution [24], [25], which in distributed dc MGs, is difficult to achieve.

In addition to the above-mentioned modulation-based methods, dc bus signaling (DBS) [26]–[31] and dc bus interacting (DBI) [32] methods take the dc bus voltage as a unified criterion to achieve information sharing. Thus, no extra modulation and demodulation equipment are required to create effective channels. Sun et al. [27] set four operating modes for 200 V photovoltaic system to achieve a unified power management. However, the fluctuation range of dc bus voltage has been expanded while refining power flow control [28]. 180 V significantly exceeds the stability range of 200 V $\pm$ 5% [29]. On the contrary, Garg et al. [30] pay attention to the voltage stability, but the voltage levels between different modes are too close, thus the system is prone to misjudgment during mode switching. In [31], the bus voltages on both sides are measured to guide the dual active bridge exchanging power between dc MGs. In [32], a DBI method based on voltage pulses uniquely is proposed. However, it impairs voltage quality during communication.

To overcome the deficiencies of the existing coordinated control methods without communication links, in this article, a bipolar-type master-slave system based on series-connected converters is designed, and a novel complementary dual-window dc bus interacting (CDBI) method is proposed to realize communication through voltage pulses without compromising voltage quality. This method is finally applied to a dc MG equipped with photovoltaics and batteries, with full consideration of the characteristics and limitations of which, the signaling protocol and the reasonable trigger conditions within the system is detailed to guarantee a long-term stable operation.

In order to clearly demonstrate the advantages of the CDBI method, Table I and Fig. 1 make a comparison concerning newly proposed methods in terms of implementation, communication speed, communication distance, voltage quality, etc. From Table I and Fig. 1, the advantages can be concluded as follows:

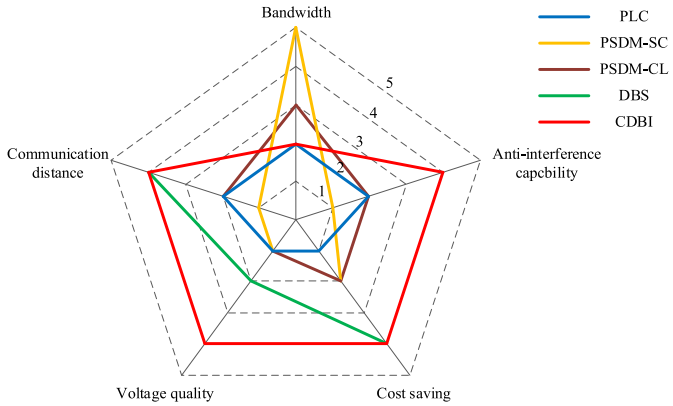

Fig. 1. Comparison of recently proposed integrated power/data coordinated control methods.

1) Low Cost of Hardware: The information exchange of CDBI is realized only through the inherent voltage and current control loop. It does not need extra power circuits to inject ac signals like PLC, nor need additional modulation/demodulation circuits for signal processing like PSDM-SC and PSDM-CL. Therefore, even if the scale of the dc MG is expanded, simple technology can still limit the cost well.

2) Strong anti-interference capability: Conventional PLC, PSDM-CL and PSDM-SC methods tend to select small ac signal as the information carrier, so as to use frequency, phase, or reactive power for information exchange [33]. However, they ignore the influence of ac pulsation introduced by various power converters. Therefore, it is difficult to obtain an ideal signal-to-noise ratio by the . However, CDBI method is not afraid of these disturbances, because this pulse-based communication strategy is essentially relying on the identification of dc components.

3) Long distance communication: The fluctuation range of dc bus voltage is $\pm$5% of the rated value, but its ripple factor range generally does not exceed $\pm$1% of the rated value. The limitation of ripple factor range makes the signal strength of PLC, PSDM-CL, and PSDM-SC methods very small.

4) High voltage quality: In general, dc MGs can only work in a continuous voltage band due to the power fluctuation inside the system. But our CDBI method makes it possible for the dc MGs to work at the rated voltage point by designing and combining two sub-dc MGs with complementary voltage control laws. Similarly, this is something that the DBS method can not do.

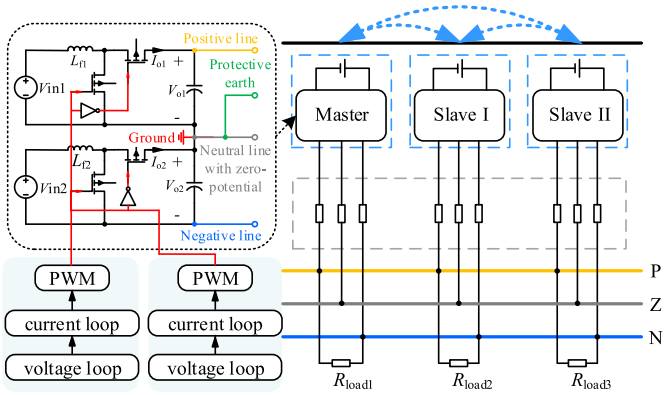

Fig. 2. Structure of the designed bipolar-type dc MG.

This article is organized as follows. In Section II, the designed bipolar-type dc MG is presented, then analysis of the basic implementation principles and configuration of signaling protocol is conducted in Section III. Section IV designs specific control strategies for the photovoltaic unit and the battery unit, based on which, multiple cases are well-planned for experimental verification in Section V. Finally, Section VI concludes this work.

II. Introduction of the Designed Bipolar-Type DC MG

A. Configuration Structure of Bipolar-Type DC MG

Fig. 2 shows the structure of the proposed bipolar-type dc MG equipped with photovoltaics and batteries. The whole system composes of a master unit and two slave units. Among them, the master unit, as the hub of the master-slave control system, is always connected to the dc bus and operates in a similar way as a voltage source to maintain the dc bus voltage. While the slave units merge or exit according to their real-time states as well as the instructions issued by the master unit. It should be noted that, to avoid system collapse, the slave units act as the backup of the master unit, and will take over the master unit when a failure occurs. Each unit in the dc MG also contains two independent bidirectional Buck-Boost converters, the output terminals of which are connected in series, thus creating a three-wire distribution structure with positive (P) line, neutral line, and negative (N) line.

For the grounding strategy, the most commonly advocated grounding configuration named TN-S (Letter T represents the bipolar-type dc system adopts direct grounding strategy, letter N represents the exposed conductive parts of the electrical equipment share the ground with the neutral line through the protective line, whereas letter S represents the protective line and the neutral line are separated.) is adopted for the bipolar-type dc MG, aiming at constructing zero-potential (Z) point on the neutral line, facilitating fault detection, and avoid safety issues [34]. Although the low grounding impedance may slightly offset the (Z) point, the introduced drift voltage is essentially a common-mode voltage between the poles, which is independent from the unipolar voltage and bipolar voltage. Therefore, the grounding configuration will definitely not affect system operation performance.

For the input terminal, the series-connected converters are powered by the same type of RESs or energy storage devices to ensure the energy balance between dual poles. Meanwhile, they adopt respective controllers, so that the P-Z region and Z-N region can independently regulate bus voltage. On the load side, +200 V between positive and negative poles is converted into required alternating current or direct current by dc–ac or dc–dc converters so as to supply power to loads with different natures. If the load balance can be ensured, multiple loads can also be symmetrically connected to the more appropriate +100 V regions in order to improve system operation efficiency.

B. Comparison of Unipolar-Type and Bipolar-Type Systems

For a more comprehensive understanding of the advantages of the separately controlled bipolar-type dc MGs, this article compares its capabilities with conventional unipolar dc MGs in three dimensions: voltage stress, operational reliability, and economy. Through this comparison, more concrete characteristics are clearly detailed below, which can be referenced to guide the design as well as the optimal configuration of bipolar-type dc MGs.

1) Voltage stress: On the premise of unified voltage level, bipolar distribution conduces to lower the bus voltage to ground. In other words, considering the same voltage stress, the proposed bipolar system transmits twice as much power as unipolar systems, which is more suitable for high voltage and high-power occasions.

2) Operational reliability: In the existing literature, there is a general consensus that the reliability of bipolar-type dc MG is higher than that of unipolar-type dc MG. Reliability in these statements is judged by the probability that one system does not completely fall into collapse. Taking a master-slave unipolar-type dc MG as an example, without regard to redundancy, the whole system does not completely collapse requiring the only master converter to function well. Therefore, the reliability of unipolar-type dc MG at one point "t" can be defined as follows:

$$R_{\mathrm{u}}(t) = 1 - \lambda(t) \tag{1}$$

where $\lambda(t)$ represents the failure rate of the master converter. As for a bipolar-type dc MG shown in Fig. 2, since the two poles are backup for each other, even if one of the poles fails, the load can still be supplied by the other pole. Therefore, the whole system does not completely collapse requiring either or both master converters to function well, and the reliability of bipolar-type dc MG at one point "t" can be defined as follows:

$$R_{\mathrm{b}}(t) = C_2^1\lambda(t)(1-\lambda(t)) + (1-\lambda(t))^2 = (1+\lambda(t))(1-\lambda(t)). \tag{2}$$

Equations (1) and (2) preliminarily validate the claim of operational reliability. However, this definition of operational reliability earlier may not be comprehensive because it ignores the assessment of power-providing capability. For this reason, a new definition of operational reliability combining two parameters, failure rate and total transmission power, is proposed to

reassess the operational reliability of the system under specific operating conditions.

Considering that the failure rate is closely related to operating states, it is more reasonable to set the total transmission power of the unipolar-type dc MG to $P(t)$, whereas bipolar-type dc MG to $2P(t)$ to ensure similar operating conditions. For a unipolar-type system, normal power supply requires the only master converter to function well, thus defining the reliability of unipolar-type dc MGs at one point "t" as follows:

$$R_{\mathrm{u}}(t) = \frac{P(t)\left(1-\lambda(t)\right)}{P(t)} = 1-\lambda(t). \tag{3}$$

Compared to unipolar-type dc MGs, which either function or collapse, bipolar-type dc MGs provide an additional intermediate state. When this occurs, the whole system has only one pole of normal power supply, but actually the loads on the fault side can be transferred to the normal side because the voltage level is perfectly matched. We count the power of low-voltage loads as $a(2P(t))$ $(0 < a < 1)$, which essentially can be fully transferred. Public loads originally powered by high-voltage level cannot be fully transferred due to the limitation of interface converters. The specific transfer ratio of the public loads is temporarily recorded as b $(0 < b < 1)$ for further analysis. Based on the above-mentioned three possible states, the reliability of bipolar-type dc MGs at one point "t" is finally defined as follows:

$$\begin{aligned} R_{\mathrm{b}}(t) &= \frac{C_2^1\lambda(t)\left[1-\lambda(t)\right]\left[2aP(t)+b\left(2P(t)-2aP(t)\right)\right]}{2P(t)} \\ &\quad + \frac{\left[1-\lambda(t)\right]^2 2P(t)}{2P(t)} \\ &= \left(1-\lambda(t)\right)\left[1+\left(2a+2b-2ab-1\right)\lambda(t)\right] \end{aligned}. \tag{4}$$

Dividing (4) by (3), the quotient of the reliability of these two systems can be expressed as follows:

$$\frac{R_{\mathrm{b}}(t)}{R_{\mathrm{u}}(t)} = 1+\left(2a+2b-2ab-1\right)\lambda(t). \tag{5}$$

Assume "$\lambda(t) = 0.2$," and a three-dimensional (3-D) reliability comparison diagram of unipolar and bipolar systems is drawn in Fig. 3. From Fig. 3, it can be observed that, although load distribution and power conversion capability of interface converters affect reliability relationship, overall, the function values fall more over the green plane, which symbolizes the isosurface. Therefore, as long as through reasonable system design, bipolar-type dc MGs can achieve higher reliability than unipolar-type dc MGs

3) Economy: Bipolar-type systems can achieve higher operational reliability at the expense of higher storage capacity and cost. Taking a unipolar-type dc MG as an example, its power rating should satisfy (6) without differentiating between grid-connected mode and island mode.

$$P_{\mathrm{u\_rating}}(t) = \max\left|P(t)-P_{\mathrm{g}}(t)\right| = P(t) \tag{6}$$

where $P_{\mathrm{g}}(t)$ represents power fed by the grid. In a bipolar-type dc MG, additional power transfer needs to be considered, so its

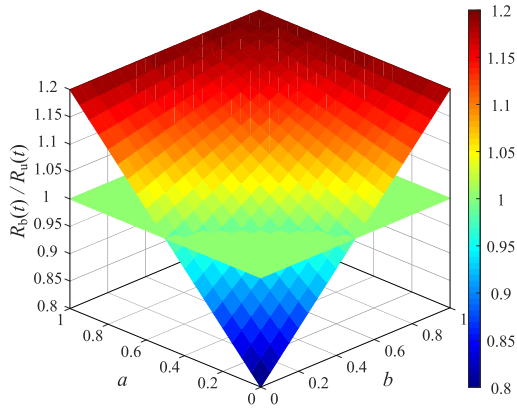

Fig. 3. 3-D reliability comparison diagram.

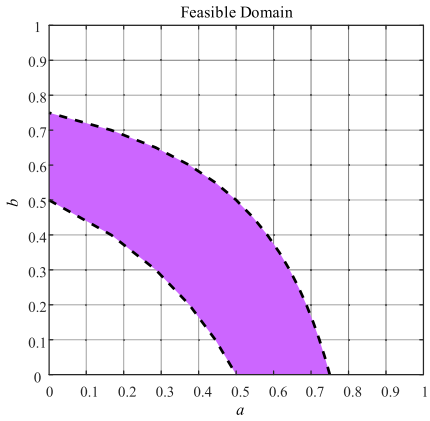

Fig. 4. Reliability comparison diagram.

power rating should satisfy (7).

$$\begin{aligned} P_{\mathrm{b\_rating}}(t) &= 2\max\left|2aP(t)+b\left(2P(t)-2aP(t)\right)-P_{\mathrm{g}}(t)\right| \\ &= 4P(t). \end{aligned} \tag{7}$$

Comparing power rating of these two systems with their total transmission power, it is not difficult to find that bipolar-type dc MGs improve reliability at the expense of double system capacity. This situation is somewhat harsh, so it is necessary to optimize configuration from the perspective of users in order to alleviate cost burdens. For example, public and unipolar loads can be accessed at specified scales, or transfer ratio of public loads can be limited. Through these optimal configurations, the capacity of bipolar-type dc MGs can be limited to less than $P_{\max}(t)$.

Fig. 4 shows a feasible domain of configuration parameters, and any combination of a and b in purple region can limit the power rating of bipolar-type dc MGs to $3P(t)$ while obtaining higher reliability than unipolar-type dc MGs.

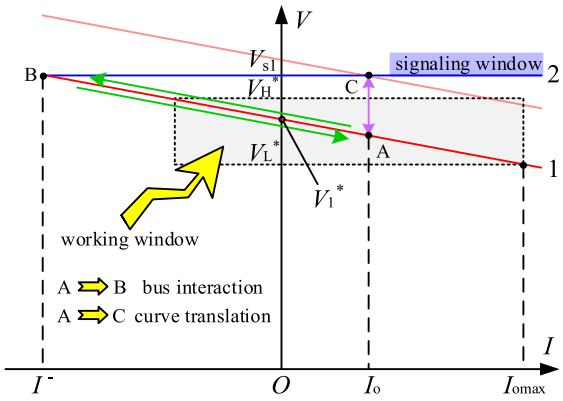

Fig. 5. Droop curves for DBI method.

III. Principles of the Proposed CDBI Method

A. Concepts and Control Rules of DBI

One prominent drawback of the master-slave system is the complexity of communication. For the purpose of helping master-slave system get rid of the dependence on highly connected communication network so as to improve the robustness in case of communication failure, a DBI method is introduced between the parallel converters in this article. The core idea of the DBI method is to employ the control unit of the power converter to adjust dc bus voltage between high and low levels according to corresponding information that needs to be transmitted. For the converters connected to the dc bus, all these distinctive voltage variations can be detected, identified, then transformed into serviceable information to guide their actions. Dual-window here represents two nonoverlapping voltage ranges of the common dc bus, which can act as a marker to identify whether the voltage level is high or low. DC bus interacting here represents different converters exchange their state information through a specific sequence of voltage pulses on the dc bus. The following part takes two nodes of a master converter and a slave converter in P-Z region as an example to illustrate the control rules.

The control rules of DBI method are shown in Fig. 5, where the master converter, as the only device to support dc bus in the whole system, always operates on the droop curve 1 with a floating voltage reference of V_1^* and a droop coefficient of R_{v1}. The allowable voltage range of the dc bus is $[V_L^* V_{s1}]$, where $[V_L^*\ V_H^*]$ is defined as the working window within which the dc bus voltage is identified as low level, while $[V_H^*\ V_{s1}]$ is defined as the signaling window within which the dc bus voltage is identified as high level. Unlike the master converter, the slave converter is originally a power-providing device, but with the purpose of enabling it to actively initiate communication, we set an additional constant voltage mode for it. When switching to this mode, the slave converter will operate on the droop curve 2 with a constant voltage reference of V_{s1} and a droop coefficient of 0. According to the direction of information transmission during the signaling period, the implementation of DBI method can be concretely divided into two processes as follows:

1) Master to slave: Taking the master converter as a signal source for communication will form an information flow from the master converter to the slave converter in dc MG. When the master converter transmits information, it will directly raise its floating voltage reference from V_1^* to V_{s1} to generate an identifiable high level since it is a voltage control unit. Therefore, generating voltage pulses on the dc bus containing concrete information by the master converter only need to shift droop curve 1 up and down according to the predesigned signal sequences. Besides, no action is required during this period. This process corresponds to the purple arrow in Fig. 5.
2) Slave to master: Taking the slave converter as a signal source for communication will form an information flow from the slave converter to the master converter in dc MG. When the slave converter transmits information, it will actively switch to the constant voltage mode in order to take over the dc bus voltage and control it at the signaling level V_{s1} higher than the upper limit of the working window. For the generation of low level in the voltage pulse, it is not the task of the slave converter, but still depends on the droop control of the master converter as the original state of the system cannot be predicted from the slave converter. This interacting process is shown by the green arrow in Fig. 5.

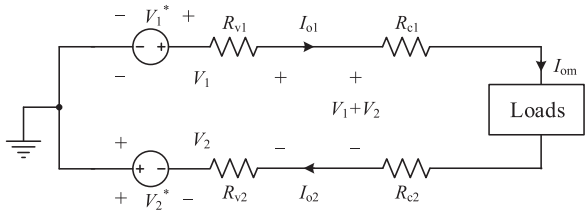

Fig. 6. Equivalent circuit of voltage-type series dc converters.

B. Introduction of the Antidroop Control

Droop control is a common current regulation method for parallel converters in the peer-to-peer system. By setting droop coefficients, each parallel converter can automatically share the loads according to the rated capacity, and the dc MG can finally reach a stable equilibrium state. In this article, the research target is a bipolar-type dc MG adopting master slave control, so there is no current distribution problem in theory. However, after introducing the DBI method in both P-Z and Z-N regions, the voltage regulation among series-connected master converters can still draw on the experience of droop control. A partial topology consisting of only two master converters and the resistive loads is considered below. According to the control rules of the DBI method, both master converters operate under droop control to maintain dc bus voltage.

Fig. 6 shows the equivalent circuit of series-connected master converters under droop control. V_1^* and V_2^* represent the floating reference voltage of two converters, respectively, R_{v1} and R_{v2} represent the droop coefficients (or virtual resistances) introduced by the droop control. R_{c1} and R_{c2} represent cable impedances, which can be ignored here as the master unit is normally placed close to the dc bus.

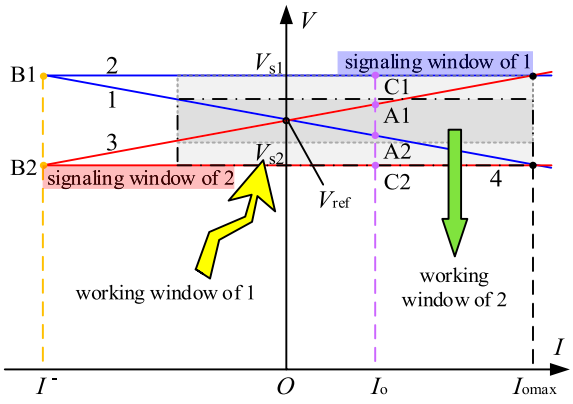

Fig. 7. Droop curves for proposed CDBI method.

Based on Kirchhoff's voltage law, the relationship between the output voltage and the output current of two master converters can be written as follows:

$$V_i = V_i^* - R_{vi} I_{oi}\ ,\ i = 1, 2. \tag{8}$$

The symmetrical configurations and synchronous actions of converters in P-Z region and Z-N region guarantee the energy balance between dual poles or only slight power deviation. Therefore, almost no current flows through the ground line, and the current flowing through these two converters are always equal. It is beyond doubt that $I_{o1} = I_{o2} = I_{om}$ is always valid in the system. On this basis, this article sets $V_1^* = V_2^* = V_{ref}$, which means the series-connected master converters have the same floating reference voltage. By substituting the above-mentioned conditions into (8), the sum of the output voltages of two converters can be written as follows:

$$V_1 + V_2 = 2V_{ref} - (R_{v1} + R_{v2})\, I_{om}. \tag{9}$$

It can be seen that the voltage difference between the positive bus and the negative bus falls dramatically due to the introduction of droop coefficients. Adding secondary control corrections to the reference voltage is the most effective way to compensate the voltage drop. However, secondary control requires additional regulators to adjust the deviation. In order to realize voltage compensation under simple control circuits, one direct idea is to raise the output voltage of the master converter on one side to compensate the voltage drop on the other side. When setting $R_{v2} = -R_{v1} = -R_{vm}$, the voltage rise in Z-N region just compensates for the voltage drop in P-Z region, and the voltage difference between dual buses can be stable at twice the reference voltage, as shown in (10).

$$V_1 + V_2 = 2V_{ref}. \tag{10}$$

As the droop coefficient of the master converter in Z-N region is the opposite number of that in P-Z region, it must be a negative value, so the slope of the *V-I* curve in Z-N region must be positive. For ease of description, it is defined as antidroop control in this article. And the improved relationship of the droop curves is shown in Fig. 7. The master converter in P-Z region operates on the droop curve 1, corresponding to (11). Meanwhile, the master converter in Z-N region operates on the antidroop curve 3, corresponding to (12). By combining the droop control with the antidroop control, the sum of the output voltages of the series-connected master converters can always be maintained at the rated value regardless of the load conditions.

$$V_1 = V_{ref} - R_{vm} I_{om} \tag{11}$$

$$V_2 = V_{ref} + R_{vm} I_{om}. \tag{12}$$

In addition, the bipolar-type dc MG designed in this article takes the unit as a whole to make state changes, so the converters in symmetrical positions always make synchronous actions. In other words, the real-time states of the series-connected master converters are consistent, and the time at which communication is triggered is also synchronous. Therefore, imitating the principle of voltage compensation between dual poles in working mode, we set the signaling level of the negative pole as follows:

$$V_{s2} = 2V_{ref} - V_{s1}. \tag{13}$$

In this way, the voltage difference between the positive and negative poles can be maintained at a high quality of 2 V_{ref} regardless of the working mode or the signaling mode. Moreover, it can be found from the curve relationship of the improved DBI method that when the slave unit is signaling, the output current in the master unit is clamped to a specific negative value, as presented in (14). Therefore, the output current of the slave unit must be positive during the dc bus interaction as presented in (15), which has no restrictions on the type of DG to be accessed.

$$I_{\mathbf{om}} = \frac{V_{\mathbf{ref}} - V_{\mathbf{s1}}}{R_{\mathbf{vm}}} = \frac{V_{\mathbf{s2}} - V_{\mathbf{ref}}}{R_{\mathbf{vm}}} < \mathbf{0} \tag{14}$$

$$I_{\mathbf{os}} = |I_{\mathbf{om}}| + I_{\mathbf{load}} > \mathbf{0}. \tag{15}$$

C. Improvements of Power Allocation During Signaling

According to the (14), the master unit is forced to output a negative current during bus interaction, which requires absorbing power from the dc MG. Therefore, the slave unit signaling on the dc bus has to provide power for both the master unit and various loads as shown in (15), which puts forward high requirements for its capability. Once the capacity of the slave unit is insufficient, the system will have power gaps and thus become unstable.

To further improve the power allocation during signaling as well as eliminate unnecessary energy exchange, the master unit will be switched to zero-current mode once the dc bus voltage is pulled to the signaling window by the slave unit. With this improvement, the slave unit only need to feed the loads, as listed in (16).

$$I_{\mathbf{os}} = I_{\mathbf{load}}. \tag{16}$$

Moreover, in the dc bus interaction, both pulse sequence with equal width and that with unequal width can be used as communication signals. Obviously, the latter has more features for signal recognition, thus it is used in this article to transmit information with limited bits for a higher communication speed. Fig. 8 illustrates a clear dc bus interaction process with arbitrary

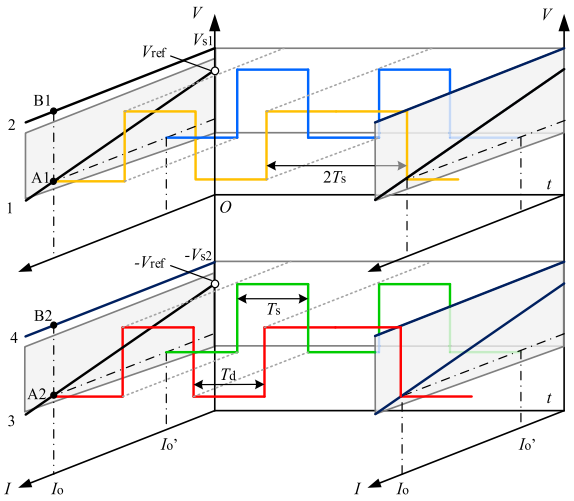

Fig. 8. Dual pulse signals for information exchange.

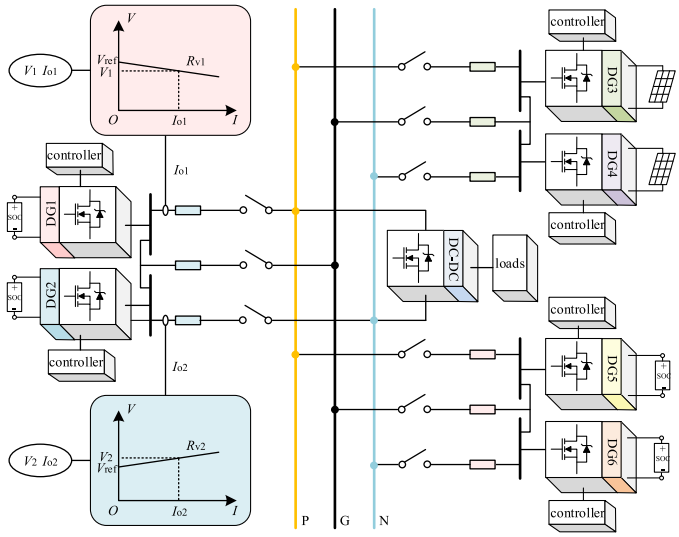

Fig. 9. Block diagram of system configuration.

TABLE II
OPERATING MODE OF EACH UNIT DURING COMMUNICATION

Electrical level	The master unit	The slave unit
High	Zero-current mode	Constant voltage mode
Low	Droop and antidroop mode	Block drive signals

dual pulse signal, from which, the detailed implementation of high and low levels on dc bus can be thoroughly comprehended.

Initially, the dc bus voltage is controlled at the working window by the master unit, for example, points A1 and A2 in Fig. 8. At some point, a slave unit changes its operating state, and thus prepares to actively broadcast its state information. So it switches to work in the constant voltage mode to pull the dc bus voltage into the signaling window for generating the high levels. As the master unit will immediately turn to zero-current mode once detecting V_{s1} on positive bus or -V_{s2} on negative bus, the slave unit will work on points B1 and B2 for supporting full loads, as shown in Fig. 8. After T_s, the drive signals of the slave converters are blocked off, and the system converts to the initial state when the master converters operate on the droop curve 1 and the antidroop curve 3 to control the dc bus voltage, corresponding to the points A1 and A2. After the delay time T_d is over, the system restarts the next cycle when the slave unit switches to the constant voltage mode to generate the high levels for another specific time. Thereafter, the dc bus voltage in each region enters respective working window again, and the voltage difference between dual poles during the whole process remain at 2 V_{ref}.

The improved rules of CDBI method are shown in Table II, where the master unit does not operate in a single voltage control mode, but switches between voltage control mode and zero-current mode. The slave unit carries out constant voltage mode in sections. In this way, there always exists a unit acting as a voltage source to take over the dc bus voltage in each period, which generates high or low level signals.

TABLE III
SIGNAL SERIES FOR THE MASTER UNIT

Pulse 1	Pulse 2	Function
T_{S1}	/	Seek help (over-discharge/failure)
T_{S1}	T_{S1}	Switch on S1 (heavy loads)
T_{S1}	T_{S2}	Switch off S1 (over-charge)
T_{S2}	T_{S2}	Switch on S2 (heavy loads)
T_{S2}	T_{S1}	Switch off S2 (light loads)

D. Design of Signaling Protocol

The bipolar-type dc MG studied in this article contains photovoltaics, batteries, and a variety of dc loads. For RESs such as photovoltaics, they are generally not suitable as the master unit due to the unpredictability and fluctuation of the output power. Compared with the photovoltaic unit, the battery unit can provide stable power to the dc MG in certain time limit. Besides, their output power is easier to control. Therefore, from the point of view of operational stability, this article sets the battery unit as the master unit, and the photovoltaic unit and other battery units as the slave units, as shown in Fig. 9.

For a bipolar-type dc MG shown earlier, the load consumption, state of charge (SoC) of the batteries and local natural conditions such as irradiance, temperature, etc., directly influence the power flow. The master unit, as a brain for balancing the power supply and demand of the whole system, not only need to follow the power changes of RESs or dc loads through fast charging or discharging, but also need to deploy other slave units to make a coordinated response. In addition, the slave units also have the obligation to inform the master unit of their state information to facilitate its deployments. On the basis of fully considering the above-mentioned elements, Tables III and IV design the dual pulse signals for various situations, with the expectation of achieving the coordinated operation of multiple units.

TABLE IV
SIGNAL SERIES FOR THE SLAVE UNIT

Serial number	Pulse 1	Pulse 2	Function
1	T_{S2}	/	Respond (agree to help)
	T_{S1}	T_{S1}	Load (high irradiance)
	T_{S1}	T_{S2}	Exit (low irradiance)
2	T_{S3}	/	Respond (agree to help)
	T_{S2}	T_{S2}	Load (high SoC)
	T_{S2}	T_{S1}	Exit (low SoC)

From Tables III and IV, it is not difficult to find that the designed signaling protocol takes sufficient account of the characteristics of different kind of energy. For example, the photovoltaic unit is arranged in the first order; hence, the master unit will give it start priority to share load power, so as to make full use of RESs. Only when the photovoltaic unit is not capable enough will the battery unit be chosen. Meanwhile, considering the rationality of power flow, the light loads condition is taken as criterion for judgment for closing the slave unit equipped with batteries, so as to avoid unnecessary energy exchange from batteries to batteries. In addition, the signaling protocol also adds overcharge protection to the master unit. Once the master unit detects the SoC exceeds the threshold, it will shut down the photovoltaic unit actively to complete self-protection.

In addition to the fluctuations of power supply and demand, the insufficient capacity or failure of the master unit will also threaten the stable operation of the system. For example, if the loads in the system are heavy, the energy of the single master unit will finally be exhausted due to continuous discharge over a certain period of time, and the power gaps will lead to collapse of the dc bus voltage. The same is true when a failure occurs. In view of the drawbacks of single master system, Tables III and IV add additional monopulse signals in order to construct a multimaster system, in which multiple master units (one is the initial master unit and the rest is the initial slave unit) work successively in the extending time. In this way, although the bipolar-type dc MG depends on a single master unit for coordination, the whole system can still operate for a long time under the alternate control of backup units without losing any function.

According to the final signaling protocol, it can be concluded that both the master unit and the slave unit can send two types of signals, monopulse signals and dual pulse signals. Monopulse signals mainly face the extreme situations such as over-discharging or failure of the master unit so as to handover the master position. Dual pulse signals are oriented to the conventional situations to transmit state information of each unit.

IV. DESIGN OF CONTROL STRATEGY FOR EACH UNIT

A. Control Strategy for the Photovoltaic Unit

Based on the principles of CDBI method and the above-mentioned signaling protocol, the control strategies for the photovoltaic unit and the battery unit are further designed. Fig. 10 shows control diagram of the photovoltaic unit, which consists of four parts: maximum power point tracking (MPPT) control, droop control or antidroop control, constant voltage control,

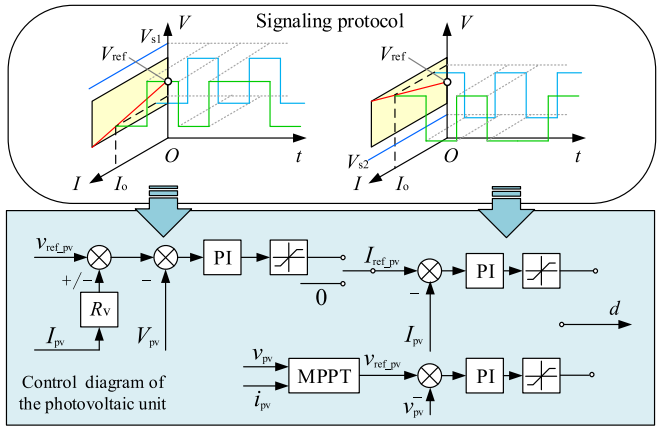

Fig. 10. Control diagram of the photovoltaic unit.

and zero-current control. When the photovoltaic unit takes over dc bus voltage as a master unit, the upper half of Fig. 10, which symbolizes droop control or antidroop control, functions. First, voltage deviation between reference voltage $V_{\mathrm{ref\,pv}}$ and measured voltage V_{pv} is fed into the proportional integral (PI) regulator with the participation of the droop coefficient. Then, reference current $I_{\mathrm{ref\,pv}}$ generated by the outer loop is compared with measured current I_{pv} and the result is sent to another PI regulator, which finally generates the PWM signals to drive the power tubes. Zero-current control is only used temporarily during dc bus interaction, when only the PI regulator of the current loop works.

Constant voltage control and MPPT control are adopted in another case where the photovoltaic unit plays the slave role. Similar to the zero-current control, the constant voltage control has the characteristic of part-time application, which will be activated just for generating the signaling levels. While MPPT control located at the bottom of the control diagram takes effect so long as the photovoltaic unit startups. On the basis of obtaining the voltage v_{pv} and current i_{pv} of the photovoltaic array at the input end, a new reference value is calculated in real-time by employing MPPT control algorithms such as perturbation and observation method or incremental conductance method. MPPT control also requires to use a PI regulator to complete the tracking of the calculated reference value to maximize the output power.

B. Control Strategy for the Battery Unit

Fig. 11 shows the control diagram of the battery unit. The only difference from the photovoltaic unit in the whole process is to replace the MPPT control with the SoC-based current control. The SoC module in the lower half of Fig. 11 is used to manage the energy so that when the SoC of the battery approaches the upper or lower limits, its maximum allowable output power will be constrained for the seek of preventing the battery from over-charging or over-discharging. The executive process inside SoC module can be divided into two steps. First, the SoC module judges whether the SoC of the battery is in the safe range. If $20\% \leq \mathrm{SoC}(t) \leq 90\%$, the maximum allowable output power of the battery will be not limited.

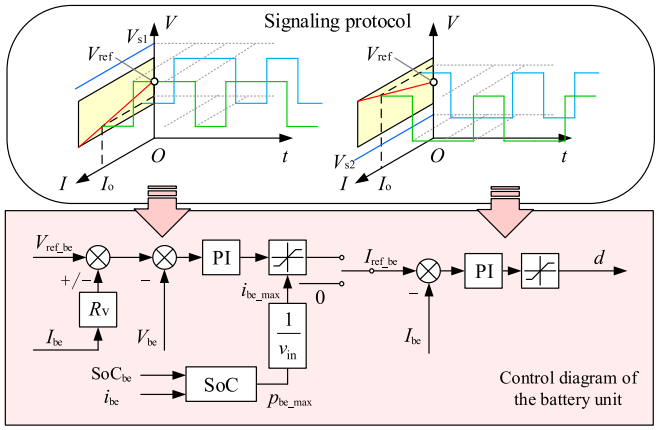

Fig. 11. Control diagram of the battery unit.

If the above-mentioned condition is not met, the corresponding instructions for power limiting will be generated based on the SoC as well as the energy transmission direction.

1) If SoC(t) $< 20\%$, and the battery is still discharging, set

$$p_{\text{be\_max}} = p_{\text{bN}} \times \left[1 - \frac{(20\% - \text{SoC}(t))^2}{25}\right]. \quad (17)$$

2) If SoC(t) $> 90\%$, and the battery is still charging, set

$$p_{\text{be\_max}} = p_{\text{bN}} \times \left[1 - \frac{(\text{SoC}(t) - 90\%)^2}{25}\right] \quad (18)$$

where $p_{\text{be·max}}$ and p_{bN} represent the maximum allowable output power and rated power of the battery unit, respectively, SoC(t) represent the current state of charge.

C. Pulsewidth Selection

Two key parameters of CDBI method are the amplitude and width of the voltage pulse. The selection of pulse amplitude V_{s1} and V_{s2} should consult the allowable operating range of dc bus voltage, which is set to 1.05 V_{ref} and 0.95 V_{ref} in this article. While the selection of pulsewidth has to consider the voltage transition process, in other words, the duration of pulse edges. DC bus filtering capacitance imposes the greatest impact on the voltage transient process, because it will introduce voltage inertia into the forward channel of the closed-loop control, which can be expressed as follows:

$$G_{\text{C}}(s) = \frac{R}{RCs + 1} \quad (19)$$

where $G_{\text{C}}(s)$ represents the transfer function of voltage inertia, and C, R represents the filtering capacitance and load resistance, respectively. In order to obtain better communication speed, it is obvious that inertia element with large time constant is not expected as it will slow down voltage transients. Therefore, this article refers to Siemens' idea of "optimal tuning" and uses the proportional differential (PD) element in the molecule of the transfer function of the PI regulator on voltage loop to eliminate voltage inertia, which can be expressed as follows:

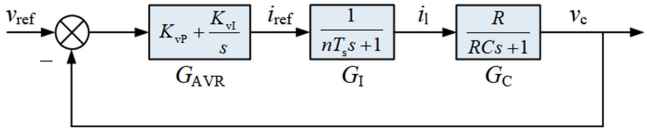

Fig. 12. Block diagram of double closed-loop.

TABLE V
RELEVANT PARAMETERS

Parameters						
C	R	T_{s}	T_{Σ}	D	K_{vP}	K_{vI}
940 μF	50 Ω	1×10^{-4} s	4×10^{-4} s	0.5	2.3	48.1

$$G_{\text{AVR}}(s) = K_{\text{vP}} + \frac{K_{\text{vI}}}{s} = \frac{K_{\text{vI}}\left(\frac{K_{\text{vP}}}{K_{\text{vI}}}s + 1\right)}{s}, \frac{K_{\text{vP}}}{K_{\text{vI}}} = RC. \quad (20)$$

PI regulator on current loop and the controlled inductance can be reasonably simplified into a first-order inertial element with a time constant of several switching cycles T_{s} as follows:

$$G_{\text{I}}(s) = \frac{1}{nT_{\text{s}}s + 1} \quad (21)$$

where $G_{\text{I}}(s)$ represents the simplified transfer function of inner current loop. On this basis, the double closed-loop can be modeled with the block diagram of Fig. 12, from which the transfer function of the whole control loop can be gained as follows:

$$G_{\text{V}}(s) = \frac{1}{\frac{T_{\Sigma}C}{(1-D)K_{\text{vP}}}s^2 + \frac{C}{(1-D)K_{\text{vP}}}s + 1} \quad (22)$$

where T_{Σ} represents total time constant while D represents the duty cycle. Obviously, the transfer function above symbolizes a second-order system whose damping ratio can be selected as $\xi = 0.707$ for fast response and sufficient phase margin, so let

$$\frac{1}{2}\sqrt{\frac{C}{T_{\Sigma}(1-D)K_{\text{vP}}}} = \frac{\sqrt{2}}{2}. \quad (23)$$

The scale factor can be finally selected as follows:

$$K_{\text{vP}} = \frac{C}{2T_{\Sigma}(1-D)}. \quad (24)$$

The hardware parameters of Boost converter used in the experiment and the PI regulator parameters designed according to the idea of "optimal tuning" are given in Table V.

Based on the above-mentioned parameters, the open-loop logarithmic frequency characteristic and the voltage step response can be obtained in Fig. 13. The middle band of the logarithmic frequency characteristic passes through the zero-decibel line at a slope of -20 dB/dec. The middle bandwidth is sufficient to ensure the stability of the system with a phase margin of 65.5°. The voltage response is within a few milliseconds and the overshoot is small. Therefore, we choose the pulsewidth on the time scale of seconds for distinction.

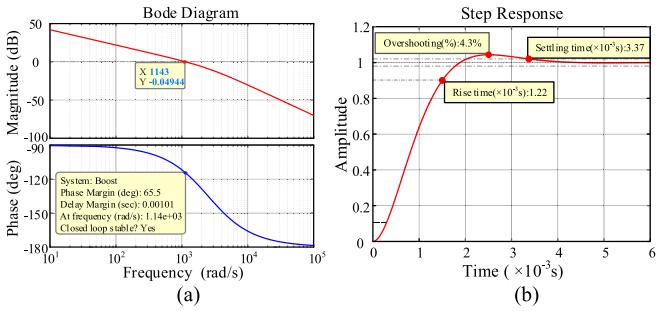

Fig. 13. Response curve. (a) Open loop logarithmic frequency characteristic curve. (b) Step response curve.

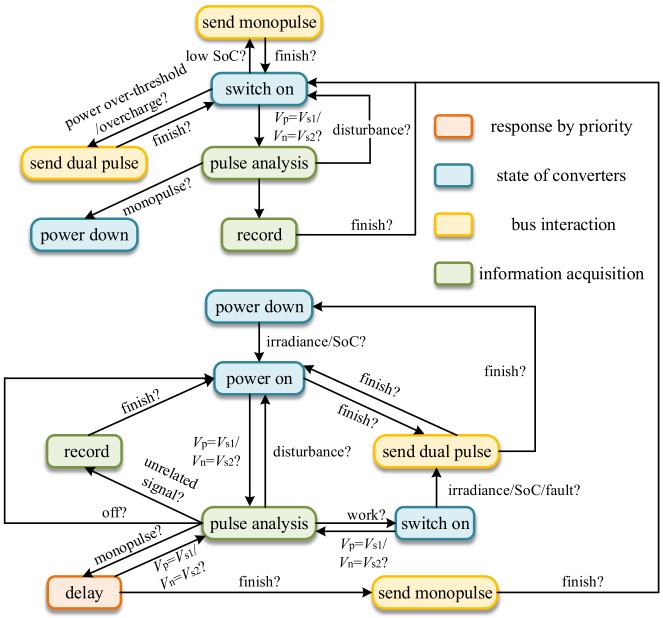

Fig. 14. State transition diagram of the master unit and the slave unit.

D. State Machine

The control logic part is implemented through C script. Without splitting the signaling process, the state transition diagram of the system is shown in Fig. 14. The master unit transits between six states, as shown in upper half of Fig. 14.

State 1: Switch ON. The series-connected master converters operate under droop control and antidroop control, respectively, to support the dc bus. Meanwhile, the master unit constantly monitors its real-time state and the dc bus voltage. If the monitor detects insufficient energy or any fault, the master unit will enter state 2. If its output power reaches the predesigned thresholds, or batteries are overcharged, it will enter state 3. If the signaling level is detected, it will enter state 4.

State 2: Send monopulse. The master unit sends a monopulse signal, signaling the whole system that it will surrender its dominance. After broadcasting its requirement globally, the master unit returns to state 1 to stabilize the dc bus voltage.

State 3: Send dual pulse. The master unit looks up the state information and start priority of each slave unit recorded in the memory, then sends a dual pulse signal which can solve the problem. After the dual pulse signal is sent, the master unit returns to state 1.

State 4: Pulse analysis. The voltage pulse is extracted from the dc bus by the master unit, then counted and identified in its controller. If the received signal is judged to be an interference signal, the master unit will immediately return to state 1. If it is judged to be a dual pulse signal, it will enter state 5. The case of a monopulse signal implies that there exists an appropriate slave unit to bear the burden of stabilizing the dc bus voltage, hence it will enter state 6.

State 5: Record. The up-to-date information is stored by the memory of the master unit, overwriting the original state of the corresponding location. After all the above-mentioned steps are completed, it will automatically return to state 1.

State 6: Power down. The master unit is separated from the dc bus.

The slave unit transits between eight states, as shown in the lower half of Fig. 14.

State 1: Power down. For the photovoltaic unit, if irradiance, temperature and other indicators meet the requirements, it will enter state 2. For the battery unit, if SoC(t) $>$ 90%, enter state 2.

State 2: Power on. If the power on process has just finished, it will enter state 3. Otherwise, it will keep in state 2 and monitor the dc bus voltage until V_{s1} and V_{s2} are detected.

State 3: Send dual pulse. Once entering state 3, the slave unit will immediately send a dual pulse to broadcast its state. After communication, it will return to states 1 or 2 according to the condition before communication.

State 4: Pulse analysis. The voltage pulse is extracted from the dc bus by the slave unit, then counted and identified in its controller. If the received signal is judged to be an interference signal, the slave unit will immediately return to state 2. If it is a command signal of other units, it will enter state 5. Only when the received signal is related to the slave unit itself will it take actions. If the signal is a monopulse signal, the slave unit will enter state 6. If it is a startup signal composed of double pulse, the slave unit will enter state 8. On the contrary, a shutdown signal will lead to a return to state 2.

State 5: Record. The up-to-date information is stored by the memory of the slave unit, overwriting the original state of the corresponding location. After all the above-mentioned steps are completed, the slave unit will automatically return to state 2 or state 8 according to the condition before communication.

State 6: Delay. The slave unit with a higher alternate priority has the right to take the lead in choosing whether to promote to a master unit. Therefore, after entering state 6, the slave unit will wait for a specific time according to the predesigned alternate priority and continue to monitor the dc bus voltage. If V_{s1} and V_{s2} are detected within this period of time, it will return to state 3. If not, it means that the slave unit with higher alternate priority are not eligible for promotion, so enter state 7.

State 7: Send monopulse. The slave unit sends a monopulse in response to the request from the master unit. When finished, it will enter state 1 of the master unit.

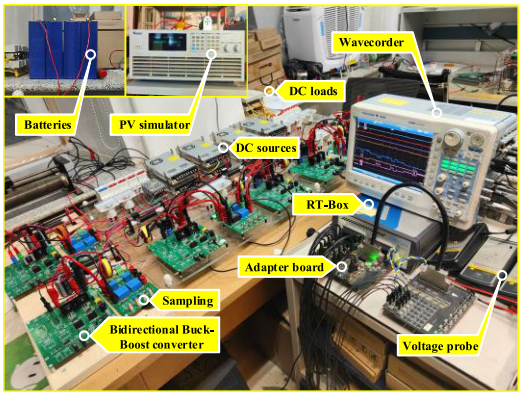

Fig. 15. Experimental platform.

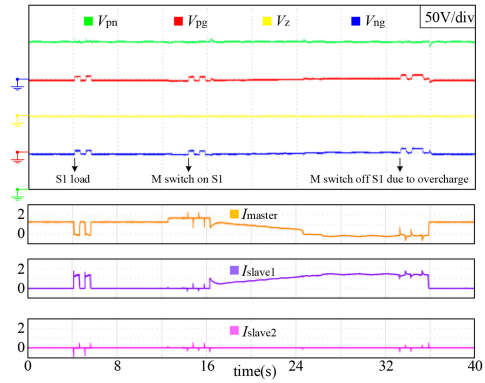

Fig. 16. Experimental waveforms containing charging scenario from the photovoltaic unit to the master unit.

TABLE VI
EXPERIMENTAL PARAMETERS

Type	Parameters				
Hardware circuits	$V_{battery}$ 48 V	P_{pv_max} 200 W	$P_{converter}$ 200 W	L 1 mH	C 940 μF
Controllers	V_{ref} 100 V	V_{s1}/V_{s2} 105/95 V	V_L^*/V_H^* 95/103 V	R_{v1}/R_{v2} 1.5/−1.5 Ω	$T_{s1}/T_{s2}/T_{s3}$ 0.5/1/1.5 s

State 8: Switch ON. The slave unit starts to provide power to the dc bus. For slave units equipped with photovoltaics, they work in MPPT mode. For battery units, they work in SoC-based current mode. After switched ON, the slave unit monitors the voltage of dual poles. Once a voltage jump is found, it will immediately return to state 4. Once a lack of energy or faults are found, it will return to state 3.

V. IMPLEMENTATION AND VERIFICATION

Fig. 15 is a photograph of the dc MG experimental platform, which is composed of six bidirectional Buck-Boost converters. Every two converters are connected in series to form three units, and which appear a parallel relationship, thus forming a three-wire distribution structure. The control logic part of the six converters is independently built in PLECS, mainly including voltage and current double closed loop control model, MPPT model, over charging/discharging protection model, pulse analysis model, state monitoring model, etc. The control signals of the six converters are output by the real-time simulator RT-Box and then sent to the PCB through the optical fiber communication line from the digital output of the adapter board, so as to drive the IGBTs on PCB. The power inductors and filtering capacitors of the converters are connected to the PCB using wires and connectors in the form of external embeddedness. In order to simulate multiple scenarios under different load conditions, a 1 kW/122 Ω sliding rheostat, two 200 W/500 Ω, and two 400 W/250 Ω cement resistors are used in the experiment. The 48 V input voltage of the battery unit is taken from the series-module composed of four 12 V batteries. The power supply of the photovoltaic unit is obtained from the photovoltaic simulator. Detailed hardware and control parameters in the experiment are listed in Table VI.

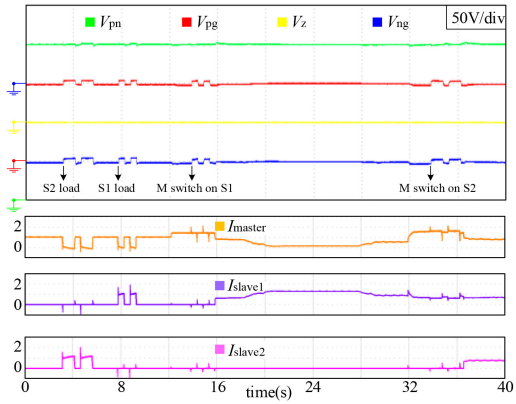

Fig. 17. Experimental waveforms under fluctuations of sources and dc loads.

The actual experiment is divided into three groups. The first group focuses on the validation of the proposed CDBI method. The second group tests the stability of the system during the handover of master position in the case of master unit faults. In the third group of experiments, secondary controllers are introduced to compensate for the voltage deviation caused by the droop control or antidroop control as well as further improve the voltage quality of the monopole.

A. Verification of Basic Functions

Figs. 16 to 18 are the related waveforms captured in the first group of experiments. In Fig. 16, the master unit has a relatively light load at $t = 0$ s. When $t = 4$ s, the photovoltaic unit perceives adequate solar energy, so it actively powers on to keep standby and sends a dual pulse signal of 0.5 s to notify its availability of the master unit. The master unit will not wake up the photovoltaic unit immediately after receiving the information due to the light load condition. When the load becomes heavier at $t = 12.5$ s, the master unit has to send a dual pulse signal of 0.5 s by changing its floating voltage reference to wake up the photovoltaic unit. Thereafter, the photovoltaic unit operates in MPPT mode to transmit power to the dc MG to the greatest extent. With the increase of irradiance, the photovoltaic unit can gradually fully feed the load. Simultaneously, it uses the

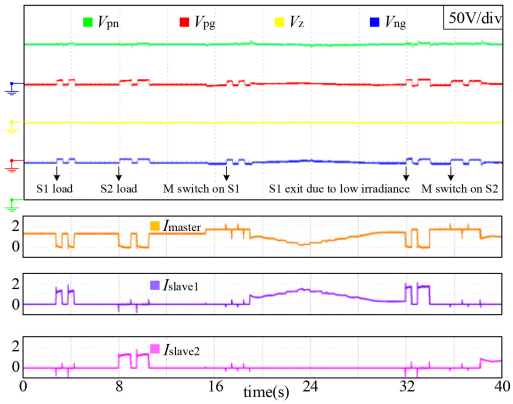

Fig. 18. Experimental waveforms containing scenario where the photovoltaic unit exits due to low irradiance.

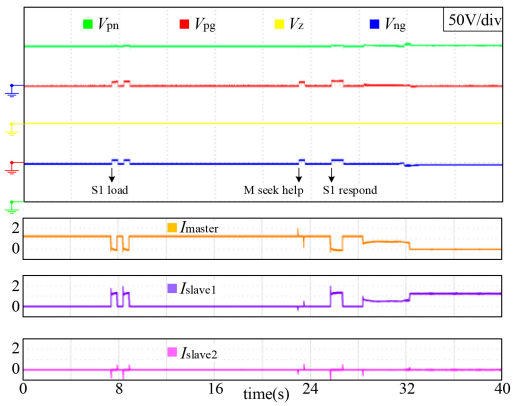

Fig. 19. Experimental waveforms in which the photovoltaic unit succeeds the master position.

remaining energy to charge the master unit until it is full. Once the master unit detects that charging is complete, it will actively shut down the photovoltaic slave unit to achieve self-protection.

In Fig. 17, two slave units actively power on to keep standby at the preliminary stage of the experiment. When the output power of the master unit approaches its limit due to the increase of the loads, it can be seen from Fig. 17 that the photovoltaic unit is preferentially enabled to make full use of RESs. When $t = 32$ s, the load in the system increases again, at which point there is no available RESs in the system, so the master unit chooses to wake up the battery unit. The dual pulse signals in Fig. 18 are similar to that in Fig. 17, except that the access of the battery unit in this figure is directly caused by the exit of the photovoltaic unit with low irradiance.

B. Validation of System Stability During Transient Process

Figs. 19–22 are the related waveforms captured in the second group of experiments. Figs. 19 and 20 show the complete transient process in which the photovoltaic unit and the battery unit make use of respective monopulse signal for substituting the dominance. After the monopulse signal transmission is completed, the original slave converters gradually output power, and

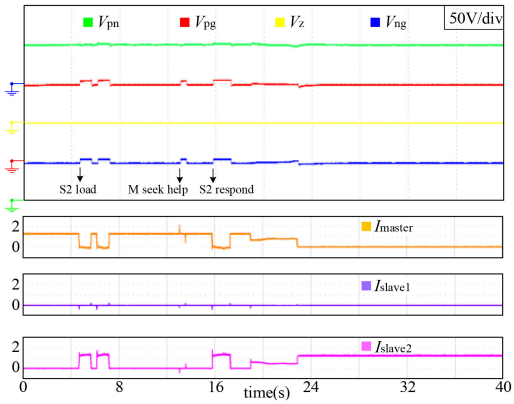

Fig. 20. Experimental waveforms in which the battery unit succeeds the master position.

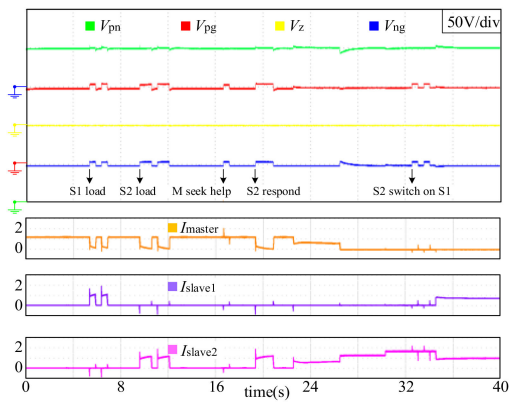

Fig. 21. Experimental waveforms in which the battery unit succeeds the master position, then actively switches on the photovoltaic unit.

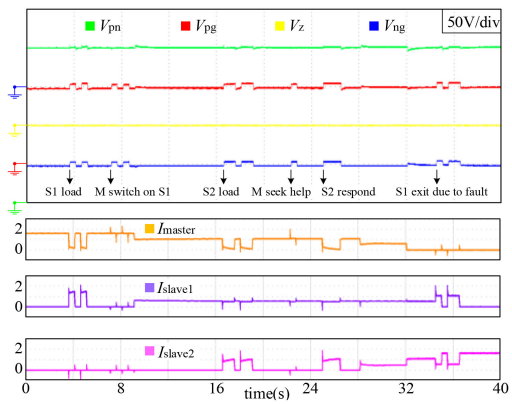

Fig. 22. Stability test of the transient process with current source type units operating.

then work under droop control or antidroop control to maintain bus voltage and thus becomes a new master unit in a new cycle.

In Fig. 21, when $t = 16.5$ s, the master unit encounters a fault and cannot continue to undertake the master control task. Therefore, a monopulse signal of 0.5 s is sent on the dc bus to seek for help. Although both the photovoltaic unit and the

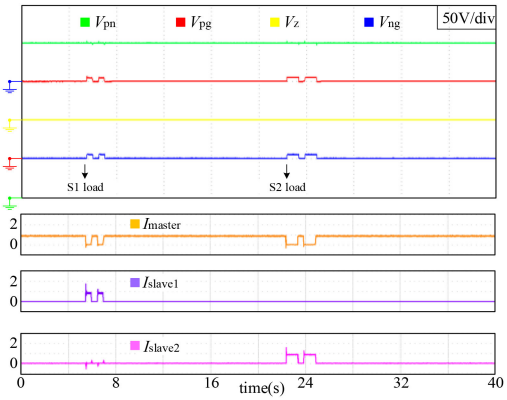

Fig. 23. System operating states under light load conditions.

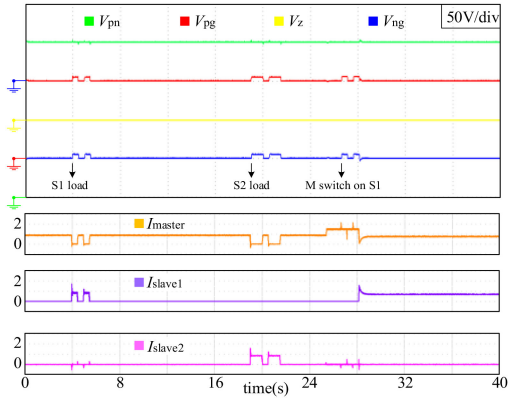

Fig. 24. System operating states with increasing loads.

battery unit are available at this time, the battery unit, which is set as the first choice, has the right to take the lead in responding because of its constant and stable output power. Only if the battery unit is not available can the photovoltaic unit be qualified as the master unit of the system. When $t = 30.6$ s, the current in the battery unit suddenly increases, and its output power again crosses the threshold. In order to relieve the pressure, the new master unit can also send a dual pulse signal of 0.5 s to wake up the photovoltaic unit. Fig. 22 illustrates that the output power of the photovoltaic unit does not affect the transient process.

From the above-mentioned two groups of experimental results, it can be seen that the CDBI method can achieve bidirectional information exchange only by detecting the local voltage in real time. In addition, by using the independent converters, complementary voltage can be output on the positive and negative buses, which makes the voltage between dual poles almost no fluctuation and greatly improves the quality of power supply.

C. Performance With Secondary Controllers

With the expectations of further improve the voltage quality of monopole, secondary controllers are added to compensate the voltage deviation in the third group of experiments.

In Fig. 23, the dc MG maintains a light load condition during the whole process, and the dc bus voltage at each pole is stabilized at the rated value with secondary controllers. In Fig. 24, upholding the principle of preferential utilization of RESs, the master unit sends a dual pulse signal of 0.5 s to wake up the photovoltaic unit first to share the loads. In Fig. 25, after the two slave units start to work as current sources, they exit the system due to low SoC and faults at $t = 28.5$ s and $t = 35.5$ s, respectively. Consequently, the adjustment of the output power in the master unit needs to rely on actively cutting off some nonimportant loads in the system. In Fig. 26, the battery unit awakened first has to quit halfway due to its low SoC, after which, the photovoltaic unit powers on and is immediately awakened by the master unit. When $t = 34$ s, after accumulating energy, the battery unit loads again and keeps standby in the system.

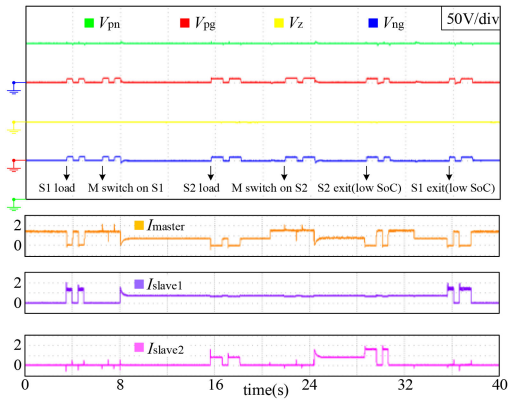

Fig. 25. System operating states containing scenarios where the photovoltaic unit exits due to faults and the battery unit exits due to low SoC.

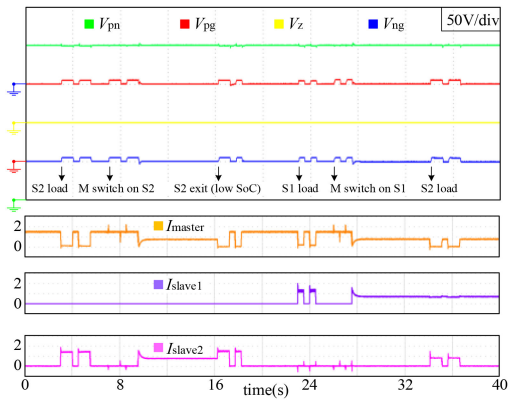

Fig. 26. System operating states under initial heavy loads and midway exit of the battery unit.

VI. Conclusion

This article proposes a CDBI method for bipolar-type dc MG based on series-connected converters. The main innovation of this method is the introduction of antidroop control and the complementary setting of the signaling levels, under which the dc bus voltage between dual poles can be kept stable at rated value without fluctuation in both working mode and signaling mode. In addition, on the basis of improving the utilization

of RESs, the combination of the monopulse signals and the dual pulse signals allows dc MG to operate independently for a longer period of time, even in some unusual circumstances such as faults. The last part of this article verifies the effectiveness of this method in a variety of simulated cases. In conclusion, the bipolar-type system and the CDBI method proposed in this article have high economy, robustness, and application value.

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