Sub Line-Frequency Stability Analysis of Single-Phase Constant Power Loads Using Envelope Impedance

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***Abstract*—Regulated constant power loads present an incremental negative input impedance that can destabilize the interconnected system. With ac, power-factor corrected (PFC) constant power loads, instabilities can arise from a dynamic instability between the source and load impedance. The dynamics involving a rectifying interface are nonlinear and evade classical impedance and stability analysis. Several efforts have been made to understand and characterize the important dynamic interaction between ac PFC converters and ac sources. This article unravels this work to present a useful model for an ac PFC converter and a tunable controller that can stabilize source–load interactions. Specifically, an envelope impedance technique is developed for analyzing ac source and PFC load. This article also demonstrates an instability arising from incompatible source and load envelope impedance in hardware, and a variable bandwidth constant power load that can correct the instability.**

***Index Terms*—Negative resistance devices, stability, stability criteria.**

I. Introduction

THE earliest electrical loads, e.g., incandescent bulbs or well-loaded motors, presented an essentially resistive impedance to the grid. These loads reduce their consumption when the utility voltage drops. They have slow dynamic behavior and are relatively immune from creating output disturbances in the event of small variations in the amplitude or frequency of the utility voltage waveform. New loads controlled by fast-acting power electronics, e.g., more recent lighting technologies (LED or fluorescent) or variable-speed motor drives, respond very rapidly to changes in the utility waveform and are prone to generate output changes that annoy the customer or ruin an industrial process. Power electronic loads are therefore frequently controlled or configured as "constant power loads" (CPLs) that fight the tendency to pass source variations to the output (e.g., light or speed) by rapidly regulating load conditions to draw constant power. For example, actively controlled components of HVAC (heating and cooling) systems can demand constant power from the utility over certain time intervals, as can uninterruptible power supplies. Modern fluorescent and solid-state lighting loads and battery chargers often present a constant-power profile to the electrical source. In consequence, if there is a decrease in input voltage, the power converter responds by increasing input current demand. The resulting negative incremental input impedance can cause system instability, especially under conditions of heavy loading. On a large enough section of a grid, instability may not be observed if the share of fast power electronic loads in the system is sufficiently small. However, once the share of fast, "aggressive" loads reach a certain threshold, instability may happen unexpectedly.

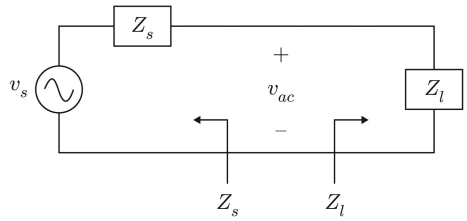

Fig. 1. An ac system with source and load impedance.

For dc systems, traditional stability analysis looks to the ratio of the source and load impedance, as shown in Fig. 1 [1]–[3]. Past work analyzed dc-bus instability caused by CPLs and presented a mitigation strategy that involved adding a damping leg to the input of the converter [4]. The dynamic benefit of the "damping leg" can be implemented as part of the CPL internal feedback loop [5]. This active damping for system stability can be modeled and analyzed using traditional stability analysis techniques. For dc systems, stability has therefore been achieved through electronic self-tuning of the CPL regulation bandwidth, avoiding the need for hardware changes and simplifying the *in situ* problem of stabilizing an existing dc distribution network.

Grids for ac operation present more complex modeling challenges. The nonlinear rectification interface between the ac grid and the dc input to a switching converter complicates the application of traditional analysis methods. A rectifier can be thought of as a modulator that multiplies grid voltage with a square wave to produce a rectified output [6]. This modulation or mixing effect of a line-frequency rectifier produces modulated

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current harmonics at more frequencies than just the frequency of an injected ac voltage perturbation. While small-signal impedance modeling of such rectifiers has been studied in both three-phase and single-phase systems [7]–[9], these do not extend to analysis of the low-frequency interactions between source and load separated by a rectifier. Some works have investigated low-frequency stability of single-phase power-factor corrected (PFC) power supplies. Chu *et al.* [10], for example, investigate the internal dynamics of a two-stage PFC load. This analysis does not consider the characteristics of the source. In this article, we focus solely on the interaction at the grid interface of the PFC load.

In power electronic systems with control bandwidths that are relatively low compared to a carrier or line frequency, such as that in PFC systems, the small-signal response relevant to the feedback network is embedded in the envelope of the carrier, rather than in the carrier itself [11]. This response in the envelope has been called the envelope impedance (EI), which is defined as the ratio between the envelope of the ac voltage and envelope of the ac current for a given envelope modulating frequency. This EI approach has been used to simulate, analyze, and stabilize the interaction between a high-frequency ballast and fluorescent lamp to a high degree of accuracy [12]. Sanders [13] examined closed-loop PFC CPLs driven by passively filtered ac grids. To account for the rectifier-induced modulation effect, this analysis looked at an EI equivalent to estimate ac-side impedance of a closed-loop PFC CPL. This reference concluded that instability should only arise in pathological cases or cases where there is a nonlinear interaction between source and load control. Hoff and Mulukutla [14] took this further by analyzing the EI to estimate the interaction of source and load impedance from the dc side, thus enabling the use of traditional dc grid stability analysis. This reference also concluded that instability primarily arises in the cases where there is an unfortunate interaction between ac source voltage regulation and closed-loop PFC CPL control.

This article examines the interaction between a regulated ac source and a controllable bandwidth PFC CPL by extending techniques borrowed from traditional dc grid impedance analysis but adapted to the concept of EI for the source. Techniques are presented that permit a converter to self-identify or self-correct this pathology. Specifically, this article presents an architecture for a controllable bandwidth PFC CPL controller. This architecture allows for tunable CPL bandwidth at the input of the load while still providing high-bandwidth regulated output power. Essentially, this control technique decouples the input impedance of the PFC CPL from its load regulation performance. With this architecture, a small-signal dc-side equivalent circuit model is developed. The EI of an exemplary regulated ac source is derived to illustrate the approach for stability analysis of the interaction between such a source and the PFC CPL controller. Both simulated and experimental demonstrations of this example ac source interacting with a controllable bandwidth PFC CPL support the use of dc-side impedance as an estimate for ac-side EI of the ac CPL.

II. Controllable-Bandwidth AC CPL Control

An ac CPL is designed to draw constant power over the long term. This is usually accomplished by regulation of the output load. When designed for an ac system, the PFC converter is designed with a regulation bandwidth less than the ac system frequency—typically less than 25 Hz in a 60-Hz system [14]. This ensures that ac power ripple is permitted, allowing the ac CPL to resemble a resistive load within the line cycle, and consequently allowing for effective power-factor correction. It may be desirable for the bandwidth to be even further reduced for stable interaction with the source.

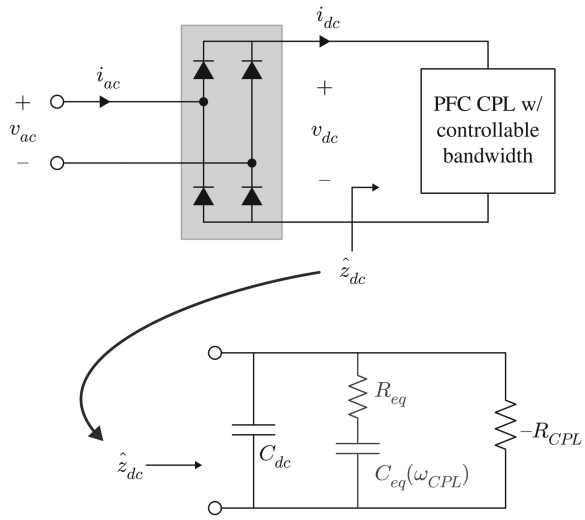

Fig. 2. AC/DC interface for PFC CPL. The dc-side small-signal impedance can be represented with an equivalent circuit model that is dependent on the controllable bandwidth of the CPL.

A controllable bandwidth allows for a tradeoff between disturbance rejection and ideal resistive behavior. When the bandwidth is high, the converter responds quickly to line voltage disturbances and so the energy storage requirement, i.e., the dc link capacitor size, decreases. Along with these benefits, however, comes increased current command distortion, worsening the distortion factor and thus power factor, and an increased chance of instability. The bandwidth may be decreased to improve the distortion and alleviate stability issues, at the cost of the disturbance rejection performance. So, the controllable-bandwidth controller is adopted to permit changes to this tradeoff in real time. This is particularly useful in applications where the amount of energy storage is constrained, either due to volume or weight requirements. The bandwidth can be increased to alleviate the worsened disturbance rejection due to less energy storage. When dynamic grid conditions do not allow such a high bandwidth, it can be reduced to ensure stability. Previous work by the authors has explored this capability in dc grids; here we expand on it for ac [5].

Fig. 2 shows the ac/dc interface for an ac CPL with PFC and controllable bandwidth. This section will show how low-frequency dc-side impedance can be modeled by an equivalent circuit model [5].

This section describes a control scheme for an ac CPL with power-factor correction, a controllable CPL bandwidth at the ac input, and high-frequency regulation for a load. An internal energy buffer balances differences between input and output power. The dc-side small-signal impedance of the converter is determined and fitted to an equivalent circuit model. Finally,

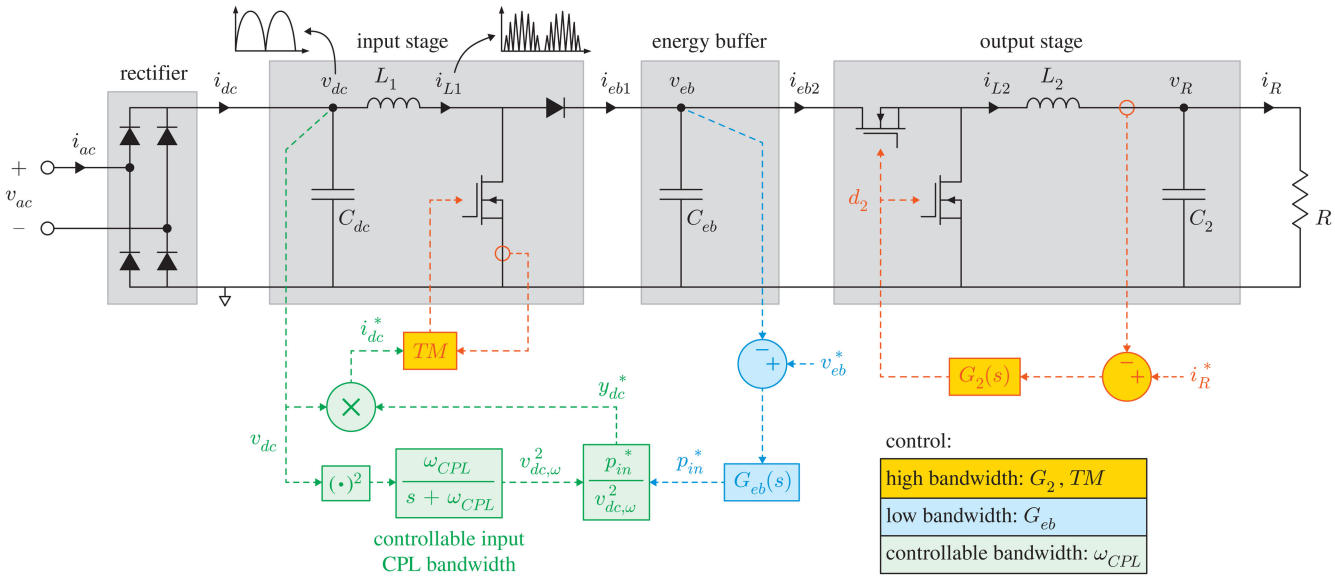

Fig. 3. Control scheme for ac CPL with controllable input bandwidth. Input stage implements power-factor correction and feedforward CPL bandwidth control. Output stage regulates load power at high bandwidth. An intermediate energy buffer provides or absorbs power imbalance.

experimental measurements of the ac-side behavior are compared to the dc-side impedance given by the equivalent circuit model.

A. Control Scheme

Fig. 3 illustrates a control scheme that permits a CPL converter to provide high-bandwidth, regulated control for a load voltage while presenting a variable input power demand to the grid. The control scheme for this system could be applied to a wide range of converter configurations; the power train shown is an example to illustrate the control scheme. Differences between the grid input power and the load requirements are absorbed over relatively short times by the energy buffer. This permits the overall system to appear "friendly" to the utility, reducing demand on short time scales in response to input voltage dips. Load regulation is unaffected, and the energy buffer is "recharged" on a longer time scale that places less demand on the utility.

A passive bridge rectifier connects the converter to the ac grid or "ac side." The "dc-side" input voltage v_{dc} is measured by the controller. This measurement consists of a squaring term, followed by a first-order low-pass filter with bandwidth ω_{CPL}. The resulting signal $v_{dc,\omega}^2$ represents the squared RMS of v_{dc}, low-pass filtered with bandwidth ω_{CPL}. Next, the reference input admittance y_{dc}^* is determined from the reference input power p_{in}^* and $v_{dc,\omega}^2$. For PFC, the controller determines the instantaneous reference input current i_{dc}^*, given by

$$i_{dc}^* = v_{dc} y_{dc}^*. \tag{1}$$

The converter demonstrated in this article implements transition mode (TM) current control of the input boost stage, as shown in Fig. 4. The current-shaping scheme allows the boost inductor current i_{L1} to rise to twice the reference current i_{dc}^* and then to fall to zero before starting the next switching cycle. This approach enables high-bandwidth feedforward current control

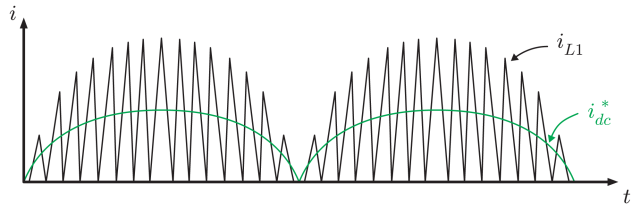

Fig. 4. Transition mode (TM) control allows for high-bandwidth feedforward input current control in PFC ac loads. Boost inductor current i_{L1} is controlled to operate in the boundary between continuous and discontinuous conduction mode.

in the input stage. The output stage shown in Fig. 3 provides high-bandwidth regulated power to an output load R. Imbalance in input and output power causes the energy buffer voltage v_{eb} to fluctuate during input voltage disturbances. An outer control loop governed by $G_{eb}(s)$ maintains v_{eb} at a nominal voltage over the long term by adjusting reference input power p_{in}^* at low bandwidth.

B. Small-Signal Analysis

DC-side input impedance below the ac system frequency can be determined by linearizing the individual elements of the control scheme. Small-signal perturbations of the RMS values of signals are denoted by hatted variables. All operating point quantities are denoted by capitalized variables. For example, the small-signal perturbation of the dc-side RMS input voltage is denoted by $\hat{v}_{dc}$, while V_{dc} represents the operating point dc-side RMS input voltage. For instance, the linear approximation of $i_{dc}^* = y_{dc}^* v_{dc}$ is

$$\hat{i}_{dc}^* = Y_{dc}\hat{v}_{dc} + V_{dc}\hat{y}_{dc}^*. \tag{2}$$

To simplify modeling the energy buffer, the input stage is considered a lossless stage with TM control precisely commanding

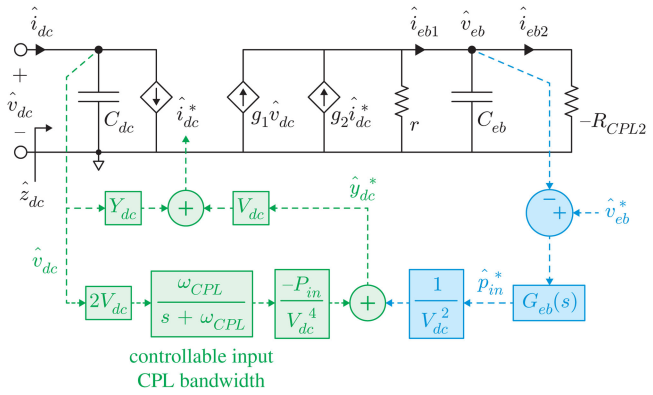

Fig. 5. Linearized small-signal model for dc circuit from Fig. 3.

reference current i^*_{dc}. With this simplification, current into the energy buffer is

$$i_{eb1} = \frac{v_{dc} i^*_{dc}}{v_{eb}}. \tag{3}$$

The linear approximation of i_{eb1} can then be simplified as

$$\hat{i}_{eb1} = \underbrace{\frac{I_{dc}}{V_{eb}}}_{g_1} \hat{v}_{dc} + \underbrace{\frac{V_{dc}}{V_{eb}}}_{g_2} \hat{i}^*_{dc} - \underbrace{\frac{P_{in}}{V^2_{eb}}}_{1/r} \hat{v}_{eb} \tag{4}$$

where g_1, g_2, and r represent linearization constants. The output stage is simplified by assuming that it draws constant power P_{in}. With this simplification, current out of the energy buffer is

$$i_{eb2} = \frac{P_{\text{in}}}{v_{eb}}. \tag{5}$$

The linear approximation of i_{eb2}, with R_{CPL2} as a linearization constant, is

$$\hat{i}_{eb2} = -\underbrace{\frac{P_{\text{in}}}{V^2_{eb}}}_{1/R_{\text{CPL2}}} \hat{v}_{eb}. \tag{6}$$

With these simplifications and linear approximations, a complete small-signal model is determined and shown in Fig. 5.

From the small-signal model, some important relationships can be determined. They can be derived from the governing equations seen in the small-signal model

$$\begin{cases} \hat{i}_{dc} &= sC_{dc}\hat{v}_{dc} + \hat{i}^*_{dc} \\ \hat{i}^*_{dc} &= Y_{dc}\hat{v}_{dc} + V_{dc}\hat{y}^*_{dc} \\ \hat{y}^*_{dc} &= \frac{-2P_{\text{in}}}{V^3_{dc}} \frac{\omega_{\text{CPL}}}{s+\omega_{\text{CPL}}} \hat{v}_{dc} - \frac{G_{eb}}{V^2_{dc}} \hat{v}_{eb} \\ \hat{v}_{eb} &= \frac{1}{sC_{eb}} \left(g_1 \hat{v}_{dc} + g_2 + \hat{i}^*_{dc} \right) \end{cases}. \tag{7}$$

The energy buffer feedback controller $G_{eb}(s)$ should be designed to maintain nominal voltage of the energy buffer capacitor C_{eb} over the long term. Its control should be low bandwidth relative to ω_{CPL} to avoid interfering with the controllable CPL input impedance. Solving for $\hat{v}_{eb}$ in terms of $\hat{v}_{dc}$ in the system (7) gives the input voltage to energy buffer voltage transfer function

$$\frac{\hat{v}_{eb}}{\hat{v}_{dc}} = \frac{\frac{V_{dc}Y_{dc}}{V_{eb}} \left(1 + \frac{s-\omega_{\text{CPL}}}{s+\omega_{\text{CPL}}} \right)}{sC_{eb} + \frac{G_{eb}}{V_{eb}}}. \tag{8}$$

Equation (8) can be used to help design $G_{eb}(s)$. For instance, consider a converter with operating point $V_{dc} = 120$ V, $Y_{dc} = 6.3$ mS, $V_{eb} = 250$ V, and $\omega_{\text{CPL}} = 2\pi 1$ rad / s, and with $C_{eb} = 100\,\mu$F. The unit step response of (8) reveals that $G_{eb}(s)$ implemented as a PI controller with proportional gain $K_p = 0.02$ and integral gain $K_i = 0.001$ results in a maximum v_{eb} perturbation of 7 V, and a settling time of 10 s for v_{eb} to return to nominal voltage.

The system can also be used to determine input impedance $\hat{z}_{dc}$. Solving for $\hat{v}_{dc}$ in terms of $\hat{i}_{dc}$ in (7) gives the input impedance

$$\hat{z}_{dc} = \frac{\hat{v}_{dc}}{\hat{i}_{dc}} = \left(sC_{dc} + \frac{Y_{dc}\frac{s-\omega_{\text{CPL}}}{s+\omega_{\text{CPL}}} - \frac{Y_{dc}G_{eb}}{sC_{eb}V_{eb}}}{1 + \frac{G_{eb}}{sC_{eb}V_{eb}}} \right)^{-1}. \tag{9}$$

If G_{eb} is designed to impose only a minor effect on impedance at frequencies significant to the controllable input behavior of the converter, then G_{eb} will be small and $\hat{z}_{dc}$ can be approximated as

$$\hat{z}_{dc} \approx \left(sC_{dc} + Y_{dc}\frac{s-\omega_{\text{CPL}}}{s+\omega_{\text{CPL}}} \right)^{-1}. \tag{10}$$

The equivalent circuit shown in Fig. 2 models the impedance (10), with

$$\begin{aligned} R_{\text{CPL}} &= \frac{1}{Y_{dc}} \\ R_{eq} &= \frac{1}{2Y_{dc}} \\ C_{eq} &= \frac{2Y_{dc}}{\omega_{\text{CPL}}}. \end{aligned} \tag{11}$$

The following section shows how this model can be used to predict the ac-side EI of the controllable CPL bandwidth converter.

III. Envelope Impedance for Stability Analysis

One type of ac CPL instability that has been observed involves the interaction between a regulated ac source, such as an uninterruptible power supply (UPS), and an ac CPL [14]. Poor interaction can occur between the respective feedback controls of the ac source and the CPL. One way to determine if source–load stability can be at risk is presented in this section, which analyzes the time-domain amplitude of ac signals to determine stability. An ac signal and its "envelope" are shown in Fig. 6. In this article, a round hatted variable is used to denote an ac signal envelope, such that for a sinusoidal ac signal with frequency ω_c given by

$$x_{\text{ac}}(t) = \widehat{x}_{\text{ac}}(t)\sin(\omega_c t) \tag{12}$$

the envelope is $\widehat{x}_{\text{ac}}(t)$. The term "envelope impedance" is used in this article to refer to s-domain relationships between voltage and current envelopes. The benefit of envelope analysis is

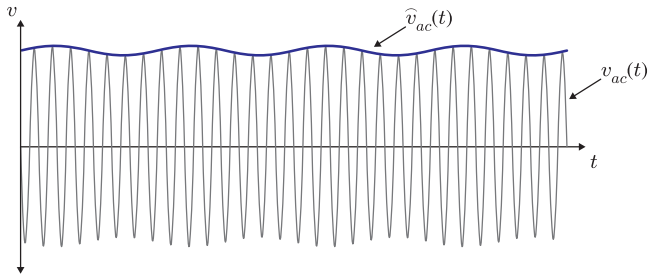

Fig. 6. An ac signal's envelope is its time-varying amplitude. It is denoted by a round hatted variable in this article, as shown in this example ac voltage.

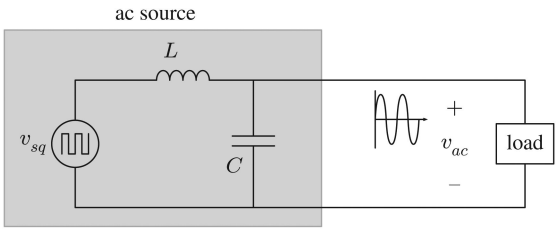

Fig. 7. An example ac source composed of a controlled square wave and a resonant LC output filter.

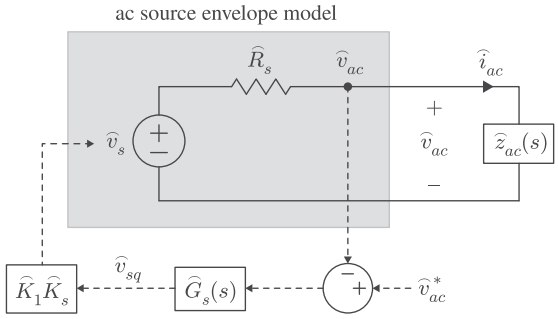

Fig. 8. Envelope model for a regulated ac source resembling Fig. 7.

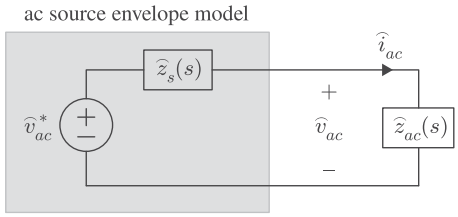

Fig. 9. Thevenin equivalent circuit for envelope model for a regulated ac source from Fig. 8.

that an ac system can be transformed into a representative dc system, for which established stability methods for dc systems can be employed. This is reminiscent of d–q analysis directly on three-phase systems, or on single-phase systems using the Hilbert transform. In a sense, shifting a single-phase system into the d–q frame is a way to investigate the envelope. Examples of the technique may be found in high-power applications such as electric locomotives, but are otherwise uncommon [15]–[17]. Such single-phase d–q frame analysis is complicated, and generally requires MIMO stability criteria [17]. In comparison, EIs are easier to measure, permit typical SISO stability criteria, and are simpler to determine analytically; thus, this approach can better inform design decisions. Furthermore, the EI works well for loads that respond to the envelope of the ac voltage, such as the controllable-bandwidth converter presented in this work. In general, EI is a useful tool for evaluating stability for a source–load system where the interaction is sufficiently slow compared to the system line frequency.

This section first discusses how a regulated ac source can be modeled using this method, and how in combination with the EI of an ac load, a stability analysis can be performed. Then, the EI of the controllable-bandwidth CPL from the previous section is related to the equivalent circuit model that was presented. Finally, stability of the system as a function of the controllable CPL bandwidth is demonstrated.

A. Example AC Source

To consider the application of EI to ac sources, a simple example source is analyzed, shown in Fig. 7. In the example, a square wave is generated at the desired ac frequency, and an LC resonant output filter shapes the output voltage v_{ac}. The regulated ac source implements feedback control to maintain output voltage at the desired magnitude. In envelope notation, the reference output voltage envelope is $\widehat{v}^*_{\text{ac}}$. Let $\widehat{G}_s(s)$ describe the dynamics of the output voltage sensing and compensator of the ac source, which outputs a square wave with envelope $\widehat{v}_{sq}$. The fundamental component of the square wave is $\widehat{K}_1\widehat{v}_{sq}$, where $\widehat{K}_1 = 4/\pi$. The LC output filter can be modeled in two steps. First, the filter amplifies the square wave fundamental by a factor $\widehat{K}_s$, which depends on the filter components, as well as the steady-state load. Second, an increase in load current magnitude will reduce the output voltage magnitude, which will reflect in the envelopes and can be expressed as a resistance $\widehat{R}_s$. This relationship will also be dependent on the filter components and steady-state load. These parameters of the ac source, as well as the EI of the load $\widehat{z}_{\text{ac}}(s)$, are shown in Fig. 8.

The Thevenin voltage is equal to the unloaded output of the ac source, which is the reference ac voltage $\widehat{v}^*_{\text{ac}}$. For stability analysis, the equivalent impedance of the ac source is determined. The equivalent envelope impedance $\widehat{z}_s(s)$, determined from the circuit in Fig. 8, is

$$\widehat{z}_s(s) = \frac{\widehat{R}_s}{1 + \widehat{K}_1\widehat{K}_s\widehat{G}_s(s)}. \tag{13}$$

The equivalent envelope model and load are shown in Fig. 9.

B. AC CPL Envelope Impedance

This analysis will evaluate the stability of this example ac source with the controllable CPL bandwidth ac load from Section II. For a PFC load, voltage on either side of the rectifier is related as $v_{dc} = |v_{\text{ac}}|$. Therefore, the dc and ac voltage envelopes are equal, and similarly with current. Thus, EI on the ac side can be approximated in terms of the dc-side small-signal impedance.

To illustrate this concept, a converter implementing the control scheme from Fig. 3 was tested. AC measurements are shown in Fig. 10 and compared with the small-signal impedance model

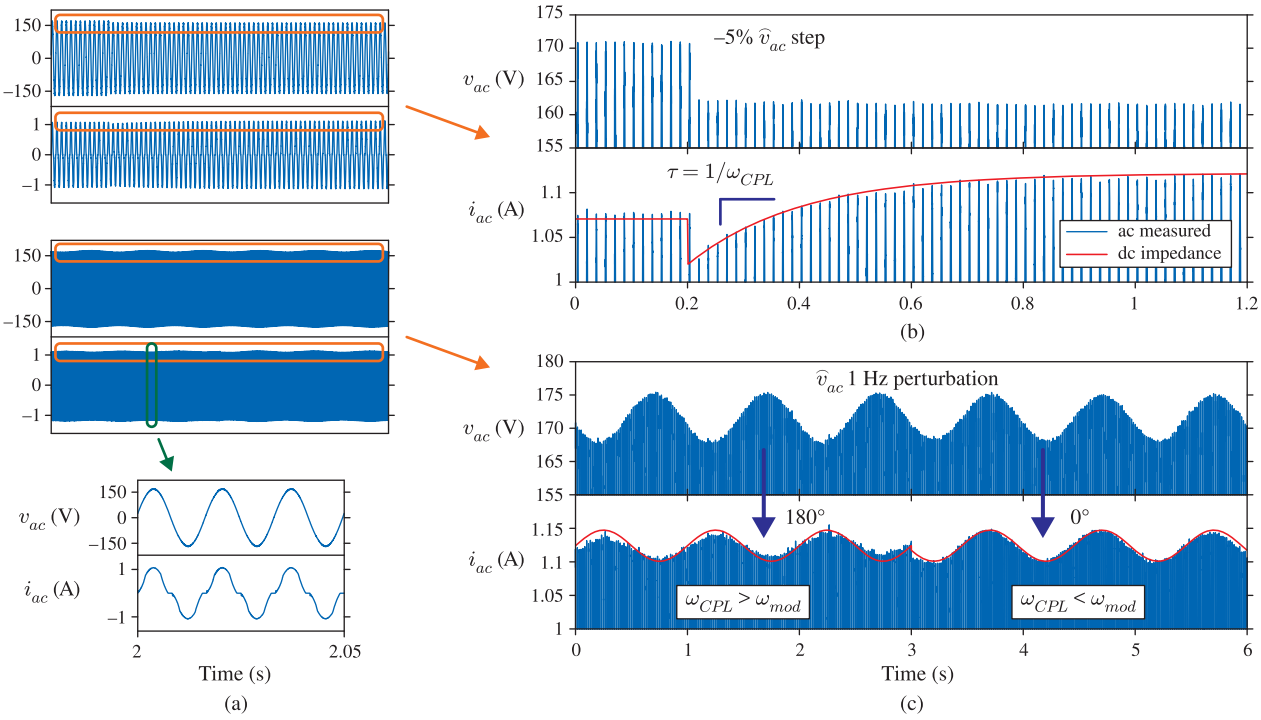

Fig. 10. Measured envelope response of the controllable input bandwidth ac CPL. (a) AC load implements power-factor correction. (b) In response to a –5% step in input voltage envelope, input current envelope initially resembles a resistive load, and resembles a CPL over a time scale determined by the controllable bandwidth ω_{CPL}. (c) Envelope response to ac voltage modulation. ω_{CPL} determines behavior at a given modulation frequency.

(10). Input current for the PFC converter is shown in Fig. 10(a). An envelope voltage step test is shown in Fig. 10(b) with the converter operating at $\omega_{\text{CPL}} = 2\pi 10$ rad/s, in which ac voltage envelope is stepped –5% at $t = 0.2$ s. The resulting measured ac input current is shown. The current labeled "dc impedance" is the resulting current from an equivalent dc voltage step acting on the impedance (10). Both ac envelope and dc response show approximately the same behavior.

Similarly, an amplitude modulation test is shown in Fig. 10(c), in which the input voltage envelope is perturbed at 1 Hz. The CPL operates at $\omega_{\text{CPL}} = 2\pi 10$ rad/s until $t = 3$ s, and then switches to $\omega_{\text{CPL}} = 2\pi 0.1$ rad/s operation. Again, the resulting ac measured current and equivalent dc impedance response from (10) are shown. The voltage and current envelopes have approximately 180° phase difference when CPL bandwidth is higher than modulation frequency, implying negative resistance CPL behavior. The phase is approximately 0° when CPL bandwidth is lower than modulation frequency.

Thus, the agreement in both tests validates that the dc impedance (10) can be used to model the ac load EI $\widehat{z}_{dc}$ at frequencies below the ac line frequency. This approximation will be used in the following envelope stability analysis.

C. Source–Load Stability Analysis

With EI models for both the ac source and CPL, a stability analysis can be performed. The system, as shown in Fig. 9, is stable if $\widehat{v}_{\text{ac}}$ is stable. The voltage can be expressed as

$$\frac{\widehat{v}_{\text{ac}}}{\widehat{v}^{*}_{\text{ac}}} = \frac{1}{1 + \frac{\widehat{z}_s(s)}{\widehat{z}_{\text{ac}}(s)}}. \tag{14}$$

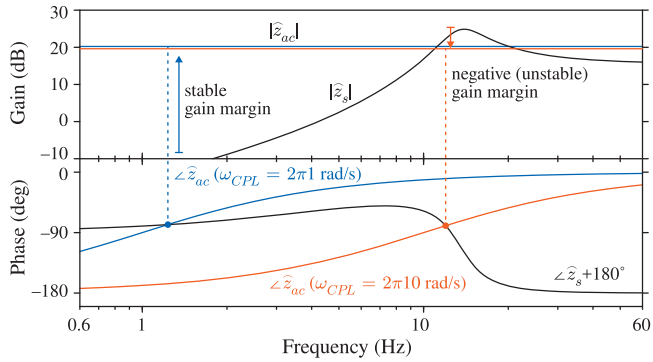

Fig. 11. Bode plot of source and load envelope impedances $\widehat{z}_s$ and $\widehat{z}_{\text{ac}}$, respectively, for gain margin stability analysis. There is negative gain margin with the CPL operating at bandwidth $f_{\text{CPL}} = 10$ Hz, implying a possible unstable interaction with the source. A stable gain margin is achieved with a reduced CPL bandwidth $f_{\text{CPL}} = 1$ Hz.

Stability can be assessed by analyzing the gain margin since $\widehat{z}_s/\widehat{z}_{\text{ac}}$ in (14) resembles the loop gain of a feedback control system [1], [2]. Gain margin is analyzed at the phase crossover frequency, when $\angle(\widehat{z}_s/\widehat{z}_{\text{ac}}) = 180°$, or equivalently, when $\angle\widehat{z}_{\text{ac}} = \angle\widehat{z}_s + 180°$. Envelope stability is implied if there is positive gain margin at the phase crossover frequency, such that $|\widehat{z}_s| < |\widehat{z}_{\text{ac}}|$.

AC source and CPL EIs are shown in Fig. 11 for gain margin stability analysis. The source is modeled as (13), with $\widehat{R}_s = 6\,\Omega$, $\widehat{K}_1 = 4/\pi$, and $\widehat{K}_s = 1.8$. $\widehat{G}_s(s)$ is modeled as a low-pass filter for ac voltage sensing, and an integrator for control

$$\widehat{G}_s(s) = \frac{\omega_s}{s + \omega_s}\frac{K_i}{s} \tag{15}$$

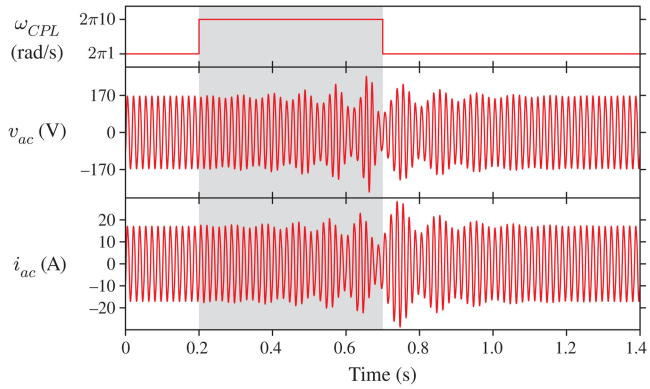

Fig. 12. Simulated load voltage and current for controllable bandwidth ac CPL from Fig. 3, and regulated ac source modeled in this section. Gain margin stability analysis from Fig. 11 predicts critical CPL bandwidth f_{CPL} for stable source– load interaction.

with $\omega_s = 2\pi 5$ rad/s and $K_i = 100$. The ac CPL is modeled as (10), with $C_{dc} = 1$ μF and $Y_{dc} = 0.1$ S. $\widehat{z}_{\text{ac}}$ for the CPL is shown at two CPL bandwidths. With the load operating at $\omega_{\text{CPL}} = 2\pi 10$ rad/s, Fig. 11 shows that the gain margin stability condition is not met since $|\widehat{z}_s| > |\widehat{z}_{\text{ac}}|$ at the phase crossover frequency, and so system stability cannot be guaranteed. However, with a reduced CPL bandwidth $\omega_{\text{CPL}} = 2\pi 1$ rad/s, the gain margin is positive, implying that the system is stable.

To validate the EI stability analysis, a simulated result is shown in Fig. 12. The interaction between an ac source and CPL as defined for the EI stability analysis was observed in a SPICE simulation. At the start of the measurement, the ac CPL is operating at $\omega_{\text{CPL}} = 2\pi 1$ rad/s, which was a stable condition in the stability analysis, and stable envelope behavior is observed. At $t = 0.2$ s, the CPL transitions to operating at increased bandwidth $\omega_{\text{CPL}} = 2\pi 10$ rad/s. The gain margin from Fig. 11 suggested this condition could induce an instability, and in fact, an envelope instability develops in the simulation. At $t = 0.7$ s, CPL bandwidth is reduced back to $\omega_{\text{CPL}} = 2\pi 1$ rad/s, and envelope stability is restored.

This section demonstrated how EI can be used as a tool for ac stability analysis of regulated sources and CPLs. For ac sources with unknown model parameters, the equivalent EI can be measured directly as described in [14]. Then, together with known EI of ac CPLs, and the control strategy from Section II that allows for controllable CPL bandwidth, a graphical gain margin analysis of the EIs can be used to determine stable operating conditions. Reducing the CPL bandwidth using the energy buffer control strategy improves or restores the stability of the source–load envelope interaction.

IV. Envelope Impedance Stability Demonstration

While the EI approach to evaluating system stability is clearly supported by simulation, this form of verification ignores many real-life variables, particularly losses, that can actually stabilize the system. A high-value, low-frequency inductor will incur significant core losses. To allay these concerns and further fortify the technique, this section demonstrates stability and instability of a 240-W PFC CPL connected to a resonant ac source.

The experimental setup is shown in Figs. 13 and 14 and consists of a resonant ac source connected to a PFC CPL. The CPL is a LT8312-based PFC controlled by a PSoC 5LP microcontroller [5]. A dc source and buck converter generates the amplitude of the square-wave source in Fig. 7. To match the model as closely as possible, the buck converter needs to appear like an ideal dependent source. The converter also needs to source and sink large amounts of reactive power because of the switched *LC* load. To meet these requirements, a bidirectional buck converter was implemented with a 50-kHz switching frequency, large input buffer capacitance, and 1-kHz unity-gain bandwidth. The high bandwidth will prevent converter dynamics from affecting the system. The dc source is implemented as a variable transformer connected through a full-bridge rectifier to a large capacitor. The capacitor voltage will have 120-Hz ripple, but the buck converter is effective at blocking this component. The buck converter and H-bridge inverter are implemented separately with Texas Instruments TMDSHVMTRPFCKIT development kits. The inverter chops the output of the buck converter to generate the square wave and feed the resonant *LC* filter. Here, the value of L is 10.5 μH and C is 300 μF. The resonant frequency is approximately 90 Hz. The output of the filter is passed through an isolation transformer to simplify grounding in other parts of the setup. The transformer introduces minimal parasitics to the circuit.

The ac source is also designed to emulate the envelope feedback shown in Fig. 8. The output voltage is sensed through a full-bridge rectifier, effectively obtaining the absolute value. The signals pass through a low-pass filter $G_1(s)$ defined by

$$G_1(s) = \frac{\omega_s}{s + \omega_s}. \tag{16}$$

As long as ω_s is much less than line angular frequency and variations in $\widehat{v}_{\text{ac}}$ are small, the output is

$$G_1(s)|v_{\text{ac}}| \approx \alpha G_1(s)\widehat{v}_{\text{ac}} \tag{17}$$

because the twice-line-frequency ripple in $|v_{\text{ac}}|$ will be filtered out. The result effectively averages $|v_{\text{ac}}|$, which will be different from $\widehat{v}_{\text{ac}}$ by a scaling constantα. It is possible to pull an amplitude out of v_{ac} using an appropriate, phase-locked sine wave. That approach performs poorly near-zero crossings, and will generate singularities. The phase of the ac source also depends on the load, which will also cause the method to fail.

The output of the low-pass filter feeds into the error amplifier. $\widehat{v}^*_{\text{ac}}$ must be appropriately scaled to give the correct output voltage. The error signal passes through the integrator defined by

$$\widehat{G}_2(s) = \frac{K_i}{s}. \tag{18}$$

The resulting signal is the command input for the buck converter, and the loop is closed. Note that $\widehat{G}_s(s) = G_1(s)\widehat{G}_2(s)$, giving the same control dynamics, as in Fig. 8.

To evaluate system stability, a 240-W PFC CPL is connected to the resonant ac source and ω_{CPL} is varied between two values on opposite sides of the edge of stability. Here, ω_s is $2\pi 5$ rad/s and ω_{CPL} is varied between $2\pi 1$ and $2\pi 10$ rad/s. This CPL consumes significantly less power than in the example at the end

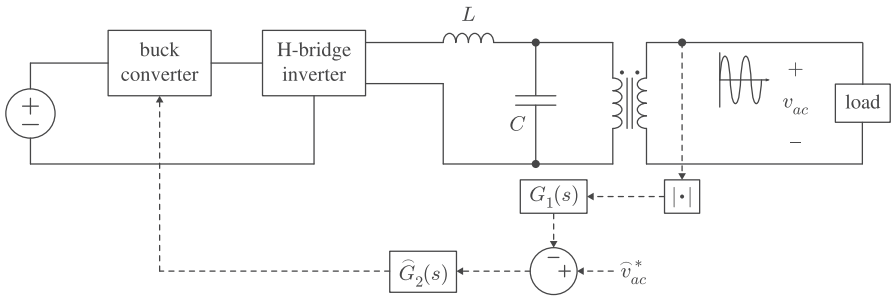

Fig. 13. Experimental setup for testing envelope-impedance-based stability analysis. The resonant ac source is a practical analog to the theoretical source in Fig. 8.

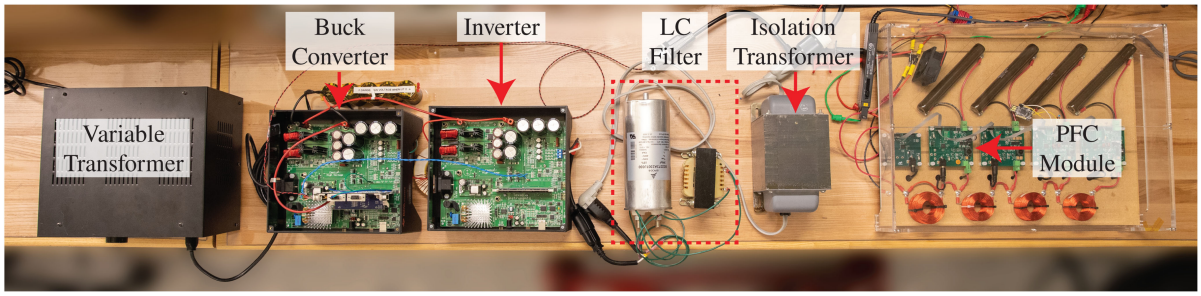

Fig. 14. Annotated experimental setup for testing envelope-impedance-based stability analysis.

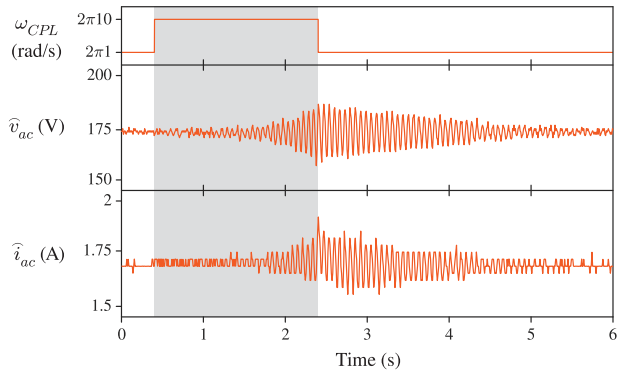

Fig. 15. Experimental load voltage and current amplitudes for controllable bandwidth ac CPL from Fig. 3, and regulated ac source as shown in Fig. 13.

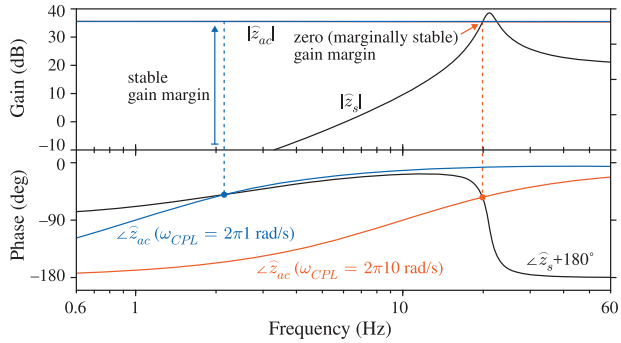

Fig. 16. Bode plot of source and load envelope impedances $\widehat{z}_s$ and $\widehat{z}_{ac}$, respectively, for gain margin stability analysis of the experimental setup. There is zero gain margin with the CPL operating at bandwidth $f_{CPL} = 10$ Hz, implying a marginally stable interaction with the source. A stable gain margin is achieved with a reduced CPL bandwidth $f_{CPL} = 1$ Hz.

of Section III, and will not go unstable based on the analysis. To account for this, the integrator gain K_i is approximately quadrupled and ω_s is lowed to $2\pi 2.5$ rad/s. Further, the value of $\widehat{K}_s$ and $\widehat{R}_s$ will change with the change in load and introduction of nonideal components.

The result of this experiment is given in Fig. 15. For visual clarity, the approximate amplitudes are plotted. The approximate amplitudes $\widehat{v}_{ac}$ and $\widehat{i}_{ac}$ are simply the peak values of $|v_{ac}|$ and $|I_{ac}|$, respectively, in each half-line cycle. The system is initially stable at a lower CPL bandwidth, but goes unstable when the bandwidth is increased. The value of K_i has been tuned to place the higher bandwidth extremely close to the edge of stability. After the bandwidth is lowered, the system immediately stops the exponentially rising oscillation, and damps the oscillation back to zero. Since the bandwidth of the PFC CPL is controllable, it is possible for the load to detect the oscillation and reduce the bandwidth to bring the system back to stability.

It is also possible to use the presented analytical stability analysis to check the agreement between the analysis and experimental results. The system can be empirically measured as in [14], but this technique can be difficult to implement without the appropriate equipment. Here, the system is well defined, and a simple parametric extraction is sufficient. The resonant ac source is operated with a fixed buck converter command, and loaded with resistors between 200 and 250 W. Measurements of buck converter output voltage, load voltage, and load current provide information about $\widehat{K}_s$ and $\widehat{R}_s$. These numbers account for nonidealities, and will work at the 240-W operating point.

Fig. 16 is an updated version of Fig. 11 with new values. Other updated parameters are $C_{dc} = 3$ μF and $Y_{dc} = 16.7$ mS. Once

again, stable operation is predicted at the lower CPL bandwidth of $2\pi 1$ rad/s. However, the higher CPL bandwidth corresponds to a system with approximately zero gain margin, implying that the system is marginally stable if the measurements and model are perfect. Since the system was tuned to be very close to marginal stability, this is an excellent result, showing good agreement between the analytical stability analysis and experimental results. While we have focused on the controllable CPL bandwidth in this work, the stability analysis demonstrated here could be performed for any of the parameters present in the system to evaluate stability.

V. Conclusion

This article has explored stability concerns for CPLs operating in ac systems. An ac CPL is commonly implemented with power-factor correction, and as such, is designed with a constant-power control bandwidth that is less than the ac voltage frequency. CPL stability concerns are not as common in ac systems, partly because of this control bandwidth limitation. However, unstable interaction between an ac CPL and a regulated ac source, such as a UPS, has been observed. This article discusses EI, which can be used to model the output behavior of an ac source and input behavior of an ac CPL. Using traditional stability methods, the EI relationship can be used to determine if the two elements are stable together. In the case that the impedance relationship reveals a possible instability, the presented ac CPL control scheme allows for apparent reduction of the CPL bandwidth, which improves stability of the source–load interaction. This modification comes at no expense to output load regulation with the use of a two-stage converter and energy buffer. Future work will focus on reusing the current shaping capabilities of a PFC converter to measure EI, and use the analysis presented here to predict the region of instability.

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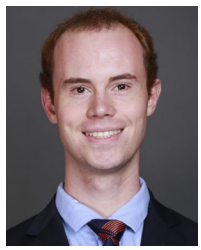

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