Self-Synchronized Class E Resonant Rectifier by Compensating Propagation Delay for Multi-MHz Switching Applications

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***Abstract*—In this article, a self-synchronized, high-frequency class E resonant rectifier is proposed to compensate for the synchronization signal mismatch due to the propagation delay. The synchronous rectification helps the power conversion system increase its efficiency by using active devices such as MOSFETS instead of diodes. Even with the MOSFETS, it is still challenging to generate an accurate synchronous signal from the input source in the multi-MHz wireless power transfer (WPT) systems due to the propagation delay from the integrated circuit (IC) components and the gate driver. In general, the propagation delay is more than 10 ns, a significant period in the multi-MHz operation. To mitigate the propagation delay, we present the self-synchronized rectifier, sensing the signal in the C_s-L_s network. The proposed design creates a proper gate signal to the active device in the rectifier by measuring the voltage of the node between C_s-L_s resonant filter. In the experiments, we tested the driving method in the class E rectifier at an output power of 228 W and a switching frequency of 13.56 MHz. While the total propagation delay was 8 ns, including the gate-driver and comparator, the leading phase of the sensing voltage successfully offsets the driver's propagation delay.**

***Index Terms*—Rectifiers, resonant power conversion, synchronization, synchronous detection.**

I. Introduction

COMPACT and efficient power converters for wireless power transfer (WPT) are crucial to develop a sustainable charging system [2]–[5]. In a conventional WPT system consisting of a dc–ac inverter, coupling coils, and an ac–dc rectifier, the rectifier must be small enough to be embedded in the vehicles or devices. The high-frequency operation allows a reduction in weight and improvement in power density. However, MHz frequencies are not favored in a conventional power converter due to high switching losses. To overcome this issue, resonant rectifiers with wide band-gap semiconductors are widely used to provide high-frequency operation by using soft-switching.

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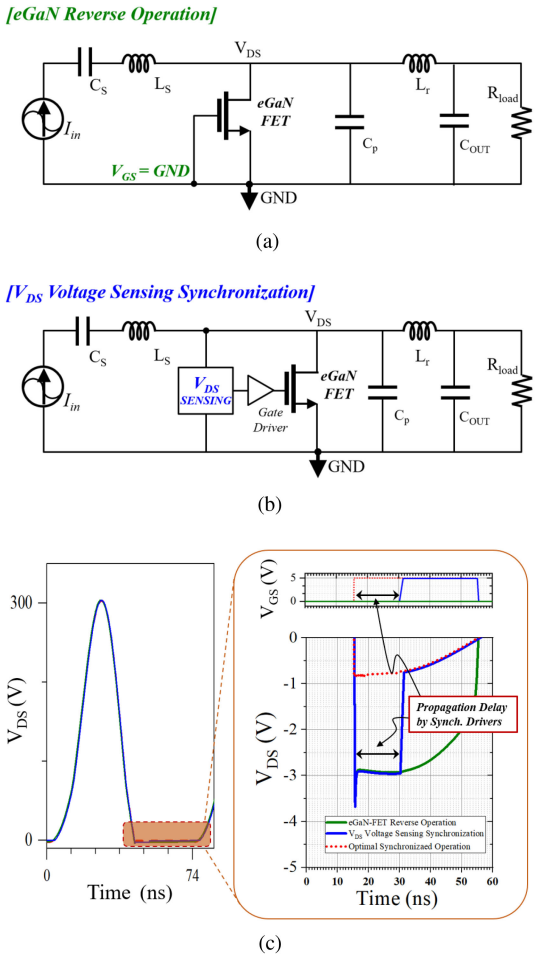

Fig. 1. Class E resonant rectifier operation with the eGaN-FET: (a) diode mode operation (eGaN reverse operation), (b) synchronous rectifying operation, and (c) V_{DS} turn-ON waveform [1].

For example, a class E resonant rectifier achieves zero voltage switching (ZVS) and zero dv/dt operation in a switching device by tuning the passive components [6], [7]. Fig. 1(a) shows a class E rectifier with an eGaN-FET operating under the diode mode without any gate signal [8]. However, the forward voltage drop, $V_F = V_{\text{th}} + I_{\text{on}} R_{\text{on}}$, causes a high conduction loss. To increase efficiency, the enhancement mode gallium nitride field effect transistor (eGaN-FET) needs to operate as an active switch mode shown in Fig. 1(b), called synchronous rectification. In a

dc-to-dc power converter, the gate signal to the FET in the rectifier has to be synchronized to the gate signal of the active device in the inverter. However, in a long-distance WPT system at high frequencies, it is challenging to generate a synchronized gate signal during a short period.

To provide accurate gate voltages, various methods have been studied [3], [4], [9]–[13]. For example, a band-pass matching network between the inverter and rectifier was used to minimize the phase shift between the drain–source voltage of the inverter and rectifier [3], [9]. The matching network allows the rectifier to be synchronized by utilizing the gate signal from the inverter without an additional synchronized gate driver. However, this is not suitable for the mid-range WPT system to communicate the gate signals between the transmitting and receiving sides because of the physical distance between them.

Furthermore, an FPGA-based phase-difference compensation method was proposed to detect the input current phase and control the gate signal for the input impedance adjustment [4], [11]. When the clock frequency is 244 MHz in the commercial FPGA, it can generate the gate signal with 10° of the phase resolution under the 6.78 MHz of the operating frequency [4]. Due to a limitation to the phase control resolution, increasing the clock frequency above the GHz range is necessary to perform the precise operation. However, the commercial FPGA controllers have limited global clock operation. In other ways, phase-lock loop (PLL) and application-specific integrated circuit (ASIC) are appropriate approaches to solve the problems. [14]. Although these methods can control the signal delay, they must have a precise reference signal or detection method. If the detected signal is inaccurate with the error and noises, it is difficult to generate a proper gate signal. In order to provide the pure reference signal, the detected signal is purified by the high-order filters or IIR filtering. However, it still has some issues, such as nonlinear phase variation under the load variant condition.

Also, there is a method to detect the $V_{\rm DS}$ signal and synchronize it as quickly as possible without the phase control [15]. If we accurately detect the ZVS duration, we can generate the same phase or inverted gate signal. By using a voltage divider, the $V_{\rm DS}$ is reduced to a logic-level magnitude to generate a synchronized gate signal with a comparator. However, the propagation delay of the voltage detection circuits and the gate-driver is significant in high-frequency operation, which degrades the performance of the rectifier, as shown in the Fig. 1(b). To overcome this issue in the direct voltage sensing method, the propagation delay must be reduced or compensated in an appropriate solution.

Therefore, this article proposes a new self-synchronization method to mitigate the propagation delay from the driving circuit in the class E rectifier. The proposed $C-L$ voltage detection method generates the gate signal for the turn-ON trigger instead of synchronizing from the external gate signal or the controller base phase compensation. The compensated propagation delay value was designed by using L_s value based on the equations and the driver's propagation delay. The proposed synchronization structure successfully generated the proper gate signal and operated the self-synchronized class E rectifier. The designed self-synchronized rectifiers demonstrated with the RF inverter as a current source under the load variant condition, 20–50 Ω and input variant condition, 3–5 A.

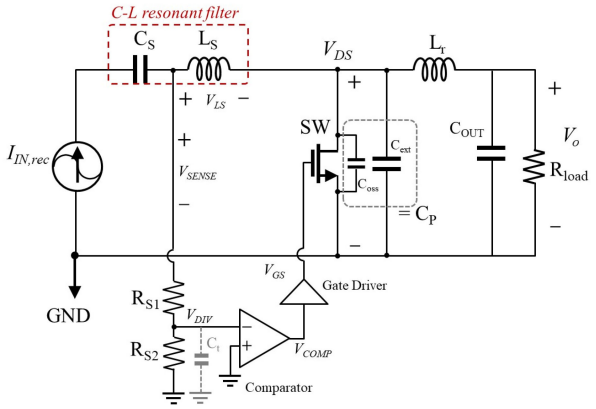

Fig. 2. Proposed self-synchronized class E resonant rectifier circuit.

II. Self-Synchronized Class E Resonant Rectifier Design

A. Class E Resonant Rectifier Design

Fig. 2 shows the circuit diagram of the proposed self-synchronized class E resonant rectifier. The output voltage is calculated by the input power and load resistance ($R_{\rm load}$) when we assume that the input impedance of the rectifier is purely resistive. However, the phase of the input impedance can be inductive or capacitive when the load or input power conditions are changed. The parallel capacitor (C_p) and the resonant output inductor (L_r) are the main factors to determine the class E rectifier's performance. The C_p and L_r are selected to follow these relationships: 1) maximum absolute value of the impedance seen by rectifier versus normalized capacitance (C_n), 2) normalized peak drain voltage versus normalized capacitance, and 3) normalized inductance (L_n) versus normalized capacitance [6], [7]. In this article, C_n is chosen to provide the minimum drain peak voltage and the minimum input impedance phase degree based on the minimum/maximum power ratio. These power ratios have a difference C_n and L_n relationship, which shows the different input impedance conditions under the load variance condition. We choose the 2:1 power ratio to minimize the phase-shift of the input impedance. The C_p value is calculated by using the C_n from the equation below [7]:

$$C_p = C_n \frac{P_{o,\max}}{2\pi f_s V_o^2} \tag{1}$$

where the C_p is the total capacitance, including the output capacitance of the device $C_{\rm oss}$ and external capacitor $C_{\rm ext}$, $P_{o,\max}$ is the maximum output power, f_s is the switching frequency, and V_o is the output voltage. The $C_{\rm oss}$ capacitance value is a nonlinear value, a function of $V_{\rm DS}$. To simplify the analysis, we assume a constant value by extracting the $C_{\rm oss}$ value at the operating $V_{\rm DS}$. Then, we define the C_p value as the sum of $C_{\rm oss}$ and $C_{\rm ext}$. Considering the output power, the switching frequency, output voltage, and the switch's equivalent internal capacitance value, we determine the proper C_n value. From the C_n versus L_n relationship, we find the appropriate L_n value and induce

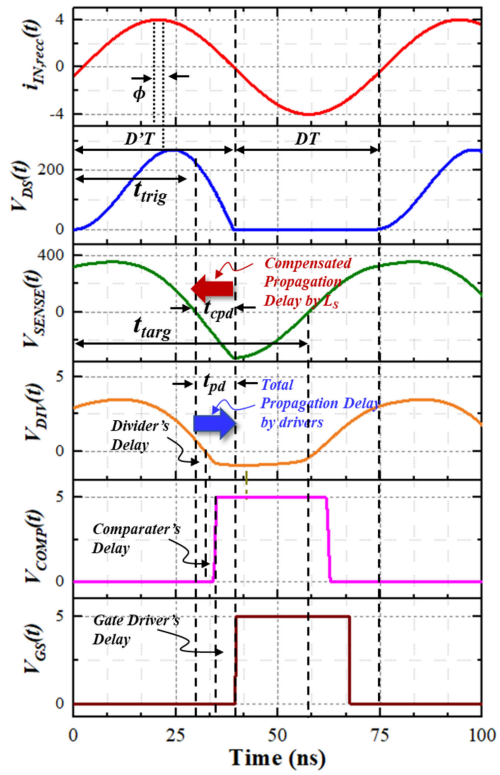

Fig. 3. Operation waveforms of the proposed self-synchronized class E rectifier.

the L_r value as the following equation [7]:

$$L_r = L_n \frac{V_o^2}{2\pi f_s P_{o,\max}}. \tag{2}$$

The C_s-L_s filter is used not only for voltage detection for synchronization but also works as an input filter for the input source of the rectifier. The $C_s - L_s$ filter resonates at the operating frequency, and it provides high purity of the rectifier input. The series Cs-Ls filter can be tuned by the equations

$$Q_{filter} = \frac{1}{R_{\text{rect,min}}}\sqrt{\frac{L_s}{C_s}} \tag{3}$$

where C_s and L_s are the input filter capacitance and inductance, respectively, $R_{\text{rect,min}}$ is the minimum value of the magnitude of the input impedance, and Q_{filter} is the quality factor of the C_s-L_s filter.

From the design specifications and the parameter relationships under $P_o = 250$ W, $f_s = 13.56$ MHz and $R_{\text{load}} = 25\ \Omega$, the calculated C_p is 421 pF, and L_r is 196 nH, when C_n is 0.92 and the L_n is 0.67. The input L_s-C_s filter operates at the resonant frequency, the same as the switching frequency. The C_t is a tuning capacitor that reduces sensing noises with voltage dividers by using 10–40 pF.

B. Proposed Method for Synchronization

For highly precise synchronization, the gate-driver circuitry must detect the ON/OFF transition in ZVS operation and synchronize it with the gate signal. At MHz frequencies, the switching turn-ON/OFF time is relatively short, and the propagation delay in the gate-driver and sensing circuits causes a non-ZVS operation. The total propagation delay ($=t_{pd}$) by the synchronization driver is defined as the total amount of the separated propagation delays

$$t_{pd} = t_{pd,\text{divider}} + t_{pd,\text{comp}} + t_{pd,gd} \tag{4}$$

where $t_{pd,\text{divider}}$ is the propagation delay of the voltage dividers, and $t_{pd,\text{comp}}$ is the propagation delay of the comparator. The $t_{pd,\text{comp}}$ is defined at the rising edge between the input signal and the output signal of the comparator. The $t_{pd,gd}$ is the delay between the input signal and the output signal of the gate-driver at the rising edge. The $t_{pd,gd}$ does not have any rising time by the slew-rate.

Fig. 2 shows the proposed self-synchronizing circuit to solve this problem by generating a proper gate signal using the voltage between C_s-L_s resonant network. The voltage between the C_s and L_s components, V_{SENSE}, has a sinusoidal waveform with a dc offset value. This voltage is used to synchronize the gate signal automatically because it leads the phase to the switching device's drain–source voltage (V_{DS}), which compensates for the propagation delays of the gate-driver and sensing circuits. To transfer the divided voltage signal (V_{DIV}) to the comparator, the sensing voltage level is reduced by 200:1 with the resistive voltage dividers. When the sensing voltage is negative, the comparator with an inverting structure generates a turn-ON signal, V_{COMP}. The sensing voltage is as follows:

$$V_{SENSE}(t) = V_{DS}(t) + V_{LS}(t). \tag{5}$$

Assume that the rectifier's input impedance is resistive and the rectifier has a pure sinusoidal input current as follows:

$$I_{IN,rec}(t) = I_{IN} sin(wt + \phi) \tag{6}$$

where I_{IN} implies the magnitude of the source current, ω_s indicates the frequency of the source current, and ϕ represents the phase difference between the drain–source voltage and the source current. Because the V_{DS} is nonsinusoidal, the V_{SENSE} is determined by calculating in the time domain. When the rectifier's input current is sinusoidal, the V_{SENSE} is calculated by taking the voltage drop of L_s component

$$V_{SENSE}(t) = V_{DS}(t) + L_s \frac{dI_{\text{IN,rec}}(t)}{dt}. \tag{7}$$

Assuming that the circuit's propagation delay has always been less than half of the period, the rectifier's V_{DS} equation is [7]:

$$V_{SENSE}(t) = V_{DS}(t) + w_s L_s I_{IN} cos(w_s t + \phi). \tag{8}$$

The reverse drain-source voltage waveform is given by [7]

$$V_{DS}(t) = \frac{I_{\text{IN}} w_s L_r}{(\frac{w_s}{w_r})^2 - 1}\Big[\sin(w_s t)\sin(\phi) - \frac{Z_r}{w_s L_r}\sin(w_r t)\sin(\phi) + \cos(w_r t)\cos(\phi) - \cos(w_s t)\cos(\phi)\Big] - V_o\cos(w_r t) - I_{IN} Z_r \sin(w_r t)\sin(\phi) + V_o, \text{ for } 0 \le t \le (1-D)T \tag{9}$$

where the resonant frequency (w_r) of the L_r-C_p is

$$w_r = \frac{1}{\sqrt{L_r C_p}} \tag{10}$$

and the characteristic impedance of the network is

$$Z_r = \sqrt{\frac{L_r}{C_p}}. \tag{11}$$

Therefore, $V_{\text{SENSE}}(t)$ is sum of a half-wave of V_{DS} and the phase-shifted sinusoidal values by L_s. When the $V_{\text{SENSE}}(t)$ value is zero, the turn-ON trigger time t_{trig} is derived

$$V_{DS}(t_{trig}) + w_s L_s I_{IN} cos(w_s t_{trig} + \phi) = 0, 0 < t_{trig} < D'T \tag{12}$$

$$t_{cpd} = D'T - t_{trig}. \tag{13}$$

The compensated propagation delay (t_{cpd}) by the L_s components

$$L_s = \frac{-V_{DS}(t_{trig})}{w_s I_{IN} cos(w_s t_{\text{trig}} + \phi)}. \tag{14}$$

When the driver's propagation delay (t_{pd}) is identical to the compensated propagation delay (t_{cpd}), the synchronized gate signal is generated accurately at the turn-ON timing. However, if t_{cpd} is higher than t_{pd} of the driver components, it causes a non-ZVS condition. If t_{cpd} is less than t_{pd} of the components, it induces a partial diode mode operation at the beginning of turn-ON period.

$$t_{cpd} \begin{cases} = t_{pd}, & \text{precise synchronization} \\ > t_{pd}, & \text{non-ZVS operation} \\ < t_{pd}, & \text{partial diode mode operation} \end{cases}$$

The turn-OFF trigger time (t_{targ}) of the synchronized gate signal is calculated under the zero-crossing point of V_{SENSE} during the ZVS duration ($D'T < t < T$). Because the V_{DS} is zero under the ZVS duration, V_{SENSE} is computed by only sinusoidal term based on equation (8)

$$V_{SENSE}(t_{targ}) = w_s L_s I_{IN} cos(w_s t_{targ} + \phi) = 0. \tag{15}$$

Under the zero-crossing point of V_{SENSE}, the turn-OFF trigger time t_{targ} is derived

$$w_s t_{targ} + \phi = \frac{3}{2}\pi, D'T < t_{targ} < T \tag{16}$$

$$t_{targ} = \frac{3}{4}T - \frac{\phi}{w_s}. \tag{17}$$

In addition, the pulse width (t_{width}) of the synchronized gate signal is expressed by the difference between turn-ON/turn-OFFtrigger time from equations (13) and (17)

$$t_{width} = t_{targ} - t_{trig}. \tag{18}$$

When we assume D is 0.5 and ϕ is zero, the pulse width is simplified as follows:

$$t_{width} = \frac{1}{4}T + t_{cpd}. \tag{19}$$

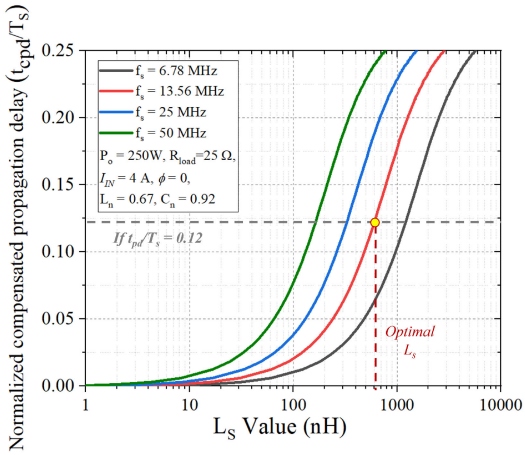

Fig. 4. Normalized compensated propagation delay in terms of the L_s inductance value under the various operating frequency.

The pulse width of the proposed method is changed from the quarter ($=T/4$) to the half period ($=T/2$) depending on the compensated propagation delay ($=t_{cpd}$) and the rectifier operation, such as D and ϕ.

The C_s-L_s value for self-synchronized rectifier is designed as the following equations:

$$C_s = \frac{1}{w_s^2 \sqrt{L_s}}. \tag{20}$$

Using (14), the optimal value of L_s for synchronization is extracted from the various multi-MHz condition, as shown in the Fig. 4. The optimal L_s value provides the perfect synchronization in turn-ON timing because the compensated propagation delay ($=t_{cpd}$) and the total propagation delay ($=t_p d$) are identical. The relationship between normalized compensated propagation delay and L_s was calculated under 250 W, $R_o = 25\ \Omega$, $\phi = 0\ °$, $\omega_r/\omega_s = 1.31$ from 6.78 to 50 MHz based on the ideal parameters (without any parasitic components) by using the Wolfram Mathematica simulation tool. This plot shows that the t_{cpd} is controlled by the L_s value. The L_s value is selected by the operating condition such as the operating frequency, the output power, and circuit parameter when the total propagation delay of the drivers is given. If we know the gate-driver's propagation delay to use, we can select the appropriate L_s design value. As illustrated in Fig. 4, the maximum compensation delay is the quarter of each frequency's period time ($T_s/4$). Because the allowable design of the driver's t_{pd} is in the narrow range ($T_s/4$) as the frequency increases, the propagation delay performance of the gate-driver and sensing circuits is critical when designing the self-synchronized class E rectifier for high-frequency operation.

The t_{cpd} value is analyzed by the phase difference (ϕ) between input current and drain-source voltage, as shown in the Fig. 5. The phase difference is the time difference between the peak value of fundamental V_{DS} and $I_{\text{IN,rec}}$ waveforms, as described in Fig. 3. The compensated propagation delay is calculated under 250 W, $R_o = 25\ \Omega$, $\omega_r/\omega_s = 1.31$ and 13.56 MHz class E rectifier based on the ideal parameter using the Wolfram Mathematica. It shows the phase difference affects the compensated propagation

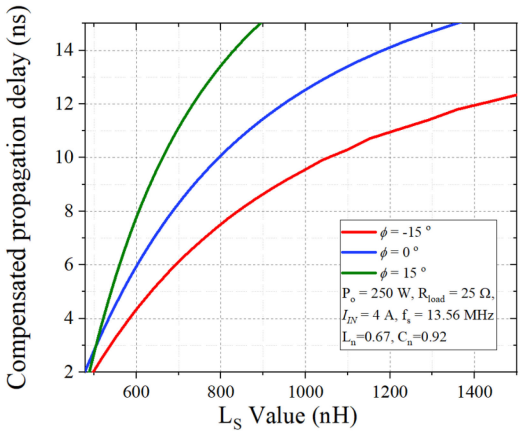

Fig. 5. Compensated propagation delay with respect to the L_s inductance value under the input voltage/current phase variance.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED SELF-SYNCHRONIZED CLASS E RECTIFIER

Parameter	Value	Type
I_{IN}	3-5 A	RF amplifier
R_{load}	20-50 Ω	Commercial dc resistors
f_s	13.56 MHz	Signal generator
L_r Q_{Lr}	200 nH 120	Custom inductor with air-core
L_s Q_{LS}	688 nH 300	Custom inductor with air-core
C_P C_S C_{out} R_{S1} R_{S2}	240 pF 200 pF 150 nF 220 kΩ 1.1 kΩ	Commercial ceramic Commercial ceramic Commercial ceramic Commercial Commercial
Comparator Gate Driver SW	LTC6752-2 LMG1025-Q1 GS66508T	Analog devices Texas instruments GaN systems

delay, and it causes the gate signal variation under the wide range load variant condition due to the input impedance variance of the rectifier. In order to reduce t_{cpd} variations, we need to select the low L_s value and reduce t_{pd} of the gate driver and sensing circuits.

III. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

The proposed self-synchronized class E rectifier was simulated in LTSpice, and the designed component values are represented in Table I. The propagation delays of the gate-driver and comparator were included in the simulation to obtain the appropriate calculation. We used the library models of the comparator, LTC6742-2 components. For the gate driver, the ideal CMOS inverter was designed and added delay between the comparator and CMOS inverter. The GS66508 T library was used as the eGaN-FET component for simulation. Fig. 6 shows the simulation waveform of the proposed self-synchronized

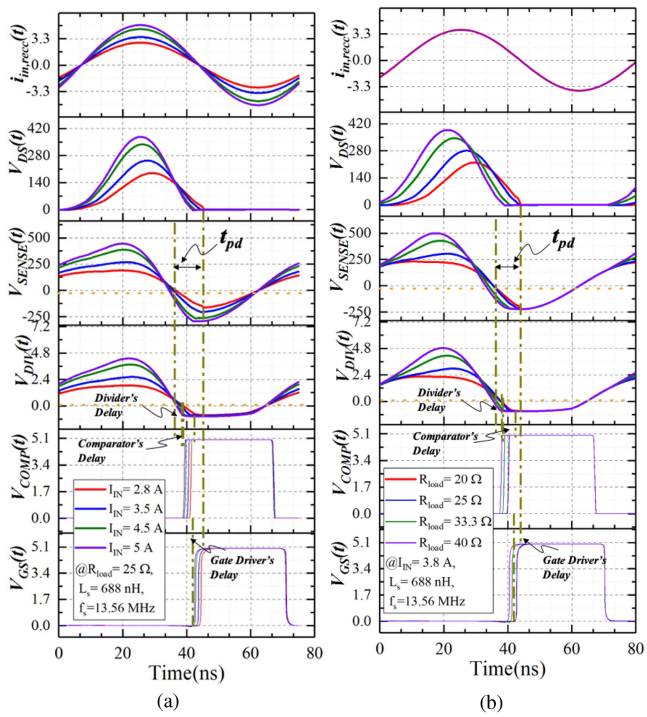

Fig. 6. Simulation waveforms of the self-synchronized class E rectifier: (a) Input current variance, (b) Output load variance.

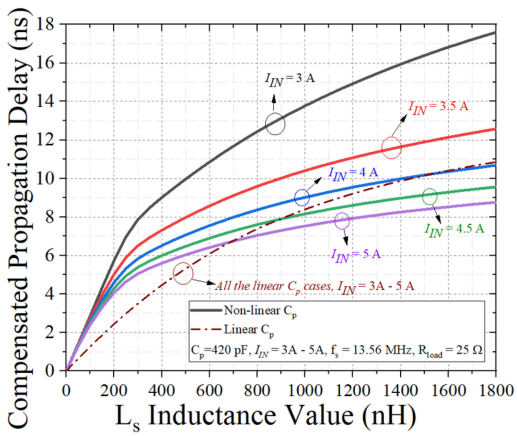

Fig. 7. Calculated compensated propagation delay (t_{cpd}) based on inductance value (L_s) depending on the input peak current under the non-linear/linear C_p condition.

rectifier with the different R_{load} and I_{IN} values. With the variant R_{load} or variant I_{IN} conditions, while the V_{DS} waveform changed and shifted, the generated gate signal adapts to synchronize with the ZVS period by shifting the phase. The simulated V_{SENSE} was 8 ns ahead of the V_{DS} ZVS period, while the V_{COMP} and V_{GS} were 8 ns behind the drain-source voltage. When the rectifier was simulated with a 13.56 MHz ac source, the efficiency was 95% at 250 W of rated output power.

The t_{cpd} value was calculated by the value of L_s, depending on the I_{IN} and R_{load} variations. As shown in Figs. 7 and 8, t_{cpd} varies with the total paralleled capacitor condition (linear/nonlinear). As mentioned in the previous section, the capacitance at the

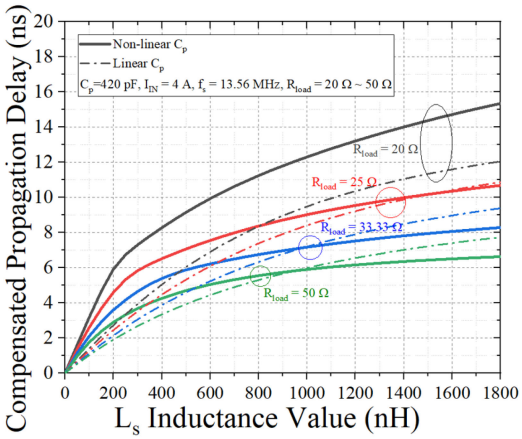

Fig. 8. Calculated compensated propagation delay (t_{cpd}) based on inductance value (L_s) depending on the load variance under the nonlinear/linear C_p condition.

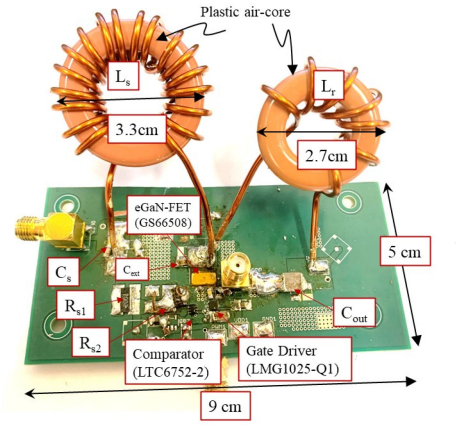

Fig. 9. Designed self-synchronized class E rectifier.

drain-source node consists of the two components, C_{oss} and C_{ext}. While C_{ext} shows a relatively constant value, C_{oss} of the switching device shows a nonlinear capacitance with V_{DS}.

In this simulation, we assume that C_p is either nonlinear or linear. While the linear C_p has a constant capacitance value, the nonlinear C_p, including the C_{oss} of GaN-FET, varies with different V_{DS} values. Fig. 7 shows the t_{cpd} has same results with the I_{IN} variations under the linear C_p operating condition. However, the t_{cpd} decreases when the I_{IN} increases under the nonlinear C_p condition because nonlinear C_p operation causes difference V_{DS} shape and turn-OFFduration. Fig. 8 shows the t_{cpd} by the L_s value according to the R_{load} variation. The nonlinear C_p operation has more variation of the t_{cpd} in specific L_s than the linear C_p operation. Therefore, reducing the nonlinear capacitance value is necessary by designing the ratio between linear/nonlinear capacitors to reduce the t_{cpd} variation. In this article, the C_p value was designed as 420 pF and we assumed the equivalent C_{oss} as 180 pF and added 240 pF as the commercial product.

B. Experimental Results

The self-synchronized class E rectifier was demonstrated in experiments using the C–L voltage detection method at 13.56 MHz. Fig. 9 depicts the self-synchronized class E rectifier. The design parameters of the self-synchronized class E rectifier are listed in Table I.

The t_{pd} of the gate driver and sensing circuits was measured as about 8 ns, and we designed the L_s value as 688 nH at the 250 W rated power condition. Toroidal-type, air-core inductors were designed and used to minimize the core loss of the high-frequency resonant rectifier. The L_s inductor was designed as a toroidal type using the plastic air-core, and the cross-sectional area of the air-core was 12 mm × 12 mm, and the outer diameter was 330 mm. The L_r inductor also was designed using the toroidal air-core plastic form with 7 mm × 11 mm cross-sectional area and the outer 270 mm diameter [16]. Other components, such as eGaN-FETs and capacitors, were commercially available products, and the PCB size was measured as 9 × 5 cm. An

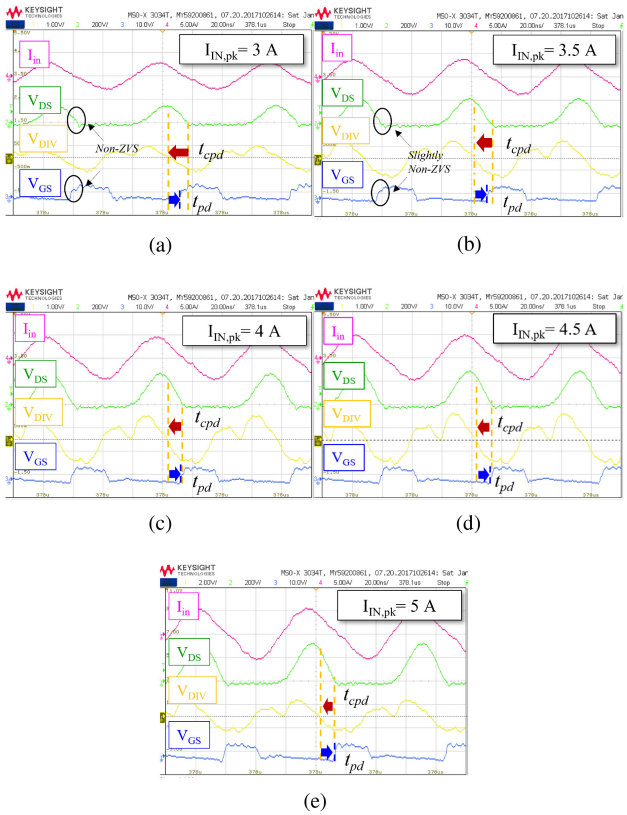

Fig. 10. Measured waveforms under the input current variance: (a) $I_{\text{IN}} = 3\ A$, (b) $I_{\text{IN}} = 3.5\ A$, (c) $I_{\text{IN}} = 4\ A$, (d) $I_{\text{IN}} = 4.5\ A$, (e) $I_{\text{IN}} = 5\ A$.

LMG1025-Q gate-driver was used to achieve a minimum level propagation delay (=2.5 ns). The sensing voltage signal was converted to a square wave signal using an LTC6752-2 comparator with a propagation delay of 3–5 ns. The resistive voltage dividers were composed of 220 $k\Omega$ and 1.1 $k\Omega$ resistors to convert the high sensing voltage to a low voltage. The 40 pF of C_t was added between the voltage divider and the comparator to minimize the sensing noise.

The operation waveforms of the self-synchronized class E rectifier were measured, as shown in the Figs. 10 and 11. RF linear amplifier supplied an input ac power to the rectifier, and the

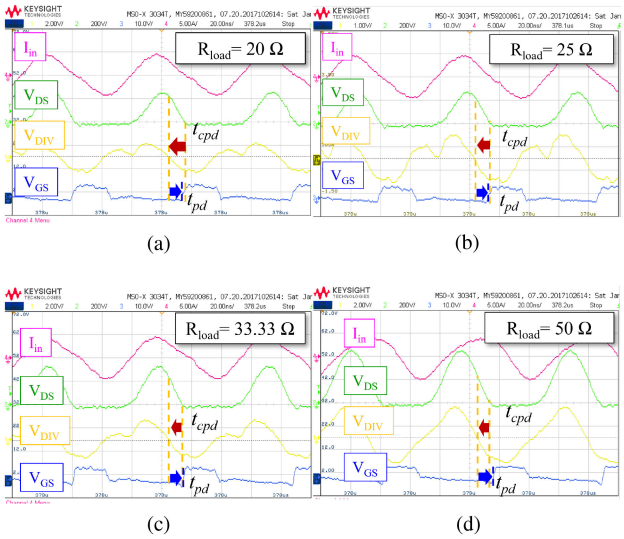

Fig. 11. Measured waveforms under the load variance: (a) $R_{\text{load}} = 20\ \Omega$, (b) $R_{\text{load}} = 25\ \Omega$, (c) $R_{\text{load}} = 33.33\ \Omega$, (d) $R_{\text{load}} = 50\ \Omega$.

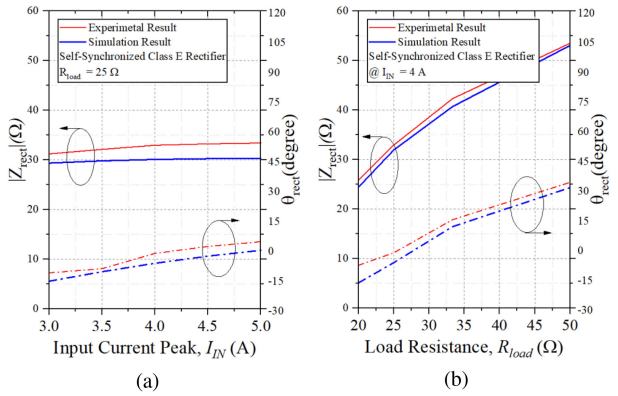

Fig. 12. Impedance of the self-synchronized class E rectifier was operated by using the ac RF source with the (a) variant current peak, and (b) variant load resistance.

rectifier operation was measured with different input currents. The V_{DIV} voltage was measured with a 0.5 pF dividing capacitor and 10:1 voltage probe in order to reduce additional propagation delay due to the internal filter of the voltage probe. The proposed class E rectifier generated the proper gate signal by adapting the input source variance. Because of the long t_{cpd} with the low I_{IN} value, non-ZVS appeared in V_{DS}, as shown Fig. 10(a). Also, with low R_{load}, the long t_{cpd} value caused non-ZVS condition, as shown in Fig. 11(a).

The input impedance of the self-synchronized class E rectifier (Z_{rect}) was calculated by using the V_{DS} and $I_{\text{IN,rec}}$ measurements, as shown in Fig. 12. The magnitude of the input impedance ($|Z_{\text{rect}}|$) was calculated by the fast fourier transform (FFT) results of V_{DS}. $I_{\text{IN,rec}}$ at 13.56 MHz and the phase of the input impedance (θ_{rect}) was measured the time difference of the fundamental peak point between V_{DS} and $I_{\text{IN,rec}}$. In this current-driven rectifier, the ϕ between V_{DS} and $I_{\text{IN,rec}}$ was determined by the Z_{rect} and the ϕ value had the opposite to the θ_{rect} value ($\theta_{\text{rect}} = -\phi$). Therefore, as the t_{cpd} increased in the Fig. 5 when the ϕ was positive, the

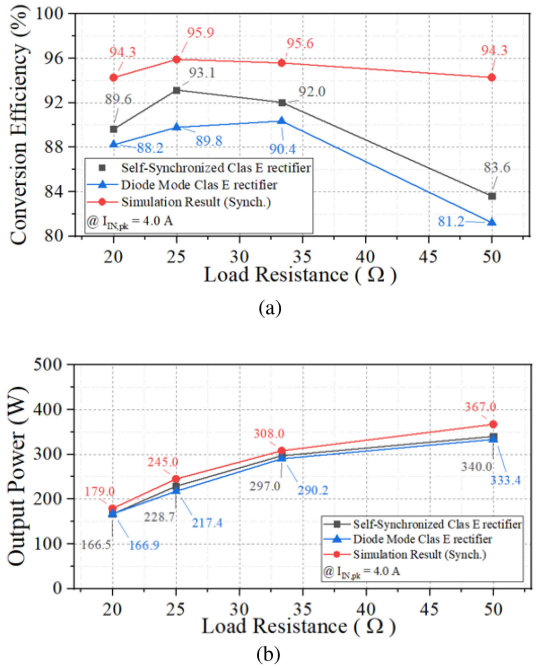

Fig. 13. Performances of the proposed self-synchronized class E rectifier under the load variance conditions: (a) Efficiency. (b) Output Power.

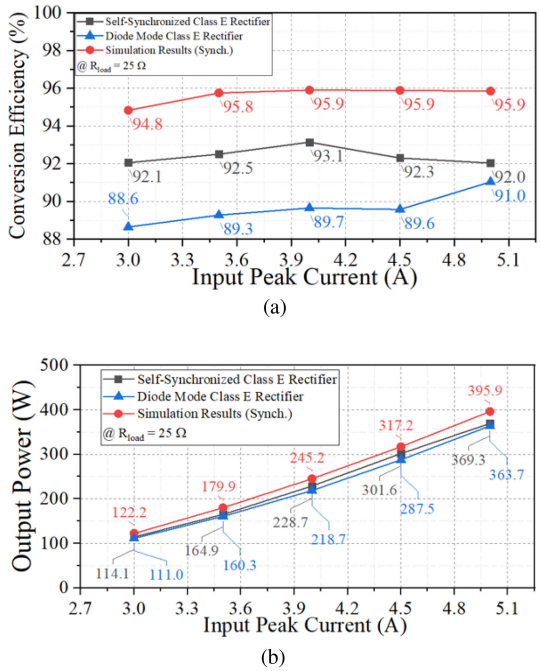

Fig. 14. Performances of the proposed self-synchronized class E rectifier under the input current variance conditions : (a) Efficiency. (b) Output Power.

t_{cpd} also increased when θ_{rect} was negative. For example, when the θ_{rect} is negative under under $I_{\text{IN}} = 3$ A and $R_{\text{load}} = 20\ \Omega$ in Fig. 12, we also discovered the non-ZVS operation due to the high t_{cpd} as measured in Figs. 10(a) and 11(a). Figs. 13 and 14 show efficiency and output power with the load and input current peak variations at the rated power condition around 250 W. The performance of the diode mode and the self-synchronized mode

TABLE II
PERFORMANCE COMPARISON WITH THE PREVIOUS STUDIES FOR A HIGH-FREQUENCY SYNCHRONOUS RECTIFIER

Work	Frequency	Rectifier topology	Synchronous Method	Self-Synchronization	Power	Efficiency
[3]	200 kHz	Class E for WPT	Microcontroller	No	15 W	–
[9]	64 MHz	Class Φ_2 for Converter	Bandpass Matching Network	No	15 W	75% (DC-to-DC)
[11]	6.78 MHz	Class E for WPT	Current Sensing & Phase-Shifter	Yes	5 W	86.5%
[4]	6.78 MHz	Full-bridge for WPT	Current Sensing & Phase-Shifter	Yes	4 W	–
[17]	1 MHz	Class E	V_{DS} detection and offset control	Yes	40 W	–
[10]	6.78 MHz	Class E for WPT	Auxiliary coil from WPT Receiver	Yes	194 W	94.6%
[18]	13.56 MHz	Class E	V_{DS} detection & monostable circuit	Yes	50 W	82% (DC-to-DC)
This work	**13.56 MHz**	**Class E for WPT**	**C-L voltage detection**	**Yes**	228 W	**93.1%**

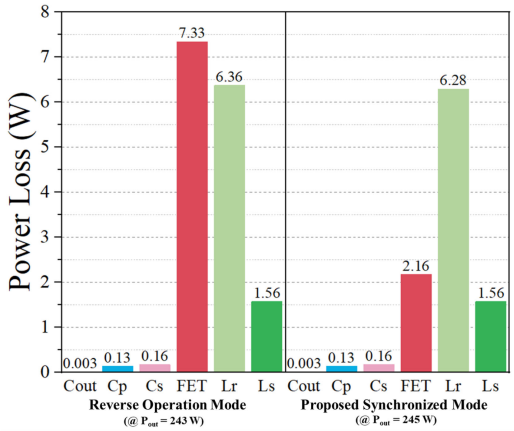

Fig. 15. Loss calculations of class E rectifier under self-synchronized mode and diode mode.

was compared with the same GS66508 T. The performance was measured by the oscilloscope under the 5% of the power based on the burst mode operation. As shown in Figs. 13(a) and 14(a), the efficiency of the self-synchronized class E inverter was increased by 2–3%, compared with the diode mode operation for both different load and input current variations. Because we designed the rectifier for the 250 W rated power condition (4.2 A, 25 Ω), the measurement results showed that the 25 Ω condition in Fig. 13(a) and 4 A condition in Fig. 14(a) achieved the highest efficiency ($\approx$ 93%). The experimental results also showed a slight decrease in efficiency due to non-ZVS operation when the input current was 3 A and 3.5 A with the $R_{\text{load}} = 20\ \Omega$, as demonstrated in Figs. 10(a), 10(b), and 11(a).

Fig. 15 shows the calculated losses of the proposed self-synchronized class E rectifier. Compared to the reverse operation mode (=diode mode), the FET loss was reduced because the proper gate signal reduced the forward voltage drop during the turn-ON period, which improved the conduction loss. Both modes provided a relatively dominant loss in the L_s component. Because of a low inductance value (= 200 nH) of the L_s, it had a low Q factor (= 120) and a large ripple current.

Table II shows the comparison between this work and the previous studies for synchronous rectifiers in the MHz range. The previous V_{DS} detection methods [17] and [18] are one of the suitable ways to operate in MHz frequency operation. The direct V_{DS} sensing method has the issue with the propagation delay of the gate-driver and sensing circuit. In order to solve this problem, Lim *et al.* [17] and Aldhaher *et al.* [18] used the offset voltage control to compensate for the propagation delay, and the offset voltage compensated for the propagation delay in terms of the turn-ON timing. However, the offset voltage induced an additional delay in the turn-OFFtiming. As the solution to the turn-OFFissue, the previous studies used the MCU [17] or monostable circuit [18] to make the fixed (or controlled) pulse duration for the turn-OFF time. However, it causes additional total propagation delay because the monostable circuit has a significant propagation delay (>100 ns), and MCU also has an internal signal delay (>2 clock cycles). Therefore, previous V_{DS} detection studies use the additional *RC* delay or manual phase-shift in MCU to synchronize precisely. It is challenging to calculate the total propagation delay accurately, and the total propagation delay can be one or two periods more than the time of the V_{DS} detection. Compared to the previous direct V_{DS} detection, the proposed method in this article is simple and fast because it requires only three parts of propagation delay (divider, comparator, gate-driver). The C–L component not only works as a detector to compensate for propagation delay, but also acts as a filter for the input source. In addition, the proposed method has a slight propagation delay (below 10 ns) and generates the gate signal within one period at the 10's of MHz operation. Huang *et al.* [10] presented a similar performance (194 W, 94.6%, 6.78 MHz) compared with this study (228 W, 93.1%, 13.56 MHz) for self-synchronized operation. The difference in the operation between the proposed method and the conventional paper [10] is how to handle the propagation delay. Huang *et al.*[10] used current detection using the additional coil at the receiver, which needs a manual tuning process to compensate for the propagation delay of the detection circuit. And the circuit in [10] operates 6.78 MHz, but the proposed rectifier operates 13.56 MHz. Even though the frequencies can drop the efficiency due to switching and inductor losses, our proposed method shows a similar performance using a simpler design with a higher frequency. Also, [10] can be used in only the WPT system, but the proposed rectifier is compatible with all systems using the class E rectifier.

IV. CONCLUSION

This article demonstrates a new self-synchronized class E rectifier with the C_s-L_s voltage detection method. We detect the voltage signal of the C_s-L_s resonant network and generate a proper gate signal using an inverting comparator to synchronize the gate signal with the turn-ON sequence. By compensating for the propagation delay using the C_s-L_s resonant network, the

synchronized turn-ON gate signal is identical to the drain-source voltage's zero-voltage duration. Also, we analyzed how the gate signal changes with the load change and the input current change. The characteristics of the self-synchronization method based on C_s-L_s detection in this article are summarized as follows:

1) Unlike the direct $V_{\rm DS}$ detection method, the C_s-L_s voltage detection method rapidly compensates for the propagation delay ($<$10 ns) within one period without any additional phase-shifter.

2) The C_s-L_s voltage detection method precisely synchronizes the turn-ON time under the rated power condition, but the gate pulse width is less than 50% ($= T/4 + t_{cpd}$).

3) Although the L_s component increases the size of the rectifier, the C_s-L_s resonant filter works not only for the synchronized signal generation, but also as the input filter of the specific frequency.

4) The proposed rectifier successfully operates under the load/current variance condition (114 W–370 W) without the additional phase-shifter. It has slight synchronization error (t_{pd} - t_{cpd}) about -2 ns to +3 ns with the load/current variation.

5) As the follow-up design method, the gate pulse width can be increased by adjusting the (+) offset voltage of the comparator. Also, the maximum compensated propagation delay can be increased by more than $T/4$ by controlling the (+) offset voltage.

6) Furthermore, if the nonlinearity of C_p by GaN-FET is negligible, the synchronization error under the input variance condition will also be minor, and the synchronization error under the load variance condition will be minimized, as shown in Figs. 7 and 8.

The proposed self-synchronized class E rectifier provides a simple and fast synchronous method without any manual phase-shifter. In addition, the proposed rectifier will be compatible with any system, such as a WPT system and dc-to-dc converter, including a class E rectifier.

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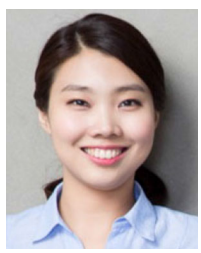

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