Letters

Modified PWM Scheme to Reduce Reverse Conduction Loss in GaN-Based Independently Controlled Multiple Output Flyback Converter

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***Abstract*—The recently proposed independently controlled multiple output flyback converter (ICMOFC) scheme improves cross-regulation by utilizing gallium nitride (GaN) switches with negative gate turn-OFF voltage. The highly inefficient reverse conduction (RC) of negative gate biased GaN devices leads to significant RC loss in the existing ICMOFC scheme. To mitigate this problem, this letter proposes a new pulsewidth modulation (PWM) scheme. The RC loss reduction is achieved by reducing the RC duration and RC current. The effectiveness of the proposed PWM strategy is analytically and experimentally verified using a 40-W dual output flyback converter. The results demonstrate a peak efficiency improvement of 1.26% over the existing ICMOFC scheme. Furthermore, the scheme also achieves high power density (51 W/in^3) and excellent cross-regulation (0.2%).**

***Index Terms*—Efficiency, gallium nitride (GaN), multiple output flyback converter (MOFC), reverse conduction (RC) loss.**

I. Introduction

THE flyback converter is a commonly used topology for low power multiple output applications. The cross-regulation is one of the major problems in conventional multiple output flyback converters (MOFC). Existing solutions, such as magnetic amplifier based techniques, increase the converter cost and volume due to several additional components [1]. The recently proposed independently controlled multiple output flyback converter (ICMOFC) regulates the outputs of conventional synchronous rectified MOFCs tightly, without using extra components in the power circuit [1].

The ICMOFC scheme applied to a two-output flyback converter is shown in Fig. 1. All active switches are enhancement mode (e-mode) gallium nitride (GaN) high electron mobility transistors (HEMTs). While the primary switch (Q_p) is driven with a unipolar gate driver, bipolar gate drivers are used to turn ON the secondary (Q_1) and tertiary (Q_2) switches during two distinct intervals. The negative gate turn-OFF voltage enables Q_1 and Q_2 to block a certain amount of voltage in the reverse direction [2], [3]. As a result, the three windings of the converter conduct current in three different intervals, as shown in Fig. 1(b). Using this property, the flow of current to each output capacitor is controlled to independently regulate each output voltage.

A significant drawback of this scheme is the reverse conduction (RC) loss in Q_1 and Q_2 during the current transitions

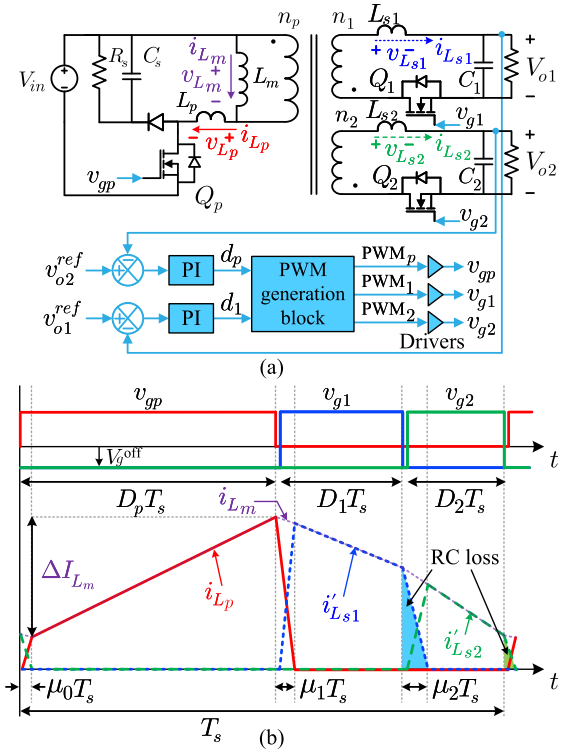

Fig. 1. GaN-based two-output flyback converter with independently controlled outputs. (a) Circuit diagram and control scheme. (b) Steady-state representative waveforms of gate-to-source voltages and winding currents. $i'_{L_{s1}}$ and $i'_{L_{s2}}$ are the secondary and tertiary winding currents referred to the primary winding.

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between windings. They continue carrying the leakage inductance currents in the reverse direction after turning OFF, as shown in Fig. 1(b). Moreover, the RC voltage drop is much larger than traditional Si MOSFETs due to the negative gate bias. As a result, the RC loss contributes to approximately 25% of the total converter loss at full load and leads to reduced overall efficiency compared to a conventional synchronous rectified MOFC [1].

Several techniques are suggested in the literature to address the RC loss in GaN-based converters [4]. One of the simplest methods is to provide an alternative low voltage drop path to the reverse current by using an extra antiparalleled Schottky barrier diode (SBD) [5]. The cost and size increment due to the additional SBD is eliminated in [6], wherein the SBD is integrated into the transistor. However, the reverse blocking capability of GaN HEMTs required by the ICMOFC scheme is lost in these methods. Another method is a three-level gate driver, proposed in [7], where an intermediate gate voltage is used during the RC to reduce the RC voltage drop and, hence, the RC loss. However, commercially available gate drivers cannot be directly used to achieve a three-level gate voltage. Operating condition based RC duration adjustment schemes are proposed in [8] and [9]. While commercial gate drivers are used with these schemes, the additional sensors used to determine the operating condition increase the cost and volume of the converter. It is clear that the methods suggested in the literature are not directly applicable, introduce several additional components to the converter, or require custom-built specialized components.

This letter proposes a modified pulsewidth modulation (PWM) strategy to reduce the RC loss in the GaN-based ICMOFC. Both the RC duration and RC currents are reduced compared to the existing ICMOFC scheme. The key contributions of this letter are as follows.

1) The RC loss in the ICMOFC scheme is reduced without introducing additional components to the circuit.
2) The total converter loss is distributed more evenly between devices, leading to easier thermal management.
3) The converter achieves excellent cross-regulation without sacrificing power density.

II. RC Loss Mechanism in Existing ICMOFC Scheme

Referring to Fig. 1(b), the RC loss in the GaN HEMTs depends on three parameters, namely the GaN HEMT reverse blocking voltage, the RC current peak, and the RC duration. First, the reverse blocking voltage (V_d) depends on the negative gate bias (V_g^{off}) and is given by

$$V_d = V_{\text{th}} + |V_g^{\text{off}}| \tag{1}$$

where V_{th} is the threshold voltage. Second, the rate of change of RC current and, hence, the RC duration depends on the voltage appearing across the leakage inductance of the transformer during the RC interval. For example, a large voltage across the leakage inductance leads to lower RC duration.

In the existing ICMOFC scheme, the current transitions from the secondary to the tertiary winding during the RC interval $\mu_2 T_s$ as shown in Fig. 1. During this period, the voltage across the secondary leakage inductance (L_{s1}) is a function of the difference between $V_{o1} + V_d$ and reflected V_{o2}. This is because the secondary and tertiary windings have identical polarities. On the other hand, the voltage across the tertiary leakage inductance (L_{s2}) during the RC interval, $\mu_0 T_s$, is a function of the addition of $V_{o2} + V_d$ and reflected V_{in}. Here, the current transitions from the tertiary to the primary winding, which have opposite polarities. Therefore, consequent opposite polarity winding conduction leads to higher voltage across the leakage inductance and, hence, lower RC durations. This property is utilized in the proposed scheme to reduce the RC loss as follows.

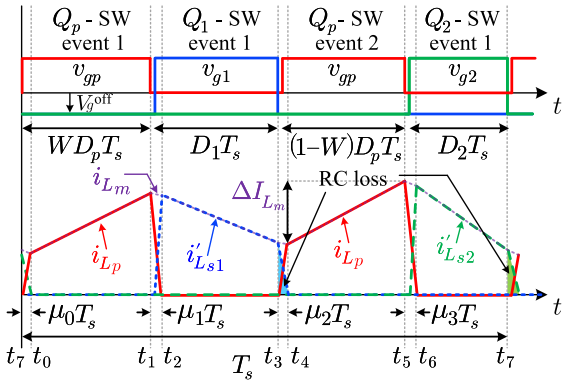

Fig. 2. Steady-state representative waveforms of the converter with the proposed PWM scheme.

TABLE I
Converter Parameters

V_{in}	V_{o1}	V_{o2}	I_{o1}	I_{o2}	f_s	L_m	V_g^{off}
48 V	15 V	5 V	1 A	5 A	540 kHz	25 μH	-3.8 V
n_p	n_1	n_2	L_p	L_{s1}	L_{s2}	C_1	C_2
8	3	1	0.3 μH	40 nH	8 nH	470 μF	1320 μF

III. Proposed Scheme for RC Loss Reduction

A. Principle of Operation

The primary switch duty cycle (D_P) is split up into two parts, WD_p and $(1-W)D_p$, where W is a weighting factor between 0 and 1. The PWM scheme is adjusted so that the primary switch conducts twice according to the aforementioned duty cycles, whereas the secondary and tertiary switches each conduct once in a switching cycle, as shown in Fig. 2. By forcing the primary winding to conduct after both the secondary and tertiary windings, the RC durations of both Q_1 and Q_2 are reduced. Moreover, W is selected to minimize the RC current peaks. In this way, the total RC losses are decreased. The stages of operation of the converter with the proposed PWM scheme are shown in Fig. 3.

B. Design Considerations

Since the magnetizing inductance of the converter remains unchanged, the magnetizing current ripple (Δi_{L_m}) reduces due to the modified PWM scheme. Moreover, peak RC currents and Δi_{L_m} in a switching cycle depend on W and the load currents. This is illustrated in Fig. 4(a) and (b), where the variation of

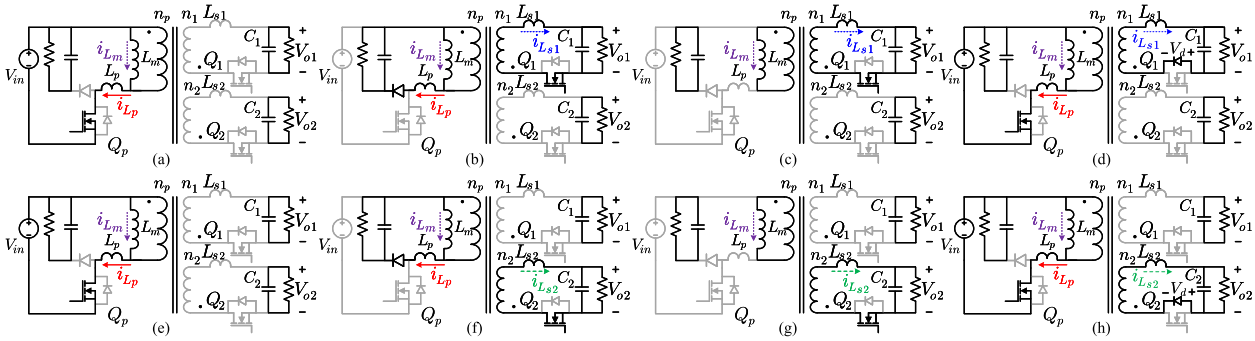

Fig. 3. Stages of operation of the converter during (a) t_0 to t_1, (b) t_1 to t_2, (c) t_2 to t_3, (d) t_3 to t_4, (e) t_4 to t_5, (f) t_5 to t_6, (g) t_6 to t_7, and (h) t_7 to t_0.

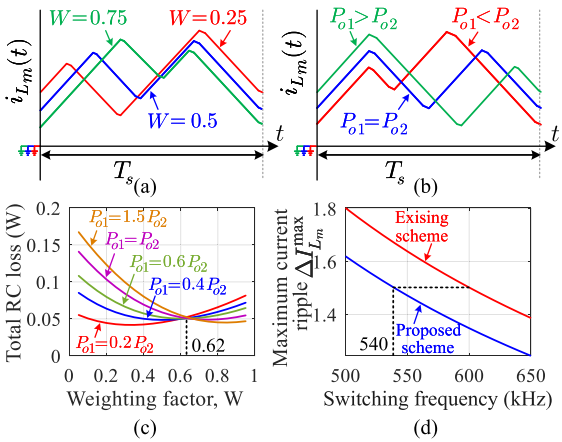

Fig. 4. Representative waveforms of the magnetizing current at (a) different values of W at full load and (b) different proportions of loads with $W = 0.5$. (c) Analytically obtained total RC loss with different values of W and different proportions of loads at 25-W output power. (d) Analytically obtained maximum magnetizing inductor current ripple with $W = 0.62$.

i_{Lm} with different W and output power conditions are shown. For a constant W, maximum Δi_{Lm} occurs when only one of the outputs is highly loaded. Hence, W and f_s are selected to minimize the overall losses under a wide range of operating conditions. The method of choosing W and f_s is explained below.

First, the RC loss of the converter with the proposed PWM scheme is obtained as follows. The peak of the primary leakage inductance (L_p) current at time t_1 [see Fig. 3(a)] is obtained as

$$i_{L_p}(t_1) = i_{L_p}(t_0) + \frac{V_{\text{in}}}{L_m + L_p}(WD_p - \mu_0)T_s. \tag{2}$$

Similarly, the currents through L_{s1} at time t_2 and t_3 [see Fig. 3(b) and (c)] are given by

$$\left.\begin{aligned} i_{L_{s1}}(t_2) &= \frac{n_p}{n_1}\left(i_{L_p}(t_1) + \frac{v_{Lm}(t)}{L_m}\mu_1 T_s\right) \\ i_{L_{s1}}(t_3) &= i_{L_{s1}}(t_2) + \frac{-V_{o1} - \frac{n_1}{n_p}v_{Lm}(t)}{L_{s1}}(D_1 - \mu_1)T_s \end{aligned}\right\}. \tag{3}$$

Then the RC loss of Q_1 during $\mu_2 T_s$ [see Fig. 3(d)] is given by

$$P_{Q_1}^{\text{RC}} = 0.5\mu_2 V_d i_{L_{s1}}(t_3) + R_{\text{sd}}^{\text{RC}}(i_{L_{s1}}(t_3)\sqrt{\mu_2/3})^2 \tag{4}$$

where $R_{\text{sd}}^{\text{RC}}$ is the RC channel resistance of the switch. μ_2 is the duty ratio pertaining to the duration $\mu_2 T_s$ and is given by

$$\mu_2 = -\frac{L_{s1} i_{L_{s1}}(t_3)}{T_s v_{L_{s1}}(t)\big|_{t\epsilon[t_3,t_4]}} \tag{5}$$

where $v_{L_{s1}}(t)$ is obtained by solving the equivalent circuit as

$$v_{L_{s1}}(t)\big|_{t\epsilon[t_3,t_4]} = \frac{-\frac{n_1}{n_p}V_{in} - (V_{o1} + V_d)(1 + \frac{L_p}{L_m})}{1 + \frac{L_p}{L_m} + (\frac{n_2}{n_p})^2\frac{L_p}{L_{s2}}}. \tag{6}$$

It is observed from (6) that the voltage across L_{s1} during the RC interval is indeed a function of addition of $V_{o1} + V_d$ and reflected V_{in} with the proposed PWM scheme. The RC loss of Q_2 is calculated in a manner similar to above.

From (2) and (3), it is observed that the peak RC current of Q_1 ($(i_{L_{s1}}(t_3))$ increases with increasing W. Consequently, (4) indicates that the RC loss of Q_1 increases with W. Meanwhile, the RC loss of Q_2 decreases with increasing W. The sum of these two RC losses considering the converter parameters listed in Table I is plotted in Fig. 4(c) for different values of W and different proportions of loads at 25-W output power. The optimum W, which results in minimal RC loss in all load proportions, is selected as 0.62. In addition, the current through L_p at time t_4 [see Fig. 3(d)] is expressed as

$$i_{L_p}(t_4) = \frac{n_1}{n_p}\left(i_{L_{s1}}(t_3) + \frac{v_{Lm}(t)}{L_m}\mu_2 T_s\right). \tag{7}$$

The subsequent currents are obtained in a similar manner. Based on the above expressions, the maximum value of Δi_{L_m} is given by

$$\Delta i_{L_m}^{\max} = \max\left\{i_{L_p}(t_1) - i_{L_p}(t_4), i_{L_p}(t_5) - i_{L_p}(t_0)\right\}. \tag{8}$$

The maximum Δi_{L_m} is then plotted in Fig. 4(d) for $W = 0.62$. This plot is compared with the current ripple of the existing ICMOFC scheme, where the switching frequency was 600 kHz. Finally, 540 kHz is selected as f_s to maintain the same current ripple in the proposed scheme. In this way, W and f_s are chosen.

C. PWM Generation

The logic diagram of the proposed PWM generation scheme is depicted in Fig. 5. The duty ratios of the converter, d_p and d_1, are calculated based on the closed-loop controller described

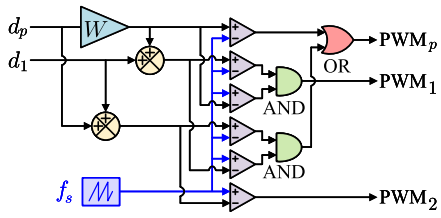

Fig. 5. Logic diagram for the proposed PWM generation scheme.

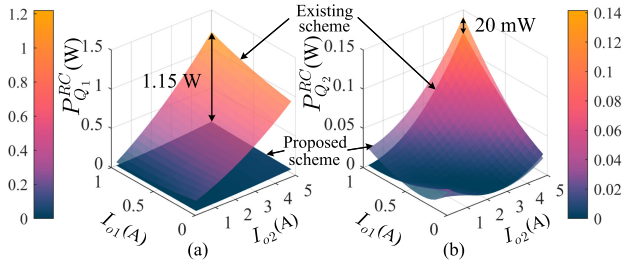

Fig. 6. Comparison of calculated RC loss of (a) Q_1 and (b) Q_2 with the existing scheme and the proposed scheme with $W = 0.62$.

TABLE II
LOSSES IN EACH SWITCHING DEVICE AT 25-W OUTPUT POWER

Scheme	Switch	Switching event	Switching loss (W)	Conduction loss (W)	RC loss (W)	Total loss (W)
Existing scheme	Q_p	1	0.221	0.079	—	0.30
	Q_1	1	0.329	0.063	0.585	0.98
	Q_2	1	0.199	0.368	0.021	0.59
Proposed scheme	Q_p	1	0.202	0.070	—	0.50
	Q_p	2	0.227			
	Q_1	1	0.263	0.036	0.026	0.32
	Q_2	1	0.195	0.459	0.030	0.68

in [1]. As shown in the diagram, weighted d_p, the sum of d_1 and weighted d_p, and the sum of d_p and d_1 are compared with a sawtooth wave of frequency f_s. The outputs of these comparators are passed through suitable logic gates to generate the PWM signals. The logic is implemented in a digital controller.

IV. RESULTS AND DISCUSSION

The validity of the proposed PWM generation method is supported by analytical calculation and experimental studies in this section. First, power losses in the switches are calculated from the device datasheet parameters and converter parameters listed in Table I. The analytically obtained RC losses of Q_1 and Q_2 with the proposed scheme as well as the existing ICMOFC scheme are plotted in Fig. 6 for different load conditions. With the proposed scheme, a reduction of 1.15 W is observed in the RC loss of Q_1 at full load (40 W), whereas the RC loss of Q_2 is comparable in the proposed and existing schemes.

The switching, conduction, and RC losses taking place in each switching device at 25-W output power in both schemes are listed in Table II. It is important to note that Q_p has two switching events in each switching cycle in the proposed scheme as shown in Fig. 2. However, the switching transition currents

TABLE III
ANALYTICAL LOSS COMPARISON

Scheme	Existing scheme			Proposed scheme		
Output power (W)	40	25	10	40	25	10
RC loss (W)	1.36	0.61	0.22	0.21	0.05	0.01
Conduction loss (W)	1.34	0.52	0.16	1.39	0.56	0.18
Switching loss (W)	0.96	0.75	0.58	1.13	0.89	0.68
Snubber loss (W)	1.25	0.79	0.44	1.42	0.86	0.47
Transformer loss (W)	0.69	0.37	0.19	0.62	0.30	0.13
Total converter loss (W)	5.60	3.04	1.59	4.77	2.66	1.47

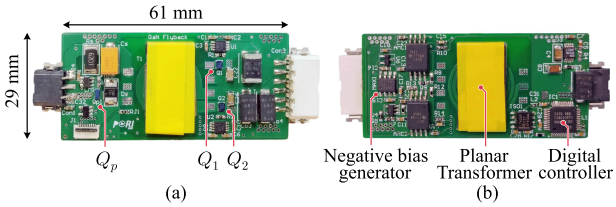

Fig. 7. 48-V input, 5–15 V output, and 40-W dual output flyback converter. (a) Top view. (b) Bottom view.

are reduced with the proposed scheme due to the alternate application of positive and negative volt-seconds to the magnetizing inductance. As a result, the increase in the total switching loss of Q_p is slightly less than two folds. On the other hand, the total switching loss of Q_1 and Q_2 reduces with the proposed scheme as transition currents are less while the number of switching events remains the same. Moreover, as observed from Table II, the overall losses are more evenly distributed instead of a high loss taking place in a particular switch (Q_1), which leads to easier thermal management. Table III compares the calculated converter losses of both schemes for three different output power conditions. It is observed that the proposed technique achieves significantly lower RC loss. This is justified due to smaller peak RC currents and RC durations. It is also noted that the proposed technique has higher snubber and switching loss than the existing technique. However, the increase in snubber loss is limited because the peak currents through the primary leakage inductance are lower with the proposed scheme. As a combined result of the above observations, the reduction in total power losses of Q_1 and Q_2 outweighs the increase in the switching loss of Q_p and snubber losses.

A 40-W experimental prototype with two outputs is developed for validating the proposed scheme as shown in Fig. 7. The negative gate bias for Q_1 and Q_2 is generated from 15-V output using a charge pump IC. EPC2012 C is used as Q_p, whereas EPC2016 C is used as Q_1 and Q_2. The power density of the prototype is 51 W/in^3.

Fig. 8(a) and (b) shows the gate and drain to source voltages of Q_1 and Q_2 for the existing and proposed scheme, respectively. The secondary and tertiary winding currents for both schemes are also shown. The oscillations in these currents are due to resonance between the leakage inductances and the switch output capacitances. In the zoomed view, the RC duration of Q_1 in the existing ICMOFC scheme is observed to be 121 ns. During the RC duration, the drain-to-source voltage of Q_1 is observed to

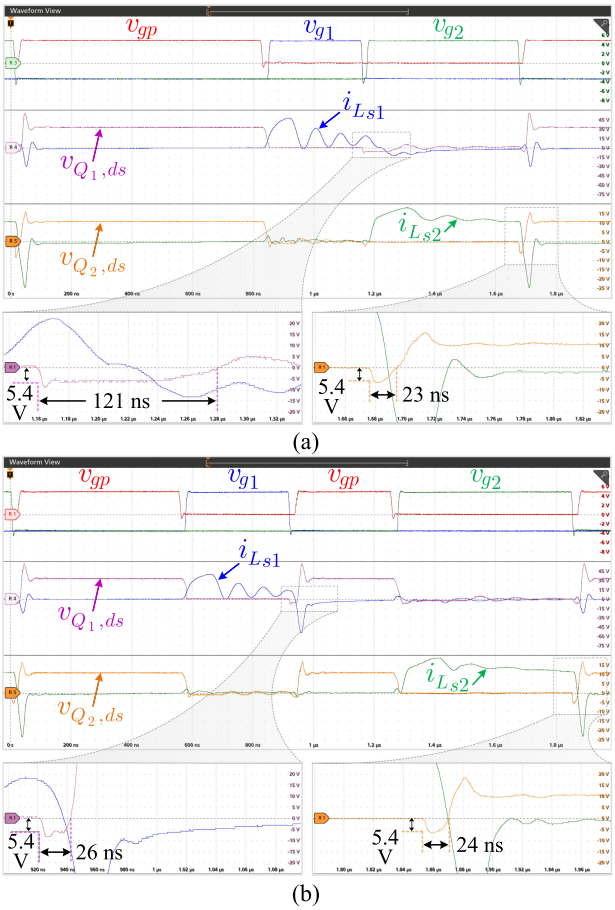

Fig. 8. Experimental voltage and current waveforms during a switching period at 25-W output power. (a) Existing ICMOFC scheme. (b) Proposed scheme; scales: v_{gp} [2 V/div], v_{g1} [2 V/div], v_{g2} [2 V/div], $v_{Q_1,ds}$ [15 V/div], $v_{Q_2,ds}$ [5 V/div], i_{Ls1} [7.5 A/div], i_{Ls2} [5 A/div], and *X*-axis: Time [200 ns/div]. Zoomed view: *Y*-axis: [5 V/div] and *X*-axis: Time [20 ns/div].

be –5.4 V. On the other hand, the RC duration of Q_1 in Fig. 8(b) is reduced to 26 ns as a result of the modified PWM scheme. Since the primary winding conducts after the tertiary winding in both the schemes, the RC duration of Q_2 is comparable. Moreover, it is seen that the conduction intervals of Q_1 and Q_2 are distinct with the proposed scheme, and, therefore, the voltages V_{o1} and V_{o2} are controlled independently as seen in the experimental load regulation waveforms shown in Fig. 9. The measured maximum cross-regulation is 0.2%.

Fig. 10 shows the experimentally measured efficiency plots for the existing ICMOFC scheme and the proposed scheme. The peak efficiency at 25-W output power with the proposed scheme is 88.22%, which indicates an improvement of 1.26% over the existing scheme. Moreover, the efficiency improvement at full load is higher at 1.44%. This supports the discussion that the highest RC loss reduction occurs at full load, as seen in Fig. 6.

V. Conclusion

This letter proposes a method to improve the efficiency of GaN-based ICMOFC. This is achieved by reducing the RC loss of the GaN HEMTs using a modified PWM scheme. Moreover, design considerations of the PWM scheme, namely the weighting factor and switching frequency, are discussed, focusing on

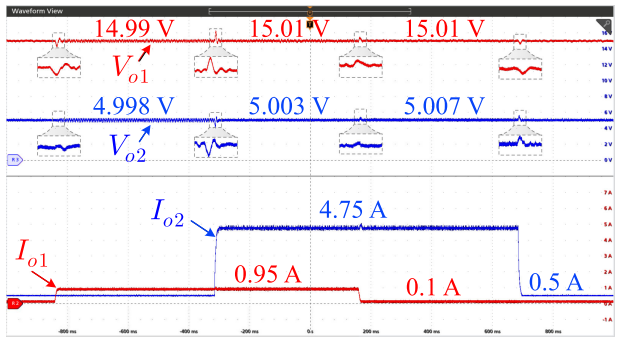

Fig. 9. Experimental load regulation waveforms with the proposed PWM scheme; scale: V_{o1} [2 V/div], V_{o2} [2 V/div], I_{o1} [1 A/div], I_{o2} [1 A/div], *X*-axis: Time [200 ms/div].

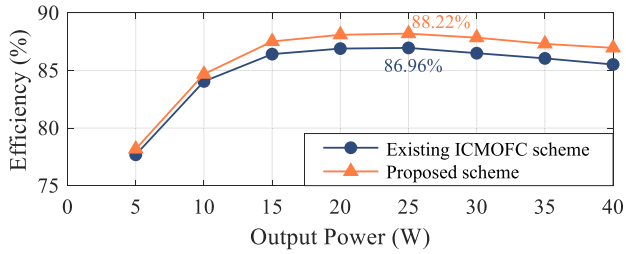

Fig. 10. Measured efficiency plots for different output powers.

their impacts on the converter efficiency. A 40-W experimental prototype with 51 W/in^3 power density, 0.2% maximum cross-regulation, and 88.22% peak efficiency is fabricated. When compared with the existing scheme, the proposed prototype achieves 1.26% improvement in peak efficiency and 1.44% improvement in efficiency at full load.

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