High-Definition High-Bandwidth DC/AC Power Conversion Through Binary Asymmetric Cascaded H-Bridges

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***Abstract*—It is known that cascaded H-bridges with heterogenous module voltages can, in theory, generate exponentially-refined output voltage levels and achieve high output resolutions from only one power source. However, several critical considerations have yet to be thoroughly studied, namely the controllability of module voltages under any load conditions, and how to schedule the switching states optimally. We present a scheduling algorithm and topological modifications for binary asymmetric cascaded H-bridges (ACHBs) to achieve complete sensorless operation under any load conditions while using only one power source. The scheduling algorithm cancels the energy intake of floating modules per time frame, while low-power auxiliary dc/dc circuits, which naturally emerge from the bridge structure, can correct any voltage drift without the need for voltage sensors. Rigorous analyses reveal an inherent performance tradeoff between reference-tracing accuracy and floating module voltage controllability for ACHBs in general, for which the proposed algorithm always achieves the Pareto front. The proposed ACHB and the algorithm are tested on an experimental setup with six modules and 65 output levels (i.e., effectively six bits).**

***Index Terms*—Binary asymmetrical cascaded H-bridges (ACHBs), DC/AC applications, high definition.**

I. Introduction

IN CONTRAST to conventional two-level inverters, cascaded H-bridge converters (CHB) provide a scalable solution to achieve any output resolution and power by simply stacking up identical H-bridge modules [1], [2]. Since the output voltage levels typically grow proportional to the module count, a large number of modules are needed for high-resolution output. The component cost and the balancing effort impede the adoption of CHBs in low-/medium-voltage applications [3]–[6].

For the purpose of achieving high-resolution output with fewer modules, a promising approach implements asymmetrical dc-link voltages to CHBs (ACHB) [7]–[16]. The dc-link voltages typically match a binary or tertiary power series in order to maximize the number of output levels (see Fig. 1). The high-resolution output renders ACHB suitable for low-/medium-voltage test equipment that is sensitive to distortions, such as motor testbenches [7]–[9] and programmable electronic loads [17].

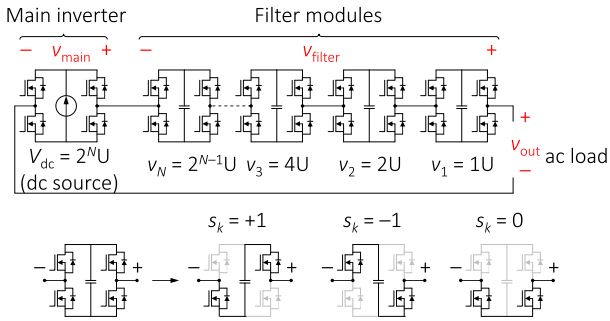

Fig. 1. Single-phase ACHB with module voltages following an exponential order. "U" denotes the unit voltage.

However, the need for independent dc sources severely limits the practicality and generality of ACHBs. Despite the efforts of reducing the number of dc sources, most so-called single dc-source ACHBs still rely on galvanically isolated power transfer [12]–[15]. The extra magnetic and semiconductor components need to process significant portions of the output power in order to stabilize the module voltages [18]. The extra losses, weight, voltage monitoring, and communication effort offset the merits of asymmetrical dc-link voltages.

In a completely different genre, other studies achieve single dc source ACHB operations by exploiting the redundancy in switching states. There, only the main module provides active power, and the remaining modules deliver pure reactive power (often referred to as *floating/auxiliary/conditioning module*) [9], [19]–[21]. Such an arrangement avoids dc/dc power transfer across modules, but makes it very challenging to regulate the module voltages due to the limited switching-state redundancy. The strong interaction of module voltage regulation with the output formation and the limited switching-state redundancy can require exhaustively search among all switching states to find a suitable discharging/charging pattern to correct the module voltages, which is impractical or impossible in many real-world solutions [19]. The search space is enormous ($O(3^N)$) given the combinatorial nature of the switching states, yet the controllability and stability of this method is unknown. Another

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type of control methods is restricted to sinusoidal waveforms and focuses on exploring the stable operating domains [7], [9], [20]–[22]. There, extensive case-by-case analyses of voltage and load current combinations are the main theme of the control development. The waveform type is restricted, and the required information about the load angle implies higher input-to-output delay and less robustness against rapid, unforeseen load changes.

This article proposes a novel solution for binary ACHBs. The proposed ACHB can be powered by a single dc source and operate under any load conditions or waveform shapes. No voltage or current sensor is required. Most computations of the algorithm can be parallelized and executed within single clock cycle of main-stream field-programmable gate arrays (FPGA), reaching a negligible input-output delay and a high throughput rate. Additionally, the proposed solution can be easily extended to practically any number of modules. The claimed features are made possible by innovations in control framework and the circuit topology.

A. Control Framework Innovation

Different from previous control methods that seek voltage controllability within harsh restrictions of reference-tracking [7], [9], [20]–[22], the proposed algorithm prioritizes complementary switching patterns for floating modules within each control frame (i.e., equal duration in positive and negative states). The duration of such a control frame is user-defined. Shorter frames are robust against irregular load currents because the inrush energy of floating modules is canceled more frequently; however, a larger reference-tracking error ensues. We proved that such tradeoff is the nature of single-source binary ACHBs, rather than the control method. We have also proved that the proposed algorithm achieves the Pareto front.

B. Circuit Topology Innovation

The proposed algorithm can ideally eliminate the inrush energy of floating modules, but residue energy will inevitably accumulate due to circuit nonidealities. We seek a hardware-level solution to regulate the dc-link voltages based on the following considerations: the remaining control redundancy is limited, which is further split into numerous load conditions already for a fixed waveform type and linear loads [7], [9], [20]–[22]. Venturing into this domain to generalize the waveform type, load condition, and module count is impractical. Thanks to the scheduling algorithm, the energy surplus/deficit on the floating modules is negligible, indicating a low effort to clear the net charge at circuit level. The CHB structure is known to allow a natural integration of such energy-transfer functionality between modules [2], [3], [23], [24]. We adopt such an approach and implement low-cost auxiliary dc/dc circuits to ACHB. We show that the desired conversion ratio of 2:1 can be achieved between any adjacent modules without knowing the actual voltage, hence the sensorless operation. The auxiliary dc/dc circuits do not interfere with aforementioned control and conduct negligible current since the residue net charge is small.

This article is presented in the following order. Section II introduces binary ACHBs and clarifies the module voltage control problem. Section III proposes the control framework and the scheduling algorithm. Important theoretical results are stated and proven. The scheduling algorithm is presented on the conventional ACHB to simplify the understanding, whereas the actual sensorless ACHB with dc/dc implementations is detailed in Section IV. Section V presents the experimental results on a lab setup of ACHB with six modules and 65 output levels.

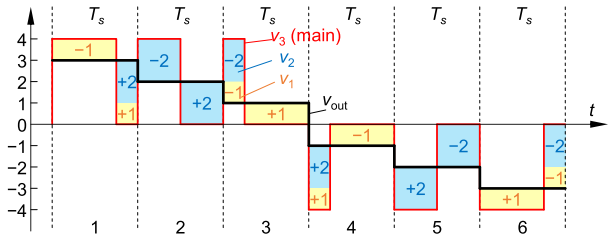

Fig. 2. Switching pattern of an ACHB with two floating modules.

II. Asymmetrical CHB

A. Topology and Operating Principle

Fig. 1 shows a binary cascaded H-bridge (ACHB) with one main inverter and N floating modules. Henceforth the term *binary* is dropped occasionally without causing ambiguities. The main inverter module is powered by a dc voltage source, while the floating modules only process reactive power. The $N + 1$ nominal dc-link voltages v_k form a binary exponential series, where $v_k = 2^{(k-1)}U$ ($k = 1, \ldots, N, N + 1$) with U being an arbitrary voltage constant. The main inverter is indexed as $N + 1$. The output voltage is confined between $-2^N U$ and $+2^N U$ to ensure the controllability over the energy of the floating modules. With the step size of U, the ACHB can output $2^{N+1} + 1$ voltage levels. This article focuses on single-phase ACHBs, but the proposed topology modifications and control theories can be easily extended to multiphasic setups.

The instantaneous output voltage of an ACHB is

$$v_{\text{out}} = \sum\nolimits_{k=1\ldots N+1} s_k 2^{k-1} U \tag{1}$$

where $s_k \in \{0, -1, 1\}$ defines the switching state in Fig. 1.

B. Module Voltage Control Problem

Since only the main inverter provides active power, it is important to eliminate the inrush charge of all floating modules during operation.

Fig. 2 gives an example of the ACHB switching pattern that tracks an output reference. If the load current is segment-wise constant, segments 2 and 5 represent two ideal cases where all floating modules clear their intake energy. Other segments, however, either charge or discharge some floating modules due to the unmatched durations in "+1" and "−1" states. If the load current is, respectively, constant in segments 1–3 and 4–6, then all floating modules can clear their net charge within the respective time frames. The same applies to the entirety of segments 1–6 if the current remains constant within.

Relaxing the charge-clearing problem to longer time frames allows more redundant switching states and makes it easier to find a suitable switching combination. However, doing so requires predicting the future current waveform and/or larger floating capacitors. Shortening the charge-clearing time frame obviously provides more robustness against the load condition, but the solution may not exist at all.

The question is therefore how to clear the floating modules' net charge within shortest possible time frame, while tracking the output voltage reference as closely as possible. Section III solves this problem with a simple scheduling algorithm. Rigorous analyses will be provided to show that the algorithm is not only effective, but also achieves the Pareto front.

III. Scheduling Algorithm

A. Scheduling Algorithm

We first introduce the algorithm in a purpose-driven manner, then detail the implementation. For simplicity, $U = 1$. We assume constant current within each time frame.

B. Initialization

In this control architecture, the voltage reference is batched into frames of length L (named *reference vector* in the following) before being processed. The algorithm aims to clear the floating modules' net charge within each time frame. We define residue voltage vector $v_{\rm dif}$ as the difference between the voltage reference $v_{\rm ref}$ and the summation of the determined module outputs. Initially, $v_{\rm ref} = v_{\rm dif}$. The algorithm progressively reduces $v_{\rm dif}$ until all modules are considered on all time slots of the time frame.

1) ***Step 1:*** Decides the duty cycle of the main inverter based on the required active power within the time frame. Control freedom exists in terms of when (from 1, …, L) to place the active switching states, for which the algorithm chooses to reduce the peak values of the residue voltage $v_{\rm dif}$.
2) ***Step 2:*** Considers all $N + 1$ modules in complementary states (i.e., any "+1" is paired with "−1" and vice versa) with the purpose of reducing the peak–peak value of the residue voltage until all modules over all time slots are considered.

The algorithm is very straightforward in terms of zeroing the charge of floating modules and tracing the voltage reference. However, since there are no extra steps to trace the committed modules across the loops and $v_{\rm dif}$ is not reduced directly (rather reduced in peak–peak values), two questions ensue: Does the algorithm consider modules at most once in any time slot? and What is the worst case of the final $v_{\rm dif}$? These two questions are answered below.

B. Properties of the Algorithm

With the frame length L, the number of floating modules N, and $|v_{\rm ref}(t)| \le 2^N$ ($t = 1, 2, \ldots, L$), we claim the following.

Property 1: After the algorithm, $\max|v_{\rm dif}(t)| \le \text{ceil}(2^{N-1}/L)$, i.e., the maximum tracing error is lower for longer frames. In particular, when $L \ge 2^{N-1}$, the maximum error $\max|v_{\rm dif}(t)| \le 1$.

Algorithm: The algorithm is detailed below.

0. ***Input:*** $v_{\rm ref}(t)$, $t = 1, \ldots, L$ // reference vector
Initialization:
1. $v_{\rm ref}(t) \leftarrow v_{\rm ref}(t)/U$ for all t // normalization
2. $s_k(t) \leftarrow 0$ for $k = 1, \ldots, N{+}1$ and t //switching states
3. $v_{\rm dif}(t) \leftarrow v_{\rm ref}(t)$ for all t // residue vector
Step 1: minimize $|\text{sum}(v_{\rm dif})|$
4. $k \leftarrow N{+}1$ // module# under consideration
5. $u \leftarrow 2^{k-1}$ // step size under consideration
6. WHILE $|\text{sum}(v_{\rm dif})| > u/2$:
7. IF $\text{sum}(v_{\rm dif}) > 0$:
8. $[v_{\max}, t_{\max}] \leftarrow [\max(v_{\rm dif}), \text{argmax}[v_{\rm dif}(t)]]$
9. $s_k(t_{\max}) \leftarrow +1$
10. $v_{\rm dif}(t_{\min}) \leftarrow v_{\rm dif}(t_{\min}) + u$ // update residue value
11. ELSE:
12. $[v_{\min}, t_{\min}] \leftarrow [\min(v_{\rm dif}), argmin[v_{\rm dif}(t)]]$
13. $s_k(t_{\min}) \leftarrow -1$
14. $v_{\rm dif}(t_{\min}) \leftarrow v_{\rm dif}(t_{\min}) + u$ // update residue value
15. ENDIF
16. ENDWHILE
Step 2: minimize $|\max(v_{\rm dif}) - \min(v_{\rm dif})|$
17. FOR $k = N{+}1 \rightarrow 1$: // loop over floating modules
18. $u \leftarrow 2^{k-1}$ // step size under consideration
19. WHILE $\max(_{\rm vdif}) - \min(_{\rm vdif}) > u$:
20. $[v_{\max}, t_{\max}] \leftarrow [\max(v_{\rm dif}), \text{argmax}[v_{\rm dif}(t)]]$
21. $[v_{\min}, t_{\min}] \leftarrow [\min(v_{\rm dif}), \text{argmax}[v_{\rm dif}(t)]]$
22. $s_k(t_{\max}) \leftarrow +1$
23. $v_{\rm dif}(t_{\max}) \leftarrow v_{\rm dif}(t_{\max}) - u$ // update residue value
24. $s_k(t_{\min}) \leftarrow -1$
25. $v_{\rm dif}(t_{\min}) \leftarrow v_{\rm dif}(t_{\min}) + u$ // update residue value
26 ENDWHILE
27. ENDLOOP
28. Output: $s_{\rm main}, s_1, s_2, \ldots, s_N$

Property 2: After the algorithm

$$\text{sum}\,|v_{\rm dif}| = \min\left\{ \begin{matrix} |\text{sum}\,(v_{\rm ref})| \bmod 2^N, \\ 2^N - \left(|\text{sum}\,(v_{\rm ref})| \bmod 2^N\right) \end{matrix} \right\} \le 2^{N-1} \tag{2}$$

i.e., the total error per frame is independent of L, bounded, and predictable from $v_{\rm ref}$.

Property 3: The energy intake of all floating modules is zero across the time frame of length L.

Property 3 is obvious since all floating modules are switched in a complementary manner, according to lines 22 and 24. To prove Properties 1 and 2, however, we need some intermediate results first.

Lemma 1: After Step 1, $|\text{sum}({v_{\rm dif}}^{(N+1)})| \le 2^N/2$.

Proof 1: $|\text{sum}({v_{\rm dif}}^{(N+1)})| \le 2^N/2$ is achieved after Lines 6–16 because each loop reduces $\text{sum}({v_{\rm dif}}^{(N+1)})$ closer to zero by the step size $u = 2^N$. Furthermore, the program only changes $\text{sum}(v_{\rm dif})$ in one direction, i.e., for each time frame, Step 1 attempts to either insert u or subtract u. Since $|\text{sum}(v_{\rm dif})| \le 2^N L$, the while-loop (lines 6–16) will terminate within L iterations.

Finally, to respect the hardware limitations, it is important to show that the loop at lines 6–16 does not overwrite the already committed time slot for the kth module (since the module can

only have one switching state per time slot). We prove this by refuting the contrary: in the case of $\text{sum}(v_{\text{dif}}) > u/2$, the program falls into the case of line 7 and attempts to reduce $|\text{sum}(v_{\text{dif}})|$ from the positive side by inserting $-u$. If $t_{\max}$ was already committed before for kth module, $x + 2^N$ must be the residue voltage at the same time slot in the previous iteration. Per the initial condition, $x + 2^N \le 2^N$ and therefore $x \le 0$. Since $x = \max(v_{\text{dif}})$, we have $v_{\text{dif}} \le 0$, and $\text{sum}(v_{\text{dif}}) \le 0$ in the previous iteration. However, $\text{sum}(v_{\text{dif}}) \le 0$ is impossible because the program would have attempted to reduce $|\text{sum}(v_{\text{dif}})|$ by inserting $+u$, contradicting to the assumption. The similar arguments apply to the case of $\text{sum}(v_{\text{dif}}) < -u/2$. As such, not only $|\text{sum}({v_{\text{dif}}}^{(N+1)})| \le 2^N/2$ is achieved after Step 1, but the module is considered at most once per time slot.

Lemma 2: After processing the main module ($k = N+1$) in Step 2, $\max({v_{\text{dif}}}^{(N+1)}) - \min({v_{\text{dif}}}^{(N+1)}) \le 2^N$.

Proof 2: We refer to the while loop in lines 19–26 under the case of $k = N + 1$. It is clear that this while loop will reduce all peak-to-peak residue voltages by inserting a pair of $+2^N$ and -2^N voltage steps. Given the initial condition $|v_{\text{dif}}| \le 2^N$, any peak-to-peak residue voltage will indeed be reduced to at most 2^N in one step; because of this, the while loop will terminate within ceil(L/2) iterations and exit with $\max({v_{\text{dif}}}^{(N+1)}) - \min({v_{\text{dif}}}^{(N+1)}) \le 2^N$.

Similar to *Proof 1*, the hardest part is to show that the (N+1)th module commits at most once per time slot. We prove this by refuting the contrary. There are two hypothetical cases where the same time slot is reused: (i) the time slot was already used in step 1, or (ii) the time slot was used in a previous iteration in Lines 19–26. For case (i), let us assume that the time slot $t_{\max}$ or $t_{\min}$ was used in step 1 to reduce $|\text{sum}({v_{\text{dif}}}^{(N+1)})|$ from the positive side, as such $t_{\max}$ was committed already where the residue voltage at $t_{\max}$ was once $v_{\max} + 2^N$. Per the condition at line 19, the peak-to-peak residue voltage was $v_{\max} + 2^N - v_{\min} > 2^{N+1}$, which contradicts to the initial condition. If, however, step 1 reduced $|\text{sum}({v_{\text{dif}}}^{(N+1)})|$ from the negative side, then $t_{\min}$ was used, at which the residue voltage was once $v_{\min} - 2^N$. Per the condition at line 19, the peak-to-peak residue voltage must once be $v_{\max} - v_{\min} + 2^N > 2^{N+1}$ and contradicts the initial condition. For the case (ii), let us assume that the time slot $t_{\max}$ was already used in the previous iteration in step 2, but appears once again as the peak location. As such, the maximum voltage in the previous iteration must be $v_{\max} + 2^N$, while the previous minimum value must be no larger than $v_{\min}$. Put together, the peak-to-peak residue voltage in the previous iteration must be at least $v_{\max} + 2^N - v_{\min}$, which is larger than 2^{N+1} according to Line 19 and violates the initial condition.

Lemma 3: After considering the kth module in the algorithm, $\max({v_{\text{dif}}}^{(k)}) - \min({v_{\text{dif}}}^{(k)}) \le 2^{k-1}$. This is a generalization of Lemma 2.

Proof 3: We show this by induction: if the same statement holds in the previous iteration of the (k+1)th module,[1] i.e., $\max({v_{\text{dif}}}^{(k+1)}) - \min({v_{\text{dif}}}^{(k+1)}) \le 2^k$, when entering Line 19, either $\max({v_{\text{dif}}}^{(k+1)}) - \min({v_{\text{dif}}}^{(k+1)}) \le 2^{k-1}$ and thus no changes apply to v_{dif} or $\max({v_{\text{dif}}}^{(k+1)}) - \min({v_{\text{dif}}}^{(k+1)}) > 2^{k-1}$. There is nothing to prove for the first case because ${v_{\text{dif}}}^{(k)}(t) = {v_{\text{dif}}}^{(k+1)}(t)$. For the second case, we have per Line 20–25

$$\begin{aligned} &\max v_{\text{dif}}^{(k)} - \min v_{\text{dif}}^{(k)} \\ &= \left|\max v_{\text{dif}}^{(k+1)} - 2^{k-1} - \min v_{\text{dif}}^{(k+1)} - 2^{k-1}\right| \\ &= \left|\max v_{\text{dif}}^{(k+1)} - \min v_{\text{dif}}^{(k+1)} - 2^{k}\right| \le 2^{k-1}. \end{aligned} \tag{3}$$

The last inequality follows the condition that $2^{k-1} \le \max({v_{\text{dif}}}^{(k+1)}) - \min({v_{\text{dif}}}^{(k+1)}) \le 2^k$.

Similar to the previous proofs, we need to show that the program assigns switching states to modules at most once per time slot. This is already ensured at (N+1)th module in proofs 1 and 2. For other modules, we only need to focus on lines 19–26. Without loss of generality, let us assume that the kth module's ith inner loop intends to overwrite $t_{\max}$, which was already assigned in the previous iteration. This indicates that the current peak-to-peak value of the residue voltage is larger than 2^{k-1} (line 19), and the maximum voltage in the previous iteration must be at least $v_{\max} + 2^{k-1}$, while the previous minimum value must be no larger than $v_{\min}$. Put together, the peak-to-peak residue voltage in the previous iteration must be at least $v_{\max} - v_{\min} + 2^{k-1} > 2^{k-1} + 2^{k-1} = 2^k$. This is impossible after processing the (k+1)th module (see Lemma 3). Note that citing Lemma 3 is allowed here because one can use this argument to backtrack the program to the (N+1)th module, where the initial condition $\max({v_{\text{dif}}}^{(N+1)}) - \min({v_{\text{dif}}}^{(N+1)}) \le 2^N$ applies.

With the above results, we can finally prove Properties 1 and 2.

Proof 4: After the program, $\max({v_{\text{dif}}}^{(1)}) - \min({v_{\text{dif}}}^{(1)}) \le 1$ (see Lemma 3). This means that the final residue voltage ${v_{\text{dif}}}^{(1)}(t)$ is either nonnegative or nonpositive. Without loss of generality, let us assume $\max({v_{\text{dif}}}^{(1)}) \ge \min({v_{\text{dif}}}^{(1)}) \ge 0$. Two cases follows: (i) $\max({v_{\text{dif}}}^{(1)}) = \min({v_{\text{dif}}}^{(1)})$ and thus $\text{sum}({v_{\text{dif}}}^{(1)}) = L{\cdot}\max({v_{\text{dif}}}^{(1)})$, or (ii) $\max({v_{\text{dif}}}^{(1)}) = \min({v_{\text{dif}}}^{(1)}) + 1$ and thus $\text{sum}({v_{\text{dif}}}^{(1)}) > L{\cdot}\min({v_{\text{dif}}}^{(1)})$. On the other hand, $\text{sum}({v_{\text{dif}}}^{(1)}) = \text{sum}({v_{\text{dif}}}^{(N+1)}) \le 2^N/2$, where the first equality follows from the fact that step 2 never changes $\text{sum}(v_{\text{dif}})$. Put together, for case (i) $\max({v_{\text{dif}}}^{(1)}) \le 2^{N-1}/L$, and for case (ii) $\max({v_{\text{dif}}}^{(1)}) < 2^{N-1}/L + 1$. Merging the two cases, we have $\max{v_{\text{dif}}}^{(1)} \le \text{ceil}(2^{N-1}/L)$. The same argument applies if $0 \ge \max({v_{\text{dif}}}^{(1)}) \ge \min({v_{\text{dif}}}^{(1)})$, completing the proof of Property 1.

Proof 5: From Proof 1, we know all residue voltages of ${v_{\text{dif}}}^{(1)}$ are either nonnegative or nonpositive. As such, $\text{sum}(|{v_{\text{dif}}}^{(1)}|) = |\text{sum}({v_{\text{dif}}}^{(1)})| = |\text{sum}({v_{\text{dif}}}^{(N+1)})|$. Due to step 1 of the program, $|\text{sum}({v_{\text{dif}}}^{(N+1)})| = \min\{|\text{sum}(v_{\text{ref}})| \bmod 2^N, 2^N - (|\text{sum}(v_{\text{ref}})| \bmod 2^N)\} \le 2^{N-1}$.

The above properties are additionally visualized by simulation results in Fig. 3, where the output voltages and tracing errors are shown for different L's. The voltage reference is a digitized sinusoid, whose vertical resolution is determined by $N = 3$ and frequency is linearly increased from 10 Hz at 0 ms to 1000 Hz at 20 ms. The voltage reference is sampled at 200 kHz and batched into time frames of various lengths ($L = 2, 4, 8$). As property 1 predicted, the peak output distortion for $L = 2, 4$ (i.e., $L \ge 2^{N-1}$) is bounded from above at 1; whereas the smaller $L = 2$ increases the peak error to 2. As property 2 predicted, larger L lowers the

[1]The algorithm iterates the (k+1)th module before the kth module.

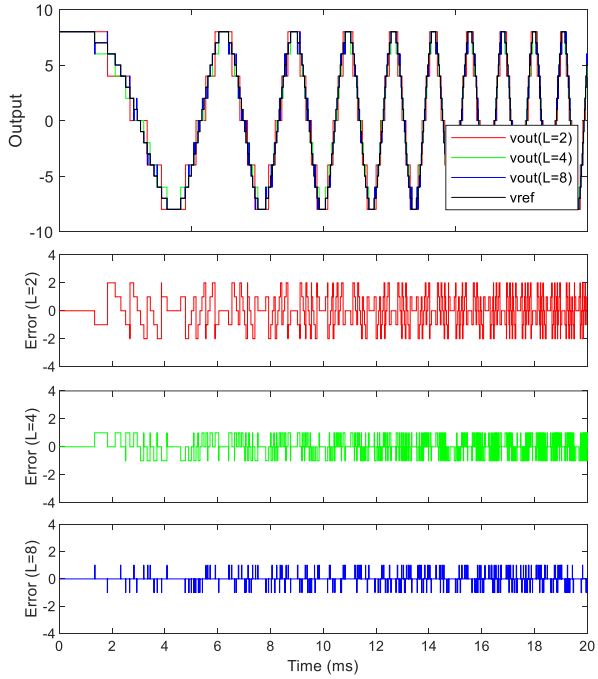

Fig. 3. Simulated output voltages with $N = 3$, $L = 2$, 4, 8. The control loop rate is 200 kHz.

average error rate (e.g., $L = 4$ vs. 8), despite the same maximum error.

C. Algorithm Achieves the Pareto Front

Properties 1–3 are very strong results that give tight upper bounds for the maximum tracing error (see Property 1) and the error rate (see Property 2) while balancing the energy intake for all floating modules (see Property 3) within the frame length L. We take a step further to show that these results are indeed the best any algorithm can possibly achieve. In other terms, the proposed algorithm is theoretically optimal in the sense that the following.

Property 4: If all floating modules are required to have complementary switching pattern within frames of length L (i.e., preserving Property 3), then

$$\max |v_{\text{dif}}| \geq \text{ceil}\left(2^{N-1}/L\right) \tag{4}$$

and

$$\text{sum}\,|v_{\text{dif}}| \geq \min\left\{\begin{array}{c} |\text{sum}\,(v_{\text{ref}})| \bmod 2^N, \\ 2^N - \left(|\text{sum}\,(v_{\text{ref}})| \bmod 2^N\right) \end{array}\right\} \tag{5}$$

for all possible $v_{\text{ref}}(t)$ and control algorithms. In other words,(4) and (5) respectively give the lower bounds for $\max|v_{\text{dif}}|$ and $\text{sum}|v_{\text{dif}}|$, which matches the upper bounds in properties 1 and 2, regardless of the switching algorithm. That means that the proposed algorithm is indeed optimal.

Proof 6: To preserve Property 3, all algorithms must assign complementary switching pairs to the floating modules. As a start, the algorithm can only insert the main module to modify $\text{sum}(v_{\text{dif}})$ with the step size of 2^N. As such,

$$|\text{sum}\,(v_{\text{dif}})| \geq \min\left\{\begin{array}{c} |\text{sum}\,(v_{\text{ref}})| \bmod 2^N, \\ 2^N - \left(|\text{sum}\,(v_{\text{ref}})| \bmod 2^N\right) \end{array}\right\}. \tag{6}$$

With $\text{sum}|v_{\text{dif}}| \geq |\text{sum}\,v_{\text{dif}}|$, the desired (5) follows.

The worst case is when $|\text{sum}\,v_{\text{ref}}| \bmod 2^N = 2^{N-1}$, where $\text{sum}|v_{\text{dif}}| \geq 2^{N-1}$. Diving both sides by L, we obtain

$$\max|v_{\text{dif}}| \geq \frac{\text{sum}\,|v_{\text{dif}}|}{L} \geq \frac{2^{N-1}}{L}. \tag{7}$$

Since $\max|v_{\text{dif}}|$ is an integer, an additional ceiling function applies to tighten the boundary, hence (4).

D. Control Implementation

The proposed algorithm requires up to L iterations in step 1 and up to $(N + 1)L/2$ iterations in step 2. It is important to accelerate the inner-loop computations (lines 7–16 and lines 21–28) to avoid bottlenecking the sampling rate. Fortunately, the entire algorithm only comprises the following operations.

1) Summation over a vector (e.g., line 7),
2) Finding max/min entries of a vector (e.g., line 8),
3) IF-ELSE flow control (e.g., lines 7, 11), and
4) Comparison, addition, subtraction (e.g., lines 19, 23, and 25).

Since the vectors have predefined length of L, and all other variables have fixed-point data type, all computations inside a loop can be performed in pure combinatoric logics and executed in one machine clock cycle. In particular, summations over fixed-length vectors can be deserialized into binary trees, and the same trick applies to finding max/min entries.

As such, the inner-loop operations per lines 7–15 and lines 20–25 can be completed in one clock cycle. The entire algorithm therefore takes at most $L + (N + 1)L/2$ clock cycles to populate the switching combination for the entire time frame of length L, reaching a throughput rate of $1+(N+1)/2$ cycles per sample. In the lab setup, we set $L = 1 \ldots 32$ and $N = 5$ on an FPGA clocked at 40 MHz (Zynq-7020, sbRIO-9627, National Instruments), and reached a sampling rate of 1 MHz, which is sufficiently higher than the semiconductor switches' normal operating range.

Fig. 4 shows the control architecture. In phase I, the reference waveform is sampled and buffered into a reference vector of length L as a frame. Reference vectors are stored and consumed in the input buffer by first-in-first-out manner. In phase II, the control algorithm processes each reference vector and generates $N+1$ (one main inverter and N floating modules) switching vectors of length L. In Phase III, the switching vectors are sorted by the sampling time before they are sent to the final stages. Therefore, the sampling rate exactly equals to the control loop rate or the throughput rate, which is limited by the computation time of the control algorithm at the order of $1+(N + 1)/2$ clocks.

E. Remarks

In summary, all ACHBs with only one power supply must clear the floating modules' charge frequently in order to adapt to arbitrary load conditions. Under this setting, let L be the number of control cycles across which the net charge is cleared, T_s be

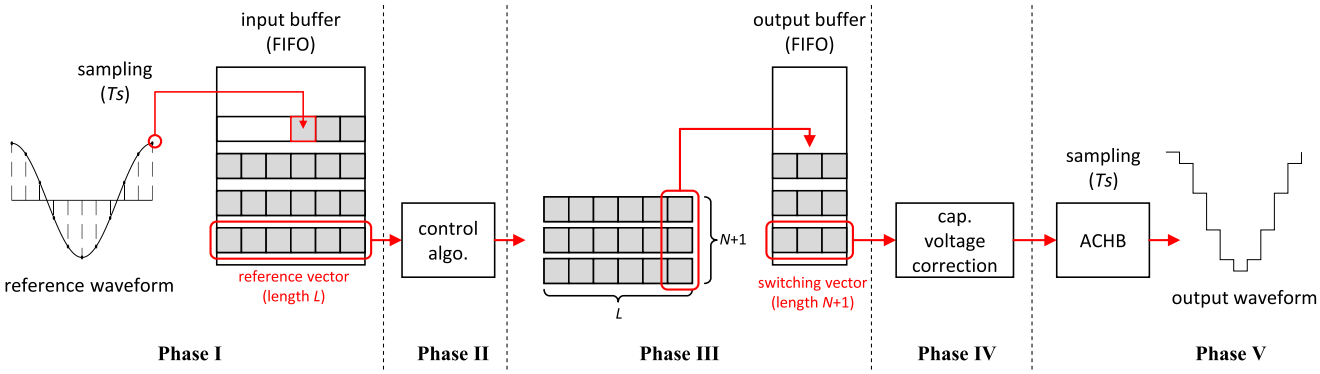

Fig. 4. Control architecture.

the control cycle, and $E = \max|v_{\text{dif}}|$ be the output level error. (7) indicates an unavoidable trade-off between L and E, which is resulted from the degree of freedom of *all* binary ACHBs, e.g., smaller L is more robust against the load current's uncertainty, but it leads to higher output error E.

As such, there is a Pareto front between L and E, and the proposed algorithm achieves exactly on that curve (see Properties 1 and 2). Choosing L is straightforward: one should reduce it if the floating modules' voltage exhibit large ripple (especially when it is larger than the smallest module's nominal voltage), or increase L if the error in the output levels E becomes a major source of distortion. Such relation between L and E is visualized by Fig. 3. The maximum operating range of the proposed method is therefore determined by the worst acceptable module voltage ripple ($\propto I_{\text{load}} L T_s$) and E, which occurs when both the load current's amplitude and frequency is high. The only way to operate beyond this limit requires increasing the control frequency $T_s{}^{-1}$, which *indirectly* increases the switching frequency. Such phenomenon is verified by the experiment results in Fig. 9.

We would also like to emphasize that as long as $L \geq 2^{N-1}$, the peak of E of the proposed algorithm is guaranteed to be no larger than the smallest module's nominal voltage. This is important. Without its guidance, adding ACHB modules does not necessarily improve the output resolution without compromising the flexibility.

The proposed algorithm makes no assumptions on the load condition other than the current being constant within each control window. As such, there is no surprise that the proposed ACHB works under dc, as is shown in Fig. 8(a).

IV. Capacitor Voltage Correction

While the aboveoutlined control can maintain the nominal capacitor voltages, it is not resilient to nonidealities such as imprecise switching timings. Also, if the load current varies notably within the L time slots, the floating modules will not clear their intake charge, which can accumulate and eventually cause notable output distortion.

In this section, we first discuss an active voltage correction method based on the ACHB's redundancy, then propose a much simpler approach based on topological modifications. The latter approach exploits the advantages of the proposed scheduling algorithm to an extent that no sensors are required, and the additional circuit components only carry negligible current compared to the load.

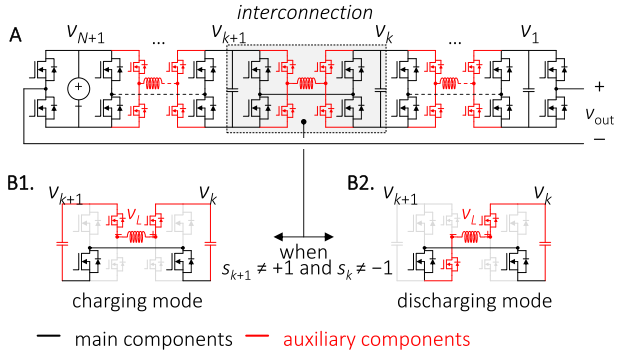

Fig. 5. (a) ACHB with self-balancing ability. The converter includes auxiliary dc/dc circuits (red) to ensure voltage gradient of 2:1. (b1) and (b2) Two dc/dc switching states that contribute to the voltage gradient of 2:1.

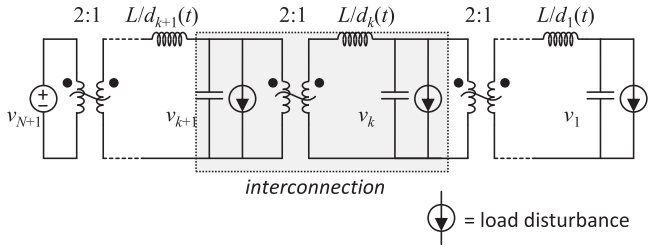

Fig. 6. Equivalent circuit for predicting the dynamics of the voltage conversion.

A. Conventional Approach

To actively correct the capacitor voltages, one can resort to a rather *conventional* approach where redistribution of the charge uses the switching redundancy of the binary ACHB. For example, $v_{\text{out}} = 1U$ can be produced by serval different switching

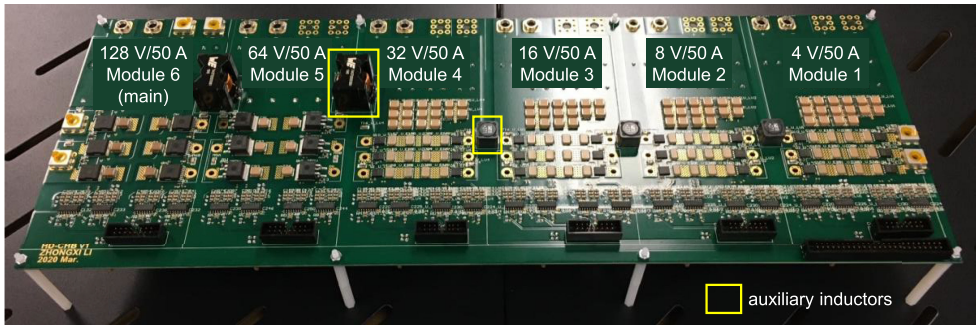

Fig. 7. Experimental setup.

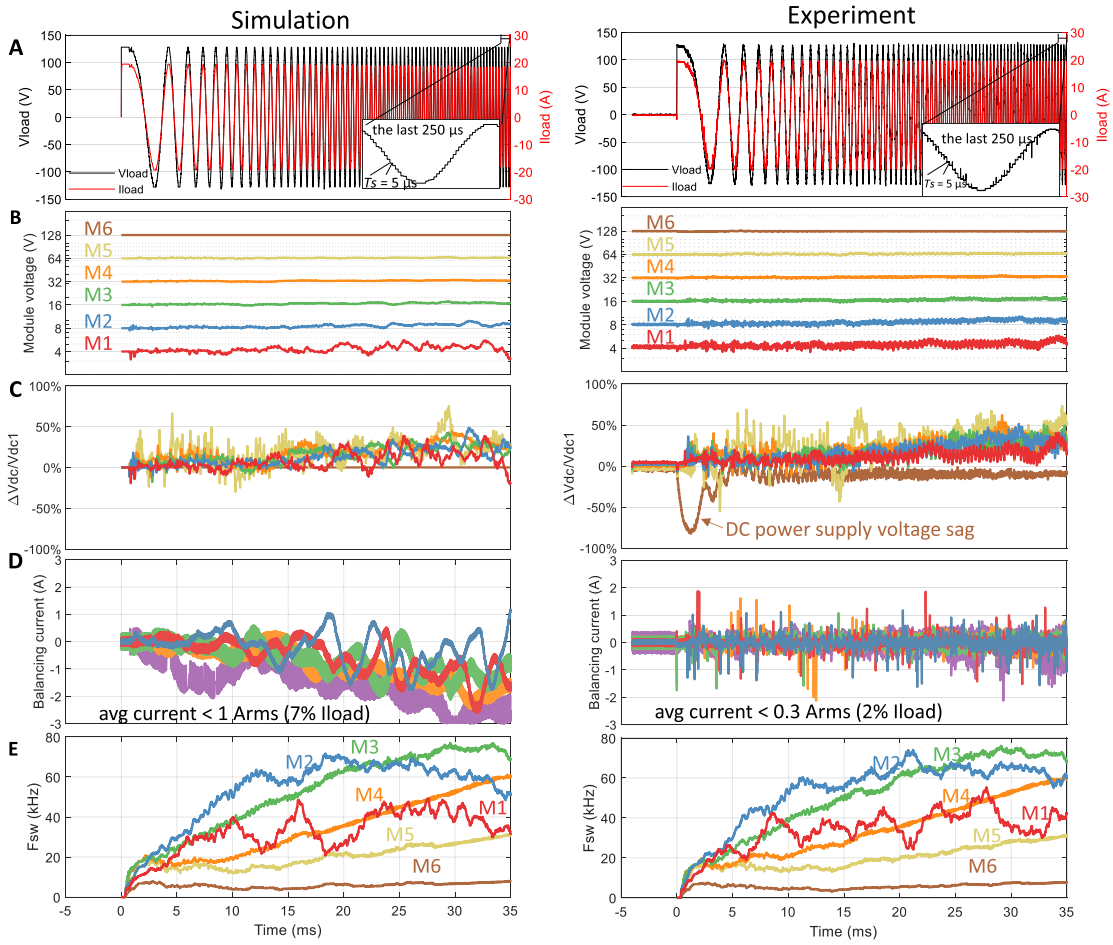

Fig. 8. Simulation (left column) and experimental (right column) waveforms under 1.3 kW load and a chirp reference (from 0 Hz at 0 ms to 4 kHz at 35 ms). The reference is sampled at 200 kHz. (a) Output voltage and current. (b) Module voltages in logarithmic scale. (c) Module voltage variations relative to the smallest module. (d) Balancing currents. (e) Real-time switching frequencies.

combinations as in $\underbrace{\begin{bmatrix} 1 & & & \\ -1 & 1 & & \\ \vdots & \vdots & \ddots & \\ -1 & -1 & \dots & 1 \end{bmatrix}}_{S(v_{\text{out}}=1)} \cdot \underbrace{\begin{bmatrix} 2^0U \\ 2^1U \\ \vdots \\ 2^NU \end{bmatrix}}_{v_k\text{'s}} = \underbrace{\begin{bmatrix} U \\ U \\ \vdots \\ U \end{bmatrix}}_{v_{\text{out}}\text{'s}}$ where each row of matrix S represents a valid combination (rightmost entry corresponds to the main module). By temporarily overriding the above control algorithm, one can re-distribute the charge of the modules with certain shares of time spent in each combination, as in

$$S^T \underbrace{[t_1, t_2, \dots, t_{N+1}]^T}_{\text{fractions of dwell time}} I_{\text{load}} = \underbrace{[\Delta q_1, \Delta q_2, \dots, \Delta q_{N+1}]^T}_{\text{charge re-distribution}}. \tag{8}$$

The controllability of the charge redistribution is guaranteed because matrix S has full rank. For example, if module 1 is overcharged, we would aim for $\Delta q_1 = -1$, $\Delta q_{N+1} = 1$, and other Δq_k's to be zero. In the case of $N = 4$, the solution is t_1: t_2: t_3: t_4: t_5 = 7:4:2:1:1, which effectively transfers power between the main inverter ($\Delta q_{N+1} = 1$) and the first floating module ($\Delta q_1 = -1$) without affecting the other modules.

In this capacitor control method, N voltage sensors and a load current sensor is required. Furthermore, similar control redundancy may not come handy at other $v_{\rm out}$'s—-for instance, there is only one switching combination that produces $\max(v_{\rm out})$ and $\min(v_{\rm out})$. Such momentary shortage of redundancy may not be a critical problem since the floating capacitor voltages can only drift slowly, and it may suffice to activate the capacitor voltage control only when $v_{\rm out} = 1$, during which the new switching pattern supersedes that of the output voltage control in Section III. However, the necessary frequency to hit $v_{\rm out} = 1$ for voltage regulation largely depends on the load current and the reference waveform.

B. Proposed Sensorless Solution

Fig. 5(a) presents a modified ACHB that can maintain the nominal capacitor voltages without any sensors and does not interfere with the scheduling algorithm in Section III.

The sensorless balancing method implements auxiliary components in the modules [marked red in Fig. 5(a)]. These auxiliary components, together with the main switches [marked black in Fig. 5(a)], form dc/dc circuits across modules. The key idea is to operate the dc/dc circuits to maintain a voltage ratio of 2:1 between adjacent modules.

Take the kth interconnection as an example. When $s_k \neq -1$, $s_{k+1} \neq +1$, the dc/dc circuit across the kth interconnection can either stay in the state of Fig. 5(b1) for duration T_1 or in the state of Fig. 5(b2) for duration T_2. For conditions other than $s_k \neq -1$ and $s_{k+1} \neq +1$, we let the auxiliary components operate synchronously with the main switches, for which we denote T_3 as the duration. Applying volt-second balance at the dc/dc inductor, we reach at equilibrium

$$\langle v_L \rangle = \frac{v_k T_1 + (v_k - v_{k+1}) T_2 + 0 T_3}{T_1 + T_2 + T_3} = 0 \Rightarrow \frac{v_{k+1}}{v_k} = 1 + T_1/T_2. \quad (9)$$

Setting $T_1 = T_2$ leads to v_{k+1}: v_k = 2:1, as desired. Appling the same strategy to all N interconnections ensures a binary exponential voltage distribution in equilibrium. Since v_{N+1} is fixed by a dc voltage source, the floating modules' voltages stay at the nominal values despite nonidealities and other perturbations.

The operation of the dc/dc circuits follow a simple switching pattern and does not require any information regarding the load current or the capacitor voltages. It should be emphasized that all switching states of the dc/dc circuits only exchange charge across the floating capacitors and do not alter the ACHB's output voltage, screened by the inductors. For implementation, $T_1 = T_2$ is easily achievable in digital controllers, which only need to identify the condition $s_k \neq -1$, $s_{k+1} \neq +1$ and distribute the two dc/dc states with equal clock counts. The control of the dc/dc circuits is appended after the scheduling algorithm, when the states of the main components are known.

According to the algorithm in Section III, the floating capacitors' intake charge per time frame should be very close to zero. The capacitor voltage ratio does not rapidly drift away from $v_{k+1} = 2v_k$. Therefore, the auxiliary circuit is expected to conduct zero dc current, while the peak–peak current is $T_1 v_k / L_k$ simply due to switching ripples. As such, cheap low-power components can serve to lower the additional hardware cost, while the capacitor voltage control is significantly simplified. In the experimental setup, we place the module voltage control at phase IV (see Fig. 4).

The equivalent circuit for predicting the energy conversion dynamics can be obtained from averaging out the switching states (see Fig. 6) [25]. The model in Fig. 6 shows three factors that limit the regulation speed: the average duty cycle $d(k)$ at which the dc/dc circuit is activated; the inductor of the dc/dc circuit; and the number of modules. The module capacitance can be small since it does not bear any importance in the steady-state voltage regulation other than providing a buffer for switching transients during the control time frame.

C. Module Capacitance

Based on the nature of the proposed algorithm, the floating modules' dc-link capacitors only have to buffer the net charge across each control window's duration LT_s. Assuming the peak load current $I_{\max}$, and maximum acceptable voltage ripple ΔV, the module capacitance C should satisfy

$$C \geq \frac{I_{\max} L T_s}{2 \Delta V}. \quad (10)$$

Equation (10) assumes the worst-case scenario where the first half of LT_s charges certain module with $I_{\max}$ and clears it during the second half. A more practical setting should keep the voltage ripple of any module to be less than the smallest module's nominal voltage, as such

$$C^{(k)} \geq \frac{I_{\max} L T_s}{2U}. \quad (11)$$

With $I_{\max} = 20$ A, $L = 32$, $T_s = (200\ \text{kHz})^{-1}$ and $U = 4$ V (i.e., the experiment setting of this article), the minimum C for all floating modules is 400 μF.

V. Experimental Results

We test the control method on an ACHB setup with six modules (five floating modules, see Fig. 7). The specifications are given in Table I. The load comprises a 6.6-Ω resistor. The control algorithm is implemented on an FPGA clocked at 40 MHz (Zynq-7020, sbRIO 9627, National Instruments). All reference waveforms are directly sampled by the control frame at 200 kHz. No extra modulation is applied despite being admissible to the proposed control algorithm. The simulation results of the same setup are provided for cross-validation. The major difference is the balancing current, which is larger in the simulations. This is mainly due to the underestimation of the stray inductance

TABLE I
SPECIFICATIONS OF THE SIX MODULES.

	Nominal voltage	Capacitance	Balancing inductor
M1	4 V	1210 µF	270 µH
M2	8 V	1210 µF	270 µH
M3	16 V	1210 µF	270 µH
M4	32 V	1210 µF	680 µH
M5	64 V	450 uF	680 µH
M6	128 V (main)	450 uF	

of the embedded dc/dc circuits (which is beneficial due to the more stable module voltages of the actual measurements). In either case, the balancing current is below 10% of the total load current, which translates to $< 1\%$ *of* the existing conduction loss.

The goal of the experiments is to find out the maximum realistic output frequency as well as the limiting factors, the magnitude of the balancing currents compared to the load current, the robustness of the capacitor voltage control, and the actual switching frequencies, which are influenced by, but not necessarily equal to the control-loop frequencies.

With these goals, we first implement a chirp signal with its frequency linearly increased from 0 to 4 Hz within 35 ms. The initial phase of the signal is set as 90° to emulate a sudden load change from 0 to 2.5 kW (peak). The measurements are gathered in Fig. 8.

A. Output Waveforms

Fig. 8(a) shows the output voltage and current. Since the voltage steps are 1/32 of the maximum voltage, they are hard to discern in the figure. The auxiliary figure details the last 250 μs of the output voltage, which reaches approximately 4 kHz. The voltage steps in the last 250 μs are more salient due to the relatively coarse sampling.

B. Sensorless Voltage Control

Fig. 8(b) demonstrates that all module capacitor voltages stay close to the nominal values and follow an exponential series until the output frequency rises to the maximum (4 kHz). Overall, the proposed sensorless voltage control is proven to be resilient considering the fact that the load current (20 A peak) is capable of charging the capacitors (0.45–1.2 mF) at the rate of 16 V/ms. Fig. 8(c) further normalizes the module capacitor voltages against the finest voltage step (i.e., 4 V in this case). Apart from the initial voltage dip that is due to the sudden load change, all module voltages stay within ±50% of the finest voltage step over the course of the output, which justifies implementing a series of six modules. Appending another floating module of 2 V does not improve the actual vertical resolution under this load condition, since the module voltage variations will exceed the finest voltage step. Higher load current frequencies cause larger voltage deviations because the control algorithm assumes constant current within each control frame.

Finally, we should point out that the initial voltage dip on the main module is caused by the dc power supply, rather than the control method since all other floating modules are not influenced by the initial transient at all.

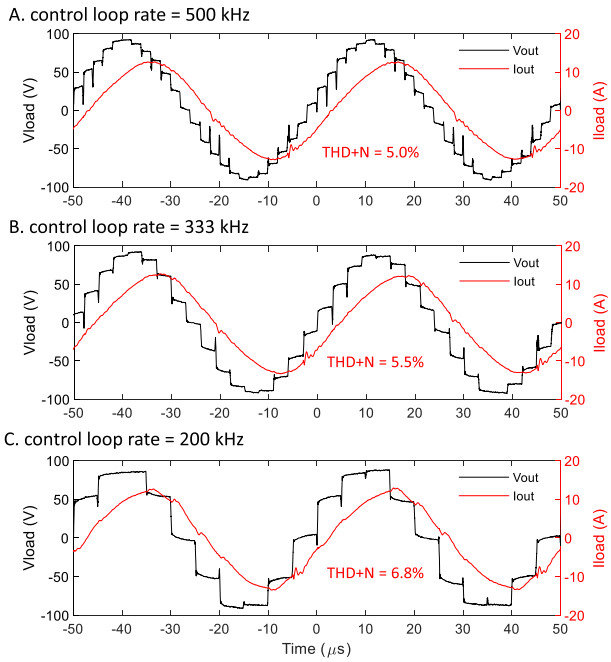

Fig. 9. 20-kHz sinusoidal output under different control loop rates. $L = 32$.

C. Balancing Current

Fig. 8(d) shows all dc/dc currents that flow locally between the adjacent modules. The balancing currents arise spontaneously to lock the voltage gradient to 2: 1. As expected, the balancing currents are negligible (< 0.3 A rms in measurements and < 1 A rms in simulations) compared to the load current (14 A rms), proving the effectiveness of the voltage control algorithm as well as justifying the use of low-power components as the balancing channel.

D. Switching Frequency

Fig. 8(e) shows the real-time switching frequencies. The frequencies are obtained by applying a 1-ms moving average window over the discrete switching events per power transistor. The measurements indicate that all modules are switched notably below the sampling rate (200 kHz), indicating a decent potential of further increasing the sampling rate without producing excessive switching loss. In particular, the switching rate is roughly inversely proportional to the nominal voltages, which is ideal for power electronics design. Such inverse relation is likely a consequence of the reference waveforms' monotonicity within most control frames, so that the switching states for the larger modules are temporarily grouped.

E. Output Bandwidth and Quality

For higher output frequencies, the sampling rate (i.e., control loop rate) may not be able to capture the details of the reference waveform, and the control frame length can be long enough for the load current to change significantly. The down-sampling and the larger capacitor voltage drifts limit the ACHB's output quality. Both factors can be alleviated by increasing the

control loop rate at the cost of proportionally higher switching frequency. This speed-up is readily feasible due to the simplicity of the algorithm and the largely unused switching reserve of the implemented semiconductors. An extreme example of 20-kHz sinusoidal output is shown in Fig. 9. Note that the control frame duration is comparable to the output cycle, so that the floating capacitors help stabilize the dc-link voltages; the long-term stability is still guaranteed by the auxiliary dc/dc circuits.

VI. Conclusion

To operate ACHBs with only one voltage source, it is important to clear the intake charge of all floating capacitors frequently. Under this constraint, we discovered an inherent performance tradeoff between reference-tracing accuracy and the charge-zeroing frequency for binary ACHBs in general.

We showed in rigorous proofs that the proposed scheduling algorithm achieves the Pareto front. To exploit such advantage while lowering the effort of operating ACHBs, we further proposed a modified ACHB with auxiliary dc/dc circuits. The dc/dc branch naturally blends in with the CHB structure and can be rather small and low-cost as it needs to manage only a negligible current—about 2% in the compared to the output current in the experimental setup.

The dc/dc circuits ensure the voltage gradient of 2:1 across the entire module chain while being ignorant to load conditions or capacitor voltages. In the lab setup with six modules, 65 output levels and single dc source, the proposed ACHB operates in a complete sensorless manner while exhibiting excellent robustness against sudden load changes.

Vouched by strict analyses and experimental results, the proposed single dc-source sensorless ACHB promises to lower the effort of high-quality, high-bandwidth dc/ac conversion for medium/low-voltage domains.

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