Dual-Buck Three-Switch Leg Converters With Reduced Number of Passive Components

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***Abstract*—Like conventional two-switch leg converters, the three-switch leg converters also have short-circuit risks and a dangerous shoot-through current is generated if switches of the same leg are turned ON simultaneously. In this article, a new dual-buck structure is proposed for three-switch leg converters. The proposed structure is reliable because of no shoot-through concerns and high quality of output waveforms can be obtained due to the reduction in pulsewidth modulation deadtime. Unlike the conventional dual-buck three-switch leg that uses many passive components such as four current limiting inductors and three external diodes, the new dual-buck three-switch leg uses only one current limiting inductor with two external diodes. To verify the performance, the proposed three-switch legs are used in single-phase dual-output inverter and detailed theoretical analysis, simulation, and experiments are performed. Both continuous and discontinuous modulation schemes are applied and it has been figured out that discontinuous modulation scheme can improve the dc-link voltage utilization in the common-frequency mode of operation.**

***Index Terms*—Dual buck, shoot-through current, three-switch leg (3SL).**

I. Introduction

POWER converters can be categorized into voltage-source converter (VSC) and current-source converter (CSC). The building block of both VSCs and CSCs is generally a switching leg with two active switches. The structures of the state-of-the-art two-switch legs (2SLs) are shown in Fig. 1(a) and (c). The switching leg of Fig. 1(a) has unidirectional voltage blocking capability and is extensively used in dc–ac [see Fig. 1(b)], ac–dc, and dc–dc VSCs. On the other hand, the switching leg of Fig. 1(c) has bidirectional voltage blocking capability and is therefore used in dc–ac [see Fig. 1(d)] and ac–dc CSCs. In spite of some inherent advantages of CSCs, the technology nowadays still prefers to use VSCs due to their advanced research works, better control, and good efficiency [1].

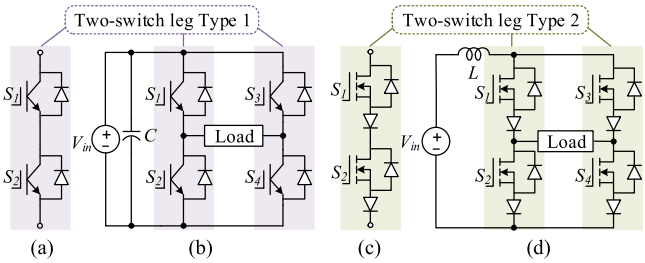

Fig. 1. (a) Unidirectional voltage blocking switching leg. (b) Single-phase voltage-source inverter. (c) Bidirectional voltage blocking switching leg. (d) Single-phase current-source inverter.

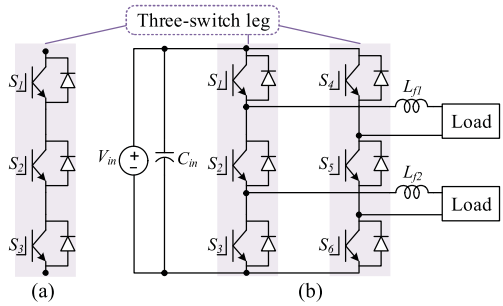

Fig. 2. (a) Unidirectional voltage blocking three-switch leg. (b) Single-phase dual-output voltage-source inverter.

Besides the 2SL, the three-switch leg (3SL) has also gained significant popularity. The reason of getting recognition from scientific community is the capability of 3SL to reduce the number of active switches in various applications and power conversion topologies [2]. The active switches require gate-driver circuitry, gate-driver supply, and pulsewidth modulation (PWM) outputs in microcontroller, which undesirably increase the cost, weight, volume, and failure probability of the entire system [3]. The structure of conventional 3SL is shown in Fig. 2(a). The

Manuscript received 28 September 2021; revised 14 February 2022 and 29 April 2022; accepted 9 June 2022. Date of publication 16 June 2022; date of current version 26 July 2022. This work was supported in part by the National Research Foundation (NRF) under Grant 2020R1A3B2079407, the Ministry of Science and ICT (MSIT), South Korea; and in part by the U.K. Engineering and Physical Sciences Research Council (EPSRC) under Grant EP/T026162/1. Recommended for publication by Associate Editor A. Ioinovici. *(Corresponding authors: Ahmad Elkhateb; Jung-Wook Park.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3183834.

Digital Object Identifier 10.1109/TPEL.2022.3183834

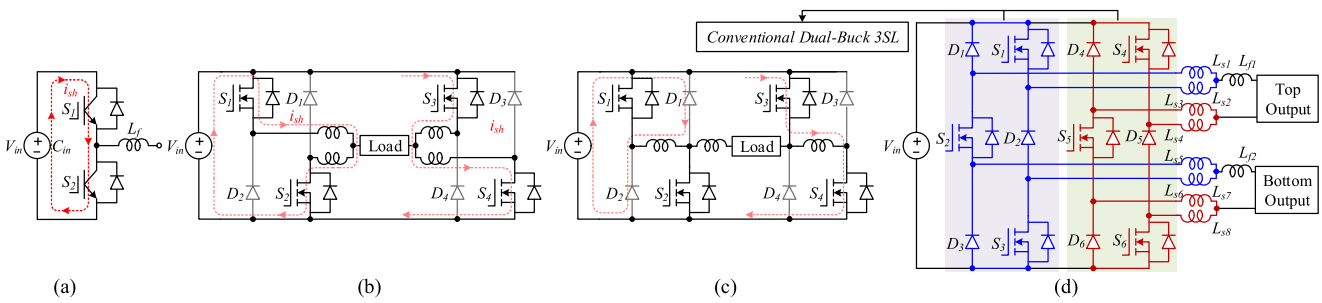

Fig. 3. (a) Current shoot-through problem in conventional 2SL. (b) 2SL dual-buck inverter proposed in [22]. (c) 2SL dual-buck inverter proposed in [24] and [28]. (d) 3SL dual-buck dual-output inverter [3].

3SL was first introduced in three-phase dual-output inverter [4] that is widely known by nine-switch converter (NSC). The NSC is versatile and is used in many different topologies such as dual-output matrix converter [5], ac–ac converter [6], motor drive [7], [8], dual-output Z-source inverter [9], dual-output boost inverter [10], and modular interlinking converter for hybrid ac/dc microgrid [11]. Besides NSC, the 3SLs are also used in single-phase dual-output inverter as shown in Fig. 2(b) [12], transformerless hybrid power filter [13], multi-input converters [14], dc–dc converter [15], and isolated ac–dc converter [16].

The previous studies signify that the conventional 3SL converters can successfully reduce 25% active switches but they also have limitations such as operating constraints [2] and short-circuit risk [3]. Fortunately, a good deal of research has already been conducted regarding operation constraints and it has been figured out that the 3SL converters can offer even better efficiency as compared to the conventional counterparts within certain operation ranges [2], [17]–[19]. On the other hand, less effort is paid toward the short-circuit risk of 3SL converters and needs further attention.

In both 3SL (see Fig. 2) and 2SL [see Fig. 1(b)] converters, the input voltage source is short-circuited if switches of the same leg are turned ON simultaneously. The 2SL converter of Fig. 1(d) has no short-circuit issue because the input is current source. However, it has open-circuit problem if either top (S_1, S_3) or bottom switches (S_2, S_4) are turned OFF together. The open-circuit issue can be eliminated by using the structures presented in [20] and [21], whereas the short-circuit issue can be resolved by the well-known dual-buck structure patented in [22]. Due to the reliable and efficient operation, dual-buck structures are used extensively in various topologies such as dc–dc converter [23], full-bridge inverter [24], three-phase inverter [25], split-source inverter [26], differential-boost inverter [27], cascaded full-bridge converters [28], and ac–ac converter [29]. It should be noted here that the dual-buck converters in [22]–[29] are based on 2SL converters. Hence, keeping in view the benefits of 3SL converters, Nguyen extended the concept of dual-buck structures to 3SL converters in [3].

The conventional 3SL dual-buck converter [3] is reliable but it has many passive components. To reduce the number of passive components, novel 3SL dual-buck structures are proposed in this article. The motivation and derivation of the proposed structure are analyzed in Section II, which is followed by switching schemes, mode analysis, and design guidelines in Section III, simulation and experimental results in Section IV, and comparative analysis in Section V. Finally, Section VI concludes this article.

II. Derivation and Motivation of the Proposed 3SL Dual-Buck Structure

The current shoot-through problem in conventional 2SL is depicted in Fig. 3. It can be observed that when both switches (S_1, S_2) of the leg are ON due to fault conditions, a low-impedance path is created and the input voltage source is short-circuited. The deadtime intervals can reduce the short-circuit risk but it deteriorates the quality of output voltage waveforms and reduces the achievable voltage gain [30]. Besides, the hard switching 2SL converters are normally implemented with insulated-gate bipolar transistors (IGBTs) and cannot avail the benefits of power MOSFETs such as lower switching and conduction losses. This is due to the slow and poor performance of the MOSFETs body diode especially under high voltages [31], [32]. The body diodes of silicon carbide MOSFETs have exceptionally low reverse-recovery losses [16], [33] and can improve the efficiency of 2SL converters but the short-circuit issue still remains a major reliability concern.

The 2SL dual-buck structure [22] as shown in Fig. 3(b) eliminates the current shoot-through problem and improves the quality of output waveforms as well. Fig. 3(b) shows that inductors appear in the current path even if switches of the same leg are turned ON and hence the current shoot-through issue can be avoided. The structure of Fig. 3(b) is reliable but 50% magnetic utilization is the downside of this topology. To improve the power density, a dual-buck structure as shown in Fig. 3(c) is proposed in [24] and [28]. The key idea of Fig. 3(c) is to use a separate filter inductor and two small-value shoot-through inductors rather than using four bulky inductors similar to Fig. 3(b).

The concept of dual-buck structure is also extended to 3SL dual-output inverters in [3], as shown in Fig. 3(d). Similar to 2SL, the 3SL dual-buck structure has no current shoot-through problem and the quality of output waveforms is improved. Furthermore, as explained in [3], the 3SL dual-buck structure has no reverse recovery issues of the body diodes despite current flowing through them because of the shoot-through inductors appearing in the current path. Besides advantages, it is noteworthy that the conventional 3SL dual-buck structure has large number of passive components. In order to reduce the number of passive

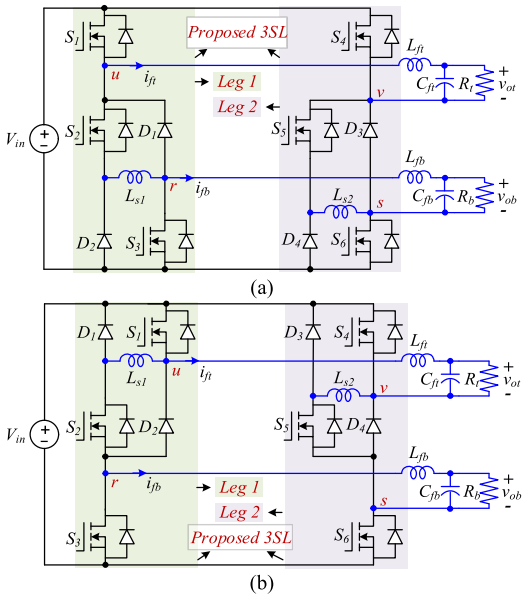

Fig. 4. Proposed single-phase 3SL dual-buck dual-output inverters. (a) Type I. (b) Type II.

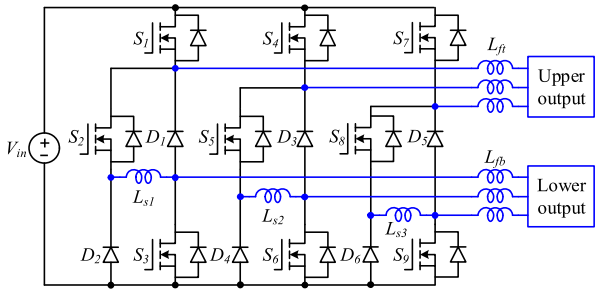

Fig. 5. Proposed dual-buck 3SL NSC.

components, two novel alternative 3SL dual-buck dual-output inverters as shown in Fig. 4 are proposed in this article. The proposed inverters are obtained by replacing only top or bottom two switches of 3SL dual-output inverter [see Fig. 2(b)] with 2SL dual-buck structure of Fig. 3(c). Unlike conventional 3SL dual-buck inverter that requires six external diodes (D_1-D_6) and eight shoot-through inductors $(L_{s1}-L_{s8})$, the proposed inverters require only four external diodes (D_1-D_4) and two shoot-through inductors (L_{s1}, L_{s2}). Furthermore, the idea of proposed dual-buck structure can be extended to the other 3SL topologies [2], [5]–[8], [10]–[16] as well. As an example, the structures of proposed NSC [2] and multi-input converter [14] are shown in Figs. 5 and 6, respectively. Considering that the key idea is same and due to limited number of allowed pages, this article focuses only on the proposed 3SL single-phase dual-buck inverter.

III. Switching Strategies, Operation Principles, and Design Guidelines of the Proposed Single-Phase Dual-Buck 3SL Inverter

Like the conventional 3SL converters, the proposed dual-output inverters of Fig. 4 also share the middle switches of

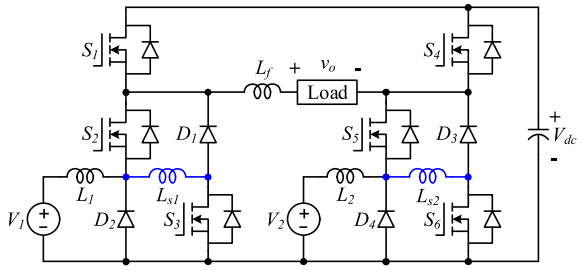

Fig. 6. Proposed 3SL dual-buck multi-input converter topology.

TABLE I
Switching States for 3SL

States	S_1	S_2	S_3
1	ON	ON	OFF
2	ON	OFF	ON
3	OFF	ON	ON

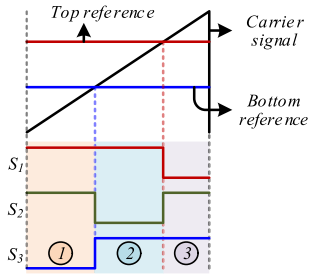

Fig. 7. Signals generation for 3SL.

each leg (S_2 and S_5) for both the outputs and hence results in switching constraints. The two output voltages are given by

$$v_{ot} = M_t\, V_{in} \sin(2\pi f_t t) \tag{1}$$

$$v_{ob} = M_b\, V_{in} \sin(2\pi f_b t + \varphi) \tag{2}$$

where v_{ot}, M_t, and f_t are the output voltage, modulation index, and frequency of the top output, whereas v_{ob}, M_b, and f_b are the output voltage, modulation index, and frequency of the bottom output. The phase difference between the two output voltages is represented by φ and it varies in the range of $0 \leq \varphi \leq \pi$. The proposed inverters can be either operated in common-frequency (CF) mode when $f_t = f_b$ or different-frequency (DF) mode when $f_t \neq f_b$. Irrespective of the operational modes, switches of the 3SL have only three permissible switching states, which are listed in Table I. The other switching states in which only one switch of the 3SL is ON results in floating the output and are not permissible. The typical modulation for 3SL is depicted in Fig. 7. It can be observed that the top and bottom references generate gate signals for the top and bottom switches (S_1 and S_3) of the 3SL, respectively. The gate signals for the middle switch S_2 of the 3SL are obtained by logical XOR operation of S_1 and S_3. In order to avoid the forbidden switching states, the top reference should be always greater than or equal to the bottom reference signal. This switching constraint results in doubling the dc-link voltage in worst cases, which can be generally avoided in ac–dc

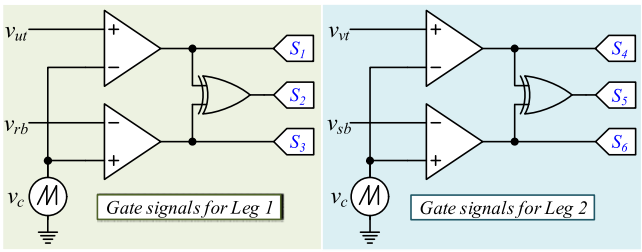

Fig. 8. Logical block diagram for gate signals generation.

system and CF modes of operation such as online UPS system, constant speed drive, and power conditioner. The continuous and discontinuous PWM schemes that can be applied to the proposed inverter are briefly analyzed in the following sections.

A. Continuous PWM Scheme

In this PWM scheme, all switches operate at high frequency. The general logical block diagram for gate signals generation is shown in Fig. 8. The gate signals for each switching leg are generated by comparing two sinusoidal modulating signals with sawtooth or triangular carrier (v_c). v_{ut} and v_{rb} represent the modulating signals for the top and bottom terminals (u and r) of leg 1, whereas v_{vt} and v_{sb} represent the modulating signals for the top and bottom terminals (v and s) of leg 2. For ease of practical implementation, the values of carrier and modulating signals are scaled down in the range of "0" to "1" and are given by

$$\begin{cases} v_{ut} = 0.5 + 0.5M_t \sin(2\pi f_t t) + v_{off-t} \\ v_{vt} = 0.5 + 0.5M_t \sin(2\pi f_t t + \pi) + v_{off-t} \end{cases} \tag{3}$$

$$\begin{cases} v_{rb} = 0.5 + 0.5M_b \sin(2\pi f_b t + \varphi) + v_{off-b} \\ v_{sb} = 0.5 + 0.5M_b \sin(2\pi f_b t + \pi + \varphi) + v_{off-b} \end{cases} \tag{4}$$

where $v_{off\cdot t}$ and $v_{off\cdot b}$ are the top and bottom offset voltages used to ensure the switching constraints. For the widest range of modulation indices, these offset voltages are given by

$$\begin{cases} v_{off\cdot t} = 0.5 - 0.5M_t \\ v_{off\cdot b} = 0.5M_b - 0.5. \end{cases} \tag{5}$$

The illustration of the block diagram of Fig. 8 to generate continuous PWM signals for the proposed inverter is shown in Fig. 9. In order to ensure that the top modulating signal v_{ut} of 3SL is always greater than the bottom modulating signal v_{rb}, the sum of maximum achievable modulation indices $(M_t + M_b)$ in DF mode must be kept less than or equal to "1." In contrast to DF mode, the CF mode can achieve higher values of modulation indices and $(M_t + M_b)$ can be equal to "2" given that the phase difference φ between the two outputs is zero. To ensure $v_{ut} \geq v_{rb}$, the following inequality, which is derived from (3)–(5) by putting $f_t = f_b = f$, should be satisfied:

$$M_b \leq \frac{2 + M_t \sin(2\pi ft) - M_t}{\sin(2\pi ft + \varphi) + 1}. \tag{6}$$

Using (6), the maximum achievable values of M_b, M_t, or φ can be determined by assigning values to any two of them.

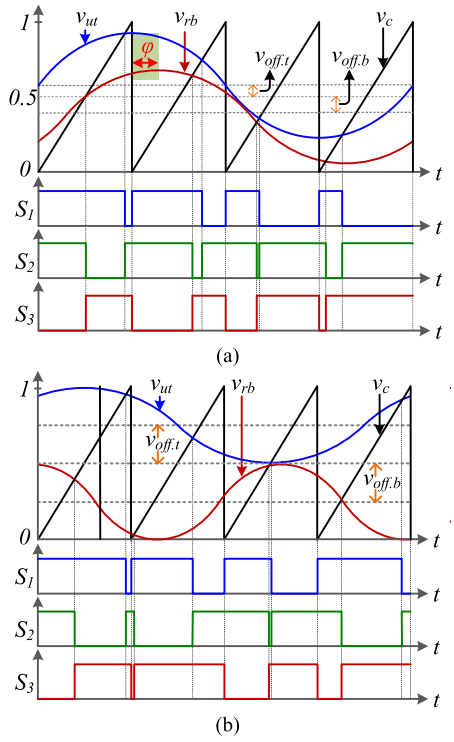

Fig. 9. Gate signals for the 3SL of the proposed inverter using continuous PWM scheme. (a) CF mode. (b) DF mode.

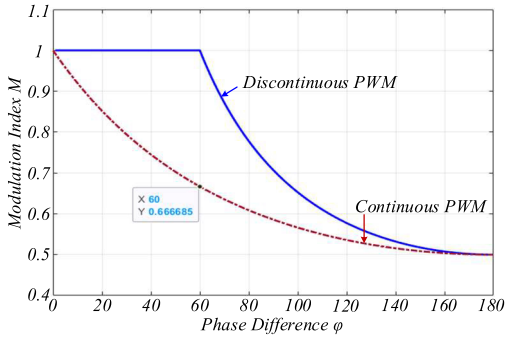

Fig. 10. Modulation index versus phase difference in CF mode with both continuous and discontinuous PWM schemes.

Putting the values of M_t and φ, the absolute minimum of right-hand side of (6) can be calculated, which in terms determine the maximum value of M_b. As an example, if $M_t = M_b = M$, (6) can be simplified to give the following equation:

$$M \leq \frac{2}{2 + \sin(2\pi ft + \varphi) - \sin(2\pi ft)}. \tag{7}$$

If $\varphi = 0°$, then (7) implies that $M \leq 1$ and hence both outputs can achieve modulation indices of "1," which verify the earlier discussion as well. The graph of modulation index M versus phase difference φ is shown in Fig. 10.

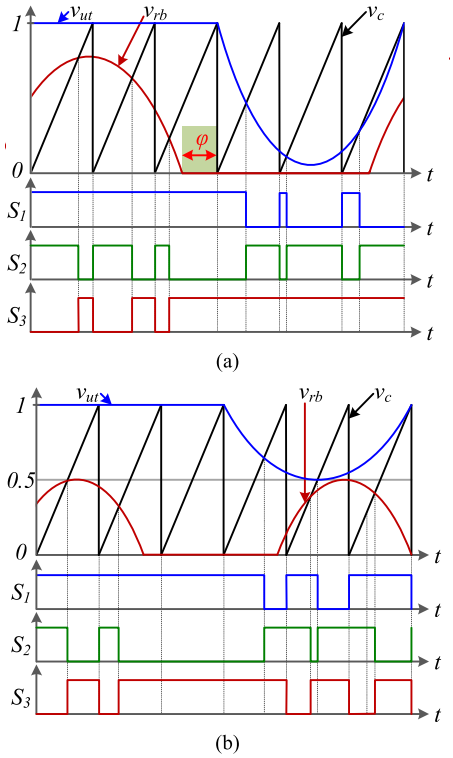

Fig. 11. Gate signals for the 3SL of the proposed inverter using discontinuous PWM scheme. (a) CF mode. (b) DF mode.

B. Discontinuous PWM Scheme

In discontinuous PWM, both top (S_1) and bottom (S_3) switches of 3SL are clamped and not switching for one half of the output voltage and hence switching losses are reduced. The gate signals generation is illustrated in Fig. 11 and the modulating signals are given by

$$v_{ut} = \begin{cases} 1; & 0 \le 2\pi f_t t \le \pi \\ 1 + M_t \sin(2\pi f_t t); & \pi \le 2\pi f_t t \le 2\pi \end{cases} \quad (8)$$

$$v_{vt} = \begin{cases} 1 + M_t sin(2\pi f_t t + \pi); & 0 \le 2\pi f_t t \le \pi \\ 1; & \pi \le 2\pi f_t t \le 2\pi \end{cases} \quad (9)$$

$$v_{rb} = \begin{cases} M_b sin(2\pi f_b t + \varphi); & 0 \le 2\pi f_b t + \varphi \le \pi \\ 0; & \pi \le 2\pi f_b t + \varphi \le 2\pi \end{cases} \quad (10)$$

$$v_{sb} = \begin{cases} 0; & 0 \le 2\pi f_b t + \varphi \le \pi \\ M_b sin(2\pi f_b t + \varphi + \pi); & \pi \le 2\pi f_b t + \varphi \le 2\pi. \end{cases} \quad (11)$$

In DF mode, the sum of maximum modulation indices $(M_t + M_b)$ is similar to continuous PWM scheme and should be less than or equal to 1. In CF mode, the following equation, which is derived from (8)–(11), must be satisfied:

$$M_b \le \frac{1 + M_t \sin(2\pi ft)}{\sin(2\pi ft + \varphi)}; \quad -\varphi \le 2\pi ft \le 2\pi. \quad (12)$$

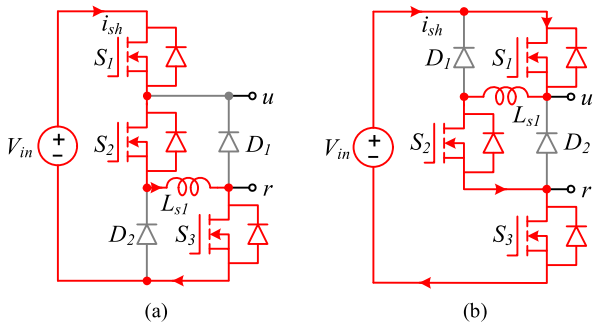

Fig. 12. Current directions in fault conditions. (a) Type I. (b) Type II.

Considering $M_t = M_b = M$, (12) can further be simplified as follows:

$$M \le \frac{1}{\sin(2\pi ft + \varphi) - \sin(2\pi ft)}; \; -\varphi \le 2\pi ft \le 2\pi. \quad (13)$$

By keeping in mind that the value of modulation index M cannot exceed unity, the graph of modulation index M versus phase difference φ is plotted and shown in Fig. 10. It can be clearly observed in Fig. 10 that in discontinuous PWM scheme, both the outputs can achieve unity modulation indices even when the phase difference φ is 60°. The modulation index goes on decreasing when $\varphi > 60°$ but it still remains higher than the continuous PWM scheme. Hence, it can be concluded that apart from reducing the losses due to clamping of switches, the discontinuous PWM scheme can also improve the maximum achievable modulation index in CF mode when $\varphi > 0°$.

C. Operation of the Proposed 3SL

The proposed Type I and Type II dual-buck 3SLs, which are shown in Fig. 4, consist of a shoot-through inductor $(L_{s1}\ or\ L_{s2})$ and therefore its operation is different from the conventional 3SLs of Figs. 2(a) and 3(d). The inductors L_{s1} and L_{s2} actually limit the shoot-through current in fault conditions and provide sufficient time for the protection circuit to shut down the system and hence improve the reliability by protecting the semiconductor devices. The current directions in the proposed 3SL when all the switches are turned ON in the fault conditions are shown in Fig. 12. The shoot-through inductors can be selected based on the following equation:

$$\Delta i_{Lf} = \frac{V_{Lf}\Delta t_f}{L_s} = \frac{V_{in}\Delta t_f}{L_s} \quad (14)$$

where $L_s = L_{s1} = L_{s2}$ represent the shoot-through inductors of the switching legs, whereas Δi_{Lf}, V_{Lf}, and Δt_f represent the increase in current of inductor L_s, voltage appearing across inductor L_s, and time duration of the fault conditions, respectively.

The current directions in the proposed Type I 3SL in normal conditions during each switching states are shown in Figs. 13 –18. Although there are only three permissible switching states for the 3SL, different modes can appear for each switching state due to various conditions of output current polarity in the proposed and conventional dual-output inverters [3], [12]. As

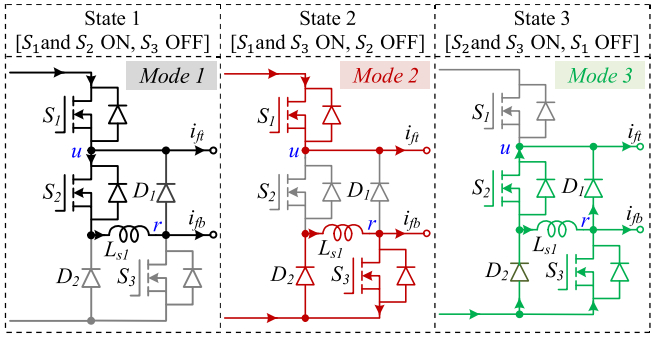

Fig. 13. Current directions in the proposed Type I 3SL during the condition when $i_{ft} > 0$ and $i_{fb} > 0$.

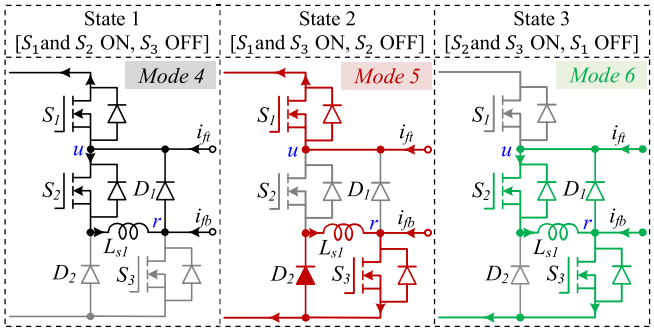

Fig. 14. Current directions in the proposed Type I 3SL during the condition when $i_{ft} < 0$ and $i_{fb} < 0$.

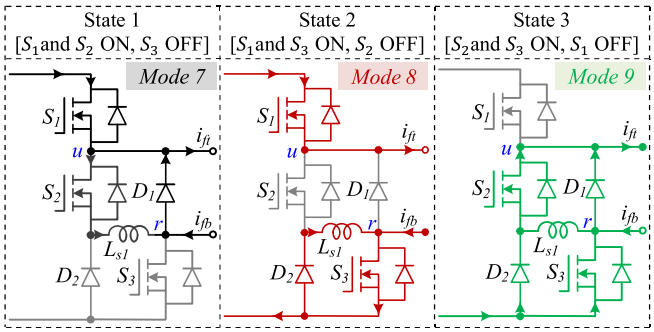

Fig. 15. Current directions in the proposed Type I 3SL during the condition when $i_{ft} > 0$; $i_{fb} < 0$; and $i_{ft} + i_{fb} > 0$.

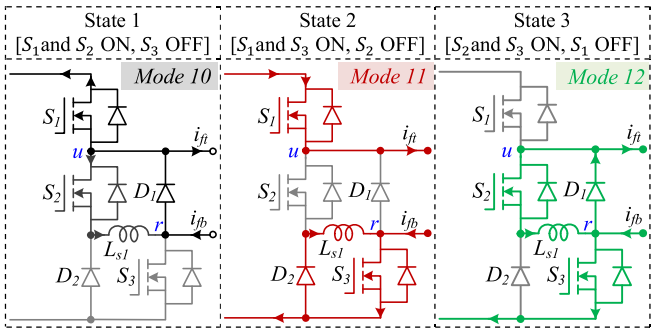

Fig. 16. Current directions in the proposed Type I 3SL during the condition when $i_{ft} > 0$; $i_{fb} < 0$; and $i_{ft} + i_{fb} < 0$.

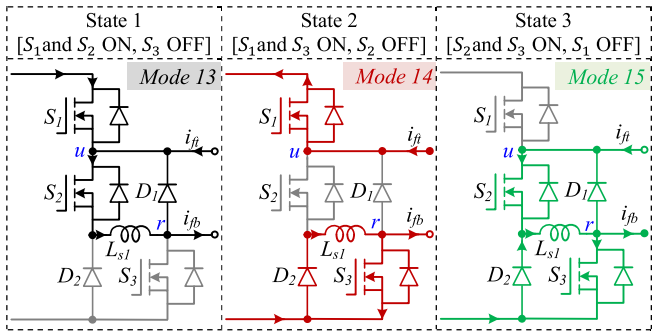

Fig. 17. Current directions in the proposed Type I 3SL during the condition when $i_{ft}\langle 0;\ i_{fb}\rangle 0$; and $i_{ft} + i_{fb} > 0$.

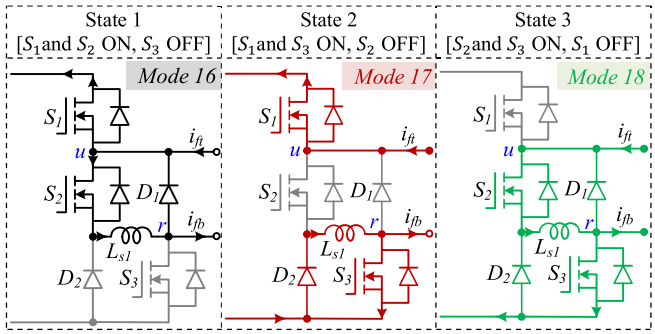

Fig. 18. Current directions in the proposed Type I 3SL during the condition when $i_{ft}\langle 0;\ i_{fb}\rangle 0$; and $i_{ft} + i_{fb} < 0$.

an example, for the switching state 1 in which S_1 and S_2 are ON while S_3 is OFF, the possible modes are 1, 4, 7, 10, 13, and 16. If the proposed inverter is operated only in CF mode with zero phase shift and unity power factor, then it means that both output voltages and currents are always in phase. As a result, only modes 1 and 4 will appear in switching state 1. However, if the inverter operates either in CF mode with some phase difference between the two outputs or in DF mode then modes 7, 10, 13, and 16 can appear due to different magnitudes and polarity of the output currents. Apart from this, the inductor current cannot change instantly and is considered constant during a switching period for simplicity in Figs. 13–18. i_{ft} and i_{fb} represent the top and bottom output filter inductor currents and are positive if they flow out of the nodes u and r, respectively. On the other hand, i_{ft} and i_{fb} are considered negative if they flow into the nodes u and r. Furthermore, current through the shoot-through inductor L_{s1} flows in only one direction and is verified through simulations and experimental results in the upcoming section. Now, consider the switching states in the condition when both i_{ft} and i_{fb} are greater than zero as shown in Fig. 13. In mode 1 of Fig. 13, switch S_3 is OFF and the diode D_2 is reverse biased. Switch S_1 conducts the total output current $(i_{ft} + i_{fb})$, whereas switch S_2 and inductor L_{s1} conduct the bottom output current i_{fb}. Diode D_1 conducts only the ripple current of inductor L_{s1} momentarily. In mode 2, switch S_1 conducts the top output current i_{ft}, whereas diode D_2 and L_{s1} conduct the bottom output current i_{fb}. Switch S_3 conducts only the ripple current of inductor L_{s1} momentarily. In mode 3, L_{s1} carries

TABLE II
CURRENT FLOWING THROUGH THE SHOOT-THROUGH INDUCTOR L_{s1}

No.	Conditions	Current in the shoot-through inductor
1	$i_{ft} > 0;\ i_{fb} > 0$	i_{fb}
2	$i_{ft} < 0;\ i_{fb} < 0$	$-i_{ft}$
3	$i_{ft} > 0;\ i_{fb} < 0;$	0 (only ripple current)
4	$i_{ft} < 0;\ i_{fb} > 0;\ i_{ft} + i_{fb} > 0$	i_{fb}
5	$i_{ft} < 0;\ i_{fb} > 0;\ i_{ft} + i_{fb} < 0$	$-i_{ft}$

the current i_{fb}, whereas the current i_{ft} flows through D_2, S_2 and S_3, D_1. The current directions in the remaining possible conditions emerging due to different polarities of i_{ft} and i_{fb} are also analyzed similarly and are shown in Figs. 14–18. The current flowing in the shoot-through inductor L_{s1} is listed in Table II. The current directions in the proposed Type II 3SL are not included due to page limitations. However, simulation results of Type II dual-output inverter in Section IV verify the functionality and effectiveness of Type II 3SL as well.

D. Design Guidelines of the Proposed 3SL Inverter

The choice of input dc-link voltage V_{in} is a very important because the voltage stresses V_{stress} of input capacitor, switches, and diodes are all equal to the input voltage. The input dc-link voltage is inversely proportional to the modulation indices and is determined by the following formula:

$$V_{\text{stress}} = V_{in} = \frac{V_{ot}}{M_t} = \frac{V_{ob}}{M_b} \tag{15}$$

where V_{ot}, V_{ob} are the magnitudes of the top and bottom outputs voltages, whereas M_t and M_b are the top and bottom modulation indices. In CF mode, each modulation index can reach to unity and hence input dc-link voltage will be equal to the peak value of the output voltages. However as mentioned earlier, the maximum achievable modulation indices (M_t, M_b) in continuous and discontinuous PWM schemes at CF mode depend on the phase difference φ between the two output voltages as well. For ease of simplification, consider the range of modulation indices for both the outputs is same, which means $M_t = M_b = M$ and $V_{ot} = V_{ob} = V_o$. Putting these values in (15), the normalized voltage stress in CF mode is given by

$$\left(\frac{V_{\text{stress}}}{V_o}\right)_{CF} = \frac{1}{M}. \tag{16}$$

Using the value of M from (7) in (16) will give the normalized voltage stresses in CF and continuous PWM scheme $(\frac{V_{\text{stress}}}{V_o})_{CF}^{CPWM}$, whereas using the value of M from (13) in (16) will give the normalized voltage stresses in CF and discontinuous PWM scheme $(\frac{V_{\text{stress}}}{V_o})_{CF}^{DPWM}$. The graph of M in continuous and discontinuous PWM scheme with respect to φ is already included in Fig. 10, whereas the graphs of $(\frac{V_{\text{stress}}}{V_o})_{CF}^{CPWM}$ and $(\frac{V_{\text{stress}}}{V_o})_{CF}^{DPWM}$, which are equal to the inverse of M, are shown in Fig. 19. The graph shows that voltage stresses are minimum when the phase difference between the two outputs is zero and they increase when the phase difference is increased. Furthermore, it can be noticed that the voltage stresses in discontinuous

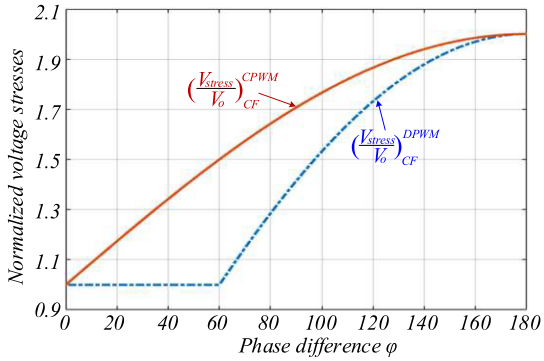

Fig. 19. Normalized voltage stresses versus phase difference in CF mode with both continuous and discontinuous PWM schemes.

PWM are always less than the continuous PWM scheme and remains at a minimum value until the phase difference is increased beyond 60°. In DF mode, $M_t + M_b \leq 1$ like conventional 3SL inverters. Depending on the modulation indices the top output voltage is either greater, equal, or smaller than the bottom voltage. As an example, if $M_b = k \cdot M_t$, where $0 \leq k \leq 1$, the top output voltage will be greater than or equal to the bottom output voltage and is represented by $V_{ob} = k \cdot V_{ot}$. Putting these values in (15), the normalized voltage stresses to the maximum output voltage (V_{ot}) in DF mode can then be calculated as follows:

$$\left(\frac{V_{\text{stress}}}{V_{ot}}\right)_{DF} = \frac{1}{M_t}. \tag{17}$$

Similarly, if $M_t = k \cdot M_b$, where $0 \leq k \leq 1$, the bottom output voltage will be greater than or equal to the top output voltage and is represented by $V_{ot} = k \cdot V_{ob}$. Putting these values in (15), the normalized voltage stresses to the maximum output voltage (V_{ob}) in DF mode can then be calculated as follows:

$$\left(\frac{V_{\text{stress}}}{V_{ob}}\right)_{DF} = \frac{1}{M_b}. \tag{18}$$

The graphs of $(\frac{V_{\text{stress}}}{V_{ob}})_{DF}$ and $(\frac{V_{\text{stress}}}{V_{ot}})_{DF}$ versus modulation index for different values of "k" are shown in Fig. 20. It can be observed that when $k = 0$, either M_t or M_b is equal to 1 and the normalized voltage stresses are minimum. As the value of k is increased the voltage stresses are also increased. It means that the DF mode of the proposed inverter is suitable for applications in which the modulation index of one of the outputs is closed to zero and the modulation index of the other output is closed to one such as power decoupling of the double line-frequency ripple in single-phase inverters.

Apart from voltage stresses, the current stresses are also important for the selection of switches and diodes. The equations for current stresses of semiconductor devices are calculated in the worst case conditions and are included in Table III. The current stresses of switches (S_1, S_3, S_4, S_6) and diodes (D_1, D_3) are represented by I_{pk-1}, whereas the current stresses of switches (S_2, D_5) and diodes (D_2, D_4) are represented by I_{pk-2}. I_{ot} and I_{ob} are the magnitudes of the current flowing through the top and bottom output loads, P_{ot} is the output power

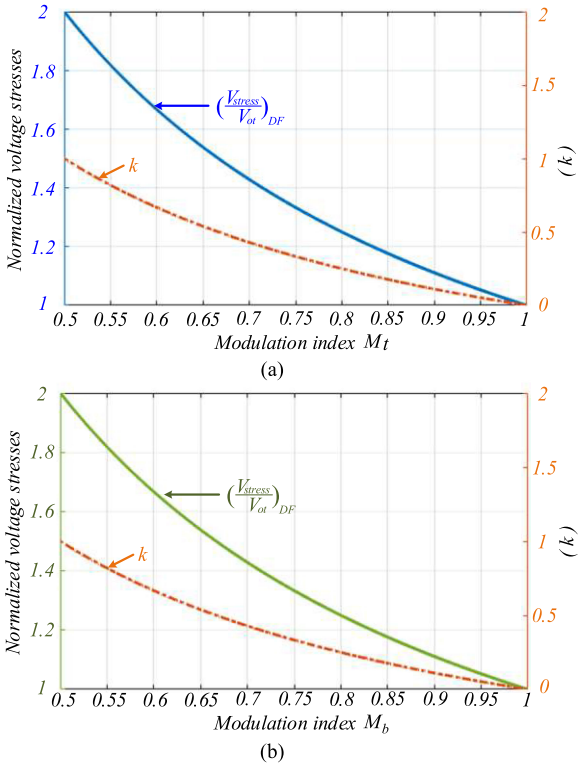

Fig. 20. Normalized voltage stresses versus modulation index for different values of "k" in DF mode. (a) $(V_{\text{stress}}/V_{ot})_{DF}$ and k versus M_t. (b) $(V_{\text{stress}}/V_{ob})_{DF}$ and k versus M_b.

TABLE III
CURRENT STRESSES OF THE SEMICONDUCTOR DEVICES

Switches (S_1, S_3, S_4, S_6) Diodes (D_1, D_3)	$I_{pk-1} = I_{ot} + I_{ob} = \frac{2P_{ot}}{V_{ot}}\left[1 + \frac{k_1}{k_2}\right]$
Switches (S_2, D_5) Diodes (D_2, D_4)	$I_{pk-2} = max(I_{ot}, I_{ob}) = max\left(\frac{2P_{ot}}{V_{ot}}, \frac{k_1}{k_2}.\frac{2P_{ot}}{V_{ot}}\right)$

of the top load, V_{ot} is the peak value of top output voltage, k_1/k_2 is a constant that can be greater than or equal to zero, and $\max(I_{ot}, I_{ob})$ is a function whose output is the maximum value between I_{ot} and I_{ob}. All the equations are derived in terms of power and voltage of the top load by using $P_{ob} = k_1 \cdot P_{ot}$ and $V_{ob} = k_2 \cdot V_{ot}$, where k_1 and k_2 are constants and they are greater than or equal to zero. As an example, let us consider $k_1 = 1$ and then putting the values of k_1 in $P_{ob} = k_1 \cdot P_{ot}$ implies that $P_{ob} = P_{ot}$. Similarly, if $k_2 = 1$, then $V_{ob} = k_1 \cdot V_{ot}$ implies that $V_{ob} = V_{ot}$. The normalized current stresses $(I_{pk-1} \cdot V_{ot}/2P_{ot})$ and $(I_{pk-2} \cdot V_{ot}/2P_{ot})$ versus k_1/k_2 are plotted in Fig. 21.

The selection of input capacitors and output filter inductors are similar to the conventional dual-output inverters [3], [12] and the shoot-through inductors can be selected based on (14). The filter inductors are determined by the following general formula:

$$L_f = \frac{v_o\,(1-D)\,T_s}{\Delta i_L} \tag{19}$$

where L_f is the top or bottom filter inductor, v_o and D are the corresponding output voltages and duty ratios, T_s is the switching time period, and Δi_L is the allowable inductor current ripple, which is usually selected in the range of $(20-40)\%$ of the corresponding peak load current. In case of motor drive, output filter inductors are not required due to the inductive nature of the motor.

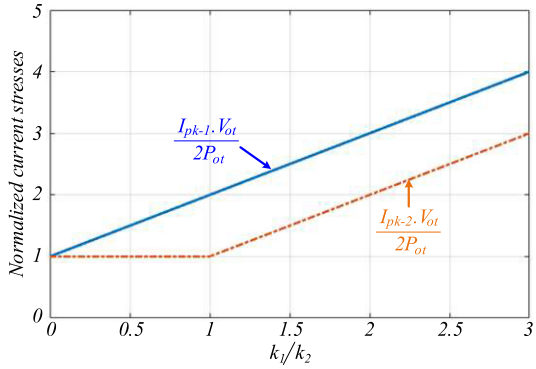

Fig. 21. Normalized current stresses of semiconductor devices versus k_1/k_2.

TABLE IV
SPECIFICATIONS OF THE PROPOSED DUAL-OUTPUT INVERTER

Input voltage (V_{in})	$(320-440)\,V$
Power (P_o)	$(0.5-2)\,kW$
Switching frequency	$50\,kHz$
Load resistors $(R_t = R_b)$	$(50-200)\,\Omega$
Switches $(S_1 - S_6)$	UF3C065040K3S
Diodes $(D_1 - D_4)$	RHRG3060
Shoot-through inductors (L_{s1}, L_{s2})	$100\,\mu H$
Output filter inductors (L_{ft}, L_{fb})	$760\,\mu H$
Output filter capacitors (C_{ft}, C_{fb})	$5.6\,\mu F$

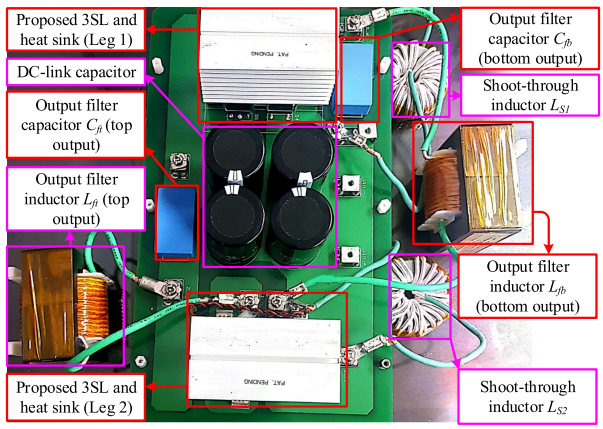

Fig. 22. Prototype photograph of the proposed Type I 3SL dual output inverter.

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the concept of the proposed dual-buck 3SL, a hardware prototype of dual-output inverter is built and both simulations and experimental results are provided with system parameters given in Table IV. The photograph of hardware prototype is shown in Fig. 22. Inductors L_{ft} and L_{fb} are output filter inductors and are not required in case motor drives. Simulation results of proposed Type I, Type II, and conventional

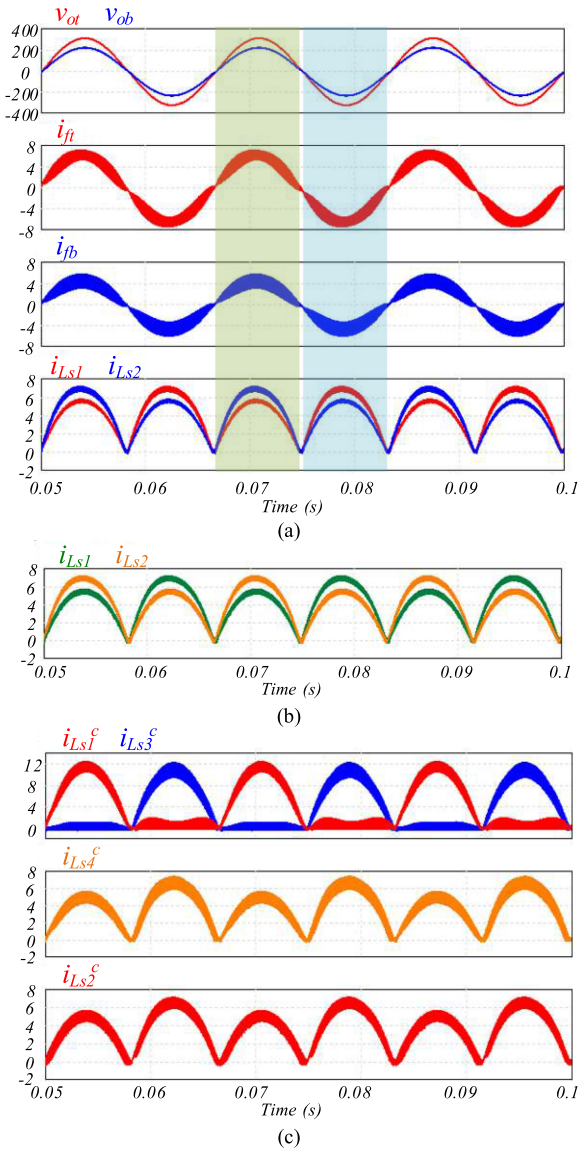

Fig. 23. Simulation results. (a) Top output voltage v_{ot}, bottom output voltage v_{bt}, top and bottom current of filter inductors $[i_{ft}, i_{bt}]$, and shoot-through inductors current $[i_{Ls1}, i_{Ls2}]$ of the proposed Type I inverter. (b) Shoot-through inductors current of the proposed Type II inverter. (c) Shoot-through inductors current $(i_{Ls1}^c - i_{Ls4}^c)$ of conventional dual-buck inverter [Fig. 3(d)].

dual-buck dual-output inverter [see Fig. 3(d)] with $M_t = 0.8$ and $M_b = 0.58$ in CF mode are shown in Fig. 23. Fig. 23(a) shows the top and bottom output voltages $(v_{ot},\ v_{ob})$, current of top and bottom filter inductors $(i_{ft},\ i_{fb})$, and shoot-through inductors current $(i_{Ls1},\ i_{Ls2})$ of the proposed Type I inverter. It can be observed that current through the shoot-through inductors is always unidirectional and the maximum value of i_{Ls1} is equal to the maximum value of i_{fb} when both i_{ft} and i_{fb} are greater than zero (see light-green highlighted region in Fig. 23). Similarly, the peak value of i_{Ls1} is equal to the maximum value of i_{ft} when both i_{ft} and i_{fb} are smaller than zero (see light-blue highlighted region). These observations exactly match with the theoretical analysis and Table II presented earlier. Fig. 23(b)

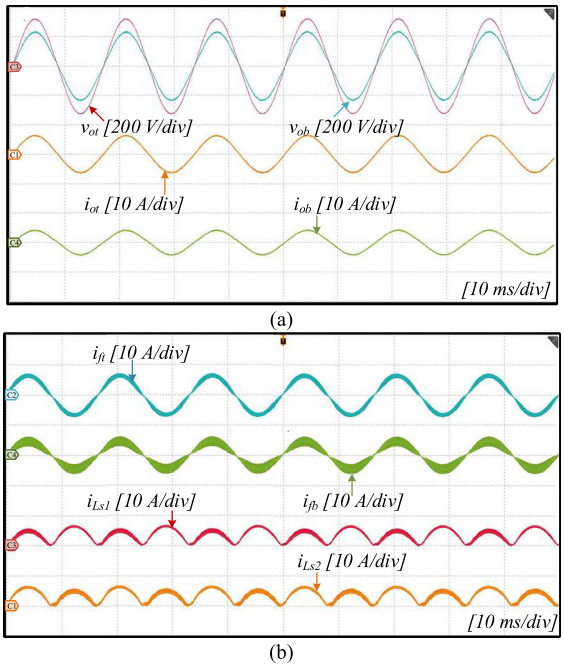

Fig. 24. Experimental results in CF mode and zero phase-shift using continuous PWM scheme. (a) Top output voltage v_{ot}, bottom output voltage v_{ob}, top output current i_{ot}, bottom output current i_{ob}. (b) Top and bottom filter inductors current $(i_{ft},\ i_{fb})$ and shoot-through inductors current $(i_{Ls1},\ i_{Ls2})$.

shows the simulation results of shoot-through inductors current of the Type II inverter at the same output voltages. The similar waveforms of Type I and Type II inverters verify the functionality of the proposed Type II 3SL as well. Fig. 23(c) shows the simulation waveforms of current flowing through the shoot-through inductors of the 3SL of conventional dual-buck dual-output inverter of Fig. 3(d) while keeping the equivalent value of shoot-through inductors similar to the proposed 3SL. It should be noticed here that the conventional 3SL dual-buck inverter uses four shoot-through inductors in each switching leg and the peak current of two of them (i_{Ls2}^c, i_{Ls4}^c) are similar to the inductor current of the proposed inverter $(i_{Ls1}\ or\ i_{Ls2})$. The current of other two inductors (i_{Ls1}^c, i_{Ls3}^c) have a high peak value that equals the sum of filter inductors current $i_{ft} + i_{fb}$.

The experimental results are performed with specifications mentioned in Table IV and a digital signal controller TMS320F28335 is used to generate gate signals with a constant 0.2 μs deadtime. Fig. 24 shows the experimental waveforms using continuous PWM scheme in CF mode, phase difference $\varphi = 0$, $M_t = 0.8$, and $M_b = 0.58$. Fig. 24(a) shows the output voltages $(v_{ot},\ v_{ob})$ and output currents $(i_{ot},\ i_{ob})$, whereas Fig. 24(b) shows the current of filter inductors $(i_{ft},\ i_{fb})$ and shoot-through inductors $(i_{Ls1},\ i_{Ls2})$. Fig. 25 shows the output voltages $(v_{ot},\ v_{ob})$ and output currents $(i_{ot},\ i_{ob})$ in the worst conditions of Table IV, that is, $V_{in} = 440$ V and $P_o = 0.5$ kW. The experimental results with phase difference $\varphi = 15^\circ$ are shown in Fig. 26. The waveforms imply that the switches (S_1, S_2, and S_3) of 3SL operate at high-frequency due to continuous PWM scheme and their peak drain-to-source voltages $(v_{ds1},\ v_{ds2},$ and $v_{ds3})$ are equal to the input voltage. Experimental

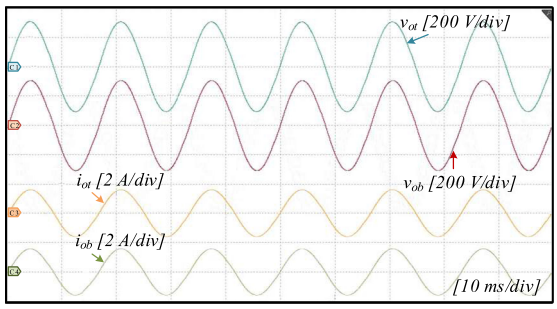

Fig. 25. Experimental waveforms of top output voltage v_{ot}, bottom output voltage v_{ob}, top output current i_{ot}, and bottom output current i_{ob} in CF mode at $V_{in} = 440$ V and $P_o = 0.5$ kW.

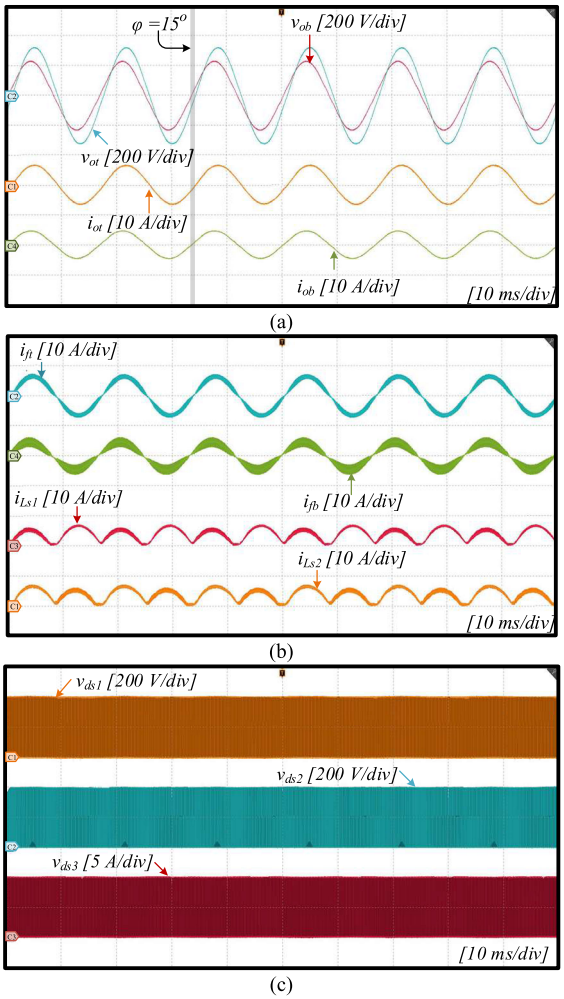

Fig. 26. Experimental results using continuous PWM and in CF mode with $\varphi = 15°$. (a) Output voltages and output currents. (b) Filter inductors current and shoot-through inductors current. (c) Drain-to-source voltages of switches S_1, S_2, and S_3.

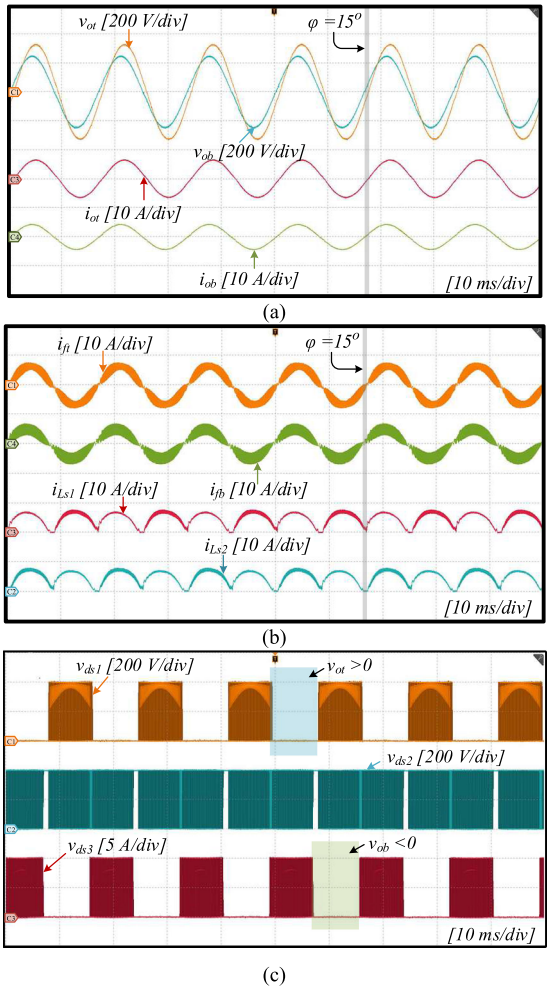

Fig. 27. Experimental waveforms using discontinuous PWM in CF mode with $\varphi = 15°$. (a) Output voltages and output currents. (b) Filter inductors current and shoot-through inductors current. (c) Drain-to-source voltages of switches S_1, S_2, and S_3.

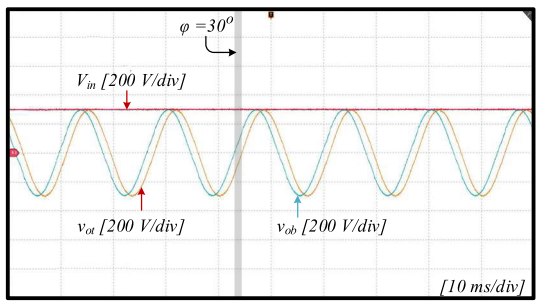

Fig. 28. Experimental waveforms of output voltages (v_{ot}, v_{ob}) and input voltage V_{in} using discontinuous PWM in CF mode with $\varphi = 30°$.

results in CF mode and discontinuous PWM scheme are shown in Fig. 27. It can be observed that switches S_1 and S_3 operate at high frequency in only one half of the output voltage and hence switching losses are reduced. The experimental waveforms at input voltage V_{in} equal to 300 V and $M_t = M_b = 1$ with phase difference $\varphi = 30°$ while using discontinuous PWM are shown in Fig. 28. The results in Fig. 28 actually confirm the previous analysis that discontinuous PWM can improve range of modulation indices and in terms reduce the voltage stresses on the switches when the phase difference between the two outputs is greater than zero degree. In order to achieve the same peak output voltages of 300 V while using continuous PWM scheme, the achievable modulation indices with $\varphi = 30°$ are reduced to 0.79

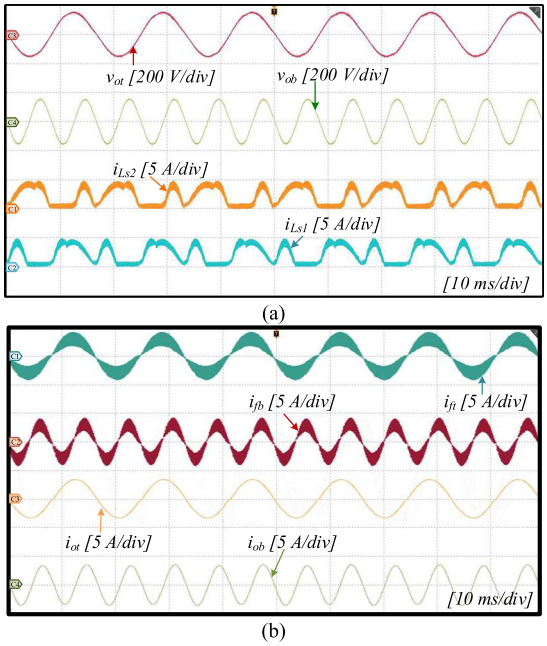

Fig. 29. Experimental waveforms in DF mode using continuous PWM scheme. (a) Output voltages and shoot-through inductors current. (b) Filter inductors current and output current.

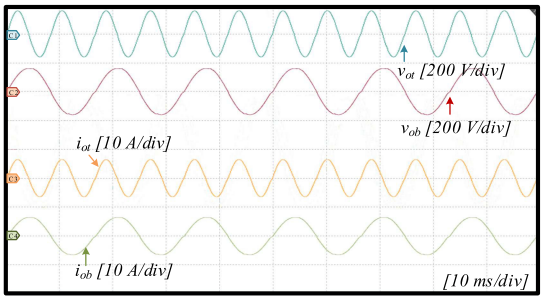

Fig. 30. Experimental waveforms of top output voltage v_{ot}, bottom output voltage v_{ob}, top output current i_{ot}, and bottom output current i_{ob} in DF mode at $V_{in} = 440$ V and $P_o = 0.5$ kW.

according to (7) and Fig. 10. It implies that the required input voltage will be equal to 380 V in continuous PWM scheme and hence results in increasing the voltage stresses on the switches. The experimental waveforms of output voltages, current through the shoot-through inductors, filter inductors current, and output currents at $V_{in} = 400$ V and $M_t = M_b = 0.4$ in DF mode are shown in Fig. 29. Fig. 30 shows the output voltages $(v_{ot},\ v_{ob})$ and output currents $(i_{ot},\ i_{ob})$ in the worst conditions of Table IV, that is, $V_{in} = 440$ V and $P_o = 0.5$ kW. Finally, two sets of experiments are performed in CF and DF modes in such a way that the top output is connected to a 50 Ω resistive load and the bottom output is connected to a nonlinear load. The nonlinear load consists of a diode bridge rectifier followed by a 560 μF capacitor and 100 Ω load resistor. The waveforms of output voltages and currents in CF mode are shown in Fig. 31(a), whereas in DF mode are shown in Fig. 31(b). These results confirm that the two outputs of the proposed inverter can work independently.

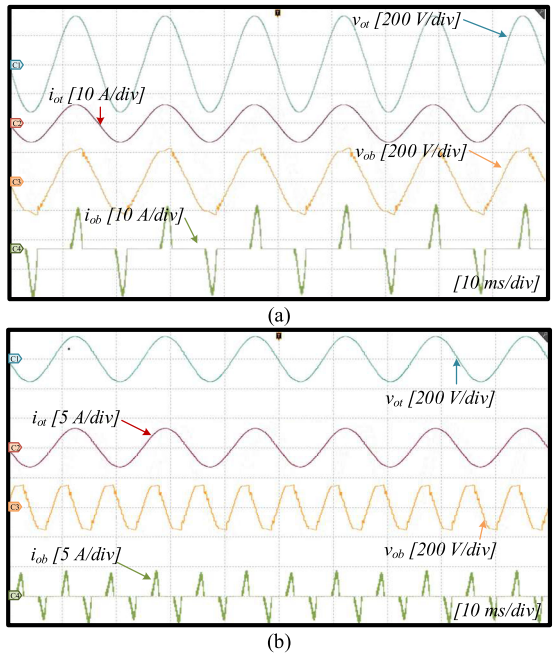

Fig. 31. Output voltages and currents of the resistive and nonlinear loads. (a) CF mode. (b) DF mode.

TABLE V
COMPARISON OF THE PROPOSED INVERTER WITH CONVENTIONAL TOPOLOGIES

Parameters	Proposed	DB-6SWI	6SWI	2FBI
No. of switches	6	6	6	8
No. of diodes	4	6	-	-
No. of shoot-though inductors	2	8	-	-
Current stresses of inductors	$max(i_{ot}, i_{ob})$	4 $[max(i_{ot}, i_{ob})]$ 4 $[i_{ot} + i_{ob}]$	-	-
Shoot-through Current Problem	No	No	Yes	Yes
Reverse recovery of Mosfets body diode	No	No	Yes	Yes
Quality of Output waveforms	High	High	High	High
Efficiency	High	High	Low	Low

V. COMPARATIVE ANALYSIS OF THE PROPOSED INVERTER

The comparison of the main features of the proposed inverter with the conventional dual-output six-switch inverter (6SWI) [12], conventional dual-buck six-switch inverter (DB-6SWI) [3], and two parallel conventional full-bridge inverters (2FBIs) is included in Table V. It can be observed that conventional 6SWI and 2FBI do not need external diodes and shoot-through inductors. However, the current shoot-through issue is a major reliability concerns for these inverters. Moreover, the quality of output waveforms is deteriorated due to the finite deadtime in the switching signals and the efficiency is low due to the slow MOSFETs body diode. For efficiency comparison of the conventional DB-6SWI with 6SWI, kindly refer to [3].

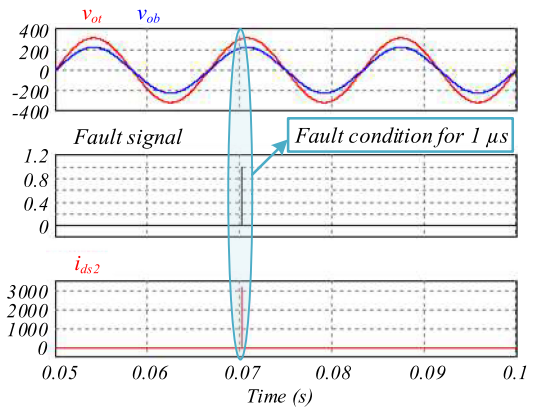

Fig. 32. Simulation results of conventional dual-output inverter during fault conditions.

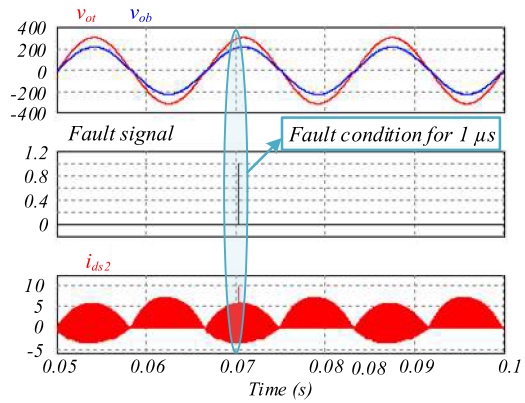

Fig. 33. Simulation results of the proposed dual-output inverter during fault conditions.

To elucidate the effectiveness of the proposed inverter during shoot-through fault, the simulations of the proposed [see Fig. 4(a)] and the conventional 6SWI [see Fig. 2(b)] are performed as an example. The simulation results are adequate because we can easily measure the switches current. To test the performance of the conventional and proposed inverters during fault conditions, all the switches of leg 1 (S_1, S_2, and S_3) are turned ON for 1 μs deliberately. The simulation results of the conventional dual-output inverter are shown in Fig. 32. In Fig. 32, v_{ot} and v_{ob} are the top and bottom output voltages, i_{ds2} is the current flowing through switch S_2 , whereas the fault signal represents the conditions in which all the switches of leg I are turned ON. It can be observed in Fig. 32 that the input voltage source is short-circuited during fault conditions and huge current spikes (31 000 A) are generated through switch S_2. These current spikes are also generated in other switches of the Leg 1 (S_1, S_3) and can destroy them. This short circuit is the main reliability killer in the conventional inverters. The simulation results of the proposed dual-output inverter are shown in Fig. 33. It can be observed that the proposed inverter works well and no dangerous current spikes are generated during fault conditions. This is because the shoot-through inductor L_{s1} protects the sudden short circuit of the input voltage source.

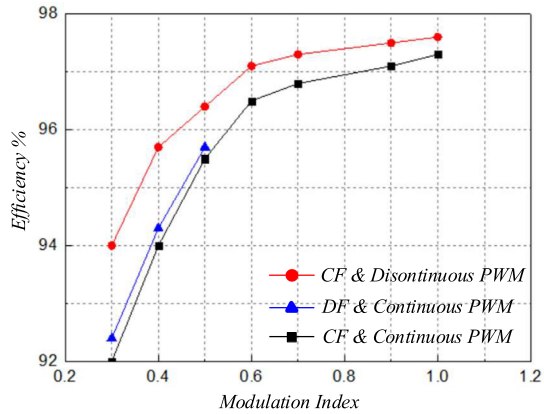

Fig. 34. Efficiency plot of the proposed inverter.

Similarly, Table V presents that the conventional and proposed dual-buck inverters have similar performance, but the proposed inverter has a smaller number of passive components and requires only two inductors and four diodes. The current stresses of the shoot-through inductors in the proposed inverter are smaller as compared to the conventional DB-6SWI and can be verified from simulation results of Fig. 23. The voltage and current stresses of the switches and diodes of the proposed DBI, which are shown in (15) and Table III, are equal to the conventional DB-6SWI [3]. However, the conventional DB-6SWI requires two extra diodes and that is why its total peak switching device power SDP_{pk} is higher than the proposed inverter. The SDP_{pk} indicates the price of semiconductor devices and can be calculated using the method adapted in [34] and [35].

For efficiency plot of the proposed inverter, experiments are performed with the same parameters as listed in Table IV except the input voltage is changed to 320 V. The modulation index is varied and the measured efficiency in CF and DF modes is plotted in Fig. 34. Obviously the discontinuous PWM scheme has the highest efficiency because of the reduced switching losses due to clamping action of the switches. The DF mode of operation has slightly higher efficiency because of the reduced conduction losses as compared to the CF mode but the maximum modulation index is limited to 0.5. Apart from this, the conventional DB-6SWI is also built using same semiconductor devices and its efficiency is compared with the proposed inverter in Fig. 35. It can be observed that efficiency of the proposed inverter is slightly higher than the conventional DB-6SWI probably due to reduced magnetic losses of the shoot-through inductors. To get idea about the profile of efficiency variation with respect to output power, the efficiency at different values of input voltage in CF and continuous PWM scheme is shown in Fig. 36.

Finally, total harmonic distortion (THD) curves of the proposed inverter with varying modulation index and constant input voltage of 320 V in CF mode are included in Fig. 37. Fig. 37 shows that when the deadtime is 0.2 μs, the THD is better as compared to 1 μs deadtime. This verifies that the proposed dual-buck inverter can achieve better quality of output waveforms due to the reduction in deadtime between the gating signals.

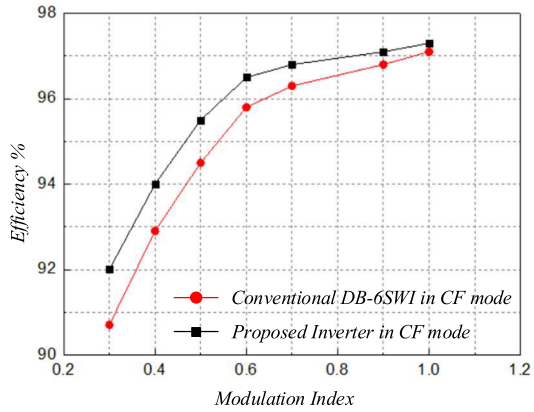

Fig. 35. Efficiency comparison of the conventional DB-6SWI with the proposed inverter.

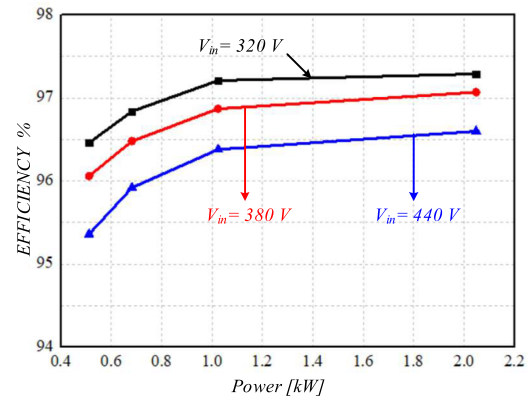

Fig. 36. Efficiency at different input voltages and output power in CF and continuous PWM scheme.

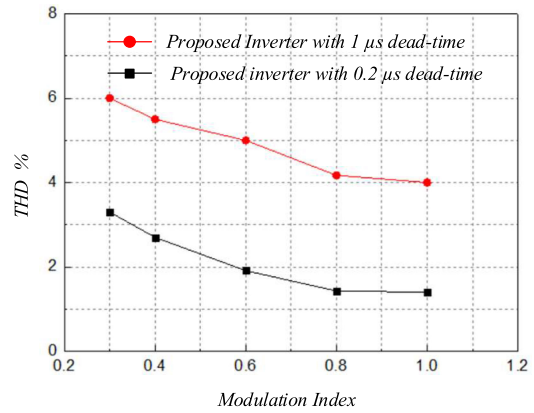

Fig. 37. THD comparison of the proposed inverter at different deadtimes in CF mode of operation.

VI. Conclusion

In this article, a new dual-buck 3SL is proposed for 3SL converters and is successfully introduced in single-phase dual-output inverter. The proposed inverter has less number of passive components as compared to the conventional dual-buck structure and has no shoot-through concerns with improved quality of output waveforms due to the reduction of deadtime. Detailed theoretical analysis, simulations, and experiments are performed and it has been revealed that discontinuous PWM scheme can improve the dc-link voltage utilization in CF mode of operation and hence reduce the switching losses.

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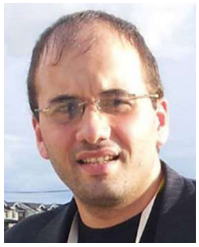

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