An Interleaved Soft Switched High Step-Up Boost Converter With High Power Density for Renewable Energy Applications

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***Abstract*—In this article, a novel soft switched interleaved boost structure with a simple auxiliary circuit is proposed which is suitable for stand-alone loads or ac grid applications. In this topology, coupled inductors and switched capacitor cells of parallel modules are merged to obtain high voltage conversion ratio. The converter also has the capability of adding extra switched capacitor cells to attain very high voltage gain. To provide soft-switching condition in the wide range of output power, a new zero-voltage transition auxiliary circuit is employed which is responsible for soft switching of both phases and benefits from low conduction losses, the minimum number of semiconductor elements, and only one auxiliary gate-driver. These merits provide very high efficiency at both full-load and light loads. More importantly, no auxiliary magnetic components are utilized by taking advantage of the leakage inductance of coupled inductors for the resonant network. All semiconductor components operate under soft switching alleviating the reverse recovery problem and switching losses. Besides, the converter benefits from common ground between input and output which simplify voltage feedback. The experimental results of the interleaved converter prototype with 400-V output voltage at 400 W and 100 kHz switching frequency are provided. The full load efficiency of 98% was achieved and the power density was observed 1.9 W/Cm^3.**

***Index Terms*—Interleaved converter, soft switching, coupled-inductors, renewable energy systems, high voltage gain.**

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I. Introduction

In THE present day, due to the deficiency of fossil fuels and serious environmental problems like global warming and air pollution, clean and eco-friendly energy sources such as fuel cells and photovoltaic systems have experienced meteoric growth [1], [33]. One of the conspicuous applications of these sources is high voltage stand-alone loads (400–800 V) or ac grid applications which require high dc voltage at the input stage. Hence, using such renewable energy sources, which have generally a low generated dc voltage (usually 12–72 V) demands high step-up and high-efficiency dc–dc converters [1], [43].

Fig. 1 illustrates the block diagram of a grid-connected renewable energy system and the importance of high step-up DC-DC converters. The classical boost converter is considered as the first solution to lift the output voltage. However, this converter suffers from low voltage gain and high voltage stress across the switch in such a way that to supply high voltage loads an extreme duty cycle is required. This results in high losses and low efficiency. To address the mentioned limitations, diverse structures have been presented so far [2]. Utilizing coupled inductors, voltage multiplier cells, and switched capacitor techniques in the boost structures are well-known solutions to obtain high voltage gain [3]–[6]. In [7], coupled inductor technique has been presented in which high voltage gain is obtained by adjusting the turn ratio of the coupled inductor. The main issue of using coupled inductor is making voltage spike across the switch due to the leakage inductance. To suppress spike voltage of leakage inductance, clamp and passive structures are applied [8]. Utilizing switched capacitor technique [3], voltage multiplier cell [4], and the combination of them [5] are other general approaches to extend voltage gain. In the converter presented in [9], the switched-capacitor technique is used to achieve high voltage gain. One of the shortcomings of the introduced converter is that the power switch suffers from relatively high voltage stress, though improved voltage gain is achieved.

Using parallel dc–dc structures to increase and attain the desired power level is a common approach for medium and high-power applications. Parallel step-up structures benefit from the plethora of merits including the realization of thermal distribution, increasing power level, reducing current stress of diodes, and size reduction of semiconductor elements.

Among parallel structures, interleaved ones can provide lower input ripple current which is an outstanding feature to reduce the size of the input filter and cost reduction. On the other hand, the same as the traditional boost converter, the conventional interleaved boost structure has low voltage gain [8]. To solve this problem, the abovementioned voltage-boosting techniques are combined with the classical interleaved boost converter, and a high voltage gain is obtained [10]. In [11] and [12], coupled inductor and switched capacitor cells are employed in the interleaved structure and high voltage gain is achieved without utilizing a large duty cycle. Also, in these converters, leakage energy is absorbed and spike voltage across the switches is suppressed by using the passive clamp technique. Nonetheless, semiconductors in these converters operate under hard switching conditions, and many passive elements are utilized resulting in excess cost and low efficiency.

The necessity of employing converters with the high-power density and high efficiency in today's power electronics applications requires using soft switching techniques to be able to augment the switching frequency and improve the efficiency of the converters [13]. Various soft-switching methods such as lossless snubbers, active clamp, and ZVT techniques have been presented by far [14]–[25]. The lossless passive snubber is a general technique to provide soft switching performance in which no extra auxiliary switch is utilized. These structures suffer from high number of passive elements resulting in high EMI and conduction losses. Also, in the lossless snubber techniques, due to providing zero-current turn-on condition (ZCS) and having capacitive turn-on loss (E_{oss}), the efficiency is adversely affected, and the switching frequency is confined [14], [15]. Another effective soft-switching technique is the active clamp, which employs a low number of components containing an extra switch and a capacitor which contributes to high efficiency and power density [16]–[20]. The main issue with this technique is losing soft switching performance at light loads, inasmuch as discharging the snubber capacitor and proving soft-switching condition at turn on instances is dependent on output current and the stored energy in the leakage inductance [13]. In [20], an active clamp interleaved step-up converter is proposed. To provide soft-switching condition in a wide range of output power, a very large leakage inductance is required to use. This results in the lost duty cycle and extra losses, degrading the voltage gain of this converter. Unlike active clamp circuits, the zero-voltage transition (ZVT) technique can provide soft-switching conditions in a wide range of output power and input voltage independent of output load. In [26]–[31], different ZVT cells composed of additional semiconductors, windings, and cores are employed for the boost converter to achieve soft switching condition which has a complex structure and requires high cost.

Using soft switching techniques in the interleaved step-up structures is also vital especially for medium and high-power high-frequency applications, but it has some challenges. As the interleaved converters inherently have a more complex topology than single module structures, providing soft-switching conditions with a simple structure, the low number of auxiliary components and low cost is of great emphasis. Also, in the high step-up applications used for solar inverters, employing a soft switched method that can operate in a wide range of output power and the input voltage is a key factor [32]. Therefore, ZVT cells can be a proper candidate for soft switching of such applications because of providing the soft-switching condition independent of output load. In [21], a ZVT cell for a high step-up interleaved converter is proposed. Although this cell can provide soft switching in a wide range, it is made up of many auxiliary components including two extra switches, two magnetic elements, and two diodes which dramatically increase the conduction losses and have a low power density. Furthermore, not only the voltage gain of this converter is relatively low, but also having no coupled inductors, the voltage gain cannot be further increased. In [5], a ZVT cell utilizing coupled inductors has been proposed in the Z-source converter to improve soft switching condition at turn off instances of the switches. This ZVT structure is also employed for the interleaved topology, which involves one auxiliary switch, two diodes, and two extra windings [30]. Also, this topology does not have high voltage gain and suffers from high conduction losses. In [22], an interleaved ZVT converter with high voltage gain and low switch voltage stress is introduced. Using two extra winding and three semiconductor components is the noticeable disadvantage of this converter. Additionally, the mentioned converter cannot operate with duty cycles lower than 0.5, which is a weakness for a high step-up converter; in practice, regulating the output voltage from no load to full load condition is essential. In [25], an interleaved ZVT high step-up converter based on coupled inductors and switched capacitors is introduced. The ZVT cell in this converter is composed of four extra diodes, one switch, and two windings which have reduced the power density and suffer from high cost and conduction losses. Moreover, despite of using high number of components, it possesses a proportionally low voltage gain, and its output diode has a very high voltage stress. In [24], a ZVT boost converter is proposed using switched capacitor technique as a multiplier cell. The introduced ZVT cell in this converter has lower number of components than the abovementioned ones, but the voltage gain of this step-up converter is not so high, it is a bit higher than the conventional boost converter. In [23], another ZVT interleaved converter with a very high voltage gain and efficiency is introduced utilizing two separate auxiliary circuits for soft switching of main switches. Not having any shared ZVT elements results in high number of components.

In this article, a new ZVT interleaved converter is proposed based on coupled inductors and switched capacitor circuits, providing high voltage gain, and low voltage stress across main switches. The proposed ZVT cell employed in this structure is compatible with high step-up coupled inductor-based boost converters. By making use of the leakage inductance in the resonant network, no extra magnetic elements are needed and only one bidirectional switch and one resonant capacitor are utilized for the ZVT structure. Note that the structure of the proposed auxiliary circuit is very similar to active clamp auxiliary circuits, but the operation is completely different. Unlike the active clamp circuit, the capacitor in this cell provides a resonant network and the soft switching is load independent. Also, only one auxiliary circuit is used for two phases of the interleaved structure. The proposed converter possesses the

Fig. 1. Block diagram of a grid-connected renewable energy system.

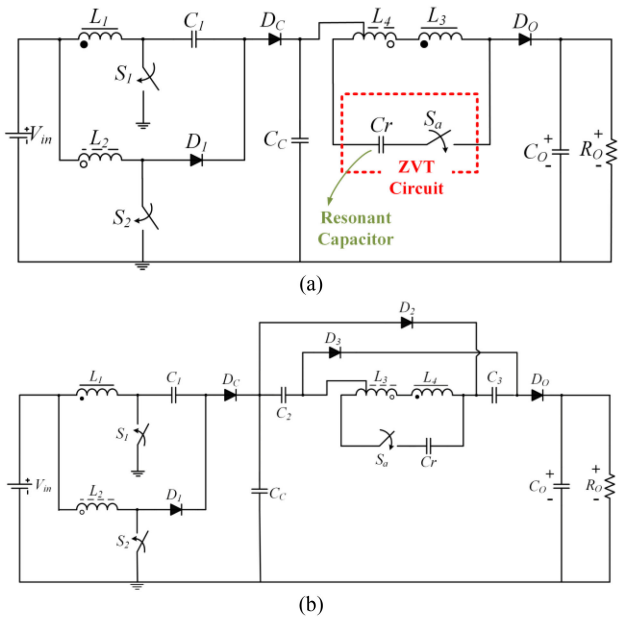


Fig. 2. Schematic of the proposed ZVT step-up converters. (a) First proposed converter. (b) Second proposed converter with higher voltage gain.

minimum number of components and has the capability to add extra multiplier cells to achieve very high voltage gains. In the proposed converters, soft switching operation of the main and the auxiliary MOSFETs is achieved independent of the line and load which results in a high efficiency in the wide range of output power. Having common ground between input and output and no reverse recovery problem are other advantages of the proposed ZVT converters.

The proposed converters are presented and analyzed in Section II and its operating modes are discussed. Design considerations are introduced in Section III. Finally, Section V provides experimental results and comparisons.

II. Operating Principles

The proposed ZVT interleaved converter is shown in Fig. 2(a). As the proposed ZVT cell employs the leakage inductance of coupled inductors, only one capacitor and one bidirectional switch are needed in the auxiliary cell. Adding extra multiplier cells can increase the voltage gain of the proposed converter, like the second proposed converter which is shown in Fig. 2(b). Due

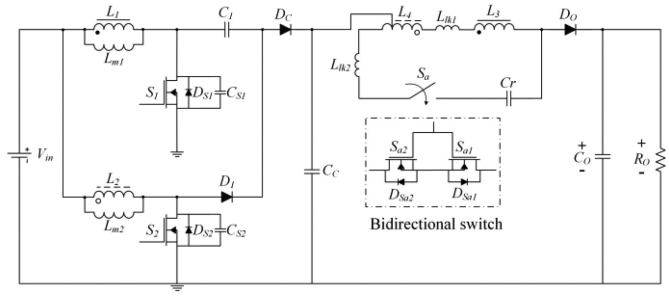


Fig. 3. Equivalent circuit of the first proposed converter.

to the similar operation of the first and second converters, the first proposed one is selected to investigate. In order to investigate the operating modes of the proposed converter, the equivalent circuit, and the key waveforms of the converter are, respectively, presented in Figs. 3 and 4. This converter is composed of two coupled-inductors L_1, L_2 and L_3, L_4 with, respectively, n_1, n_2, n_3, and n_4 winding turns ($\frac{n_3}{n_1} = \frac{n_4}{n_2} = n$), and the power switches S_1 and S_2, capacitors C_1, C_C, and C_O, and diodes D_1, D_C, and D_O. Also, the auxiliary circuit is composed of C_c capacitor and a bidirectional switch S_a, which is implemented with two unidirectional switches S_{a1} and S_{a2}. In order to simplify the analysis, diodes and switches are assumed ideal, the voltage of capacitors C_1, C_C, and C_O and the magnetizing inductances L_{m1} and L_{m2} are supposed to have low current ripple so that they are considered constant and V_{c1}, V_{Cc}, and V_{Cr} are equal to $\frac{V_{\text{in}}}{1-D}$, $\frac{2V_{\text{in}}}{1-D}$, and $\frac{nV_{\text{in}}}{1-D}$.

Mode 1 *[t_0–t_1]* [see Fig. 5(a)]: At the beginning of this mode, the main switch S_1 is turned OFF under ZVS condition due to the existence of the snubber capacitor, C_{s1}. During this mode, all switches and diodes are OFF excluding switch S_2. In addition, C_{S1} capacitor is linearly charged via magnetizing inductance current *(I_{Lm2})* and the load is supplied by the output capacitor. Below equation is true for the voltage of the snubber capacitor

$$V_{Cs1} = \frac{I_{Lm}}{C_{s1}}\ (t - t_o)\,. \tag{1}$$

At the end of this mode, the voltage of snubber capacitor V_{C1} reaches $\frac{V_{\text{in}}}{1-D}$, in which D is the duty cycle of main switches. Therefore, the time duration of this mode is as follows:

$$t_{10} = \frac{V_{\text{in}}.\ C_{s1}}{(1-D)\,I_{Lm1}}\,. \tag{2}$$

Mode 2 *[t_1–t_2]* [see Fig. 5(b)]: At the start of this mode, by reaching V_{Cs1} to the voltage of clamp capacitor (V_{Cc}), D_c and D_o starts to conduct. So, I_{Lk1} increases and reaches $(\frac{I_{Lm1}}{n+1})$ at the middle of this mode. During this time, C_1 is discharged and C_c is charged. When I_{Lk1} reaches $(\frac{I_{Lm1}}{n+1})$, I_{Cc} reaches zero and then it becomes negative and C_C starts discharging. It is noted that depending on the load current and duty cycle, if the duration of this mode is large enough, I_{Lk1} would increase to $\frac{I_{Lm1}}{n}$ and thus I_{DC} reaches zero. In this mode, it is considered that I_{Lk1} do not reach $\frac{I_{Lm1}}{n}$, and D_C do not turn OFF at t_2, so the operating modes can be examined more generally. Considering the short period of the resonances which occur once the auxiliary switch

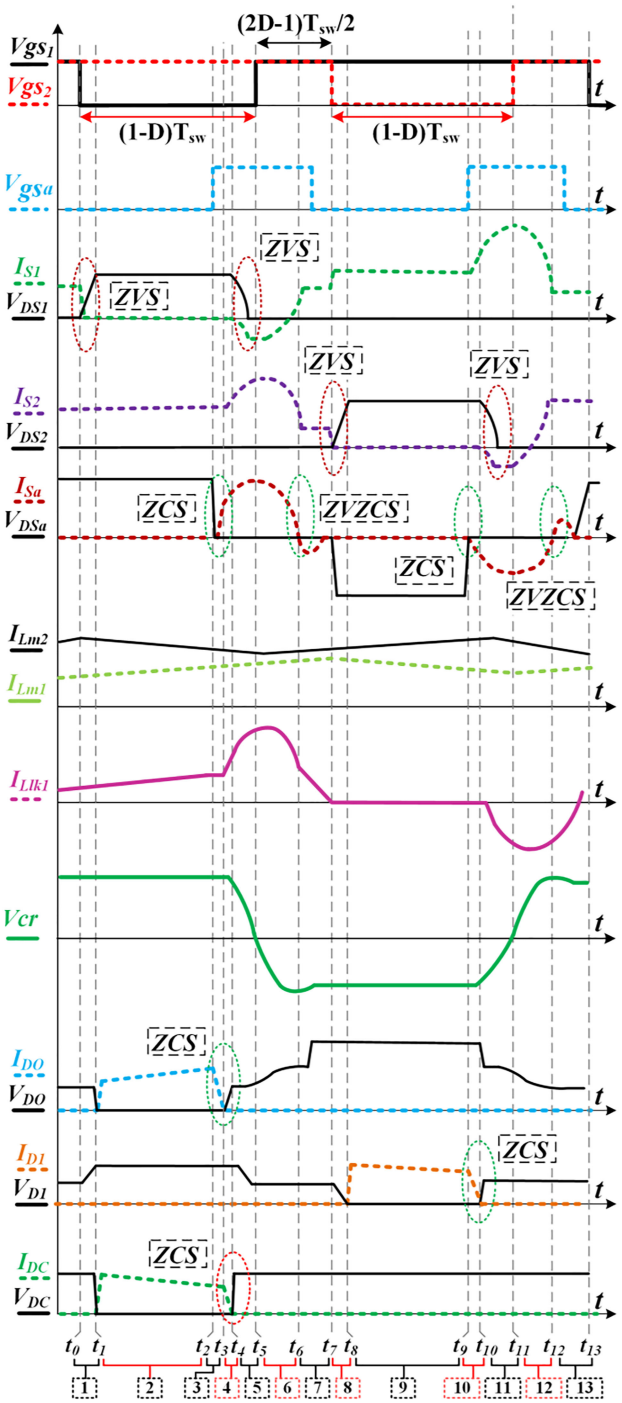


Fig. 4. Key waveforms of the proposed converter.

is triggered, the time duration of this mode is approximately equal to $(1-D)T_{\text{sw}}$

$$I_{Lk1} = \frac{[(n+1)\,V_{Cc} - nV_{c1} - V_o]}{L_{k1}}\,(t-t_2) \tag{3}$$

$$I_{Do}\,(t_2) = I_{Dc}(t_2) = \frac{[(n+1)\,V_{Cc} - nV_{c1} - V_o]}{L_{k1}}\,(1-D)\,T_{\text{sw}} \tag{4}$$

where V_{c1} and V_{Cc} are equal to $V_{in}/(1-D)$ and $2V_{in}/(1-D)$.

Mode 3 *[t_2–t_3]* [see Fig. 5(c)]: At the commence of this mode, the auxiliary switch S_a turns ON under ZCS condition due to the existence of L_{lk2}; S_{a1} and the anti-parallel diode of S_{a2} starts to conduct. In this mode, I_{lk1} is equal to I_o and is considered almost constant, but I_{Lk2} starts to increase linearly. Thus, I_{Do} and I_{Cc} decrease. When I_{Lk2} reaches I_o current, I_{Do} becomes zero and D_o turns off under ZCS condition. Due to the short duration of this mode, its time interval can be neglected

$$I_{Lk1} = I_o \tag{5}$$

$$I_{Lk2} = \frac{V_{Cr(0)} + \frac{n}{(1-D)}Vin}{L_{lk2}}\,(t-t_2) \tag{6}$$

$$I_{Dc} = I_{Lm1} - I_o \tag{7}$$

$$t_{32} = t_3 - t_2 = \frac{I_o.L_{lk2}}{V_{Cr(0)} + \frac{n}{(1-D)}V_{\text{in}}} \tag{8}$$

where $V_{Cr(0)}$ is equal to $nV_{\text{in}}/(1-D)$.

Mode 4 *[t_3-t_4]* [see Fig. 5(d)]: Once *Do* turns OFF at t_3, a constant voltage is placed across leakage inductances and I_{Dc} starts to decrease linearly. At the end of this mode I_{lk2} reaches $\frac{I_{Lm1}}{n}$ and I_{Dc} becomes zero. So, D_c turns off under ZCS condition at *t*4. The equations of this mode are as follows. The time duration of this mode is short and can be neglected

$$I_{Lk1} = I_{Lk2} = I_o + \frac{V_{Cr(0)} + \frac{n}{(1-D)}Vin}{L_{kT}}\,(t-t_3) \tag{9}$$

$$I_{Dc} = I_{Lm1} - n \times \left(I_o + \frac{V_{Cr(0)} + \frac{n}{(1-D)}Vin}{L_{kT}}\,(t-t_3) \right) \tag{10}$$

$$t_{43} = t_4 - t_3 = \frac{\left(\frac{I_{Lm1}}{n} - I_o\right).(L_{kT})}{V_{Cr(0)} + \frac{n}{(1-D)}V_{\text{in}}} \tag{11}$$

where $L_{kT} = L_{lk2} + L_{lk1}$.

Mode 5 *[t_4-t_5]* [see Fig. 5(e)]: By turning D_c OFF at t_4, a resonant network is formed between C_r, L_{lk1}, L_{lk2}, and C_{s1}. During this resonance, I_{lk1} increases and V_{cs1} and V_{Cr} decreases. By the end of this mode, V_{cs1} reaches zero and body diode of switch D_{s1} conducts

$$I_{Lk1} = I_{Lk2} = nI_{Lm1}\left(\frac{C_{T1}}{C_{s1}}\right)(1-\cos\omega_1 t) + \frac{I_{Lm1}}{n}\cos\omega_1 t + \left(\frac{V_{Cr(0)+\frac{nV_{\text{in}}}{1-D}}}{Z_1}\right)\sin\omega_1 t \tag{12}$$

$$V_{Cr} = \frac{C_{T1}}{C_r}\left[\frac{C_r}{C_{T1}}V_{Cr(0)} - \frac{nI_{Lm1}}{C_{s1}}\,t - \left(\frac{1}{n} - \frac{n.C_{T1}}{C_{s1}}\right)Z_1.I_{Lm1}\sin\omega_1 t - \left(V_{Cr(0)+}\frac{nV_{\text{in}}}{1-D}\right)(1-\cos\omega_1 t)\right] \tag{13}$$

$$V_{Cs2} = \frac{V_{\text{in}}}{1-D} \tag{14}$$

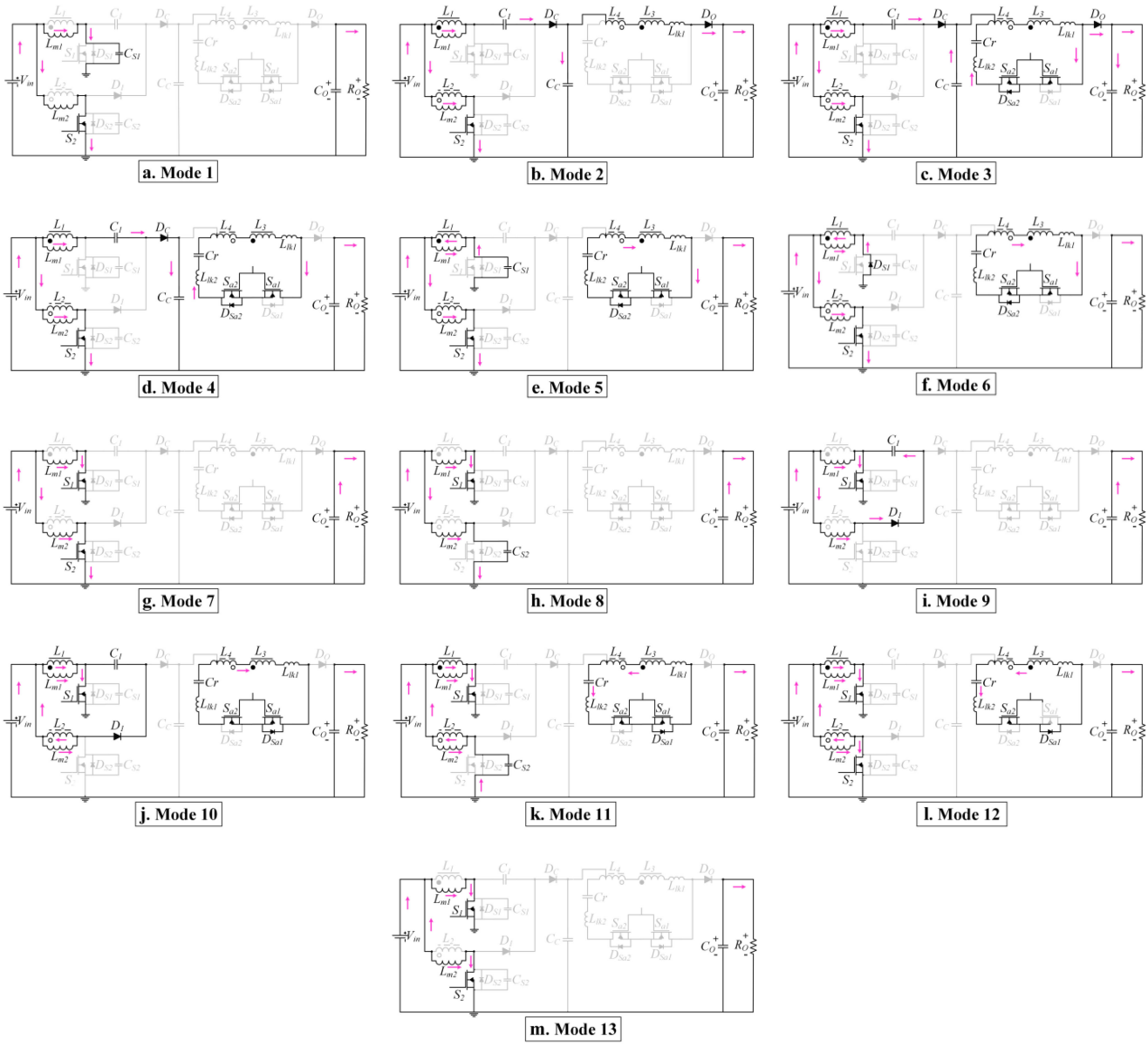


Fig. 5. Equivalent circuit for each operating interval of the proposed converter.

$$V_{Cs1} = \frac{n.C_{T1}}{C_{S1}}\left[\frac{C_{S1}}{n.C_{T1}}\left(\frac{V_{in}}{1-D}\right) - \left(\frac{n}{C_{s1}} - \frac{1}{n.C_{T1}}\right) I_{Lm1}.t - \left(\frac{1}{n} - \frac{n.C_{T1}}{C_{s1}}\right) Z_1.I_{Lm1}\sin\omega_1 t - \left(V_{Cr(0)+}\frac{nV_{\text{in}}}{1-D}\right)(1-\cos\omega_1 t)\right] \quad (15)$$

Where $Z_1 = \sqrt{\frac{L_T}{C_{T1}}}$ and $\omega_1 = \frac{1}{\sqrt{C_{T1}.L_T}}$, $L_T = L_{k1} + L_{k2}$, and $C_{T1} = \frac{C_{s1}.C_r}{n^2C_r+C_{s1}}$.

Mode 6 [*t5, t6*) [see Fig. 5(f)]: In this mode, the resonance continues between C_r, L_{k2} and L_{k1} and the leakage inductance current decreases in a resonant manner. Also, due to conduction of D_{s1}, the main switch S_1 can be turned ON under ZVS condition at any time during this mode. In this interval, the voltage of C_r capacitor decreases to zero, then charges in a negative direction and at the end of this mode, V_{cr} is clamped to $-(V_o - V_{Cc})$ voltage, which is approximately equal to $\frac{-nV_{\text{in}}}{1-D}$. Also, at t_6, I_{lk1}, and I_{lk2} decreases to zero, and the body diode of S_{a1} turns OFF under ZCS conditions. Thereafter, the auxiliary switches can be turned OFF under ZCS condition

$$I_{Lk1} = I_{Lk2} = I_{Lk}\ (t_5)\cos\omega_2 t + \frac{V_{Cr}\ (t_5)}{Z_2}\sin\omega_2 t \quad (16)$$

$$V_{Cr} = I_{Lk2} = V_{Cr}\ (t_5)\cos\omega_2 t - Z_2 I_{Lk}\ (t_5)\sin\omega_2 t \quad (17)$$

where $Z_2 = \sqrt{\frac{L_T}{C_r}}$ and $\omega_2 = \frac{1}{\sqrt{C_r.L_T}}$, $V_{Cr}\ (t_5) = \frac{-nV_{\text{in}}}{1-D}$.

Mode 7 *[t_6-t_7]* [see Fig. 5(g)]: In this interval, both main switches are ON and the input voltage is applied across L_{m1} and L_{m2} so that their currents are increased. The time duration of this mode is equal to $\frac{(2D-1)T}{2}$.

Mode 8 [t_7-t_8] [see Fig. 5(h)]: At the beginning of this mode, the main switch, S_2, turns OFF under ZVS condition due to the snubber capacitor C_2. So, C_{s2} is linearly charged by the magnetizing inductance current I_{Lm2}. At the end of this mode, V_{Cs2} reaches $\frac{V_{\text{in}}}{1-D}$

$$V_{Cs2} = \frac{I_{Lm2}}{C_{s2}}\ (t - t_o) \tag{18}$$

$$t_{10} = 2\frac{V_{\text{in}}.\ C_{s2}}{(1-D)\, I_{Lm2}}. \tag{19}$$

Mode 9 *[t_8-t_9]* [see Fig. 5(i)]: At t_8, V_{Cs2} reaches the voltage of C_1 capacitor ($\frac{V_{\text{in}}}{1-D}$). Because the clamp capacitor voltage is equal to $\frac{2V_{\text{in}}}{1-D}$, D_c remains OFF and D_1 starts to conduct. In this mode, I_{Lm2} passes through D_1, C_1, and S_1 switch and C_1 is charged. The equivalent circuit in this mode is shown in figure.

Mode 10 *[t_9-t_{10}]* [see Fig. 5(j)]: At t_9, S_{a2} is turned ON under ZCS condition. Also, the body diode of Sa1, D_{sa1} starts to conduct. In this mode, because of the initial voltage of C_r, which is applied across the leakage inductances, their current increases in the negative direction and thus I_{L2} starts to increase. Therefore, I_{D1} decreases and when I_{Lk1} reaches $\frac{I_{Lm2}}{n}$, D_1 turns OFF under ZCS condition at the end of this mode

$$I_{Lk2} = I_{Lk1}\ = \frac{V_{Cr}\,(t_8) + \frac{n}{(1-D)}Vin}{L_{kT}}\ (t - t_2) \tag{20}$$

$$I_{D1} = I_{Lm2}\ - n.I_{Lk1} \tag{21}$$

$$t_{32} = t_3\ -\ t_2 = \frac{\frac{I_{Lm2}}{n}.L_{kT}}{V_{Cr}\,(t_8) + \frac{n}{(1-D)}V_{\text{in}}} \tag{22}$$

Mode 11 *[t_{10}–t_{11}]* [see Fig. 5(k)]: At t_{10}, D_1 turns OFF and a resonant circuit is made between C_r, C_{s2}, L_{lk1}, and L_{lk2}. In this resonance, C_{s2} starts to discharge and I_{lk2} increases in a negative direction. At the end of this interval, C_{s2} voltage reaches zero and D_{s2} turns ON

$$I_{Lk1} = I_{Lk2}\ =\ nI_{Lm2}\left(\frac{C_{T2}}{C_{s2}}\right)(1-\cos\omega_3 t) + \frac{I_{Lm2}}{n}\cos\omega_3 t + \left(\frac{V_{Cr}\,(t_{10}) + \frac{nV_{\text{in}}}{1-D}}{Z_3}\right)\sin\omega_3 t \tag{23}$$

$$V_{Cr} = \frac{C_{T2}}{C_r}\left[\frac{C_r}{C_{T2}}V_{Cr(0)} - \frac{nI_{Lm2}}{C_{s2}}\ t - \left(\frac{1}{n} - \frac{n.C_{T2}}{C_{s2}}\right)Z_3.I_{Lm2}\sin\omega_3 t - \left(V_{Cr(0)+}\frac{nV_{\text{in}}}{1-D}\right)(1-\cos\omega_3 t)\right] \tag{24}$$

$$V_{Cs2} = \frac{n.C_{T2}}{C_{S2}}\left[\frac{C_{S2}}{n.C_{T2}}\left(\frac{V_{in}}{1-D}\right) - \left(\frac{n}{C_{s2}} - \frac{1}{n.C_{T2}}\right)I_{Lm2}.t - \left(\frac{1}{n} - \frac{n.C_{T2}}{C_{s2}}\right)Z_3.I_{Lm2}\sin\omega_3 t - \left(V_{Cr(0)+}\frac{nV_{\text{in}}}{1-D}\right)(1-\cos\omega_3 t)\right] \tag{25}$$

where $Z_3 = \sqrt{\frac{L_T}{C_T}}$ and $\omega_3 = \frac{1}{\sqrt{C_T.L_T}}$, $L_T = L_{k1} + L_{k2}$, and $C_{T2} = \frac{C_{s2}.C_r}{n^2C_r.C_{s2}}$.

Mode 12 *[t_{11}–t_{12}]* [see Fig. 5(l)]: At the beginning of this mode, by conducting D_{S2}, S_2 can be switched ON under ZVS condition. Also, the resonance continues between C_r, L_{k2} and L_{k1} and the leakage inductance current decreases. At the end of this mode, I_{lk1} and I_{lk2} reaches zero, the voltage of C_r is clamped to $(V_o - V_{Cc})$ and the body diode of S_{a2} turns OFF under ZCS condition. Therefore, the auxiliary switches can be turned OFF under ZVZCS

$$I_{Lk1} = I_{Lk2}\ = I_{Lk}\ (t_{11})\cos\omega_2 t + \frac{V_{Cr}\,(t_{11})}{Z_2}\sin\omega_2 t \tag{26}$$

$$V_{Cr} = I_{Lk2}\ = V_{Cr}\ (t_{11})\cos\omega_2 t - Z_2 I_{Lk}\,(t_{11})\sin\omega_2 t. \tag{27}$$

Mode 13 *[t_{12}–t_{13}]* [0see Fig. 5(m)]: In this mode, both S_1 and S_2 switches are ON and V_{in} is applied across both magnetizing inductances L_{m1} and L_{m2} and they are charged linearly.

III. Analysis and Design Considerations of the Proposed Converter

In this section, first the voltage gain ratio of the proposed converters are precisely calculated by considering the leakage inductances and are compared with the voltage gain ratio in the ideal form. The design of the components of the proposed converter including the ZVT cell and the main power circuit are presented. Also, in order to select proper MOSFETs and diodes, voltage and current stresses of semiconductor elements are calculated.

A. Voltage Gain Ratio of the Proposed Converter

In order to calculate the voltage gain of the proposed converter, at the beginning the voltage of the capacitors C_1 and Cc should be calculated by volt-second balance relations of L_{m2} and L_{m1} inductors in (28) and (29), respectively

$$(V_{\text{in}})\,D\ =\ (V_{c1} - V_{\text{in}})\ (1-D) \rightarrow$$

$$V_{C1} = \frac{V_{\text{in}}}{1-D} \tag{28}$$

$$(V_{\text{in}})\,(D) = (-V_{\text{in}} - V_{c1} + V_{Cc})\,(1-D)\,. \tag{29}$$

Substituting (28) into (29), V_{Cc} is given as follows:

$$V_{Cc} = \frac{2V_{\text{in}}}{1-D}\,. \tag{30}$$

By neglecting the voltage of $L_{lk1}$and considering $V_o = [(n+1)V_{Cc} - V_{c1}]$ from mode 2, the output voltage relation is achieved as

$$V_O = \frac{(n+2)\,V_{\text{in}}}{1-D}\,. \tag{31}$$

Also, by following the same procedure for the second proposed converter in Fig. 2(b), its voltage gain relation is obtained by

$$V_O = \frac{(n+4)\,V_{\text{in}}}{1-D}\,. \tag{32}$$

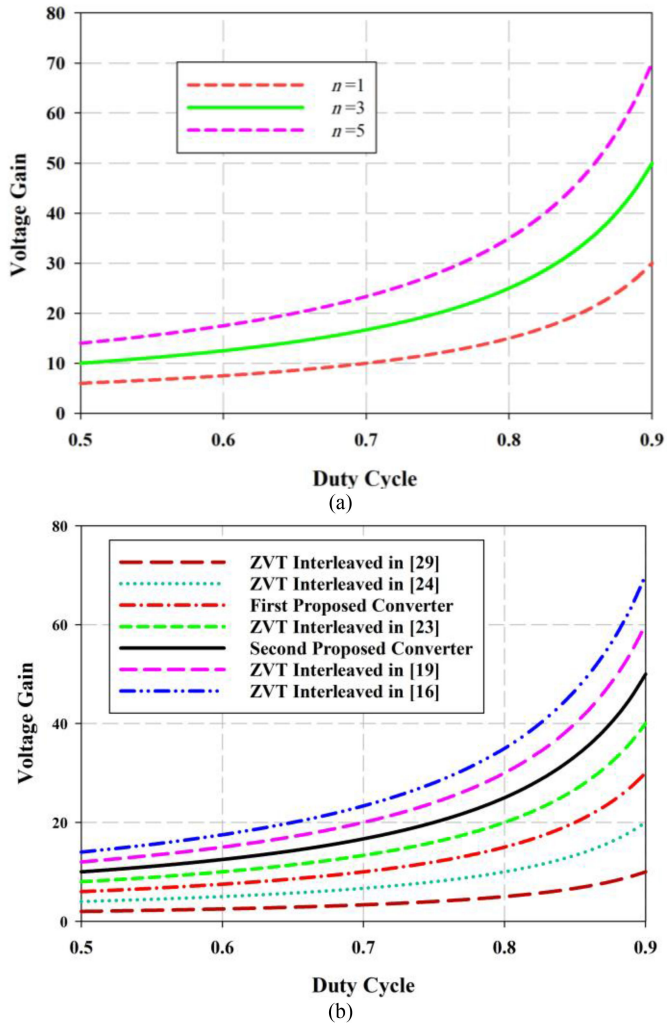


Fig. 6. Voltage gain vs. duty cycle. (a) First proposed converter with different turns ratio (n). (b) Comparison of the proposed converters with other converters in [16], [19], [23], [24], and [29] ($n = 1$ and $k = 1$.).

The ideal voltage gain plot of the first proposed converter with several turns ratio is resented in Fig. 6(a). It is obvious that the turns ratio has a remarkable impact on the voltage gain of the proposed converter. Fig. 6(b) illustrates the ideal voltage gain plot of the proposed converters and five other coupled-inductor-based interleaved converters in the literature. In this plot, the turn ratio (n) is considered one and the coupling factor (k) is unity. Note that a detailed comparison of the proposed converter with the existing interleaved converters is presented in Section IV-B.

In case of considering leakage inductances, the voltage gain should be calculated more precisely. By considering the average current of the output diode ($I_{Do(\text{avg})}$), the voltage-gain can be derived by considering the impact of leakage inductances. I_{Do} current starts increasing linearly during mode 2, culminates at t_2, and reaches zero during mode 3. Considering m_r and m_f as the rising and falling slopes of D_o current, and t_r and $t_f$as the rise time and fall time of I_{Do} current, the following equations can be written:

$$m_r = \frac{[(n+1)\,V_{Cc} - nV_{c1} - V_o]}{L_{k1}} \tag{33}$$

$$m_f = \frac{[n\,(V_{Cc} - V_{c1}) + V_{Cr}]}{L_{k2}}\,. \tag{34}$$

Substituting 28 and 30 into 33, and considering $V_{cr} = (V_o - V_{Cc})$ from mode 6, m_r, m_f, t_r, and t_f are achieved as follows:

$$m_r = \frac{\frac{n+2}{1-D}V_{\text{in}} - V_o}{L_{k1}} \tag{35}$$

$$m_f = \frac{\frac{n-2}{1-D}V_{\text{in}} + V_o}{L_{k2}} \tag{36}$$

$$t_r = (1-D)\;T_{\text{sw}} \tag{37}$$

$$t_f = \frac{I_{Do(\text{peak})}}{m_f} = \frac{L_{k2}}{L_{k1}}\;\frac{(n+2)\,V_{\text{in}} - V_o\,(1-D)}{(n-2)\,V_{\text{in}} + V_o\,(1-D)}(1-D)\,T_{\text{sw}}. \tag{38}$$

In (38), the peak current of I_{Do} ($I_{Do(\text{peak})}$) is achieved by (4) based on mode 2, and it is equal to $\frac{(n+2)V_{\text{in}} - (1-D)V_o}{L_{k1}}T_{\text{sw}}$. Considering the waveform of the output diode current as a triangle form, the following equation can be written for $I_{Do(\text{avg})}$:

$$I_{Do(\text{avg})} = I_o = \frac{1}{2}\,\frac{t_r + t_f}{T_{\text{sw}}}I_{Do(\text{peak})}. \tag{39}$$

Replacing (37) and (38) into (39) and considering $I_o = \frac{V_o}{R_o}$, the following relation is achieved between input and output voltage of the proposed converter

$$\frac{1}{2L_{k1}}\,[(n+2)\,V_{\text{in}} - V_o\,(1-D)]\,(1-D)\,T_{\text{sw}} + \frac{L_{k2}}{2L_{k1}^2}\,\frac{[(n+2)\,V_{\text{in}} - V_o\,(1-D)]^2}{(n-2)\,V_{\text{in}} + V_o\,(1-D)}\,(1-D)\;T_{\text{sw}} = \frac{V_o}{R_o}\,. \tag{40}$$

Equation (40) is dependent on both leakage inductances $L_{k1}$and L_{k2}. However, due to the very short value of t_f ($t_f << t_r$), it can be ignored and thus the effect of L_{k2} can be neglected in the voltage gain equation. Therefore, the second term in (40) can be removed and the following equation is achieved between $V_{\text{in}}$and V_o

$$\frac{1}{2}\;[(n+2)V_{\text{in}} - V_o\,(1-D)] = \frac{L_{k1}}{T_{\text{sw}}R_o\,(1-D)}\;V_o. \tag{41}$$

Considering the voltage gain ratio of the proposed converter $G = \frac{V_o}{V_{\text{in}}}$, and $R_o = \frac{P_o}{V_o^2}$, the voltage gain relation is achieved by (42) as a function of duty cycle and the output power, which is affected by L_{lk1}

$$G = \frac{n+2}{1-D + \frac{2P_{\text{out}}\cdot f_{\text{sw}}}{V_o^2(1-D)}L_{k1}}. \tag{42}$$

In (42), the factor $2P_{\text{out}}L_{k1}/T_{\text{sw}}V_o^2(1-D)$ represents the effect of leakage inductance. Equation (42) is depicted via MATLAB software for two values of coupled inductors turn ratio ($n = 1$ and $n = 2$) in Fig. 7. Note that the parameters presented in Table II are used for plotting this equation. According to (42) and Fig .7, the voltage-gain for no load condition ($P_{\text{out}} = 0$) will be equal to the ideal voltage gain relation in (31). It can be inferred from Fig. 7(a) and (b) that the voltage-gain for duty

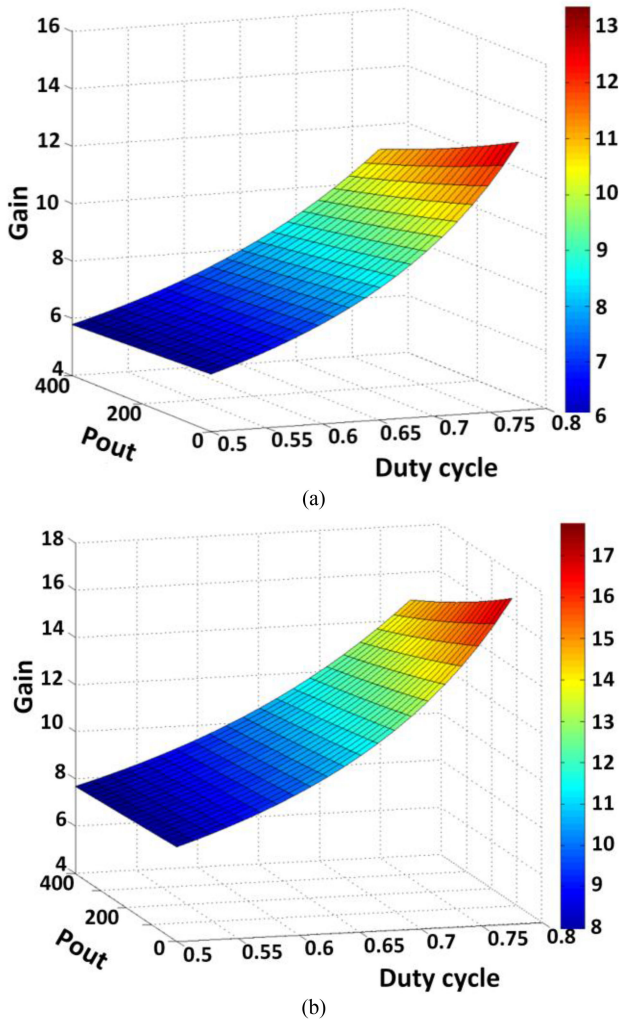


Fig. 7. Non-idealized voltage gain ratio of the proposed converter vs. duty cycle and output power considering the impact of L_{k1}, a) $n = 1$, b) $n = 2$.

cycles less than 0.7 is almost constant in the whole range of output power and is less affected by leakage inductance. Also, comparison of Fig. 7(a) and (b) illustrates that by increasing the turn ratio (n) of the coupled inductors, the desired voltage gain can be achieved via lower duty cycles. As a result of which, it can be concluded that the more the turn ratio of the coupled inductors (n) is increased, the less voltage gain will be affected by the leakage inductance at nominal loads.

B. Components Design

1) Semiconductor Components: According to mode 2, the peak voltage across the main switch S_1, the auxiliary switch S_a, and diode D_1 are equal to $[V_{Cc} - V_{c1}]$, $[n(V_{Cc} - V_{C1}) + V_{cr}]$, and V_{Cc}, respectively. Also, according to mode 9, the voltage stress of S_2, diode D_c, and diode D_o are, respectively, equal to V_{c1}, $[V_{Cc} - V_{c1}]$ and $[\mathrm{V_o} + n\mathrm{V_{C1}} - V_{Cc}]$. Replacing (28) and (30) into the previously mentioned relations, the voltage stress of semiconductor components is achieved and presented in Table I. Also, the current of $S_a$and S_2switches reach the highest value

TABLE I
CURRENT AND VOLTAGE STRESS OF SEMICONDUCTOR ELEMENTS

COMPONENTS	CURRENT STRESS	VOLTAGE STRESS
SWITCH S_1	$I_{Lm1} + \frac{n^2 C_{T2}}{C_{s2}} I_{Lm2} + \frac{2n^2 V_{in}}{Z_3(1-D)}$	$V_o/(n+2)$
SWITCH S_2	$I_{Lm2} + \frac{n^2 C_{T1}}{C_{s1}} I_{Lm1} + \frac{2n^2 V_{in}}{Z_1(1-D)}$	$V_o/(n+2)$
SWITCH S_a	$\frac{nC_{T1}}{C_{s1}} I_{Lm1} + \frac{2nV_{in}}{Z_1(1-D)}$	$2nV_o/(n+2)$
DIODE D_1	I_{Lm1}	$2nV_o/(n+2)$
DIODE D_C	$\frac{(n+2)V_{in} - V_o(1-D)}{L_{k1}} T_{sw}$	$V_o/(n+2)$
DIODE D_o	$\frac{(n+2)V_{in} - V_o(1-D)}{L_{k1}} T_{sw}$	$2nV_o/(n+2)$

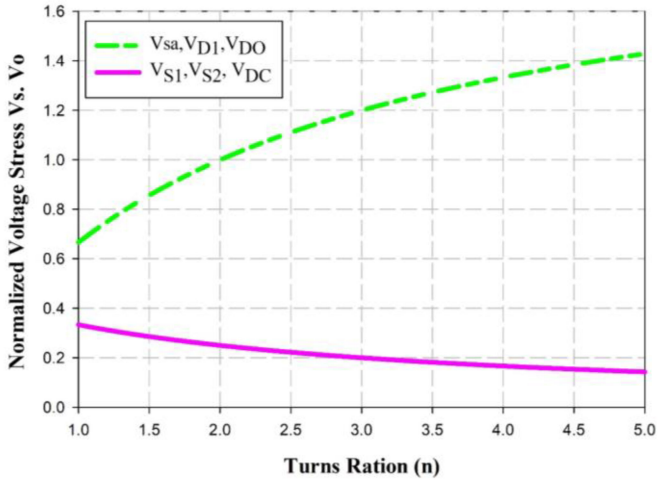


Fig. 8. Normalized voltage stress of semiconductor components versus turns ratio.

during mode 5 and the current of S_1 peaks during mode 11. So, using (12) and (23), the current stress of switches is achieved.

Fig. 8 shows the relationship between the normalized voltage stress of semiconductor components of the first proposed converters versus coupled inductors turn ratio(n). As n increases, the auxiliary switch voltage stress V_{sa}, V_{D1} and V_{Do} increase, and in contrast, the main switches voltage stress V_{s1}, V_{s2}, and $V_{Dc}$are increased. Therefore, the MOSFETs with low $R_{DS(on)}$ can be utilized to reduce the conduction losses of the main switches.

Fig. 9 shows a comparison which is made between D_o voltage stress of the proposed converter and interleaved converters in [22], [23], and [25]. As duty cycle raises, the voltage stress of the output diode is increased. Therefore, the maximum duty cycle determines the voltage stress of the output diode.

2) Coupled Inductors Design: To design coupled inductors, two parameters should be determined, the turn ratio and the magnetizing inductance. The turns ratio of the coupled inductors is a key factor that affects the main switches' voltage stress. Based on Table I, the higher the turn ratio, the less main switches' voltage stress would be. Also, based on the desired voltage gain and considering the point that when D is larger and turn ratio is lower, less power is processed magnetically through coupled

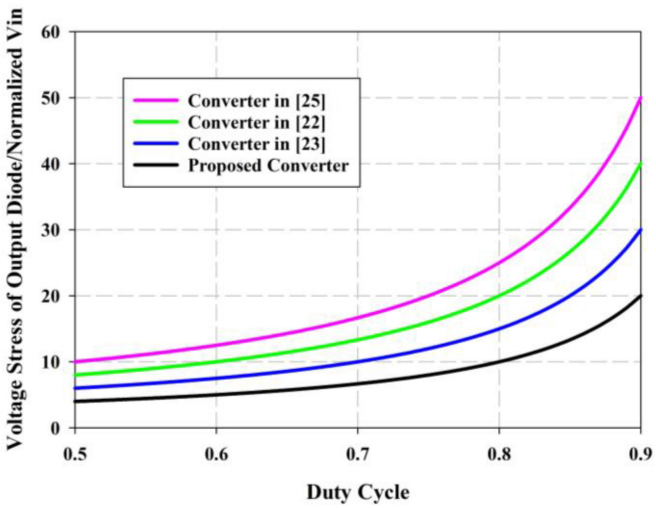


Fig. 9. Output diode voltage stress comparison of the proposed converter with other interleaved converters in [22], [23], and [25]. ($n = 1$ and $k = 1$).

inductors, the maximum value of the turn ratio can be designed as follows:

$$\mathrm{n} < \left(\frac{V_O\,(1-D)}{V_{\text{in}}} - 2 \right). \tag{43}$$

The magnetizing inductances of the coupled inductors determine the input current ripple (ΔI_{in}). Considering that the input current has a frequency twice the switching frequency (f_{sw}), the magnetizing inductances L_{m1} and L_{m2} can be derived as

$$L_{m1} = L_{m2} = \frac{V_{\text{in}}.D}{2f\Delta I_{\text{in}}}\,. \tag{44}$$

Additionally, the capacitors C_1, C_c, and C_o are designed based on their peak-to-peak ripple voltage; thus, they derived as follows:

$$C_1 = \frac{I_{Lm2}\,(1-D)}{f_{\text{sw}}.\Delta V_{C1}} \tag{45}$$

$$C_c = \frac{I_{m1}\,(1-D)}{4f_{\text{sw}}.\Delta V_{C2}} \tag{46}$$

$$C_o = \frac{I_o\,(1-D)}{f_{\text{sw}}.\Delta V_{Co}}\,. \tag{47}$$

3) Resonant Capacitor Design: In the proposed converter, the resonant capacitor should provide ZVS condition at turn-on for the main switches. Therefore, according to mode 3, 4, and 5, the resonant capacitor should have enough energy to increase the current of L_{k2} from zero to $\frac{I_{Lm1}}{n}$ during mode 3 and 4, and the curent of L_{k1} from I_o to $\frac{I_{Lm1}}{n}$ during mode 4. Then during the resonance in mode 5, the remained energy of this capacitor should be consumed to reduce the voltage of C_{s1} form $V_{\text{in}}/(1-D)$ to zero. As the initial voltage of C_r capactor is considered $\frac{nv_{\text{in}}}{1-D}$ the following equation should be satisfied:

$$\frac{1}{2}C_r\left(\frac{nv_{\text{in}}}{1-D}\right)^2 > \frac{1}{2}L_{k1}\left(\frac{I_{m1}}{n} - I_o\right)^2 + \frac{1}{2}L_{k2}\left(\frac{I_{m1}}{n}\right)^2 + \frac{1}{2}C_{s1}\left(\frac{V_{\text{in}}}{1-D}\right)^2. \tag{48}$$

Rewriting (48) yields the following limitation on the selection of C_r capacitor:

$$C_r > \frac{C_{s1}}{n^2} + \frac{L_{k1}\left(\frac{I_{m1}-nI_o}{n}\right)^2 + L_{k2}\left(\frac{I_{m1}}{n}\right)^2}{\left(\frac{nV_o}{n+2}\right)^2}. \tag{49}$$

C. Circuit Startup

There are two main concerns for the startup process of this topology. The first problem is the excessive output voltage overshoot and inrush current at the startup time, which is a common issue among step up boost structures, because the voltage of the output capacitor and the clamp and the multiplier capacitors is zero at the beginning. By using soft-start function that ramps the output voltage in a controlled manner upon startup, excessive output voltage overshoot and inrush current will be controlled [44]. The second and the most important concern for the startup process is providing soft switching. For the soft switching at switch turn-off instants, the snubber capacitor reduces the overlap between voltage and current independent of the circuit operation. So, there is no concern for switches' turn-off. But soft switching at turn-on is achieved by ZVT circuit. During each duty cycle of the switch, C_r capacitor charges up to $-(V_o - V_{Cc})$ then discharges through resonant network and again charges in a negative direction and its voltage is clamped to $(V_o - V_{Cc})$ to provide soft switching for the other switch. The problem is that during start-up, the clamp and the output capacitors have low voltages and thus the C_r capacitor voltage cannot reach the desired value to provide soft switching. As a result of which, the soft switching at turn-on of the switch is lost and the snubber capacitor discharges through the switch during startup. Losing soft switching at the startup does not affect on the circuit operation and efficiency but the snubber capacitor energy should be low enough in order not to damage the switch during startup time. The energy of the snubber capacitor depends on the value of snubber capacitor (C_r), the output capacitance of the switch (C_{oss}), voltage stress of the switch, and the startup time (t_{ss}), during which the capacitor discharges throughout the switch

$$W_{\text{loss}} = 0.5\ (C_s + C_{oss})\,V^2.f.t_{ss}\,. \tag{50}$$

This energy should be lower than the maximum power that switches S_1 and S_2 can dissipate throughout their heatsink. Due to the short duration of start-up time which is around 1–10 ms depends on the soft-start time [44] and by considering the components in Table II and (50), dissipated energy during startup time of the switch is around 30 mJ, which is negligible and much less than that to cause the switch to damage.

IV. Results

A. Experimental Results

To verify the performance of the proposed converter and validate its advantages, a laboratory prototype with the specifications is presented in Table II is built. Since in this converter, the gate-source of the auxiliary switches S_{a1} and S_{a2} are floating and separate from the main ground of the circuit, an isolated gate-driver is required. There are different options for implementing

TABLE II
IMPORTANT PARAMETERS OF THE IMPLEMENTED PROTOTYPE

PARAMETER	VALUE
Input voltage V_{in}	48V
Output voltage V_o	400V
Output power P_o	400W
Switching frequency f_s	100kHz
Full load Efficiency	98 %
Main switches S_1 and S_2	IRF150P221
Auxiliary Switches S_{a1} and S_{a2}	IPB200N25N3G
Diodes D_1	*STTH1003S*
Diodes D_C	*STTH1002C*
Diodes D_o	*STTH1003S*
(L_1, L_3) and (L_2, L_4) cores	EE3329
Magnetizing inductances L_{m1} and L_{m2}	300 µH
Leakage inductances L_{lk2}, L_{lk2}	3µH
Turns ratio (n)	1
Gate driver inductor L_g	10uH
Snubber capacitors C_{s1}, C_{s2}	2.2 nF / 200V
Resonant Capacitor C_r	22 nF / 250V
Capacitor C_1	4.7 µF / 300V
Clamp capacitor C_C	4.7 µF / 200V
Output capacitors C_O	47 µF / 450V
Gate driver Diodes Dg_1 and Dg_2	ES2A
Gate driver Capacitors Cg_1 and Cg_2	4.7 uF (Tantalum)

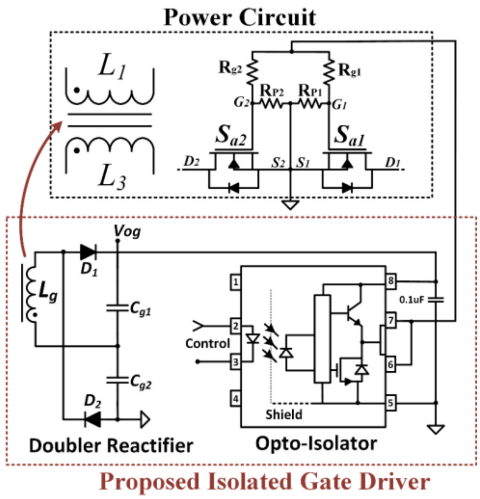
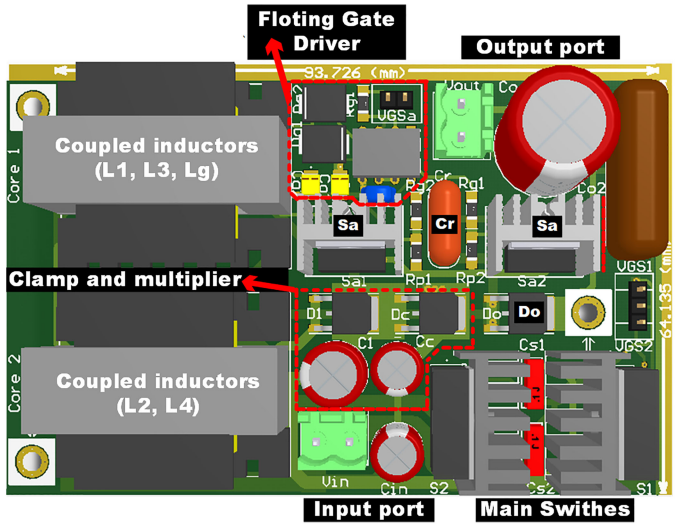
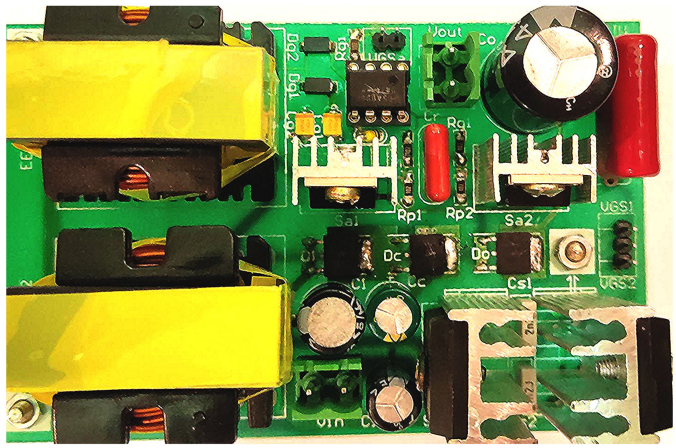


Fig. 10. Proposed isolated gate driver for the auxiliary switches (s_a).



(a)



(b)

Fig. 11. PCB of the proposed Circuit. (a) 3D prototype. (b) Implemented prototype.

the isolated gate driver such as opto-isolators. These methods require an extra isolated power supply resulting in lower power density. In this section, an optimized gate driver circuit based on opto-isolators is proposed for driving the auxiliary switches, which is beneficial for specific applications that demand higher power density. The proposed gate-driver circuit is presented in Fig. 10. A small tertiary winding (L_g) is employed which is coupled with the coupled inductors $L_1$and L_3 to fulfill the need for isolated power source and prevent extra space occupation. The needed power for the gate-driver circuit is very low (below 1W), so L_g winding does not take much space. But for further reduction in the volume of L_g, a voltage-doubler circuit is employed to rectify the pulsating voltage across L_g. Due to boosting the voltage by voltage-doubler circuit, the number of turns of L_g coil (n_g) is reduced. The positive voltage across L_g is a ratio of V_{in} and the negative voltage is a ratio of $(V_{\text{in}} - V_{c1} - V_{cc})$. As, V_{og} is the summation of V_{cg1} and V_{cg2}, it is given by

$$V_{og} = \frac{n_g}{n_1} V_{in} + \frac{n_g}{n_1} \frac{D}{1-D} V_{\text{in}}. \tag{51}$$

Therefore, the number of turns of L_g inductor (n_g) is achieved by

$$n_g = \frac{n_1 (1-D)}{V_{\text{in}}} V_{og} \tag{52}$$

where n_1 is the number of turns of L_1 and V_{og} is the required voltage for the auxiliary switches' gate driver, which is typically below 20 V, depending on the type of power MOSFET.

The implemented prototype of the proposed converter is presented in Fig. 11 and the experimental waveforms are illustrated in Figs. 12 and 13. Current and voltage waveforms of the main switches S_1, S_2 and the auxiliary switch S_a are shown in Fig. 12(a)–(c). It is noted that S_a switch is a series combination of MOSFETs $S_{a1}$and S_{a2}. As can be seen in these figures, ZVS condition at turn-ON and turn-OFF are achieved for the main switches, and the auxiliary switch is properly turned OFF under

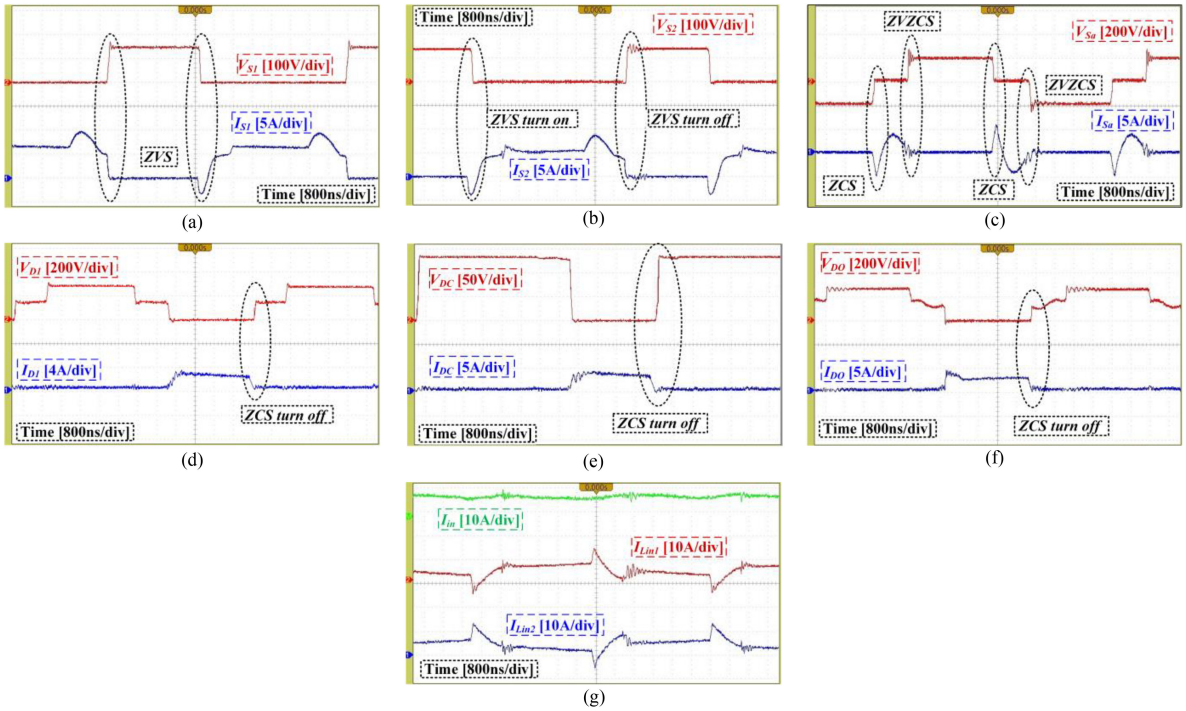


Fig. 12. Experimental waveforms of the implemented prototype at full load. (a) Main switch S_1. (b) Main switch S_2. (c) Auxiliary switch S_a. (d) Diode D_1. (e) Diode D_C. (f) Diode D_O. (g) Input currents $I_{\text{in}1}$, $I_{\text{in}2}$, and I_{in}.

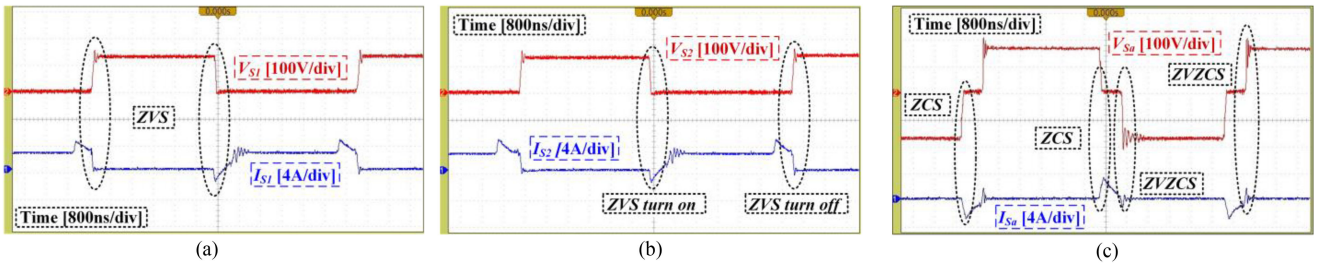


Fig. 13. Experimental waveforms of the switches at light load (20% of nominal load). (a) Main switch S_1. (b) Main switch S_2. (c) Auxiliary switch S_a.

ZVS and is also turned ON under ZCS condition. Fig 12(d)–(f), respectively, show the voltage and current of diodes D_1, D_c, and D_o. The achieved ZCS turn OFF condition for all three diodes can alleviate reverse recovery effect of power diodes. Fig. 12(g) illustrates the input current (I_{in}) and the magnetizing inductance currents (I_{Lm1} and I_{Lm2}). Due to the interleaved structure, the input current ripple is low, because it is the summation of two parallel modules with 180-degree phase shift and thus the current ripple of coupled inductors can be canceled in the input current. Moreover, to validate the capability of providing soft switching at light loads, voltage and current waveforms of the switches at 20% of nominal load (80 W) are presented in Fig. 13. These waveforms illustrate the capability of the proposed converter in providing soft switching for a wide range of output power.

B. Comparison of the Proposed Converter With Previous Converters

The proposed ZVT auxiliary cell which is highlighted via the red box in Fig. 2(a) is compared with the existing ZVT cells used for the interleaved boost structures in [21]–[29], and [31]. Comparison results are presented in Table III. Note that in this table the active clamp circuits are not referred and they are compared in Table IV, because as mentioned in the introduction section, the soft-switching condition, which can be provided via active clamp circuits, is load dependent and has limited soft-switching range. So, only ZVT cells which can provide soft switching independent of load for interleaved boost structures are referred in this section. Compared to the other ZVT structures, the main advantage of the proposed ZVT cell is using the minimum number of circuit elements. As can be observed in Table III, only one bidirectional switch is used as a semiconductor element in the proposed cell which is implemented via two power MOSFETS and thus merely a single gate driver is employed; while for the other schemes, three or more semiconductor elements including power switches and diodes are required. This results in low conduction losses of the proposed ZVT cell and the ZVT cell presented in [23]. Due to employing the leakage inductance of the power circuit as the resonant inductor, no additional magnetic cores and auxiliary

TABLE III
COMPARISON OF THE PROPOSED AUXILIARY CELL WITH THE EXISTING ZVT CELLS APPLIED TO THE INTERLEAVED BOOST TOPOLOGIES

ZVT CELL	SEMICONDUCTOR ELEMENTS	THE TYPE AND THE NUMBER OF GATE DRIVERS	AUXILIARY WINDING	EXTRA CORE	CAPACITOR	CONDUCTION LOSS
REF. [26]	5	1 – N[1]	3	2	0	HIGH
REF. [27]	5	1 – N	1	1	1	HIGH
REF. [28]	5	1 – N	2	2	1	HIGH
REF. [25]	5	1 - N	2	0	1	HIGH
REF. [24]	4	1 - N	1	1	1	HIGH
REF. [21]	4	2 - N	2	2	4	HIGH
REF. [31]	3	1 – I[2]	1	1	0	LOW
REF. [29]	3	1 - N	2	1	1	LOW
REF. [22]	3	1 - N	2	0	0	LOW
REF. [23]	2	2 - N	2	2	2	VERY LOW
PROPOSED	1*	1 – I	0	0	1	VERY LOW

*A bidirectional switch implemented via two unidirectional power MOSFETs.
[1]Non-isolated gate driver.
[2]Isolated gate driver.

TABLE IV
COMPARISON OF THE PROPOSED CONVERTERS WITH OTHER SOFT SWITCHING INTERLEAVED BOOST CONVERTERS

Converters	Voltage Gain (M)	Voltage Gain (n=1, D=0.65)	Switch Voltage Stress	Soft Switching range	C-G*	No R.R*	Number of Components					
							MOS*	D*	Cap*	Win*	Core	T*
Ref. [14]	$\frac{2n_m}{(1-D)}$[1]	$5.7.n_m$	$\frac{V_o}{2n_m}$	LI*	✘	✘	2	$5+2n_m$	$2+2n_m$	4	4	$11+4n_m$
Ref. [15]	$\frac{2n_2(1+n_1)+1}{3n_2(1+n_1)+2}$	-	$\frac{V_o}{3n_2(1+n_1)+2}$	LI	✘	✓	2	8	7	7	3	20
Ref. [16]	$\frac{6N+1}{(1-D)}$	20	$\frac{V_o}{6N+1}$	LD*	✓	✓	4	6	7	4	2	19
Ref. [17]	$\frac{2(N+1)}{(1-D)}$	11.4	$\frac{V_o}{2(N+1)}$	LD	✓	✓	4	4	5	5	3	16
Ref. [18]	$\frac{5}{1-D}$	14.3	$\frac{V_o}{5}$	LD	✘	✓	4	7	9	6	4	24
Ref. [19]	$\frac{2(2N+1)}{(1-D)}$	17.2	$\frac{V_o}{2(2N+1)}$	LD	✓	✘	4	4	5	4	1	14
Ref. [20]	$\frac{2(N+1)}{(1-D)}$	11.4	$\frac{V_o}{2(N+1)}$	LD	✓	✓	4	2	3	2	2	11
Ref. [21]	$\frac{2N+1}{(1-D)}$	8.6	V_o	LI	✓	✘	4	8	7	6	4	23
Ref. [22]	$\frac{2(N+2)}{(1-D)}$	17.2	$\frac{V_o}{2(N+2)}$	LI	✘	✓	3	6	4	6	2	15
Ref. [23]	$\frac{2(N+1)}{(1-D)}$	11.4	$\frac{V_o}{2(N+1)}$	LI	✓	✓	4	6	7	8	4	21
Ref. [24]	$\frac{2}{(1-D)}$	5.7	$\frac{V_o}{2}$	LI	✓	✓	3	5	3	3	3	14
Ref. [25]	$\frac{1+3n}{(1-D)}$	11.4	$\frac{V_o}{1+3n}$	LI	✓	✓	3	10	6	8	3	22
Proposed Converter	$\frac{n+2}{(1-D)}$	8.6	$\frac{V_o}{n+2}$	LI	✓	✓	4	3	4	4	2	13
Proposed with extra switched cap cell	$\frac{n+4}{(1-D)}$	14.3	$\frac{V_o}{n+4}$	LI	✓	✓	4	5	5	4	2	16

MOS: MOSFET; **D**: Diode; **Cap**: Capacitor; **Win**: Winding, **T**: Total **LD**: Load-Dependent, **LI**, Load-Independent **C-G**, common Ground **R.R**, Reverse Recovery
[1]Number of multiplier cells

windings are needed for the proposed ZVT cell, whereas at least one auxiliary winding is necessary for other topologies. Having no extra diodes, employing the lowest number of switches and no extra magnetic elements in the proposed ZVT cell are distinctive advantages of the proposed cell. All these factors result in very low conduction losses and high-power density of the proposed ZVT cell.

In Table IV, the proposed interleaved converters are compared with several similar structures from different aspects. In terms of the soft-switching point of view, [14] and [15] use lossless snubber circuits to create soft-switching condition. The ZCS turn-on condition in these converters results in E_{oss} losses for both main switches. Also, the converter in [15] has only ZCS condition at turn-on instants and turn-off soft switching is lost. Moreover, they lack common ground between the input and output voltage which makes the control scheme more complex. Converters in [16]–[20] employ the active clamp technique to provide ZVS conditions for power switches, but the limitation of these converters is the dependency of the soft-switching condition on the load. Making use of ZVT cells, the proposed converters along with converters in [21]–[25] create ZVS conditions and guarantee soft-switching in the whole range of output load. The first proposed converter benefits from the lowest number of components among all converters in Table II excluding [20] and also it has higher voltage gain than converters in [14] and [24] and similar voltage gain with converters in [21] and [25]. The second proposed converter retains the benefits of the first proposed one and has higher voltage gain than converters in [14], [17], [20], [21], [23]–[25] and a similar gain with [15] and [18]. In comparison to the proposed converters, the circuits in [16] and [19] have a bit higher voltage gain and lower switch voltage stress, at the expense of using a higher number of semiconductor components but, the soft-switching condition is load-dependent in these converters. Moreover, the reverse recovery loss is considered in [19]. The only ZVT interleaved converter in Table II has higher voltage gain than the second proposed converter is [22]. In sharp contrast, it has serious issues such as high number of components including nine semiconductor elements and six windings which degrades the power density and total efficiency. In the proposed converters, only two magnetic cores are required, while four separate magnetic cores are used in [14], [18], [21], and [23] which raise circuit volume and losses. To sum up, the proposed converters provide a high voltage conversion ratio with low switch voltage stress and soft-switching performance independent of output load and input voltage using minimum magnetic cores and circuit elements. Wide range of soft-switching performance dramatically reduces switching losses and provides high efficiency in a wide range. Also, common ground is another noteworthy feature of these converters which simplify the voltage feedback.

C. Power Loss and Power Density Analysis in Comparison With Other Converters

Since one of the outstanding features of the proposed ZVT converter is utilizing small number of components as well as low losses at both full loads and light loads, this feature must be investigated. In this section, a detailed losses breakdown is presented for the proposed converter at both full load and light load (20% of the nominal load) conditions and two other ZVT interleaved high step-up converters in [23] and [24] (see Fig. 14). OrCAD PSPICE software is used in this section for simulating the mentioned converters and analysis. In Fig. 14, the main and the auxiliary power components including power switches, diodes, and inductors are separately considered and the rest of the losses associated with the gate driver and ESR of capacitors are aggregated in the chart under the name of "Others." A-switches, A-diodes, and A-windings stand for the auxiliary switches, diodes, and windings used in each ZVT cell, and M-switches, M-diodes, and M-windings denote the main power components of each converter. Note that losses of the main switches consist of conduction losses and switching losses at turn off, because the ZVS condition at turn off is achieved via snubber capacitor and switching losses would not be completely

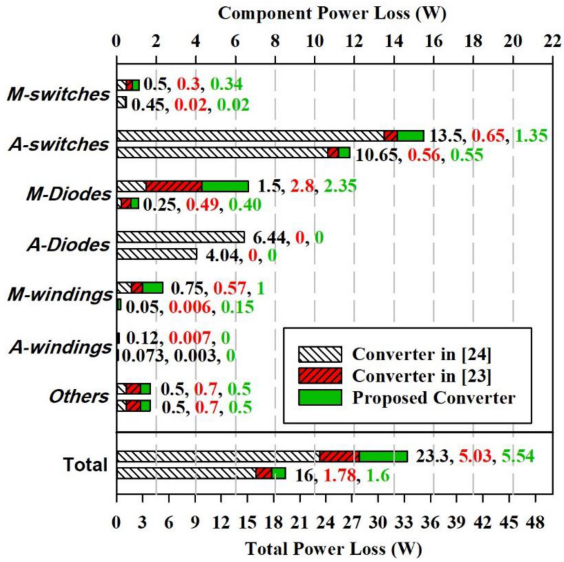


Fig. 14. Loss distribution of the proposed converter in comparison with converters in [23] and [24] at full-load (first rows) and light-load (second rows).

TABLE V
CONDUCTION LOSSES OF THE COMPONENTS USED IN THE PROPOSED CONVERTER

Component	Resistance [Ω]	RMS Current [A]	Power Loss [W]
Main switches S_1, S_2	0.0036	6.9	2×0.17
Auxiliary Switch S_a	0.02	2	2×0.08
Inductors L_1, L_2	0.012	5.7	2×0.39
Inductors L_3, L_4	0.014	2.87	2×0.115
Component	**Forward Voltage [V]**	**Average Current [A]**	**Power Loss [W]**
Diode D_1	0.8	1	0.8
Diode D_C	0.75	1	0.75
Diode D_O	0.8	1	0.8
Body diode of S_a	0.8	0.73	2×0.59
Total conduction losses			**5.04**

TABLE VI
POWER DENSITY AND COMPONENTS SPECIFICATIONS OF THE PROPOSED CONVERTER AND CONVERTERS IN [23] AND [24] (400 *W*, 48–400 *V*)

ZVT Step-up Converters	Power Density (W/Cm^3)	Main Switch (S_1, S_2)	Aux. Switches (S_{a1}, S_{a2})	D_{o1}, D_{o2}	D_{c1}, D_{c2}	D_1, D_2	C_o	C_{r1}, C_{r2}	C_1, C_2	C_{c1}, C_{c2}	C_{s1}, C_{s2}
Proposed Converter (Fig. 18)	*1.9*	133V-9A 133V-9A *IRF150P221*	210V-7A 210V-7A *IPB200N25N3*	300V-5A (Only Do1) *STTH1003S*	150V-5A (Only Dc1) *STTH1002C*	300V-5A (Only D1) *STTH1003S*	400V 47uF	200V-22nF (Only C_{r1})	150V-4.7uF (Only C_1)	300V-4.7uF (Only C_{c1})	200V-2.2nF 200V-2.2nF
Converter in [23] (Fig. 16)	1.5	110V-14A 110V-14A *IRF150P221*	200V-8A 200V-8A *IPB200N25N3*	290V-3A 290V-3.5A *STTH1003S*	120V-8A 120V-8A *STTH1002C*	290V-3A 290V-3.5A *STTH1003S*	400V 47uF	100V-100nF 100V, 100nF	250V-4.7uF 250V-4.7uF	150V-4.7uF 150V-4.7uF	150V-2.2nF 150V-2.2nF
Converter in [24] (Fig. 17)	*1.7*	210V-9A 210V-9A *IPB200N25N3*	133V-9A (Only Sa1) *FDL100N50F*	200V-6.5A (Only Do1) *STTH1002C*	200V-9A 200V-9A *STTH1002C*	400V-6.5A 400V-12A *STTH16R04C*	400V 47uF	250V-22nF (Only C_{r1})	No Capacitor	200V-4.7uF (Only C_{c1})	250V-2.2nF 250V-2.2nF

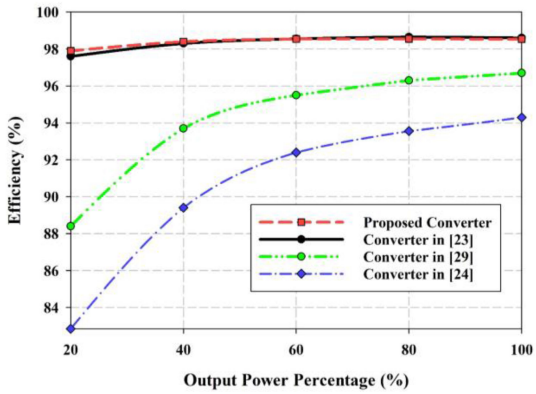


Fig. 15. Efficiency of the proposed converter in comparison with the ZVT interleaved converters in [23], [24], and [29].

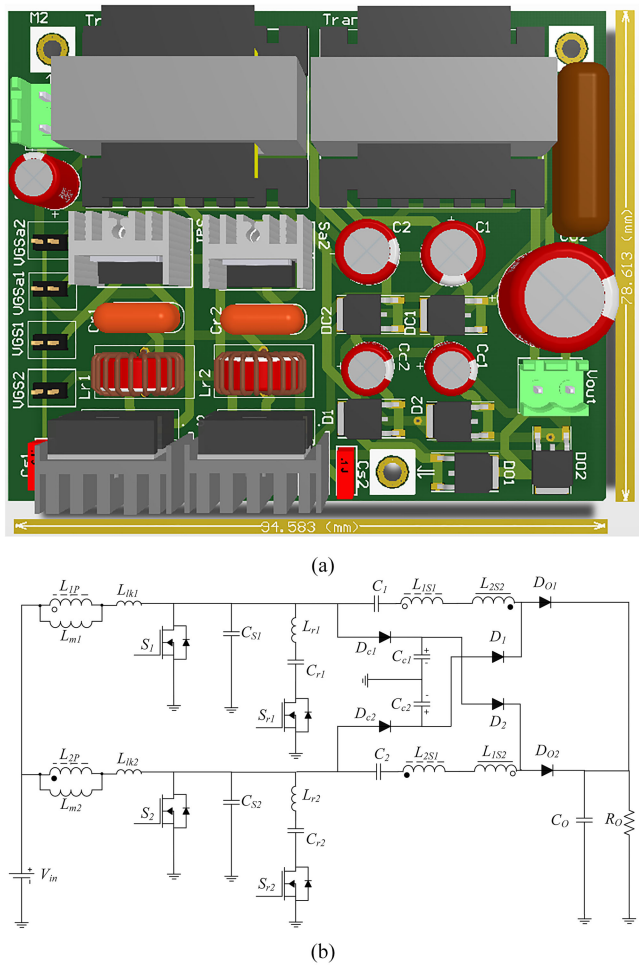


Fig. 16. Converter in [23]. (a) 3D prototype. (b) Schematic.

zero. For the auxiliary switches which are turned ON under ZCS condition, in addition to the conduction losses, E_{oss} losses are also considered. For the proposed converter, M-diodes losses are the summation of D_1 , D_c, and D_o conduction losses. According to Fig. 14, losses of the auxiliary diodes (A-diodes) of the converters in [24] are of the highest value and have devoted a huge share of losses to themselves, but in the proposed converter and converter in [23], this term is zero. Also, the main diode losses in the proposed converter are lower than the converter in [13] because of utilizing fewer power diodes in the proposed topology. The effects of auxiliary diodes are more significant at light loads and it is one of the parameters which causes high efficiency at light loads. This is because the proposed ZVT cell has used no auxiliary diode and only one semiconductor component is utilized. Table V presents the details of conduction losses calculations for the proposed converter at nominal load including switches, diodes, and windings losses.

In terms of efficiency, the proposed converter is compared with ZVT interleaved converters in [23], [24], and [29] by using computer simulations (PSpice software) and the results are presented in Fig. 15. The specifications of the simulated converters are the same as that of the proposed converter in Table II. Note that, *IRF150P221* ($V_{DS} = 150$ V, $R_{ds(on)} = 3.6$ mΩ, $C_{oss} = 1.5$ nF) is utilized for S_1 and S_2 switches of the proposed converter and the converter presented in [23] which benefits from lower voltage stresses. Also *IPB200N25N3* ($V_{DS} = 250$ V, $R_{ds(on)} =$ 20 mΩ, and $C_{oss} =$ 0.297 nF) and *STP20NK50Z* ($V_{DS} = 500$ V, $R_{ds(on)} = 250$ mΩ, $C_{oss} = 0.328$ nF) are, respectively, used for the main switches of the converters in [24] and [29], since they need switches with higher voltage stress. To select the proper auxiliary switch and optimizing its losses, two factors including rms current and the voltage stress of the auxiliary switch which result in the conduction loss and the E_oss losses must be considered. For the proposed converter and converter in [23] due to the low rms current and low voltage stress at turn-ON

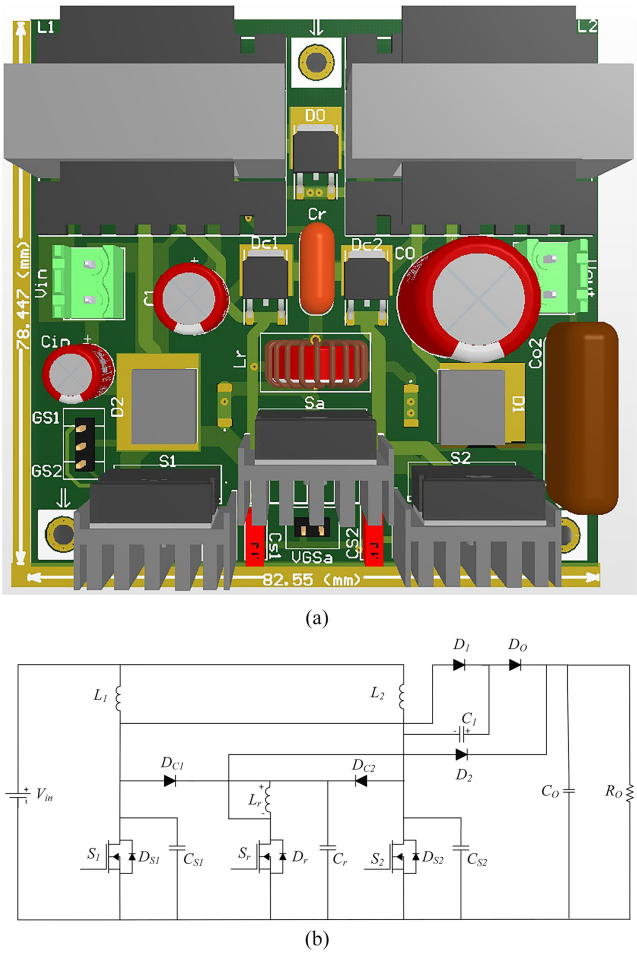


Fig. 17. Converter in [24]. (a) 3D Prototype. (b) Schematic.

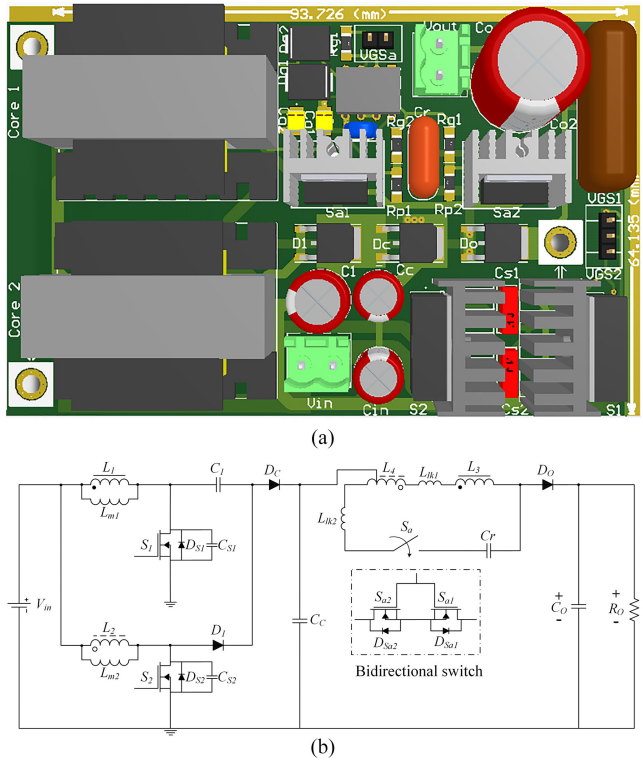


Fig. 18. Proposed converter. (a) 3D prototype. (b) Schematic.

instances, *IPB200N25N3* (V_{DS} = 250 V, $R_{ds(on)}$= 20 mΩ, and C_{oss} = 0.297 nF) is selected. In order to have a fair comparison, it is highly important to select a MOSFET with low drain-source resistance for the auxiliary switch in [24], due to the very high rms current. So *FDL100N50F* (V_{DS} = 500 V, $R_{ds(on)}$= 43 mΩ, and C_{oss} = 1.7 nF) is selected. In contrast, for converter in [29] due to having high voltage stress at turn-ON instant of the switch and thus high E_{oss} losses, a switch with low output capacitance (C_{oss}) must be selected, which is *STP20NK50Z* (V_{DS} = 500 V, $R_{ds(on)}$= 250 mΩ, C_{oss} = 0.328 nF). Note that to have a fair comparison, it is tried to use switches with almost the same cost for the mentioned converters.

As can be observed in Fig. 15, the proposed converter and converter in [23] have the highest full load efficiency which is around 98.7% at 400 W output power. In addition, there is no considerable efficiency drop at light loads thanks to the simple ZVT circuit which is around 98%. This is because of the low number of components and low conduction losses of the proposed converter. Despite providing soft-switching condition and removing switching losses, the main issue for the converter in [24] is having high conduction losses for the auxiliary switch which has degraded the efficiency not only at full loads but also at light loads. Also, the converter in [29] suffers from high voltage stress over both the main and the auxiliary switches which resulted in higher conduction and E_{oss} losses. Considering the fact that the efficiency of the proposed converter is almost equal to that of the converter in [23] at full loads and it is a bit higher at light loads, the main advantage of the proposed converter over converter in [23] is benefiting from the lower number of power components and employing a simpler ZVT cell with no extra magnetic element and auxiliary diodes.

In addition to investigation of losses breakdown and efficiency, the power density as well as voltage and current stress of semiconductor components is presented in Table VI. The three-dimensional prototype of the proposed converter and converters in [23] and [24] are presented in Figs. 16–18 to compare power density. For each prototype, the best-matched components are chosen based on the current and voltage stress of each converter (see Table VI). The power density of the proposed converter is 20% higher than the converter in [23] and 10% higher than [24] at 400 W due to having fewer components. For higher output powers, this difference is increased because the auxiliary circuit and extra capacitors and diodes in [23] will highly affect the power density in case of increasing the output power.

V. Conclusion

In this article, a novel soft switched interleaved step-up converter for distributed generation applications was presented. Utilizing a simple ZVT auxiliary circuit, composed of only one bidirectional switch and a small capacitor, as well as containing the minimum number of power components has made this a highly efficient topology and an appropriate candidate for high

power density dc–dc applications. The capability of increasing voltage gain to the desired value with a low number of power components, as well as low voltage stress across switches has resulted in low conduction losses for the proposed converter. Additionally, by providing soft-switching condition in a wide range of output power and alleviating reverse recovery problems, an experimental efficiency of 98% and a theoretical efficiency of 98.7% were observed at full load (400 W). Also, at 20% of nominal load, a theoretical efficiency of 98% was achieved. The power density of the implemented prototype was observed at 1.9 W/Cm^3.

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