A Dynamic ZVS-Guaranteed and Seamless-Mode-Transition Modulation Scheme for the DAB Converter That Maximizes the ZVS Range and Lowers the Inductor RMS Current

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***Abstract*—The dual active bridge (DAB) converter operating with a relatively high switching frequency is well suited for deriving a high-power density electric vehicle (EV) charger. In this case, safeguarding the realization of zero voltage switching (ZVS) for a wide operating range becomes crucial to ensure a good performance in terms of efficiency and control reliability. Unfortunately, most modulation schemes available today in the literature require a detrimental compromise in the achievable ZVS range, particularly the ones working mainly toward the minimization of the current stress. Due to the fact a public EV charger will work with multiple vehicles having quite different charging profiles, i.e., with wide operational voltage and currents ratings, the ZVS operation may be prone to fail to undermine the whole cycle charging efficiency. To relieve the issues, this article proposes a new modulation scheme for the DAB converter featuring a maximized ZVS range and a quasi-optimal inductor rms current. Herein, the concept of dynamic settings of the required modulator's ZVS-current is utilized and a straightforward implementation with seamless circuit mode transition is achieved. With the above characteristics, the dynamic and static losses of the component circuits can be reduced together. By adopting the dynamic ZVS-current settings strategy, the turning-ON currents of the DAB switches are adjusted in real-time guaranteeing the ZVS operation under various operating conditions. With the seamless transition, the inductor current can be smoothly regulated to ensure system stability. The proposed modulation scheme is introduced, analyzed, validated, and benchmarked in a 4.5 kW/100 kHz SiC-based DAB prototype, whose peak efficiency can reach 96.3% when operated at partial load.**

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***Index Terms*—Dual active bridge (DAB) converter, dynamic zero voltage switching (ZVS) current, rms current optimization, seamless mode transition, ZVS range.**

I. Introduction

DUAL active bridge (DAB) dc–dc converters are commonly adopted in applications aiming for high-power density, bidirectional power flow, galvanic isolation, and power scalability by circuit series or parallel modularity. This circuit concept, which is shown in Fig. 1, is particularly suited for applications demanding the wide input-to-output voltage range where zero voltage switching (ZVS) characteristics can be maintained for critical operating conditions. Therefore, the overwhelming characteristics of the DAB have attracted extensive attention since the 1990s when the circuit was first proposed in [1]. Moreover, as the DAB converter can be adopted as power electronics building blocks for both series or parallel modularity, it has become a prevalent solution in the future low- and medium-voltage power electronics markets featuring dc grids [2], [3], or solid-state transformers [4], [5], electric vehicles (EVs) [6], [7], and energy storage systems [8], [9], among others.

As the mainstream control strategy for the DAB converters, phase shift control first appeared in the form of single phase shift (SPS) control [1]. Subsequently, several extensions of the SPS control have been proposed in the literature aiming to enhance the DAB circuit's design metrics, such as the double phase shift (DPS) control [10], the extended phase shift (EPS) control [11], and the triple phase shift (TPS) control [12]. As the unified form of the SPS, DPS, and EPS controls, the TPS control is the most widely studied method at present. Based on the TPS concept, many scholars conducted studies optimizing the DAB performance from the perspectives of widening the ZVS range [13]; eliminating the backflow power [14], [15]; the reduction of circulating reactive power [16], [17], and overall improvements to the circuit components' peak [18], [19] and rms current stresses [20]–[22]; and multiobjective optimization combining several metrics [23].

As a general observation, most DAB control studies and proposed circuit design guidelines are concerned at improving

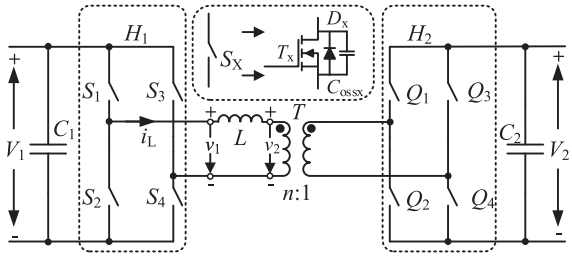

Fig. 1. Circuit diagram of the DAB converter.

the power efficiency of the system. In the DAB system, the major source of power losses can be divided into active semiconductors' dynamic (or switching) and static (or conduction) losses, and passive (magnetic and capacitor) losses, where particularly at heavy load the static loss can play a dominant role in the achievable power efficiency [24], [25]. Since the rms value of the transformer or inductor current is positively correlated with the static semiconductor and passive circuitry losses, the most intuitive way to improve power efficiency becomes the optimization logic to minimize this rms current. Single-objective optimization of the DAB's inductor rms current is carried out in [20]–[22]. The global optimal condition (GOC) method is proposed in [20] to obtain the optimal solution in the full power range. Artificial intelligence algorithms are also widely investigated in power electronic control [21], [22]. Nevertheless, the optimization performance is basically consistent with the numerical optimization solution in the GOC.

In the pursuit of high-power density in the EV charger application [26], SiC devices are widely adopted and the volume of the magnetic components can be significantly reduced with the adoption of a high switching frequency operation [27]. However, caution needs to be taken to the semiconductor switching loss caused by a possible hard-switching operation, which will limit the design improvements attainable by raising the switching frequency. In the optimization schemes focusing on the inductor rms current presented in [20]–[22], the realization of ZVS is ignored and only zero current switching (ZCS) can be realized. Herein, strict constraints are applied to the backflow power, which benefits the selection of ZCS against the ZVS strategy. This occurs because the ZVS process naturally leads to a higher backflow power, which would reduce the effectiveness of the proposed optimization method. With the increment of the switching frequency, the switching loss gradually plays a dominant role in the system efficiency, thus the mitigation of the semiconductors' switching-on loss by ZVS becomes advantageous. In ZCS operation it becomes difficult to fully eliminate the switching loss caused by the stored charge across the semiconductors' parasitic capacitances. Additionally, the smoother *dv*/*dt* of the ZVS operation also can suppress high-frequency crosstalk and ease electromagnetic compatibility design in the megahertz range. In fact, the ZVS operation of all DAB's switches (called here as all-ZVS operation) can be realized at light load by sacrificing a small proportion of rms current. Herein, the additional backflow power can be used to reduce switching loss and further improve system efficiency [28]. Consequently, multiobjective optimization strategies crosslinking the ZVS operation and reduction of component's current stress have been studied in [23] and [28]–[30]. Based on the Karush–Kuhn–Tucker condition, the Lagrange multiplier method, or the artificial intelligence algorithm, the current optimization effects in [23] and [28]–[30] are almost similar.

For the realization of ZVS, the work in [30] proposes a dead time control method to optimize the ZVS range and the peak current across the circuit, by which the dead time is adjusted to allow the complete charge balance during the switching transition. Although a reasonable amount of the backflow power can be eliminated, the dead time control is particularly sensitive to parasitic parameters. In addition, in [30], the proposed dead time calculation expression employs antitrigonometric functions that are too complex to be applied in effective real-time control. From another point of view, the ZVS operation can also be realized by controlling the turning-ON current of the switch without requiring the change of dead time [28], [29]. This is simpler to be realized in real-time control, and it is relatively more robust to parasitic parameters. The works in [28] and [29] use the H-bridge inverter phase shift angles to control the turning-ON current of the switches, while aiming for the minimization of the current necessary for realizing ZVS, which for now on will be called the ZVS-current. Nonetheless, the ZVS-current could be inaccurate, which is only determined from the perspective of inductance energy or capacitor charge. Once the dead time is too long or too short, the complete realization of ZVS would fail. Moreover, the required ZVS-current is closely bound up with circuit electrical parameters. During the battery charging process, the output voltage and current of the DAB are required to be adjusted with the state of charge (SOC). Unfortunately, the ZVS-currents in [28] and [29] are always kept constant and the realization of ZVS cannot be accomplished in a wide operating range.

In [28] and [29], at light load, the ZVS operation can always be achieved for all active semiconductors (an all-ZVS operation). However, at medium load, the ZVS operation only can be achieved in two switches (called here a two-ZVS operation). In [30], a near-all ZVS control strategy is proposed and the ZVS range is extended only under the buck-type operation. Moreover, the realization of ZVS in the aforementioned works is analyzed separately in each mode. If the ZVS-current is not consistent, the discontinuous change would occur in the control variables during the circuit mode transitions, bringing uncontrolled distortions to the inductance and output currents. A seamless modes transition is considered in [28], and the system stability is reinforced but the ZVS-current cannot be dynamically adjusted, restraining the system efficiency under various operating conditions.

Based on the above analysis, to further improve system efficiency and to enhance operational stability of a high-frequency operated DAB converter, a multiobjective optimization combined with the SPS, the EPS, and the TPS controls is proposed in this article to achieve a wide ZVS range and low rms current stress across the circuit components. At light load, an all-ZVS operation can be achieved and the extra backflow power is eliminated for the reduction of the inductor rms current. At

medium load range, a six-ZVS (six switches featuring ZVS turn-ON) operation can be realized, whereas only the two-ZVS operation can be implemented in the previous listed works. At heavy load, an optimal rms current control is adopted where an all-ZVS operation also can be naturally achieved. Herein, the system operation is divided into four modes under the buck- or boost-type voltage gains, respectively. Additionally, the seamless transition of all utilized operating modes is also considered in the proposed modulation scheme, by which the inductor and output currents can be smoothly regulated for enhancing operation stability. Furthermore, based on the system operation modes, the unified ZVS-currents for the switches located at the transformer's primary or secondary sides are derived from the point of charge exchange and dead time, only by which the ZVS conditions of all switches in any mode can be satisfied. This advantageously reduces the calculation complexity. Since the seamless continuous change of the ZVS-currents under various operating conditions can be achieved, the real-time control and dynamic adjustment of the ZVS-current can be realized together. Therefore, the wide ZVS range and low rms current characteristics still can be achieved in transient operations.

The main contributions of this article are as follows.

1) The proposal of a multiobjective optimization strategy that widens the DAB converter's ZVS range and obtains a quasi-optimal rms current stress across the circuit components for the full operating range of an EV charger system.
2) The concept of unified ZVS-current is proposed for all switches of the DAB converter. This is suitable for real-time control and it can be dynamically adjusted for the realization of ZVS under a wide operating voltage range.
3) Seamless transition of all utilized circuit's operating modes is achieved for the constant voltage (CV) and constant current (CC) EV charging profiles, by which the inductor current and output current can be smoothly regulated.
4) The analytical and experimental validation of the study.

The rest of this article is organized as follows. In Section II, combined with the SPS, EPS, and TPS controls, the proposed control strategy of this article is described. In Section III, the necessary conditions for achieving ZVS are discussed and the expressions for the ZVS-currents are determined. In Section IV, the control loop is designed, and the ZVS range and smooth transition of all selected operating modes are analyzed. In Section V, a DAB prototype is built to verify the correctness of the theoretical analysis. Finally, Section VI concludes this article.

II. Analysis of the Proposed Control Method for the Maximized ZVS Range and Optimal RMS Current

A. DAB Model Under TPS Control

The DAB topology studied in this article is shown in Fig. 1. C_1 and C_2 represent the input and output capacitors, respectively. Herein, V_1 and V_2 are the input and output voltages of the circuit, respectively. The primary side H-bridge inverter H_1 and the secondary side H-bridge rectifier H_2 are composed of the controllable switches S_1–S_4 and Q_1–Q_4, respectively. Normally, switch S_x can be regarded as the combination of a transistor T_x,

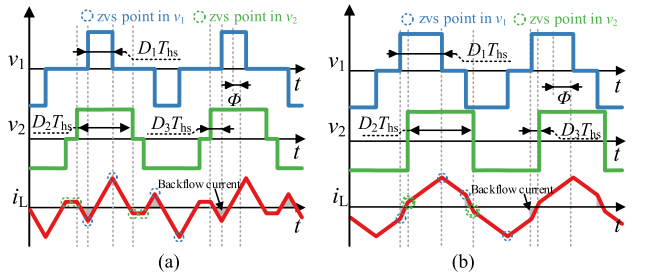

Fig. 2. Typical modes of DAB converter with an all-ZVS operation and low rms current under the buck-type operation. (a) All-ZVS mode at light load ($1 \geq D_2 \geq D_1 \geq 0$ and D_1–$D_2 \leq D_3 \leq 0$). (b) All-ZVS mode at heavy load ($0 \leq D_1 \leq D_2 \leq 1$ and $0 \leq 1$–$D_2 \leq D_3 \leq D_1 \leq 1$).

an antiparallel diode D_x, and an output capacitance C_{ossx}. H_1 and H_2 are connected by a transformer T and inductor L, where L can be seen as the sum of an auxiliary inductance and the transformer leakage inductance. The transformer turn ratio is n : 1 and the voltage gain ratio $M = nV_2/V_1$. $M < 1$ and $M > 1$ delimit the buck- and boost-types voltage gain operating ranges, respectively.

As shown in Fig. 2, D_1 and D_2 represent the duty cycle of v_1 and v_2. D_3 is the lag duty cycle of Q_4 compared with S_4. T_{hs} denotes the half switching cycle. The auxiliary variable $\Phi = D_3 + (D_2$–$D_1)/2$ represents the phase difference of the central axis in v_1 and v_2. The sign of Φ determines the direction of power flow. In general, the operation of the DAB can be divided into 12 modes under the buck-type and boost-type operations [21]. However, only two modes can achieve low rms current and all-ZVS operation simultaneously, as shown in Fig. 2(a) and (b). The gray part in i_L represents the backflow current, which would be reversely processed to the source and bring unnecessary power loss during the ZVS process. Moreover, during the transition of two modes, only a two-ZVS operation can be achieved at medium load [28], [29].

In order to realize a wide ZVS range, an optimal rms current stress, and a seamless mode transition, the system operations of the proposed control scheme (PCS) are divided into four modes under buck-type and boost-type operations, respectively. This is shown in Figs. 3 and 4. The ZVS-currents I_P and I_S denote the switching current of the primary and secondary side switches necessary for realizing the ZVS turn-ON. The per-unit values of the inductor current at each commutation time and the corresponding ZVS conditions of each switch are presented in Table I, where $I_p = I_P/I_N$, $I_s = I_S/I_N$, and $I_N = V_1/(4f_sL)$. According to the symmetry of the DAB operations, S_1, S_4, Q_1, and Q_4 are selected as the analysis objects. As only the ZVS-ON can be realized in the DAB converter, the following ZVS all refer to the ZVS-ON. Since the ZVS condition is closely related to the control modes, the PCS is described first, and the calculation of the ZVS-currents is analyzed subsequently.

B. Operation Modes Under the Buck-Type Voltage Gain Case

a) **Mode I:** Fig. 3(a) corresponds to the starting of mode I, where t_{PX}, t_{SX} and $I(t_{PX})$, $I(t_{SX})$ represent the switching time and switching current of switch X in the transformer's

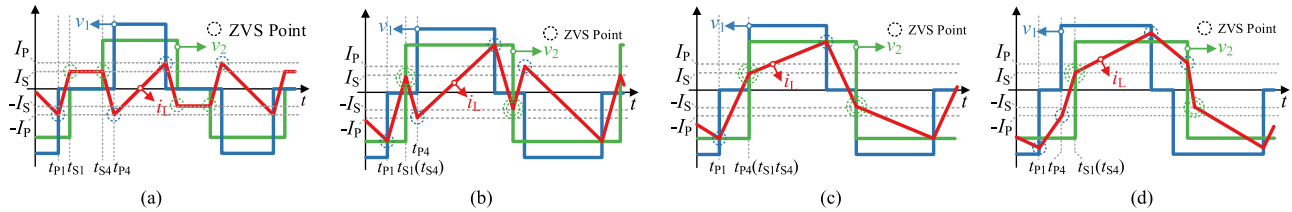

Fig. 3. Operating modes under the buck-type operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

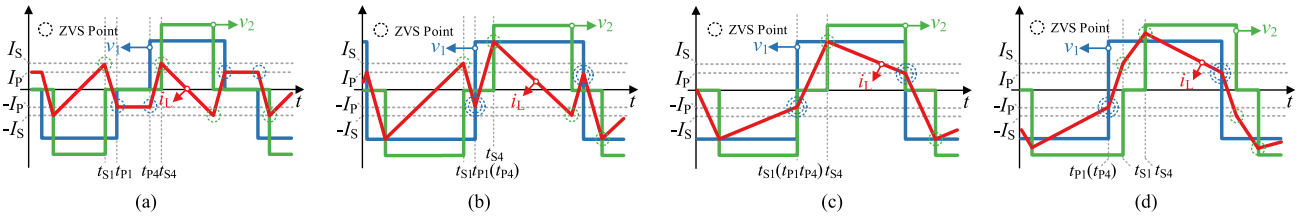

Fig. 4. Operating modes under the boost-type operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

TABLE I
PER UNIT INDUCTOR CURRENT EXPRESSIONS OF ALL MODES AND THE ZVS CONDITIONS OF EACH SWITCH

Mode Classification	$i_L(t_{P1})$	$i_L(t_{P4})$	$i_L(t_{S1})$	$i_L(t_{S4})$
Buck-type, Modes I, II	$(2M-1)D_1-MD_2-2MD_3$	$-D_1+MD_2+2MD_3$	$-D_1+MD_2$	$-D_1+MD_2$
Buck-type, Modes III, IV	$(2M-1)D_1-MD_2-2MD_3$	$-D_1-MD_2-2MD_3+2M$	$-D_1+MD_2+2D_3$	$-D_1+MD_2+2D_3$
Boost-type, Modes I, II	$-D_1+MD_2$	$-D_1+MD_2$	$D_1+(M-2)D_2-2D_3$	$-D_1+MD_2+2D_3$
Boost-type, Modes III, IV	$(2M-1)D_1-MD_2-2MD_3$	$(2M-1)D_1-MD_2-2MD_3$	$-D_1+MD_2+2D_3$	$-D_1+MD_2+2D_3$
ZVS Conditions	S_1 turns on: $i_L(t_{P1})<-I_p<0$	S_4 turns on: $i_L(t_{P4})<-I_p<0$	Q_1 turns on: $i_L(t_{S1})>I_s>0$	Q_4 turns on: $i_L(t_{S4})>I_s>0$

the primary and secondary sides, respectively. The peak current occurs at the t_{P1} instant, and the ZVS operation can be naturally achieved in S_1 with processed power being increased. To achieve an all-ZVS operation and maintain a low rms current at light load, the following constraints should be fulfilled:

$$\begin{cases} I(t_{P1}) \leqslant -I_P \\ I(t_{P4}) = -I_P \\ I(t_{S1}) = I(t_{S4}) = I_S. \end{cases} \tag{1}$$

Combining (1) with the current expressions in Table I, each optimal phase shift angle can be expressed as follows:

$$\begin{cases} D_1 = \dfrac{2M\Phi + I_p}{1-M}, \Phi \propto P^* \\ D_2 = \dfrac{D_1 + I_s}{M} = \dfrac{2M\Phi + I_p + I_s(1-M)}{M(1-M)} \\ D_3 = \dfrac{-(I_p + I_s)}{2M} \end{cases} \tag{2}$$

where $P* = P/P_N$ and $P_N = nV_1V_2/(8f_sL)$. In mode I, the system operates under TPS control. As Φ increases with P^*, $D_2 = 1$ and the system operation enters the EPS control and changes to mode II.

b) **Mode II:** Fig. 3(b) corresponds to the starting of mode II. Due to the increase of Φ, t_{P4} and t_{S1} are bound to overlap. Due to the reduction of switching current, the ZVS conditions of S_4 can be lost, thus the all-ZVS operation cannot be realized when t_{P4} overlaps with t_{S1}. The following system operation can be categorized into four cases.

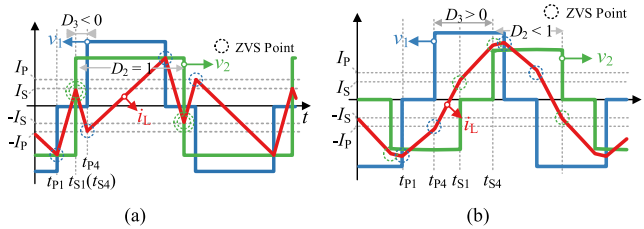

Fig. 5. Waveforms of all-ZVS case. (a) Waveform of the staring of mode II. (b) All-ZVS case with unsmooth change in D_2 and D_3.

1) All-ZVS case. Only when t_{P4} lags t_{S1} for a sufficient time so that the change of inductor current is greater than $(I_P + I_S)$, the all-ZVS operation can be maintained. As shown in Fig. 5(b), an all-ZVS operation is realized but an abrupt change occurs in D_2 and D_3. The peak inductor current will suddenly change with the phase shift angles, enlarging the switching-OFF and passive components' losses. In the high-frequency operations, serious electromagnetic interference (EMI) might be brought by the current abruption, which could transmit to the switch drive loop through the common-mode loop and result in the system missing protection and the damage of the complementary switches due to the crosstalk. Therefore, the all-ZVS case is not considered.
2) Two-ZVS case. During the switching transition, the absolute values of $I(t_{S1})$ and $I(t_{P4})$ can be reduced synchronously, and when t_{P4} overlaps with t_{S1}, $I(t_{S1}) = I(t_{P4})$

$= 0$ [28], [29]. In such a case, the ZVS operation can only be realized in two switches, i.e., S_1 and S_3. Although ZCS operation is achieved in the other six switches, the switching-on loss cannot be fully eliminated, as the energy stored in C_{ossx} cannot be fully released before switches turning-ON.

3) Four-ZVS case. Maintaining $I(t_{P4}) = -I_P$ and decreasing $I(t_{S1})$, when t_{P4} overlaps with t_{S1}, $I(t_{S1}) = I(t_{P4}) = -I_P$ can be achieved. The ZVS operation can be attained in all primary side switches, whereas the ZVS in all secondary side switches is lost.
4) Six-ZVS case. Maintaining $I(t_{S1}) = I_S$ and increasing $I(t_{P4})$, when t_{P4} overlaps with t_{S1}, $I(t_{S1}) = I(t_{P4}) = I_S$ can be achieved. The ZVS operation can be attained in all secondary side switches. In the primary side, the ZVS operation can be naturally achieved in S_1 and S_3, which are switching-ON at the peak current time. Thus, considering the advantages of a seamless mode transition and the achievable ZVS range, the six-ZVS case is selected in this work as the most promising operating case for mode II. The phase shift angles can be expressed as follows:

$$\begin{cases} D_1 = M - I_s, D_2 = 1 \\ D_3 = \Phi - \dfrac{1 - M + I_s}{2}, \Phi \propto P^*. \end{cases} \tag{3}$$

With the increase of Φ, t_{P4} would overlap with t_{S1}, i.e., $D_3 = 0$ and the system operation changes to mode III.

c) **Mode III:** Fig. 3(c) corresponds to the starting of mode III, where $I(t_{S1}) = I_S$ is still maintained to keep six-ZVS transition and low rms current. Meanwhile, $I(t_{P4})$ is gradually decreased to $-I_P$ for reaching an all-ZVS state. Each phase shift angle can be expressed as follows:

$$\begin{cases} D_1 = 2D_3 + M - I_s, D_3 \propto P^* \\ D_2 = 1, \Phi = \dfrac{1 - M + B}{2}. \end{cases} \tag{4}$$

Generally speaking, the shape of the inductor current would be changed with the increment of the processed power, so that the all-ZVS operation could be naturally achieved at heavy load [20]. Thus, at heavy load, the optimization of the rms current is analyzed first, and then a smooth transition between mode III and an optimal inductor rms current algorithm is analyzed next.

Combined with the current expression of mode III, the square value of the inductor rms current can be expressed as follows:

$$\begin{aligned} i^2_{LRMS}(D_1, \Phi) &= M - 2D_1^3 - 6D_1^2 M\Phi + 3D_1^2 M + 3D_1^2 \\ &+12D_1 M\Phi - 6D_1 M + M^2 - 8M\Phi^3 + 12M\Phi^2 - 6M\Phi. \end{aligned} \tag{5}$$

The Lagrange multiplier method is suitable for solving such an optimization problem, by which the cost function can be translated into the following form:

$$F(D_1, \Phi, \lambda) = i^2_{LRMS}(D_1, \Phi) + \lambda (P - P^*) \tag{6}$$

where $F(D_1, \Phi, \lambda)$ is the Lagrange function, combined with the following constraints:

$$\frac{\partial F(D_1, \Phi, \lambda)}{\partial D_1} = \frac{\partial F(D_1, \Phi, \lambda)}{\partial \Phi} = \frac{\partial F(D_1, \Phi, \lambda)}{\partial \lambda} = 0. \tag{7}$$

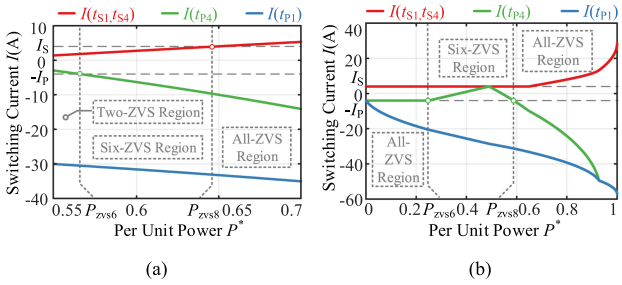

Fig. 6. Switching currents of switches under the buck-type operation. (a) Currents of optimal rms current algorithm when $V_1 = 320$ V, $V_2 = 160$ V, $n = 1, f_s = 100$ kHz, $L = 14$ μH, $I_S = I_P = 4$ A. (b) Switching currents of PCS under the same condition.

The phase shift angles solved for the optimal inductor rms current can be written as follows:

$$\begin{cases} D_1 = \dfrac{M + 2\Phi - 1 + \Phi_x}{M}, \Phi \propto P^* \\ \Phi_x = \sqrt{(2\Phi - 1 + M)^2 + M^2(2\Phi - 1)^2}. \end{cases} \tag{8}$$

Combined with the current expression in Table I, the switching current of each active semiconductor can be obtained, as depicted in Fig. 6(a).

The P_{zvs6} and P_{zvs8} correspond to the minimum power points of the system, where six-ZVS operation and all-ZVS operation can be just achieved, respectively. When

$$D_3 = \frac{I_s M + I_s - M^2 + \sqrt{I_s + M^2(I_s - M)^2}}{2M} \tag{9}$$

is satisfied, $P* = P_{zvs8}$ can be achieved. Thus, when (9) is true, the system switches to the optimal rms current algorithm and enters mode IV.

d) **Mode IV:** Fig. 3(d) corresponds to the starting of mode IV. According to (8), to ensure the optimal rms current and all-ZVS operation, the phase shift angle can be written as follows:

$$\begin{cases} D_1 = \dfrac{M + 2\Phi - 1 + \Phi_x}{M}, \Phi \propto P^* \\ D_2 = 1, D_3 = \dfrac{\Phi(2 + 2M) - 1 + \Phi_x}{2M} \\ \Phi_x = \sqrt{(2\Phi - 1 + M)^2 + M^2(2\Phi - 1)^2}. \end{cases} \tag{10}$$

With the processed power increasing, $D_1 = 1$ and the system enters the SPS control.

The switching current of each active semiconductor is shown in Fig. 6(b). In mode I, due to $I(t_{S1}, t_{S4}) = I_S$ and $I(t_{P4}) = -I_P$, the all-ZVS operation is achieved and the extra backflow power is limited. In modes II and III, although the all-ZVS operation cannot be achieved, $I(t_{S1}, t_{S4}) = I_S$ is still set to optimize the inductor rms current. In mode IV, the system transitions to an optimal inductor rms current algorithm, and the ZVS-state is back to an all-ZVS state. In general, all the switching current of each active semiconductor changes smoothly and at least six switches could realize ZVS in the full power range.

TABLE II
PHASE SHIFT ANGLES IN EACH OPERATING MODE UNDER BOOST-TYPE CASE

Mode classification	Phase shift angles		Figure
Mode I	$D_1=\frac{2M\Phi+I_sM}{M-1}+I_p, \Phi\propto P^*$ $D_2=\frac{D_1-I_p}{M}=\frac{2\Phi+I_s}{M-1}$ $D_3=2\Phi+\frac{I_p+I_s}{2}$	(11)	Fig. 4(a)
Mode II	$D_1=1, D_2=\frac{1-I_p}{M}$ $D_3=\frac{2M\Phi+M-1+I_p}{2M}, \Phi\propto P^*$	(12)	Fig. 4(b)
Mode III	$D_1=1, \Phi=\frac{M-1+I_p}{2M}$ $D_2=\frac{2M(1-D_3)-1+I_p}{M}$ $D_3\propto P^*$	(13)	Fig. 4(c)
Mode IV	$D_1=1, \Phi\propto P^*$ $D_2=1+M(2\Phi-1)+\Phi_y$ $D_3=\frac{1+(1-M)(2\Phi-1)-\Phi_y}{2}$ $\Phi_y=\sqrt{(M(2\Phi-1)+1)^2+(2\Phi-1)^2}$	(14)	Fig. 4(d)

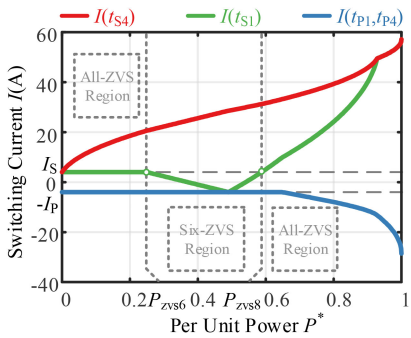

Fig. 7. Switching current under boost-type operation when $V_1 = 160$ V, $V_2 = 320$ V, $n = 1, f_s = 100$ kHz, $L = 14$ μH, $I_S = I_P = 4$ A.

C. Operation Modes Under the Boost-Type Voltage Gain Case

As the operation symmetry of the DAB converter, under the boost-type case, the circuit behaves similarly to the buck-type case described previously. The phase shift angles for this operating case are summarized in Table II.

As shown in Fig. 7, under the boost-type operation, all the switching currents also change smoothly and all-ZVS operation can be achieved at light and heavy loads, whereas the six-ZVS operation can be realized at medium load.

Compared with Fig. 6(b), the change of switching currents under boost-type operation is symmetry to the buck-type operation. In general, an all-ZVS operation can be realized in the switches of the lower level voltage side, and the ZVS operation can be naturally achieved in the switches that are turning-ON at the peak current instant in the higher level voltage side.

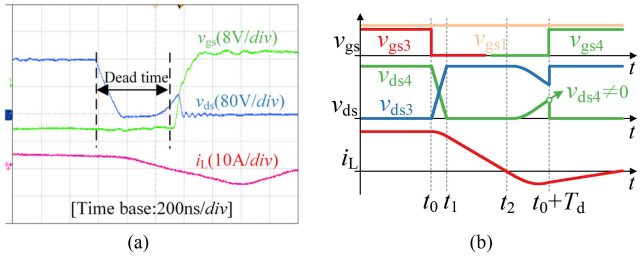

Fig. 8. Hard-switching ON caused by an unnecessary long dead time. (a) Experimental results. (b) Theory results.

III. SOLUTION FOR THE DYNAMIC ZVS-CURRENT

The main DAB converter operation modes have been introduced in Section II, where computation of the ZVS-currents I_P and I_S are crucial to the ZVS realization. Considering that the realization of ZVS would be affected by dead time, capacitor voltage, and other electric parameters, the ZVS-currents would be analyzed and solved in the following section from multiple perspectives.

A. Analysis of the ZVS Process

From the traditional energy-based perspective, during the dead time, the energy stored in the inductor should be large enough to fully release the energy stored across the semiconductors' parasitic capacitance C_{oss}. The basic relationship is shown as follows:

$$\frac{1}{2}LI_L^2 \geqslant C_{oss}V_{DS} \tag{15}$$

where V_{DS} represents the drain–source voltage across the switch. Note that in (15), the dead time influence is not considered. Even if the inductance current is large enough, the energy of C_{oss} may be fully released during a short dead time. Based on the charge-exchange perspective, the charge stored in C_{oss} should be completely released within the dead time, written as follows:

$$\int_0^{T_d} I(t)\,dt \geqslant 2Q_{oss} = 2C_{oss}V_{DS} \tag{16}$$

where T_d stands for the dead time and Q_{oss} represents the charge stored in C_{oss}. C_{oss} is negatively correlated with V_{DS} and can be fitted from the switch datasheet. Note that although condition (16) can be satisfied with a long T_d, the realization of ZVS could be lost, as illustrated in Fig. 8.

In Fig. 8(a), the experimental result shows that the realization of ZVS is lost by the unnecessary long dead time. Furthermore, Fig. 8(b) illustrates the theory result of such phenomenon more clearly. After the interval $[t_0$–$t_1]$, ZVS operation could have been fully achieved if the switching transition of S_4 had occurred within the interval t_1–t_2, because in this case the antiparallel diode is conducting the impressed current. After t_2, the inductor current reverses polarity and the antiparallel diode stop conducting current. Thus, the impressed current starts to charge the C_{oss} of S_4 and discharge the C_{oss} of S_3. When S_4 is turned ON, $V_{DS4} > 0$ and the ZVS operation is lost. To avoid the loss of ZVS, the

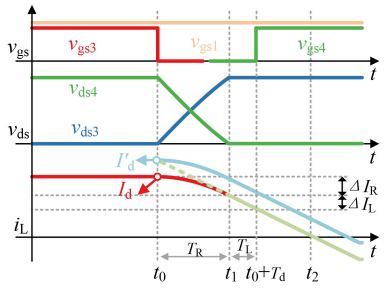

Fig. 9. Waveform of the simplified current variation within the dead time.

following condition must be satisfied:

$$\begin{cases} I_{\mathrm{L}}(t_0+T_{\mathrm{d}}) = I_{\mathrm{L}}(t_0) + \Delta I_{\mathrm{R}} + \Delta I_{\mathrm{L}} \geqslant 0, I_{\mathrm{L}}(t_0) > 0 \\ I_{\mathrm{L}}(t_0+T_{\mathrm{d}}) = I_{\mathrm{L}}(t_0) + \Delta I_{\mathrm{R}} + \Delta I_{\mathrm{L}} \leqslant 0, I_{\mathrm{L}}(t_0) < 0 \end{cases} \tag{17}$$

where ΔI_{R} and ΔI_{L} are the resonant value and linear value of inductor current during the dead time, respectively.

B. Analysis of the Dynamic ZVS-Current

In the resonance process, the resonant value of the inductor current can be written as follows [30]:

$$\Delta I_{\mathrm{R}} = 2I_{\mathrm{L}}(t_0)\sin\left(\frac{\omega T_{\mathrm{R}}}{2}\right)^2 + \frac{V_{\mathrm{L}}}{L\omega}\sin(\omega T_{\mathrm{R}}) \tag{18}$$

where $\omega = 1/(C_{\mathrm{oss}}L)^{1/2}$. V_{L} represents the inductor voltage and T_{R} denotes the resonance time. The product ωT_{R} is a minimum value due to the short resonance time T_{R}. Therefore, (18) can be simplified as follows:

$$\Delta I_{\mathrm{R}} \approx \frac{(\omega T_{\mathrm{R}})^2}{2} I_{\mathrm{L}}(t_0) + \frac{V_{\mathrm{L}}}{L} T_{\mathrm{R}} \approx \frac{V_{\mathrm{L}}}{L} T_{\mathrm{R}}. \tag{19}$$

As shown in Fig. 9, T_{L} denotes the linearly change time and $T_{\mathrm{L}} = T_{\mathrm{d}}$–$T_{\mathrm{R}}$. As can be seen, the sinusoidal change of the inductor i_{L} occurs in the resonance process, whose max change rate appears at the end of the resonance time t_1. Therefore, the current variation in the dead time process can be fully linearized, by which the absolute value of linearized current $I_{\mathrm{d}}{}'$ is always greater than $|I_{\mathrm{d}}|$. Similarly, the same results can be obtained in other switching states.

In practical, the large C_{oss} variation will lead to the nonlinear changes in inductor current and capacitor voltage of the switch, which is hard to estimate accurately. Once the dead time is unreasonable, the ZVS operation will be lost and the switching-on loss cannot be eliminated. However, the linearization hypothesis adopted in this article can not only simplify the analysis but also increase the margin of the ZVS operation, by which the influence of the large variation in the capacitor C_{oss} can be buffered.

Based on the above analysis, combined with (16) and (17), the ZVS-currents can be calculated as follows:

$$\begin{cases} I_{\mathrm{L}}(t_0) \geqslant \max\left(I_{\mathrm{Q}} : \frac{2Q_{\mathrm{oss}}}{T_{\mathrm{d}}} - \frac{V_{\mathrm{L}}T_{\mathrm{d}}}{2L}, I_{\mathrm{DT}} : -\frac{V_{\mathrm{L}}T_{\mathrm{d}}}{L}\right), \\ \quad I_{\mathrm{L}}(t_0) \geqslant 0 \\ I_{\mathrm{L}}(t_0) \leqslant \min\left(I_{\mathrm{Q}} : -\frac{2Q_{\mathrm{oss}}}{T_{\mathrm{d}}} - \frac{V_{\mathrm{L}}T_{\mathrm{d}}}{2L}, I_{\mathrm{DT}} : -\frac{V_{\mathrm{L}}T_{\mathrm{d}}}{L}\right), \\ \quad I_{\mathrm{L}}(t_0) \leqslant 0 \end{cases} \tag{20}$$

where I_{Q} and I_{DT} denote the ZVS-currents calculated from the charge-based perspective (16) and the dead time (17), respectively. Table III presents the inductance voltage V_{L} when each switch turns ON. Combined with (20), the ZVS-current required by each switch in all modes can be obtained. If various ZVS-currents are adopted in different modes, according to (2) and (3), the control variables would be changed discontinuously, bringing the risk of control instability. For the smooth transition, the ZVS-currents of all DAB switches should be calculated as follows:

$$\begin{cases} I_{\mathrm{Px}} = -\min\{I_{\mathrm{Px\_I}}, I_{\mathrm{Px\_II}}, I_{\mathrm{Px\_III}}, I_{\mathrm{Px\_IV}}\}, X = 1,4 \\ I_{\mathrm{Sx}} = \max\{I_{\mathrm{Sx\_I}}, I_{\mathrm{Sx\_II}}, I_{\mathrm{Sx\_III}}, I_{\mathrm{Sx\_IV}}\}, X = 1,4 \\ I_{\mathrm{P}} = -\min\{I_{\mathrm{P1}}, I_{\mathrm{P4}}\} \\ I_{\mathrm{S}} = \max\{I_{\mathrm{S1}}, I_{\mathrm{S4}}\} \end{cases} \tag{21}$$

where I_{PX} and I_{SX} represent the ZVS-current corresponding to the switch X in the primary and secondary side, respectively, by which the ZVS conditions of switch in modes I–IV could be satisfied simultaneously. Combined with (21) and Table II, the ZVS-current under the buck- and boost-type operations can be calculated as follows:

$$\begin{cases} I_{\mathrm{P}} = -\min\left\{-\frac{2Q_{\mathrm{oss1}}}{T_{\mathrm{d1}}} - \frac{(V_1+nV_2)T_{\mathrm{d1}}}{2L}, -\frac{(V_1+nV_2)T_{\mathrm{d1}}}{L}\right\} \\ I_{\mathrm{S}} = \max\left\{\frac{2Q_{\mathrm{oss2}}}{T_{\mathrm{d2}}} + \frac{nV_2T_{\mathrm{d2}}}{2L}, \frac{nV_2T_{\mathrm{d2}}}{L}\right\} \text{ buck-type case} \end{cases} \tag{22}$$

$$\begin{cases} I_{\mathrm{P}} = -\min\left\{-\frac{2Q_{\mathrm{oss1}}}{T_{\mathrm{d1}}} - \frac{(V_1+nV_2)T_{\mathrm{d1}}}{2L}, -\frac{(V_1+nV_2)T_{\mathrm{d1}}}{L}\right\} \\ I_{\mathrm{S1}} = \max\left\{\frac{2Q_{\mathrm{oss2}}}{T_{\mathrm{d2}}} + \frac{V_1T_{\mathrm{d2}}}{2L}, \frac{V_1T_{\mathrm{d2}}}{L}\right\} \\ I_{\mathrm{S4}} = \max\left\{\frac{2Q_{\mathrm{oss2}}}{T_{\mathrm{d2}}} + \frac{(nV_2-V_1)T_{\mathrm{d2}}}{2L}, \frac{(nV_2-V_1)T_{\mathrm{d2}}}{L}\right\} \\ \begin{cases} I_{\mathrm{S}} = I_{\mathrm{S1}}, 1 < M < 2 \\ I_{\mathrm{S}} = I_{\mathrm{S4}}, M > 2 \end{cases} \text{ boost-type case.} \end{cases} \tag{23}$$

According to (22) and (23), the realization of ZVS is sensitive to the input and output voltages. The EV chargers often operate in CC charging mode, where the output voltage would change with the SOC. When the output voltage is charged from a low to a high level, the ZVS operation could fail if the ZVS-currents are kept constant. Therefore, the dynamic adjusting ability of the ZVS-currents is necessary for the realization of ZVS under various operation conditions.

Combined with (22) and (23), the changes of the ZVS-currents in various input and output voltage conditions are shown in Fig. 10. Q_{oss} is curve-fitted from the datasheet of IMZ120R030M1H and is found to be $Q_{\mathrm{oss}} = (102.42V_{\mathrm{DS}} + 17125) \times 10^{-12}$. As shown in Fig. 10(a) and (b), no abrupt change occurs in I_{PDT}, I_{SDT}, I_{PQ}, and I_{SQ}, so I_{P} and I_{S} can be changed smoothly, as shown in Fig. 10(c) and (d). Combined with the smooth change characteristics of the proposed ZVS-currents and

TABLE III
INDUCTOR VOLTAGE CORRESPONDING TO EACH SWITCHING MOMENT OF ALL MODES

Operating condition	Classification	Mode I	Mode II	Mode III	Mode IV
Buck-type operation	V_L when S_1 turns on	nV_2	nV_2	nV_2	nV_2
	V_L when S_4 turns on	$V_1 - nV_2$	$V_1 - nV_2$	$V_1 + nV_2$	$V_1 + nV_2$
	V_L when Q_1 turns on	0	$-nV_2$	$V_1 - nV_2$	$V_1 - nV_2$
	V_L when Q_4 turns on	$-nV_2$	$-nV_2$	$V_1 - nV_2$	$V_1 - nV_2$
Boost-type operation	V_L when S_1 turns on	0	V_1	$V_1 + nV_2$	$V_1 + nV_2$
	V_L when S_4 turns on	V_1	V_1	$V_1 + nV_2$	$V_1 + nV_2$
	V_L when Q_1 turns on	$-V_1$	$-V_1$	V_1	V_1
	V_L when Q_4 turns on	$V_1 - nV_2$	$V_1 - nV_2$	$V_1 - nV_2$	$V_1 - nV_2$

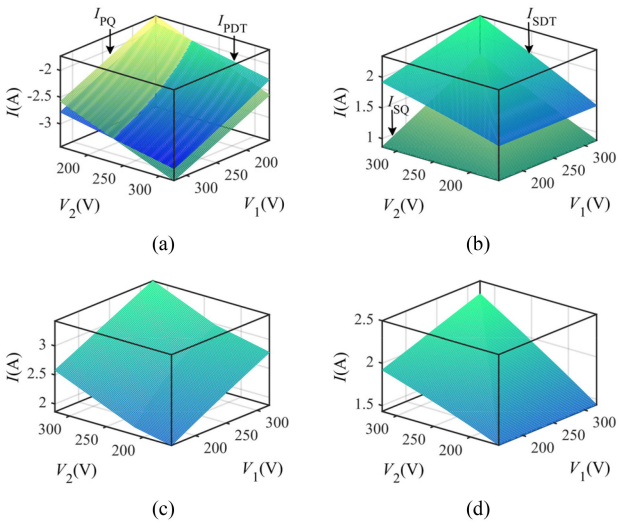

Fig. 10. ZVS-currents in V_1 and $V_2 = [160\text{ V}, 320\text{ V}]$, $L = 14\ \mu$H, $T_{d1} = T_{d2} = 75$ ns. (a) I_{PDT} and I_{PQ}. (b) I_{SDT} and I_{SQ}. (c) I_P. (d) I_S.

simple calculation process, the dynamic adjustment of the ZVS-currents can be realized in a real-time control. Furthermore, as the ZVS process is unchanged with the types of the switches, the proposed calculation methods of the ZVS-currents are still applicable even if different SiC MOSFETs, Si Super Junction MOSFETs, or GaN HEMT transistors are employed in the primary and secondary sides. The only influence is the variation trends of the ZVS-currents are diverse with different types of switches.

In general, the ZVS condition of any switch in any mode can be satisfied by the ZVS-currents proposed in this article. Compared with the dead time control method discussed in [30], the proposed algorithm is simpler to be calculated and convenient for real-time control. Meanwhile, the linear hypothesis of (19) increases a certain margin of ZVS and reduces the sensitivity to parasitic circuit parameters. The ZVS-current control algorithm with a fixed dead time presented in [28] and [29] has limitations in the ZVS operation because the computation of the ZVS-currents only considers the energy- or charge-based perspectives. The ZVS-currents of PCS are calculated from multiple perspectives and can be dynamically adjusted to realize the ZVS operation under a wide voltage range, which is suitable for EV chargers operating in CC charging mode and should lead to a higher operational power efficiency.

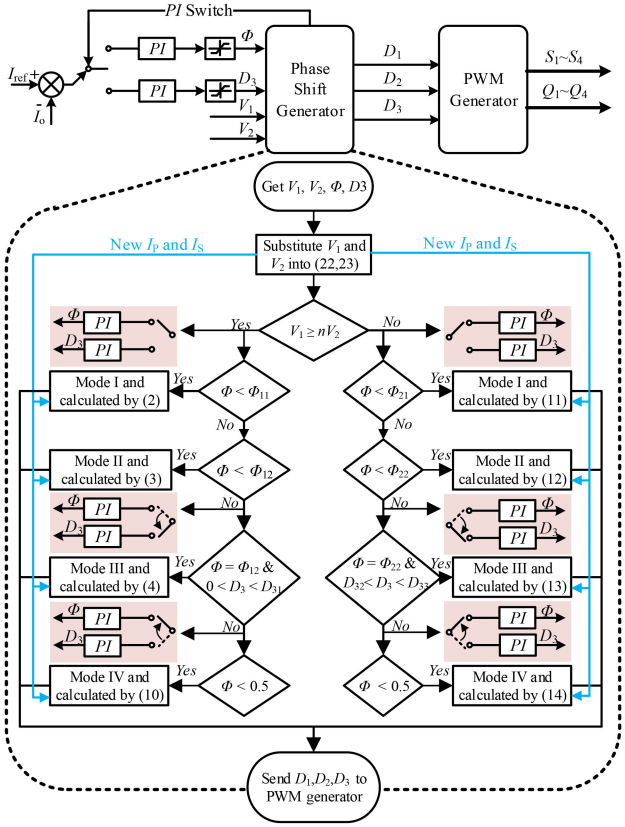

Fig. 11. Control loop of the system with the PCS.

IV. DESIGN OF THE SYSTEM CONTROL LOOP AND ANALYSIS OF THE SYSTEM OPERATIONAL CHARACTERISTICS

A. Design of the System Control Loop

A suitable system control loop for the DAB converter operating with the PCS is shown in Fig. 11. In modes I, II, IV, Φ is chosen as the output of the propotional-integral (PI) controller. In mode III, D_3 is switched as the PI output and Φ is kept constant. The boundary values of each mode are summarized in Table IV, by which the modes can be switched from mode I to mode IV, and seamless transition of all modes can be realized.

B. Analysis of the ZVS Range and Inductor RMS Current

Fig. 12 compares the ZVS range of the PCS and the GOC in [20], the seamless TPS (STPS) in [28], and the wide-ZVS TPS (ZTPS) in [29]. The operating conditions are consistent

TABLE IV
BOUNDARY VALUES OF Φ AND D_3 IN EACH MODE

	Boundary value
Buck-type Condition	$\Phi_{11}=\dfrac{(M-I_s)(1-M)-I_p}{2M}, \Phi_{12}=\dfrac{1-M+I_s}{2}$
	$D_{31}=\dfrac{I_sM+I_s-M^2+\sqrt{I_s^2+M^2(I_s-M)^2}}{2M}$
Boost-type Condition	$\Phi_{21}=\dfrac{(M-1)(1-I_p)-I_sM}{2M}$
	$\Phi_{22}=\dfrac{M-1+I_p}{2M}, D_{32}=\dfrac{M-1+I_p}{M}$
	$D_{33}=\dfrac{2M-1+(1-M)I_p-\sqrt{I_p^2M^2+(I_p-1)^2}}{2M}$

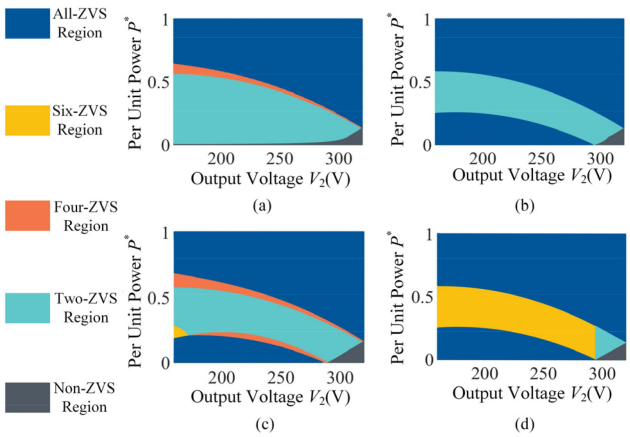

Fig. 12. ZVS region comparison among [20], [28], [29] and PCS under buck-type operation. (a) GOC [20]. (b) STPS [28]. (c) ZTPS [29]. (d) PCS.

with Fig. 6. In [20], Tong *et al.* propose the GOC algorithm to optimize the inductor rms current. As the ZVS-current is assumed to be zero, Tong *et al.* [20] own the optimal inductor rms current, but unfortunately obtain the worst ZVS range. Guo [28] and Yan *et al.* [29] consider the valid implementation of ZVS at light load. But at medium load, the ZVS operation can only be realized in the two switches, which turn ON at the peak current point. Evidently, in most voltage ranges, all-ZVS operation at light and heavy loads can be realized in the PCS, and at medium load six-ZVS operation can be achieved. Therefore, the PCS has a maximized ZVS range, by which the switching-on loss of the switches can be effectively eliminated and system stability can be reinforced in the full operating range. Furthermore, the dynamic adjusting of the ZVS-current in the PCS could safeguard the realization of ZVS operation under the various operating conditions, by which the maximized ZVS range characteristics can be maintained. As the optimization of ZVS cannot be realized under the SPS, the non-ZVS region only occurs at light load under the SPS, where M is close to 1.

The inductor rms currents obtained with the SPS, GOC, and PCS are compared in Fig. 13. As the realization of ZVS would bring additional backflow power, the rms current of PCS is slightly higher than that of GOC at light load, as shown in

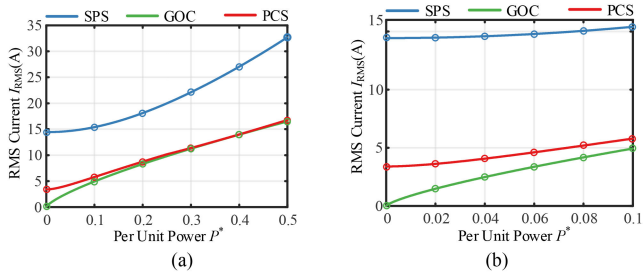

Fig. 13. Benchmark of rms value across the inductor current. (a) Power range of 0–0.5. (b) Power range of 0–0.1.

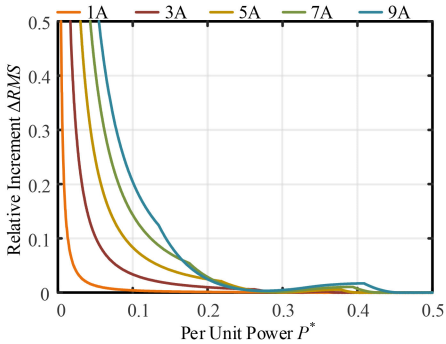

Fig. 14. ΔRMS of different critical ZVS-current of the PCS versus GOC.

Fig. 13(b). However, with a higher processed power, the rms current of PCS tends to converge to the one achieved with GOC.

Fig. 14 shows the relative increment of rms current between PCS and GOC from $I_P = I_S = 1$ A to 9 A and $\Delta\text{RMS} = (I_{\text{RMS·Proposed}} - I_{\text{RMS·GOC}})/I_{\text{RMS·GOC}}$. Although ΔRMS is positively correlated with the ZVS-current, ΔRMS remains below 5% in most power range. Only in extreme light load condition, ΔRMS is relatively high but the corresponding power range is so small that can be ignored. Therefore, the wide ZVS range and quasi-optimal rms current in full power range can be realized by the PCS.

C. Seamless Transition of the Control

Fig. 15 shows the change of phase shift angles under the full power range and a wide operational voltage gain. Although the ZVS-current varies with the changes in the input and output voltages, the process is so smooth that it will not disrupt the seamless transition of the control variables.

Fig. 16 shows the changes of all phase shift angles under specific conditions. As can be seen, all control variables change smoothly and the changes of Φ are completely consistent. Under the buck or boost-type operations, $V_1 = 320/160$ V and $V_2 = 160/320$ V, the exchange of V_1 and V_2 leads to the exchange of D_2 and D_1 but the change process is completely the same. Thus, the PCS is symmetric and matched with the bidirectional and symmetrical operation characteristics of the DAB.

Fig. 17 shows the power section of all modes. Each line represents the maximum power under the corresponding mode. As can be seen, the power range of each mode is completely

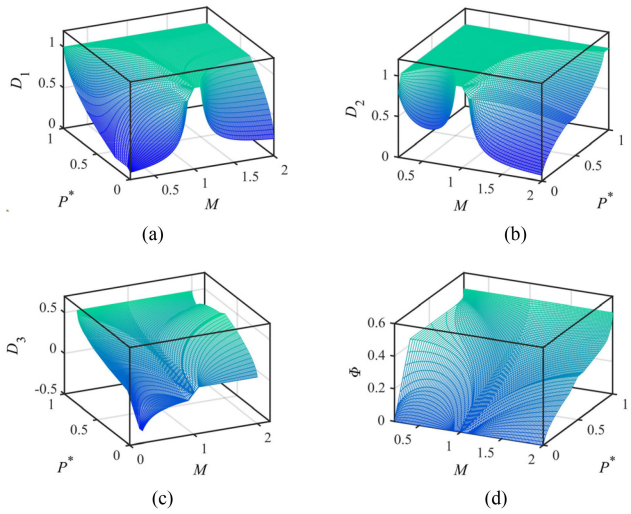

Fig. 15. Seamless change of all phase shift angles in the full power and operational gain. (a) D_1. (b) D_2. (c) D_3. (d) Φ.

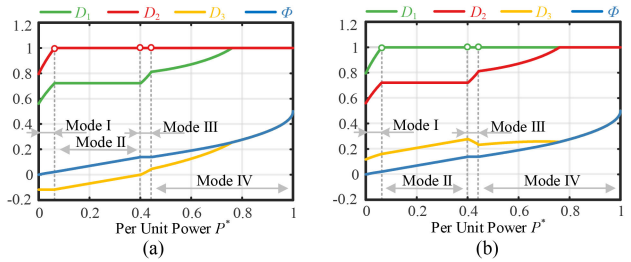

Fig. 16. Phase shift angle variations in the full power range. (a) Buck-type operation $V_1 = 320$ V and $V_2 = 160$ V. (b) Boost-type operation $V_1 = 160$ V and $V_2 = 320$ V.

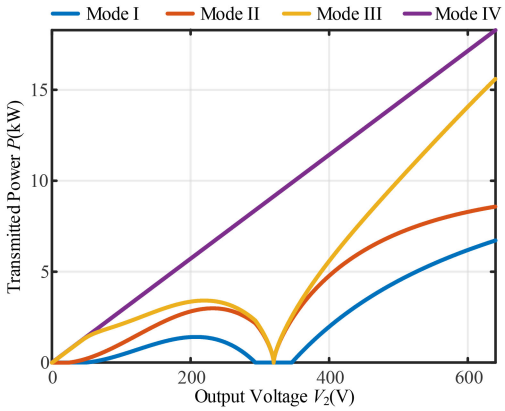

Fig. 17. Power segments over a wide voltage range.

continuous without any overlaps, which ensures the system stability.

V. Experimental Verification

To substantiate the validity of the theoretical analysis, a 4.5 kW/100 kHz SiC-based DAB prototype is built, as shown in Fig. 18. All the magnetic devices are buried in the liquid-cooled box for achieving a better heat dissipation.

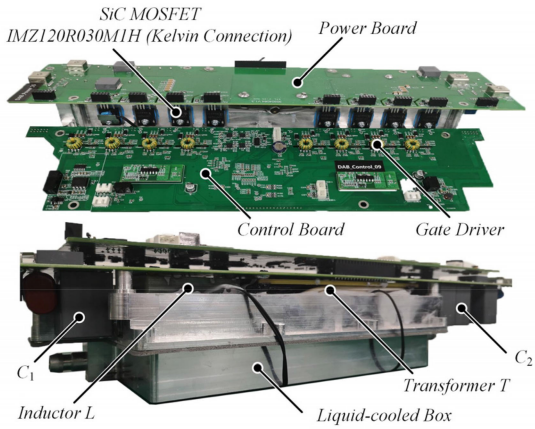

Fig. 18. 4.5 kW/100 kHz SiC-based DAB prototype.

TABLE V
Key Components and Specifications of the DAB Converter Prototype

Items	Parameter
Input voltage V_1	160 V–320 V
Output voltage V_2	160 V–390 V
Rated processed power	4.5 kW
Inductor specifications	Inductance L: 14 μH Litz wire: 8 turns, 0.1 mm*750 strands (0.002 Ω) Core: PQ5050, Material: DMR95 (DMEGC)
Transformer specifications	Turns ratio n:1 = 1:1 Pri: 11 turns, litz wire 0.1 mm*100 strands×8 (0.003 Ω) Sec: 22 turns, litz wire 0.1 mm*400 strands×1 (0.013 Ω) Form: two connected in input-series and output-parallel Core: EE65/65/20, Material: 3C95 (DMEGC)
Switches $S_{1\text{-}4}$ and $Q_{1\text{-}4}$	IMZ120R030M1H
SiC MOSFET Driver	Si8286BC
Buffer capacitor	2*470 pF
Controller	STM32G474RET6
Switching frequency f_s	100 kHz
Dead Time T_{d1} and T_{d2}	150 ns

The key system components and specifications are presented in Table V. The ARM chip STM32G474RET6 is selected as the digital controller. Especially, a hi-resolution and complex waveform builder (HRTIM) is integrated in the controller, by which the all pulsewidth modulation waveforms can be accurately generated. The max computation time of the proposed control loop is 7.8 μs as the chip's floating process unit can speed up the floating-point calculations. Notably, the SiC MOSFET IMZ120R030M1H has a small gate charge $Q_g = 63$ nC, which enables a higher switching speed and reduces switching losses. The Kelvin-connection package is utilized in the switch, which advantageously eliminates the effect of package and boards the parasitic elements with the additional source connection. Furthermore, for the same switched current, the switching-ON energy of the SiC MOSFET is often about three to five times greater than the switching-OFF energy, so the efficiency can be further improved by the ZVS operation. Two 470 pF lossless snubber capacitors are paralleled to each switch in the DAB prototype to ease the voltage spike and EMI problem caused by the hard-switching-OFF of the switches.

A. Steady-State Experimental Results

1) Buck-Type Operation: Fig. 19 shows the steady-state waveforms of each mode, where the points encircled by dotted

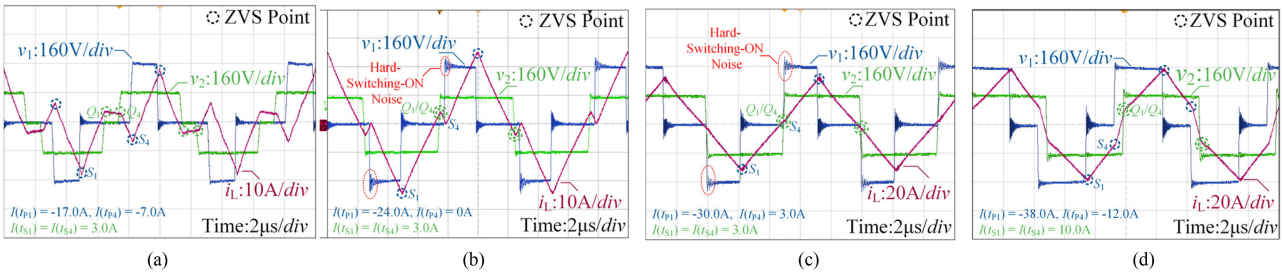

Fig. 19. Waveforms of all modes for $V_1 = 320$ V and $V_2 = 160$ V. (a) Mode I, $P* = 0.1$. (b) Mode II, $P* = 0.4$. (c) Mode III, $P* = 0.5$. (d) Mode IV, $P* = 0.7$.

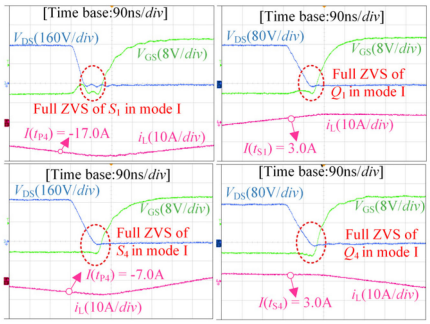

Fig. 20. ZVS waveforms for the switches in mode I under buck-type operation.

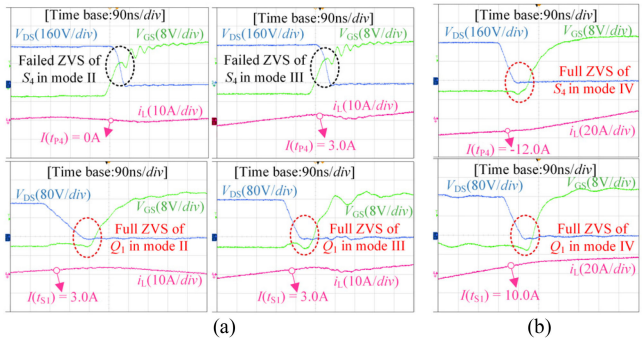

Fig. 21. ZVS waveforms for the switches in modes II–IV under buck-type operation. (a) ZVS states of S_4 and Q_1 in modes II and III. (b) ZVS states of S_4 and Q_1 in mode IV.

line indicate that the ZVS operation is realized in the corresponding switch. According to (22), the ZVS-current under buck-type operation is calculated as $I_P = 6.6$ A, $I_S = 2.9$ A. As shown in Fig. 19(a) the system operates at light load under TPS control. The ZVS waveforms are shown in Fig. 20. all-ZVS operation is achieved and the ZVS-currents of the primary and secondary sides follow closely with I_P and I_S.

As the power increases, the system enters in the EPS control and switches to modes II and III, as shown in Fig. 19(b) and (c). As S_1 is switching at the peak current point and whose ZVS operation has been realized in mode I, the ZVS operation of S_1 could still be achieved with the increase of power. Under the EPS control, the switching current of Q_1 and Q_4 are identical, as Q_1 turns ON with Q_4. Thus, the ZVS states of S_1 and Q_4 are omitted and the ZVS states of S_4 and Q_1 are shown in Fig. 21(a).

As can be seen, the ZVS operation of Q_1 is still realized in modes II and III. This signifies that the ZVS operation can be achieved in all secondary side switches. The realization of ZVS is lost in the switches S_3 and S_4, which results in the hard-switching-ON noises shown in Fig. 19(b) and (c). In modes II and III, the switching current of secondary switches is kept constant at 3.0 A, for realizing ZVS operation and reducing the backflow power simultaneously. In general, the six-ZVS operation can be realized in modes II and III.

As shown in Fig. 19(d), the system operates in mode IV when $P^* = 0.7$ and Q_1 turns ON after S_4. The ZVS states of S_4 and Q_1 are shown in Fig. 21(b). The ZVS operation of S_4 is reimplemented, eliminating the hard-switching-ON noise.

2) Boost-Type Operation: Fig. 22 shows the steady-state waveforms of each operational mode. The ZVS-currents under the boost-type operation change to $I_P = 5.1$ A and $I_S = 4.9$ A. At light load, the system operates under TPS control, as shown in Fig. 22(a). The ZVS states of all switches are shown in Fig. 23, where an all-ZVS operation is realized and the switching current is close to I_P or I_S.

At medium load, the system converts the EPS control and operates in modes II and III, as shown in Fig. 22(b) and (c). The ZVS states of S_4 and Q_1 in modes II and III are shown in Fig. 24(a). To ensure the six-ZVS transition, $I(t_{S1}) = I(t_{P4}) = -I_P = -5.1$ A should be achieved when t_{P4} overlaps with t_{S1}. Thus, the ZVS operation of Q_1 is lost in modes II and III, resulting in a hard-switching-ON noise. The ZVS operations of all the primary side switches are still maintained, as shown in Fig. 24(a).

With the power increased, the system switches to mode IV and the hard-switching-ON noise decreases, as shown in Fig. 22(d). Fig. 24(b) illustrates the ZVS states of S_4 and Q_1 in mode IV at heavy load, where an all-ZVS operation is achieved again. In general, an all-ZVS operation can be realized at light and heavy loads. At medium load, six-ZVS operation can be achieved.

B. Seamless Modes Transition Verification

To simulate the system operation under the CV charging mode of an EV charger, the transitions from mode I to mode IV under buck- and boost-type operations are shown in Figs. 25 and 26, respectively. During the transient process, the output current i_o and inductance current i_L are smoothly regulated, owing to the seamless transition of all modes. The corresponding modes in each subgraph are consistent with Figs. 19 and 22.

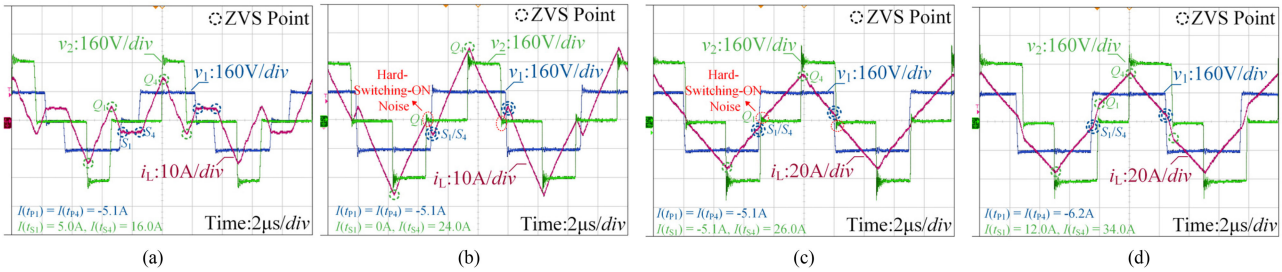

Fig. 22. Waveforms of all modes for $V_1 = 160$ V and $V_2 = 320$ V. (a) Mode I, $P* = 0.1$. (b) Mode II, $P* = 0.4$. (c) Mode III, $P* = 0.5$. (d) Mode IV, $P* = 0.7$.

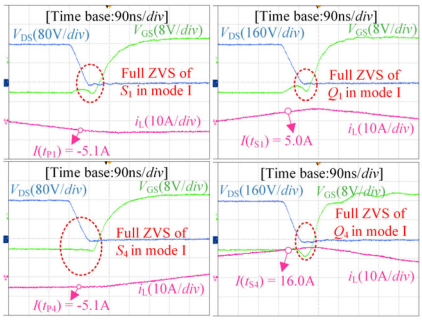

Fig. 23. ZVS waveforms of the switches in mode I under boost-type operation.

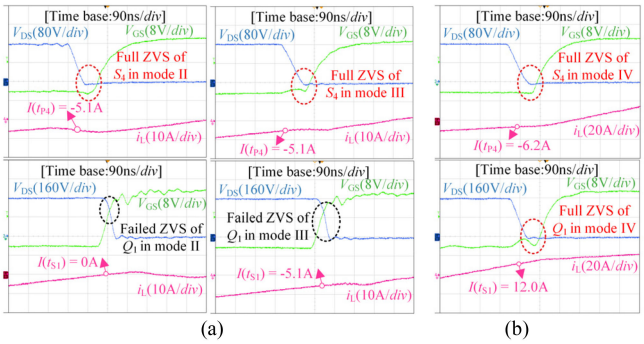

Fig. 24. ZVS waveforms of the switches in modes II–IV under the boost-type operation. (a) ZVS states of S_4 and Q_1 in modes II and III. (b) ZVS states of S_4 and Q_1 in mode IV.

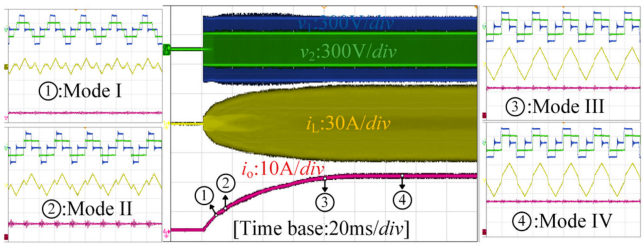

Fig. 25. Modes transition in $V_1 = 320$ V, $V_2 = 160$ V from $P* = 0$ to 0.65.

As can be seen in Fig. 26, since the soft-switching OFF cannot be realized in the DAB system, the hard-switching OFF at the peak current will generate high-frequency oscillation and bring conducted interference to the measurement. Therefore, the output current inevitably contains the certain high-frequency noises, which are not related to the PCS. The ripple rate of the

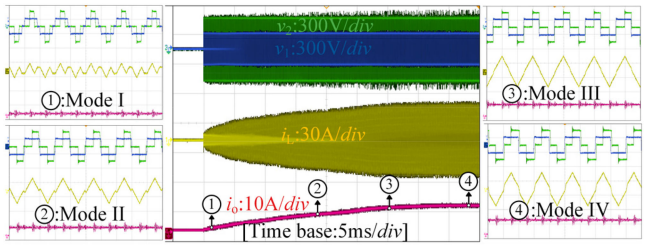

Fig. 26. Modes transition in $V_1 = 160$ V, $V_2 = 320$ V from $P* = 0$ to 0.65.

output current keeps small, as the main ripple component can be filtered by the *CLC* filter circuit in this article. Therefore, the PCS would not deteriorate the rippling property under the buck- or boost-type operations. Conversely, the ripple characteristics are mainly influenced by the hardware parameter design of the *CLC* filter circuit.

C. Dynamic ZVS-Current Verification

To simulate the system operation under CC charging mode of an EV charger, the input voltage $V_1 = 320$ V and the output current $i_o = 5$ A are kept constant during the transient process. The dynamic process is illustrated in Fig. 27.

Fig. 27(a) shows the main operation waveforms of the DAB system operating with CC. At the initial condition that $V_1 = 320$ V and $V_2 = 160$ V, the DAB converter works under the TPS control, where an all-ZVS operation is achieved, as shown in Fig. 27(b).

The output power P_o increases with V_2, and thus when $V_2 = 250$ V, the system switches to mode II and works under the EPS control, where a six-ZVS operation can be realized. The ZVS-current is dynamically changed from $I_P = 6.6$ A, $I_S = 2.98$ A to $I_P = 7.0$ A, $I_S = 4.4$ A. Due to $I(t_{P4}) = -4.5$ A $> -I_P$, the ZVS operation of S_4 cannot be fully achieved. However, the switching current of the secondary side switches follows closely with I_S, the ZVS operation of all secondary side switches is maintained, as shown in Fig. 27(c).

When $V_2 = V_1 = 320$ V, the system enters the SPS control. As only one phase shift angle can be adopted to meet the power processing requirements, the realization of ZVS cannot be controlled under the SPS control. Only the secondary side switches can fully realize ZVS, as shown in Fig. 27(d).

When $V_2 = 390$ V, the system operates at the start of mode II under boost-type operation, and the ZVS-current is seamlessly

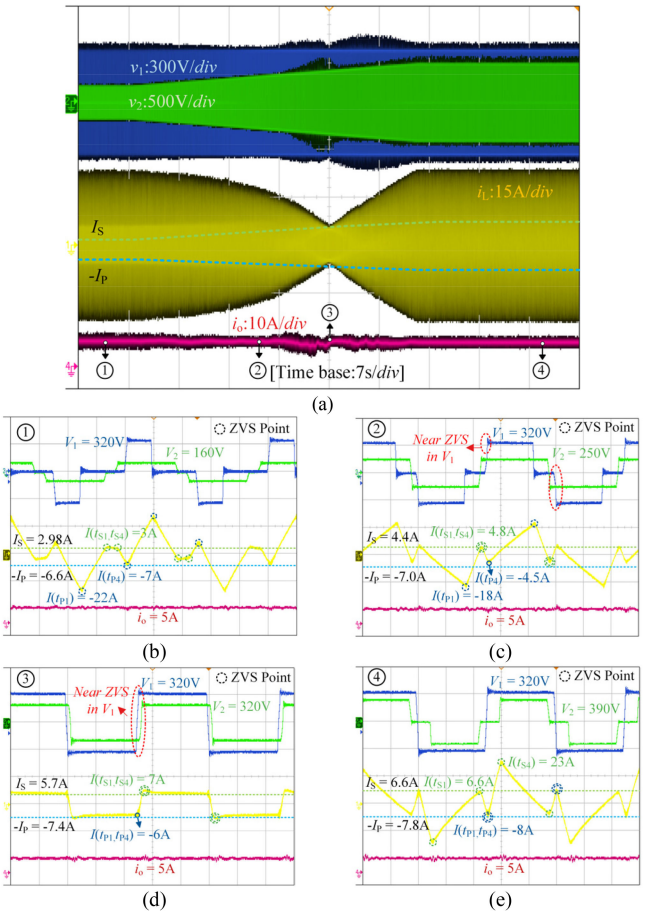

Fig. 27. Key waveforms of the dynamic ZVS-current transitions. (a) Waveform of system transitioning from $V_2 = 160$ to 390 V. (b) $V_2 = 160$ V, $M = 0.5$. (c) $V_2 = 250$ V, $M = 0.78$. (d) $V_2 = 320$ V, $M = 1$. (e) $V_2 = 390$ V, $M = 1.22$.

transitioned to $I_P = 7.8$ A, $I_S = 6.6$ A. As shown in Fig. 27(e), the turning-ON current of the switches still follows closely with the change of the ZVS-currents, and an all-ZVS operation is reimplemented. If one could keep the ZVS-current constant at $I_P = 6.6$ A, $I_S = 2.98$ A, the realization of ZVS would be lost and the system efficiency would be decreased.

In general, the stable operation and smooth transition under CC charging mode are achieved in the proposed algorithm. During the transition, the ZVS-current can be dynamically adjusted to ensure the realization of the ZVS operation under a wide voltage range.

D. Efficiency, Inductor RMS Current, and Power Loss Benchmarking

1) Buck-Type Operation: Fig. 28 shows the efficiency comparison among the SPS, GOC [20], STPS [28], PCS, and PCS1. In GOC, the realization of ZVS is ignored, and only the optimal inductor rms current can be realized. In the STPS, same as (16), the realization of ZVS is only considered in charge-based perspective. The ZVS-current $I_P = 4$ A, $I_S = 2$ A in STPS is inaccurate and the realization of ZVS cannot be fully achieved. In PCS1, the control scheme is identical to PCS but the ZVS-current is set as $I_P = I_S = 6.6$ A under the buck-type operation, which is greater than $I_P = 6.6$ A, $I_S = 2.9$ A in PCS.

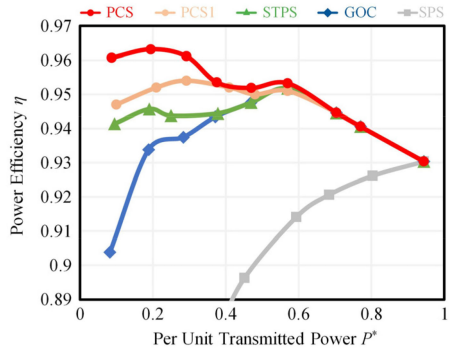

Fig. 28. Efficiency benchmarking for $V_1 = 320$ V, $V_2 = 160$ V, $M = 0.5$.

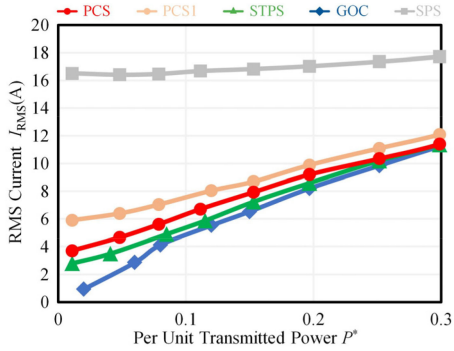

Fig. 29. Benchmarking of rms current for $V_1 = 320$ V, $V_2 = 160$ V, $M = 0.5$.

As shown in Fig. 28, as expected, the efficiency of PCS is higher than for the other algorithms at light load and medium load. At light load, the ZVS operation can be fully realized in PCS and PCS1, whose efficiencies are higher than for the STPS and GOC. Although an all-ZVS operation can be achieved in PCS1, the inaccuracy of the used ZVS-currents enlarges the unessential backflow power, so the efficiency is lower than that of the PCS. Noted that, at medium load, the efficiency of the PCS slightly decreases, as the system transition from all-ZVS state to six-ZVS state, but is still higher than that of GOC and STPS where only two-ZVS operation can be realized. With the increase of power, an all-ZVS operation can be realized naturally, and the efficiency of PCS and PCS1 is improved again. At heavy load, the PCS transitions to the optimal inductor rms current control, whose efficiency is basically consistent with GOC. When $P^* = 0.9$, all methods switch to the SPS control, so the efficiencies are the same as the SPS.

Fig. 29 compares the inductor rms current of the SPS, PCS, PCS1, STPS, and GOC under the buck-type operation. In general, as the single objective optimization of inductor rms current is realized, the GOC owns the smallest rms current among all analyzed algorithms. As only a control variable can be adopted in the SPS method, it does not have the ability to optimize inductor rms current. For the PCS1 control, a larger ZVS-current $I_P = I_S = 6.6$ A is considered, leading to a lager backflow power, so the inductor rms current of the PCS1 is not optimal. For the PCS control, the ZVS-current is $I_P = 6.6$ A, $I_S = 2.9$ A and it is greater than the current $I_P = 4$ A, $I_S = 2$ A used in the STPS control. Therefore, the inductor rms current of PCS is larger than

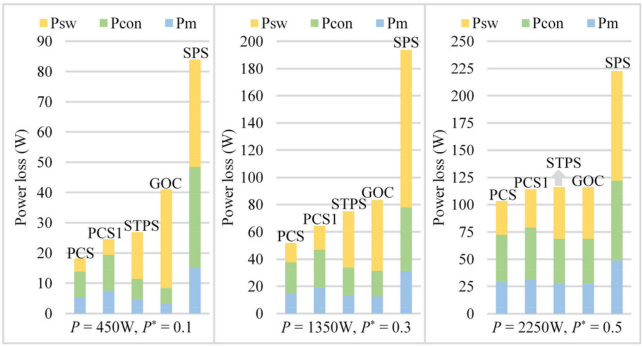

Fig. 30. Power losses comparison for $V_1 = 320$ V, $V_2 = 160$ V, $M = 0.5$.

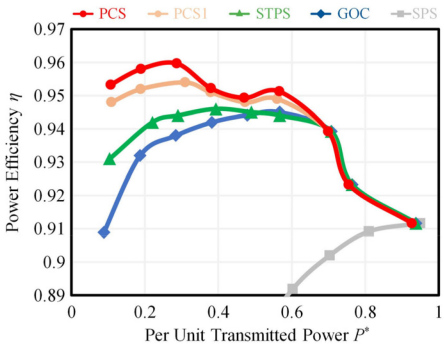

Fig. 31. Benchmarking of efficiency for $V_1 = 160$ V, $V_2 = 320$ V, $M = 2$.

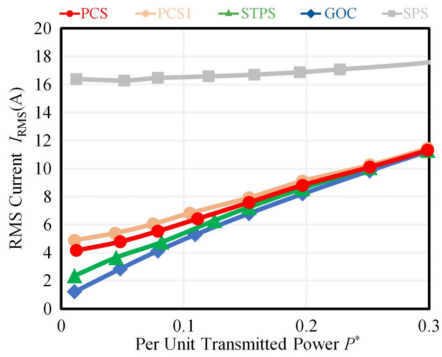

Fig. 32. Benchmarking of rms current for $V_1 = 160$ V, $V_2 = 320$ V, $M = 2$.

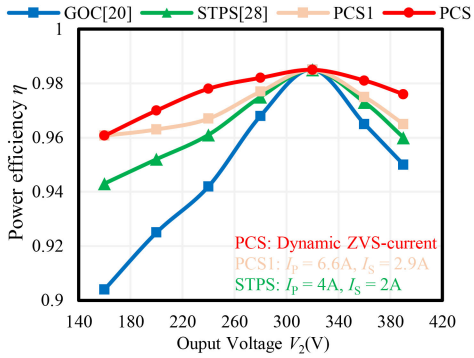

Fig. 33. Benchmarking of efficiency under various output voltage conditions $V_1 = 320$ V, $I_o = 5$ A, $V_2 = [160$ V, 390 V].

that of the STPS, particularly at light load. However, with the increment of the processed power, the additional rms current required by the ZVS operation becomes a fraction of the overall rms current value, and thus the obtained rms current of most algorithms tends to converge.

The power loss breakdown of all control methods is shown in Fig. 30, where P_{sw}, P_{con}, and P_m represent the switching loss, conduction loss of the switches, and the magnetic loss, respectively. At light load when $P^* = 0.1$, the switching losses of the PCS and PCS1 are the minimum as all-ZVS operation can be realized. At medium load when $P^* = 0.3$, only two-ZVS operation can be realized in STPS, whose switching loss is increased and consistent with GOC. However, by adopting six-ZVS transition, the switching losses of PCS and PCS1 are kept at a small value. With the power increased, an all-ZVS operation can be naturally realized in all analyzed control methods, so the loss differences are minimized.

2) Boost-Type Operation: The system efficiency of all algorithms under the boost-type operation is compared in Fig. 31. The ZVS-current of STPS is calculated as $I_P = 2$ A, $I_S = 4$ A and the ZVS operation still cannot be fully realized. In PCS, the ZVS-current is calculated as $I_P = 5.1$ A, $I_S = 4.9$ A, and the ZVS-current of the PCS1 is still set as $I_P = I_S = 6.6$ A. As can be seen, the efficiency of PCS and PCS1 is still higher than that of STPS and GOC as an all-ZVS operation can be realized.

As shown in Fig. 32, under the boost-type operation, the ZVS-currents of the STPS and PCS are $I_P = 2$ A, $I_S = 4$ A and $I_P = 5.1$ A, $I_S = 4.9$ A, respectively. The ZVS-current of the PCS1 is still set as $I_P = I_S = 6.6$ A. As can be seen, the GOC still owns the smallest inductor rms current. The largest additional backflow power is required in the PCS1, causing a high inductor rms current occurs. As the ZVS-currents calculated by the PCS method are larger than that for the STPS, the inductor rms current for the PCS becomes slightly higher than that of the STPS. Similarly, as for the buck-type operation, as the power increases, the rms current of each algorithm tends to converge.

In general, for high-frequency operations, the optimization schemes aiming mostly for the minimization of the inductor rms current may suffer for poorer efficiency performance because of the consequent narrow ZVS range. Although the inductor rms current of PCS is slightly increased, the switching loss can be effectively suppressed by the widen ZVS operation range, which advantageously improve the system efficiency at light and medium load conditions.

3) Various Output Voltage Operation: Fig. 33 compares the efficiency of the PCS, PCS1, STPS, and GOC under the CC charging mode. As only one control variable can be adopted to transmit the specified power in the SPS control, there is no redundant combination of phase shift angle for adjusting the ZVS operation. Therefore, the SPS control is not included in the comparison. The ZVS-current of the PCS1 is set as $I_P = 6.6$ A, $I_S = 2.9$ A and the ZVS operation can only be realized when $V_2 = 160$ V. Since the ZVS-current of the PCS can be dynamically adjusted, the PCS owns the highest efficiency over the full voltage range. The ZVS-currents of the STPS and PCS1 are kept constant, so the realization of ZVS is lost when $V_2 >$

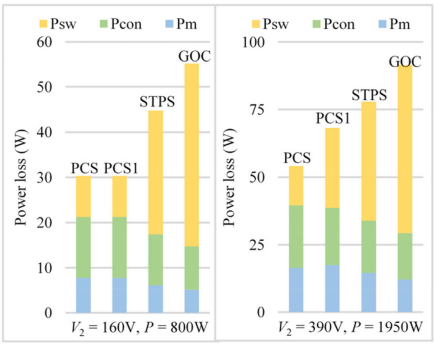

Fig. 34. Power loss breakdown under $V_2 = 160$ and 390 V conditions.

160 V and both efficiencies are lower than that achieved with PCS. When $V_2 = V_1 = 320$ V, all control schemes operate under SPS control, the operating efficiencies reach the highest point.

The power loss breakdown under $V_2 = 160$ V and 390 V conditions is shown in Fig. 34. As can be seen, the switching loss of the PCS is always the minimum among all control methods. Keeping the constant ZVS-current from $V_2 = 160$ V to $V_2 = 390$ V, the switching loss of PCS1 is considerably increased, as the realization of the ZVS cannot be realized in $V_2 = 390$ V. Therefore, the ability of dynamic adjustment in ZVS-current is necessary for the realization of ZVS under a wide voltage range, which is useful for EV chargers operating in the CC mode.

VI. Conclusion

This work has evaluated the DAB converter employing a new phase shift modulation scheme, which is especially suited for the EV charger application. The PCS widens the ZVS operating range while delivering a quasi-optimal inductor rms current. Combined with the SPS, EPS, and TPS controls, all the phase shift angles in the PCS are deduced for the goals of wide ZVS range, low inductor rms current, and seamless modes transition. To achieve the ZVS operation and to simplify the system control, the unified ZVS-current is proposed and determined from the perspectives of the charge exchange and dead time, only by which the ZVS conditions of all switches in any mode can be satisfied. Furthermore, as the operation conditions of the DAB in EV chargers would vary with the SOC of the battery, the real-time dynamic adjustment of the ZVS-currents has been equipped and the ZVS operation can be maintained under a wide voltage variation. The ZVS characteristics and rms current in the full power and voltage range have been analyzed and compared with previous works of literature. Simulation results have shown that the ZVS range in the PCS is effectively expanded with low inductor rms current and the seamless transition of all modes is realized. Experimental results have been adopted to verify the effectiveness and superiority of the proposed method. In the CV charging mode, the peak efficiency of 96.3% can be reached at light load when $M = 0.5$. Under the CC charging mode, as the ZVS operation can be real-time guaranteed by the implemented dynamic ZVS-currents, the overall efficiency is 2% higher than that achieved by the conventional solutions in full operational voltage range.

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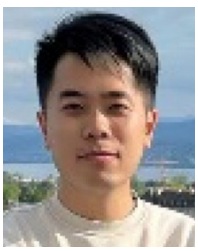

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