A Carrier-Based Discontinuous PWM Scheme With Optimal PWM Sequences for a Five-Level Flying Capacitor Rectifier

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***Abstract*—Five-level flying capacitor (5L-FC) rectifier is advantageous in unidirectional power applications due to its less power devices, higher power density, better reliability, etc. To further improve the efficiency, discontinuous PWM (DPWM) methods are preferred. This article investigates a carrier-based implementation of DPWM for the 5L-FC rectifier to reduce the switching losses. Since there is always a pair of redundant switching modes that have opposite effects on the neutral point (NP) in each region of the space-vector diagram, the NP voltage regulation can be easily realized by selecting suitable clamping modes in each control period, even with unbalanced dc loads. The generated PWM sequences based on the phase disposition PWM are also optimally redistributed to realize minimal switching loss with FC voltage balancing in two consecutive carrier periods. In addition, the permissible range of unbalanced dc loads is theoretically deduced. Finally, simulations and experiments are conducted to verify the performance of the proposed carrier-based DPWM scheme.**

***Index Terms*—Carrier-based discontinuous PWM (DPWM), five-level flying capacitor (5L-FC) rectifier, neutral-point (NP) voltage regulation, optimized pulsewidth modulation (PWM) sequence, phase disposition PWM (PDPWM), unbalanced dc loads.**

I. Introduction

FOR some common industrial applications, such as wind turbine systems, dc charger systems, and power factor corrections, it is not necessary to realize bidirectional energy flow. Therefore, it can be considered to reduce the number of fully controlled switches as much as possible so as to save production cost, reduce system complexity, and improve the operation reliability, while accomplishing high-performance rectification. Many different types of unidirectional rectifiers [1]–[6] have been proposed one after the other. And one superior topology [3] among them is shown in Fig. 1, which can be viewed as obtained by replacing some active switches of five-level neutral-point (NP) clamped converter with diodes (D_1–D_4). The inverter mode is eliminated as a cost to minimize the number of active switches. Each phase leg only needs four switches, four diodes, and one flying capacitor (FC). Three-phase legs are connected to two common split dc-link capacitors C_1 and C_2.

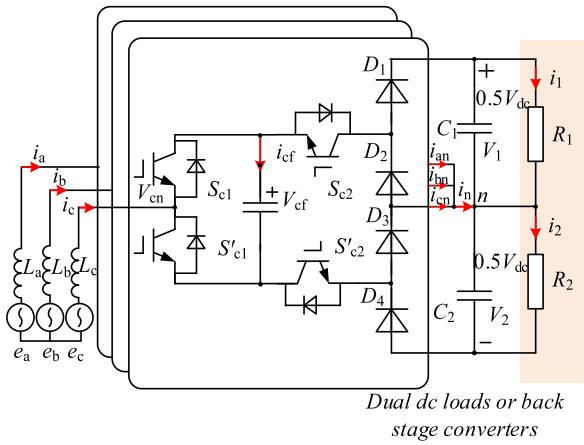

Fig. 1. Topology of the 5L-FC rectifier.

NP voltage balancing is the primary issue for the rectifier's reliable steady-state operation. Many pieces of literature have proposed solutions. The carrier-based balancing methods [7]–[10] use the freedom of zero-sequence voltage in three-phase systems, which are relatively simple and easy to realize. The optimal compensation component is calculated according to the relationship between the average NP current and zero-sequence component and injected into the three-phase reference signals. The space-vector-based balancing methods [11]–[14] are more complicated to implement but have more freedoms to simultaneously realize other control objectives, such as decreasing common voltages [14], minimizing the current ripples [12], and improving harmonic performance [13]. The essential idea of the space-vector-based suppression method is to adjust the relative dwell times of redundant small vectors that have opposite effects on the NP. The essential consistency of these two modulation methods has also been studied in many pieces of literature [15], [16]. Besides, virtual vector modulation [17]–[19] is

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viewed as another effective solution at random modulation indices and power factors. The reference vector is synthesized by using a series of virtual vectors with no effect on NP, while the switching loss is inevitably increased due to which more basic vectors are used in one carrier period.

There is no doubt that the above strategies have excellent performance in terms of NP voltage balancing. Nevertheless, for a well-outstanding modulation strategy, simple implementation and low switching loss are two other important aspects that also need to be highlighted. In order to satisfy the requirement of high-efficiency and high-power density applications, the switching loss needs to be minimized. Comparatively, discontinuous pulsewidth modulation (DPWM) schemes are preferred choices because there is always one-phase leg clamped to the points of the dc link without switching actions. The switching loss can be reduced significantly.

The conventional DPWM schemes [20], named DPWM0–DPWM3, lack the ability of NP voltage balancing since the clamping modes at each moment are fixed and cannot automatically adjust according to the NP voltage deviation. To solve the NP voltage issue, various modified DPWM schemes are proposed. In [21], continuous pulsewidth modulation (CPWM) and DPWM are combined to realize NP voltage balance and switching loss reduction. Nevertheless, the introduction of CPWM increases the switching loss. There are also several full-DPWM schemes with NP voltage controllability. In [22], an extended DPWM strategy for three-level inverters that can balance the NP voltage under the full range of modulation indices and power factor is given. The average NP current can be kept at zero. But the special polarity constraint of the five-level flying capacitor (5L-FC) rectifier results in this scheme failing to work. In [23], a novel DPWM strategy is proposed for three-level inverters to reduce switching loss and control NP voltage simultaneously. NP voltage is controlled by selecting proper clamping modes. And in [24], for further avoiding unexcepted switching transitions during the clamping mode switching process, the pulsewidth modulation (PWM) sequence is improved by adopting both convex and concave carriers. Unfortunately, these schemes have the problem of zero-crossing current distortion when applied to unidirectional rectifiers.

Considering the current polarity constraint of unidirectional rectifiers [25], several pieces of literature have provided different solutions with superior performance. In [26], a modified space-vector DPWM with active NP voltage ability is proposed for Vienna rectifiers. Redundant clamping modes near the current peak are switched to regulate the NP voltage within every switching period. However, it is relatively complicated in terms of sector judgments and dwell time calculation compared with the carrier-based implementation. In [27] and [28], the phase with the largest current is clamped to the top/bottom of the dc link for minimizing the switching loss. Two redundant switching modes are alternatively used to stable the NP voltage in a fundamental period. And recently, in [29], a hybrid DPWM based on three-level to two-level conversion that combines the modulation degree of freedom is presented to simultaneously minimize the switching loss and reduce the NP voltage fluctuation. It is worth emphasizing that the above strategies only consider operating conditions with one dc load. Under steady state, the average NP current during a fundamental period is kept zero. These schemes do not have the ability to provide continuous constant NP current during a whole fundamental period.

To make full use of the topology and to extend the dc voltage range, the rectifier can provide dual dc voltages to second-stage dc/dc converters or different loads with the same rated voltages [30]–[33], as shown in Fig. 1. Due to the load differences, the upper and lower power cannot be equal, resulting in the dc-link unbalanced with serious current distortions if the rectifier does not provide enough NP current to keep the power balance [32]. A dynamic-space-vector DPWM with superior current total harmonic distortion (THD) performance and efficiencies is proposed in [34] for providing dual dc voltages. But regrettably, this scheme also does not have the ability to provide continuous constant NP current. The dual dc voltage ratio is completely determined by the backstage loads. When the loads change, the dual dc voltages change accordingly, which greatly limits this scheme's applications. The DPWM schemes proposed in [35] and [36], theoretically, have the ability to provide continuous NP current with dual unbalanced loads, but unfortunately, the permissible range of unbalanced dc loads is not explored further.

Based on the pieces of literature discussed above, few pieces of literature have investigated the ability to output continuous constant current at NP and permissible unbalanced power range of dual loads with adopting DPWM schemes. In this article, a different carrier-based DPWM scheme for the 5L-FC rectifier is proposed based on the equivalence between carrier-based modulation and space-vector modulation. NP potential can provide a certain continuous constant current for dc loads by switching different clamping modes in each region of the space-vector diagram. And the generated PWM sequence based on phase disposition PWM (PDPWM) is also redistributed for simultaneously realizing FC voltage regulation and switching loss minimization in two consecutive periods. Both high efficiency and low THD performance are realized. The permissible range of unbalanced power is detailedly investigated for industry reference.

The rest of this article is organized as follows. In Section II, the operational characteristics and available clamping modes in the space-vector diagram of the 5L-FC rectifier are presented. In Section III, a carrier-based DPWM with low calculation burden is detailedly presented. The permissible unbalanced power range of dual loads is also deduced theoretically. In Section IV, simulations and experiments are presented to verify the performance of the proposed carrier-based DPWM. Finally, Section V concludes this article.

II. Operational Characteristics of 5L-FC Rectifier

The structure of the 5L-FC rectifier is shown in Fig. 1. Each phase leg is composed of one FC, four switches, and four diodes. Three-phase legs are connected to a common dc bus with a voltage amplitude of $V_{\rm dc}$. i_x ($x = a, b, c$) is the phase current, and i_{xn} is the phase current flowing into the NP. V_{xf} and i_{xf} represent the FC voltage and FC current, respectively. Their

TABLE I
SWITCHING STATES OF 5L-FC RECTIFIER WITH EFFECTS ON NP AND FC

i_x	S_{x1}	S_{x2}	V_{xn}	S	i_{xf}	i_{xn}	Level
	1	1	$0.5V_{dc}$	V_8	0	0	4
+	1	0	$0.25V_{dc}$	V_7	i_x	i_x	3^+
	0	1	$0.25V_{dc}$	V_6	$-i_x$	0	3^-
	0	0	0	V_5	0	i_x	2_+
	1	1	0	V_4	0	i_x	2_-
-	1	0	$-0.25V_{dc}$	V_3	i_x	i_x	1^-
	0	1	$-0.25V_{dc}$	V_2	$-i_x$	0	1^+
	0	0	$-0.5V_{dc}$	V_1	0	0	0

positive directions are shown by red arrows in Fig. 1. Under steady state, FC voltage V_{xf} and dual dc voltages should be kept at $0.25V_{\rm dc}$ and $0.5V_{\rm dc}$, respectively.

Table I presents eight different switching states and their effects on the NP and FC. The generated terminal voltage is also related to the current polarity due to the unidirectional characteristic of diodes D_1–D_4. Taking the NP as the zero potential, there exist five voltage levels $0.5V_{\rm dc}$, $0.25V_{\rm dc}$, 0, $-0.25V_{\rm dc}$, and $-0.5V_{\rm dc}$. For convenience, they are represented by 4, 3, 2, 1, and 0. Note that Levels 1 and 3 have two redundant states (V_2 and V_3, and V_6 and V_7) with opposite effects on the FCs and can be used to regulate FC voltages. They are distinguished by 3^+ and 3^-, and 1^+ and 1^-. 3^+, 1^+ charge FCs, while 3^-, 1^- discharge FCs. 2_+ and 2_- represent the same voltage level but consist of different switching states due to the opposite current polarities.

The rectifier operates at a unity power factor. The input current i_x can be expressed as follows:

$$\begin{cases} i_a = I_m \cos(\omega t) \\ i_b = I_m \cos(\omega t - 2\pi/3) \\ i_c = I_m \cos(\omega t + 2\pi/3) \end{cases} \tag{1}$$

where I_m and ω are the amplitude and frequency in rad/s, respectively.

Considering the filter impedance L, three-phase reference signals lag behind the three-phase currents by a small phase angle, which can be written as

$$\begin{cases} v_a = m \cos(\theta - \varphi) \\ v_b = m \cos(\theta - 2\pi/3 - \varphi) \\ v_c = m \cos(\theta + 2\pi/3 - \varphi) \end{cases} \tag{2}$$

where m is the modulation index, which is normalized at $0.5V_{\rm dc}$ and satisfies $0<m<1.15$. φ is the lagging angle caused by the filter impedance and calculated as $\tan^{-1}(\omega L I_m/V_m)$ [37]. V_m is the peak value of the input ac voltages.

The five-level space-vector diagram of the rectifier is shown in Fig. 2(a) with a large number of redundant vectors and basic vectors. It tilts the horizontal line by an angle φ. These redundancies provide the freedom to simultaneously accomplish other objectives, such as balancing NP voltage, decreasing common voltage, and reducing switching losses.

The terminal voltage is related to the current polarity; hence, not all basic vectors can be used at the same instant. Three-phase current polarities remain the same within 60°. The diagram can be divided into six sectors according to the polarity divisions, as shown in Fig. 2(a). For instance, the basic vector 400 can only be used in sector 1 and cannot be used in other sectors. There are only 26 basic vectors available in each sector synthesis. For easing analysis, each sector can be further divided into six subsectors, as shown in Fig. 2(b). And each subsector consists of four regions, as shown in Fig. 2(c).

For the convenience of analysis, define S as the total sector label. It satisfies $S = 100S_5+10S_3+S_2$. S_5, S_3, and S_2 are the labels of the sector, the subsector, and the region, as shown in Fig. 2, respectively.

When the reference vector is located in region 3, as shown in Fig. 2(c), there are different vector combinations by using three nearest vectors due to the redundancy of basic vectors. For improving the efficiency, one-phase leg can be kept at a fixed voltage for reducing the switching loss. Hence, there exist five available combinations, including (311, 310, 300), (411, 421, 422), (311, 310, 411), (200, 300, 310), and (311, 411, 421).

It should be noted that, in practical applications, the capacitance of FC is generally much smaller than the dc capacitors. If levels 1 and 3 are also selected as clamping levels, the phase current will flow across the FC in one direction during the clamping intervals, causing large voltage ripples on the FC [36]. Thus, levels 1 and 3 are not suitable as clamping levels. There are only three clamping levels, including 0, 2, and 4, for the 5L-FC rectifier, similar to three-level converters. Only two combinations (411, 421, 422) and (200, 300, 310) are available when located in region 3 of Fig. 2(c).

For the purpose of the following description, define "*X*–*Y*" as Phase *X* ($X = A, B, C$) clamped to Level *Y* ($Y = 0, 2, 4$).

Following the same combination principle, all the available clamping modes in the regions of sector 1 are selected out and shown in Table II. Note that 1 and 3 have a pair of redundant switching states with opposite effects on FC, as shown in Table I. In steady state, the relative dwell times of these two pairs of redundant switching states must be equal to ensure FC voltages balancing. It is assumed that the dwell times of the redundant switching states of 1 and 3 in every clamping mode are equal. Hence, the effects of different clamping modes on NP are determined. In a carrier period, the average NP current of different clamping modes can be calculated as

$$i_n = \sum_{x=a,b,c} i_{xn} = \sum_{x=a,b,c} (t_{x1-} + t_{x2} + t_{x3+}) i_x \tag{3}$$

where t_{x1-}, t_{x2}, and t_{x3+} are the dwell times of 1^-, 2, and 3^+ in a carrier period, respectively. If i_n of one clamping mode is smaller than 0, it means that this clamping mode has a negative effect on the NP. Correspondingly, if i_n is bigger than 0, this clamping mode has a positive effect on the NP. The positive/negative effects on the NP are represented by "+/−." Thus, the effects of all clamping modes on the NP in sector 1 are known, as shown in Table II. Clamping modes and their effects in other sectors can be analyzed in the same way.

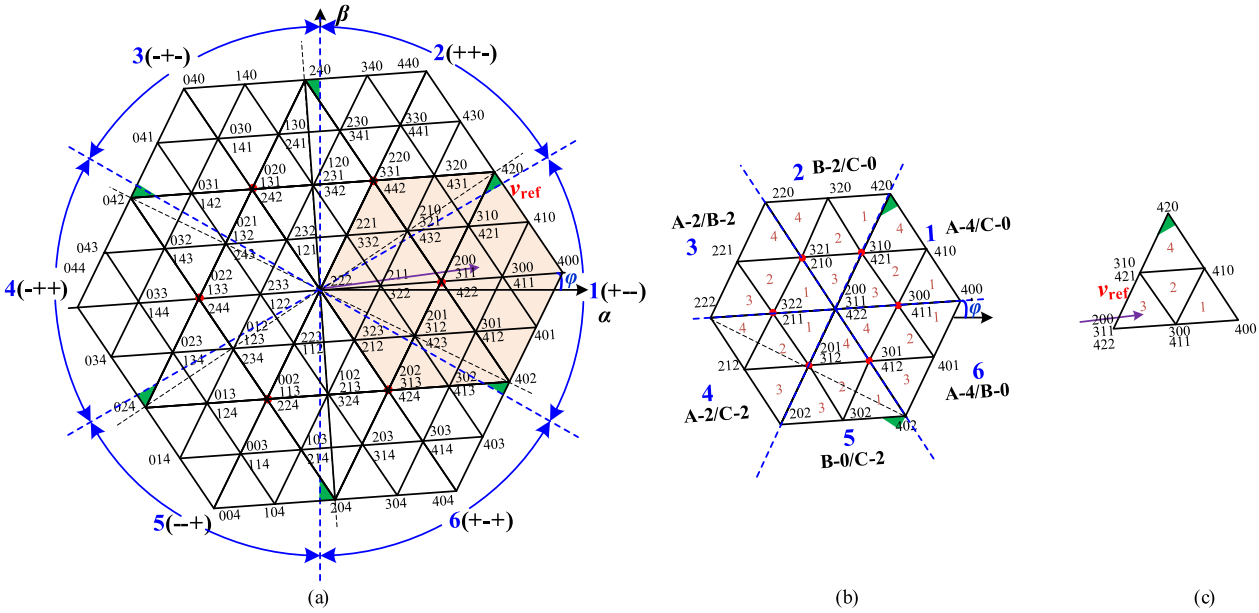

Fig. 2. Space-vector diagram. (a) Five-level space-vector diagram with sector divisions. (b) Subsector divisions in sector 1 ($S_3 = 1$). (c) Region divisions in subsector 1 ($S_2 = 1$).

TABLE II
CLAMPING MODES, COMPENSATION COMPONENTS, AND THEIR EFFECTS ON NP IN SECTOR 1

S_3	S_2	Clamping mode	synthetic vectors	Effect on NP	S_3	S_2	Clamping mode	synthetic vectors	Effect on NP
1	1	C-0	300,400,410	+	2	1	C-0	310,320,420	+
		A-4	400,410,411	-			B-2	320,420,421	-
	2	C-0	300,310,410	+		2	C-0	210,310,320	+
		A-4	410,411,421	-			B-2	320,321,421	-
	3	C-0	200,300,310	+		3	C-0	200,210,310	+
		A-4	411,421,422	-			B-2	321,421,422	-
	4	C-0	310,410,420	+		4	C-0	210,220,320	+
		A-4	410,420,421	-			B-2	220,320,321	-
3	1	A-2	200,210,211	+	4	1	A-2	200,201,211	+
		B-2	321,322,422	-			C-2	312,322,422	-
	2	A-2	210,211,221	+		2	A-2	201,211,212	+
		B-2	221,321,322	-			C-2	212,312,322	-
	3	A-2	211,221,222	+		3	A-2	201,202,212	+
		B-2	221,222,322	-			C-2	202,212,312	-
	4	A-2	210,220,221	+		4	A-2	211,212,222	+
		B-2	220,221,321	-			C-2	212,222,322	-
5	1	B-0	301,302,402	+	6	1	B-0	300,400,401	+
		C-2	302,402,412	-			A-4	400,401,411	-
	2	B-0	201,301,302	+		2	B-0	300,301,401	+
		C-2	302,312,412	-			A-4	401,411,412	-
	3	B-0	201,202,302	+		3	B-0	301,401,402	+
		C-2	202,302,312	-			A-4	401,402,412	-
	4	B-0	200,201,301	+		4	B-0	200,300,301	+
		C-2	312,412,422	-			A-4	411,412,422	-

From Table II, it can be clearly seen that there is always one pair of redundant clamping modes with opposite effects on the NP in each region of the diagram. NP voltage can be adjusted bidirectionally by choosing suitable clamping modes. And four regions in one subsector have the same clamping modes but different vector combinations. The clamping modes with positive/negative effects on the NP are defined as positive/negative clamping modes, respectively.

III. PROPOSED CARRIER-BASED DPWM SCHEME

A. DPWM Reference Signal Calculation

Section II describes all the available clamping modes in the space-vector diagram. The redundancy of the clamping modes provides the possibility to actively balance NP voltage. However, the space-vector-based implementation of DPWM is quite complex, especially for this five-level rectifier. Thus, to reduce

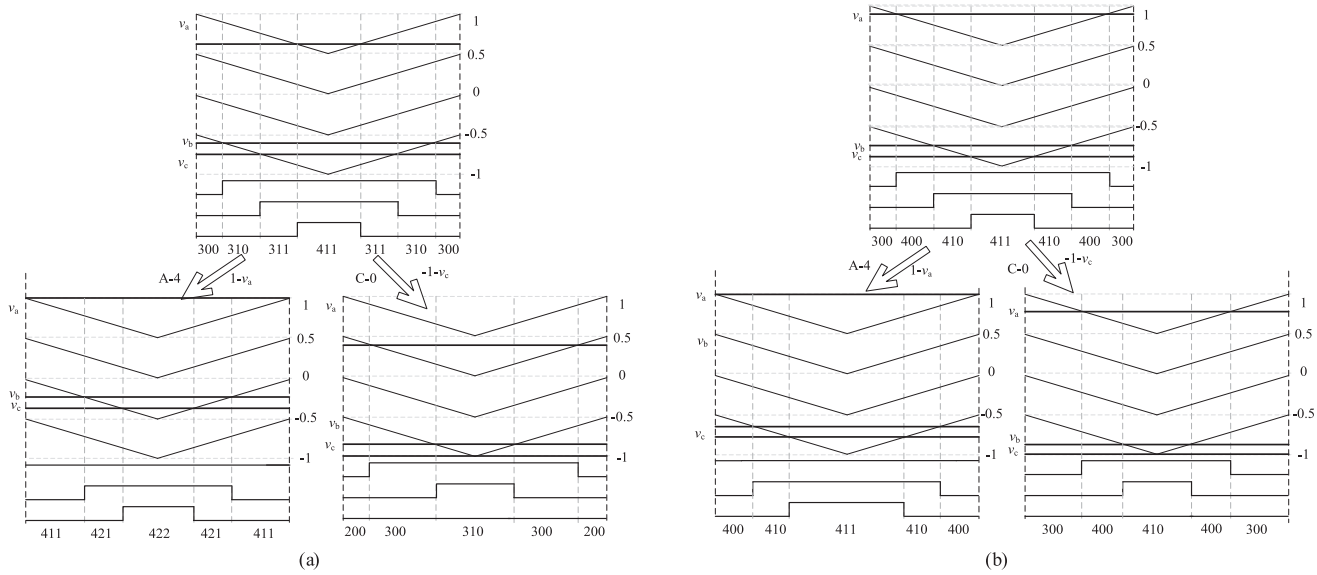

Fig. 3. Vector sequence. (a) DPWM sequence when $S = 113$. (b) DPWM sequence when $S = 111$.

TABLE III
CLAMPING MODES, COMPENSATION COMPONENTS, AND THEIR EFFECTS ON NP IN 36 SUBSECTORS

S_5	S_3	clamping mode (effect on NP)	Compensation component v_{con}	S_5	S_3	clamping mode/effect on NP	Compensation component	S_5	S_3	clamping mode (effect on NP)	Compensation component v_{con}
1	1	A-4(-)/C-0(+)	1-v_a/-1-v_c	2	1	A-4(-)/C-0(+)	1- v_a/-1-v_c	3	1	A-2(-)/C-2(+)	- v_a/-v_c
	2	B-2(-)/C-0(+)	- v_b/-1-v_c		2	B-4(-)/C-0(+)	1- v_b/-1-v_c		2	B-4(-)/C-2(+)	1- v_b/-v_c
	3	B-2(-)/A-2(+)	- v_b/-v_a		3	B-4(-)/A-2(+)	1- v_b/-v_a		3	B-4(-)/A-0(+)	1- v_b/-1-v_a
	4	C-2(-)/A-2(+)	- v_c/-v_a		4	C-2(-)/A-2(+)	- v_c/-v_a		4	C-4(-)/A-0(+)	1- v_c/-1-v_a
	5	C-2(-)/B-0(+)	- v_c/-1-v_b		5	C-2(-)/B-2(+)	- v_c/-v_b		5	C-4(-)/B-2(+)	1- v_c/-v_b
	6	A-4(-)/B-0(+)	1- v_a/-1-v_b		6	A-4(-)/B-2(+)	1- v_a/-v_b		6	A-2(-)/B-2(+)	- v_a/-v_b
4	1	A-2(-)/C-2(+)	- v_a/-v_c	5	1	A-2(-)/C-2(+)	- v_a/-v_c	6	1	A-4(-)/C-2(+)	1- v_a/-v_c
	2	B-4(-)/C-2(+)	1- v_b/-v_c		2	B-2(-)/C-2(+)	- v_b/-v_c		2	B-2(-)/C-2(+)	- v_b/-v_c
	3	B-4(-)/A-0(+)	1- v_b/-1-v_a		3	B-2(-)/A-0(+)	- v_b/-1-v_a		3	B-2(-)/A-2(+)	- v_b/-v_a
	4	C-4(-)/A-0(+)	1- v_c/-1-v_a		4	C-4(-)/A-0(+)	1- v_c/-1-v_a		4	C-4(-)/A-2(+)	1- v_c/-v_a
	5	C-4(-)/B-2(+)	1- v_c/-v_b		5	C-4(-)/B-0(+)	1- v_c/-1-v_b		5	C-4(-)/B-0(+)	1- v_c/-1-v_b
	6	A-2(-)/B-2(+)	- v_a/-v_b		6	A-2(-)/B-0(+)	- v_a/-1-v_b		6	A-4(-)/B-0(+)	1- v_a/-1-v_b

the computation burden, this article proposes a carrier-based implementation.

It is well-recognized that PDPWM can equivalently produce the same symmetrical seven-segment sequence as nearest-three-vector space vector PWM (SVPWM). Hence, PDPWM is adopted in this article. Comparing the reference signals with four-level-shifted carriers, seven-segment vector sequence consisting of nearest three vectors is naturally obtained, as shown in Fig. 3. For instance, when $S = 113$ and 111, the sequences are "300-310-311-411-311-310-300" and "300-400-410-411-410-400-300," respectively. All available clamping modes of these two regions have been analyzed in Section II. They can be easily obtained by injecting suitable clamping compensation components 1-v_a/−1-v_c. Fig. 3 shows the detailed implementation. The vector sequences of the clamping modes A-4 and C-0 when $S = 113$ are 411-421-422-421-411 and 200-300-310-300-200, respectively, while the sequences of A-4 and C-0 when $S = 111$ are 400-410-411-410-400 and 300-400-410-400-300, respectively. All clamping modes in 36 subsectors and their corresponding compensation components are summarized and shown in Table III.

For realizing NP voltage regulation, a hysteresis controller is used to switch redundant clamping modes back and forth. $\Delta_{\rm band}$ is the predefined error band. If the upper voltage derivation ΔV_1 is greater than the predefined error band, negative clamping mode is chosen to discharge NP. On the contrary, positive clamping mode is selected to charge NP if ΔV_1 is smaller than $-\Delta_{\rm band}$.

The DPWM reference signals v'_x can be simply expressed as

$$v'_x = v_x + v_{\rm con} \tag{4}$$

where $v_{\rm con}$ is the clamping compensation component. If X-0, X-2, and X-4 are chosen (X represents the phases a, b, and c), $v_{\rm con}$ equals $-1-v_x$, $-v_x$, and $1-v_x$, respectively. Table III presents the corresponding compensation components of 36 subsectors.

It should be highlighted that the basic vectors cannot cover the green zones, as shown in Fig. 2. For mitigating current

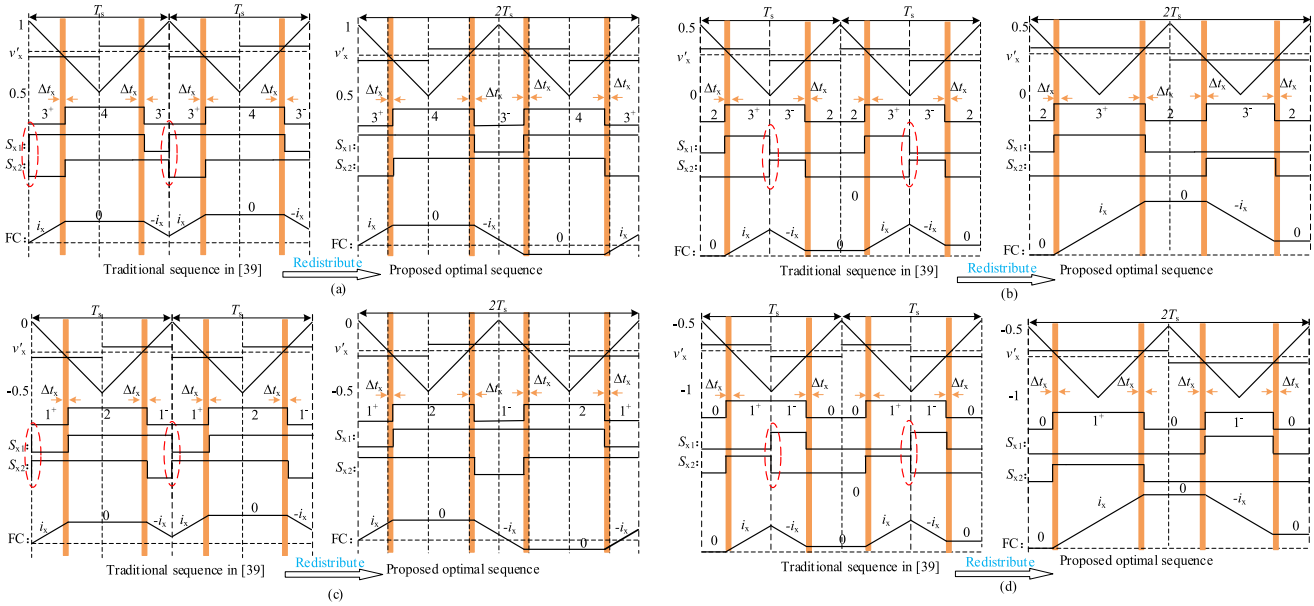

Fig. 4. Voltage balancing of FC under different ranges of v'_x. (a) $0.5<v'_x<1$. (b) $0<v'_x<0.5$. (c) $-0.5<v'_x<0$. (d) $-1<v'_x<-0.5$.

distortions, the trajectory of the reference vector cannot pass through these zones. Hence, according to the mathematical geometric relationship, the modulation range is calculated as follows [38]:

$$m \leq \frac{1}{\sqrt{3}\sin(\pi/6+\varphi)}. \tag{5}$$

B. FC Voltage Regulation

For multilevel converters, PDPWM is the most common modulation strategy for its optimal line voltage harmonic performance. As shown in Table I, there are two pairs of redundant switching states with opposite effects on the FC. Therefore, under the steady-state condition, the dwell times of the redundant switching states should be equal to ensure that the sum of the current flowing across FC in one control period is zero. Under unbalanced condition, the relative dwell times of two pairs of redundant switching states (V_2 and V_3, and V_6 and V_7) can be slightly adjusted to keep balance according to the FC voltage deviation.

The left part of Fig. 4 shows the traditional modulation diagram in [39] under different ranges of v'_x. 1^+, 3^+ are used in the first half of the symmetric triangular carrier, while 1^-,3^- are used in the second half of the symmetric triangular carrier. Under balanced condition, the dwell times of redundant switching states are equal; hence, FC voltage is naturally balanced. Taking Fig. 4(a) as an example, if the dwell time of 3^+ increases by Δt_x; correspondingly, the dwell time of 3^- decreases Δt_x, which does not affect the average terminal voltage in one carrier period. There is $2i_x\Delta t_x$ current flowing thorough FC, resulting in FC voltage increased. FC voltage balancing can be realized by adjusting Δt_x.

However, these traditional sequences lead to additional switching losses. The number of switching transitions of S_{x1} and S_{x2} reach up to eight times in two carrier periods. Besides, when the terminal voltage V_{xn} is changed from 3^+ (1^+) to 3^- (1^-), S_{x1} and S_{x2} switch as the same time, as shown in the red-dotted circles of Fig. 4(a), which is unexpected in practical applications and should be avoided.

In this article, for minimizing the switching losses and avoid simultaneous switch of S_{x1} and S_{x2}, the PWM sequences are optimally redistributed, as shown in the right part of Fig. 4. Two consecutive carrier periods are viewed as one control period. The terminal voltage is kept same at both the starting and ending of one control period. The number of switching transitions of S_{x1} and S_{x2} is minimized to four times, which greatly reduces the switching losses. But, as a price, as the two consecutive carrier periods are viewed as one control period, the FC voltage ripple is doubled when v'_x falls in the range of $(0, 0.5)$ and $(-1, -0.5)$, as shown in Fig. 4(b) and (d). There is a total of $4i_x\Delta t_x$ current flowing through FC in one control period. FC voltage balancing can also be easily realized by adjusting Δt_x.

Define $i_{xf\,\mathrm{ref}}$ as the required current for FC voltage regulation. A proportional controller is adopted in this article. Hence, Δt_x is solved as

$$\Delta t_x = \frac{i_{xf\_\mathrm{ref}}}{4i_x} = \frac{K_p(0.25V_{\mathrm{dc}} - v_{xf})}{4i_x}. \tag{6}$$

Fig. 5 shows the overall block diagram of the proposed DPWM scheme, including four steps.

1) Positive/negative clamping mode selection: According to the upper voltage deviation ΔV_1, positive or negative clamping mode can be chosen to adjust the NP voltage.
2) Clamping compensation component injection: According to the region where the reference signal is located, the corresponding compensation component is obtained and directly injected to three-phase reference signals.

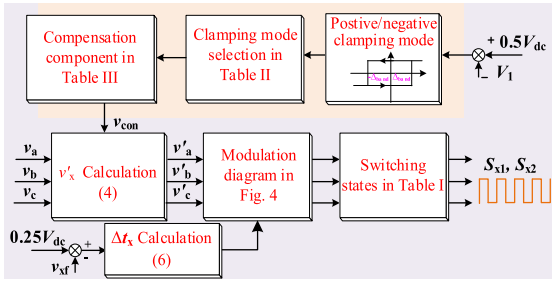

Fig. 5. Block diagram of the proposed DPWM scheme.

3) FC voltage regulation: By dynamically adjusting the dwell times of redundant switching states (3^+ and 3^-, 1^+ and 1^-) with adopting the redistributed sequences in Fig. 4, FCs can be charged or discharged to keep balancing with minimal switching transitions. A simple proportional controller can be used for regulation.
4) Pulse generation: Combining with Table I, the switching states of S_{x1} and S_{x2} can be obtained to control the rectifier.

C. Permissible Range of Unbalanced Loads

Due to the existence of redundant clamping modes, the proposed scheme has NP voltage balancing capability even with unbalanced loads. This section explores the permissible unbalanced power range. The range is directly determined by the NP current provided by different clamping modes. By adopting the redistributed PWM sequences, as shown in Fig. 4, the NP current in (3) can be simplified as

$$i_n = \sum_{x=a,b,c} (i_x - v'_x\,|i_x|) = -\sum_{x=a,b,c} v'_x\,|i_x|. \tag{7}$$

Fig. 6 shows the corresponding NP current waveforms of two extreme cases (only positive/negative clamping modes are used in a fundamental period) when $m = 0.9$ and 0.5. Due to the three-phase symmetry, only one-phase current and reference signal are shown. DPWMP represents the DPWM signal with only using the positive clamping modes, while DPWMN represents the DPWM signal with only using the negative clamping modes. It can be clearly seen that DPWMP is always above the original signal and DPWMN is always below the original signal. These two DPWM signals generate the NP currents of equal magnitude but opposite sign. With a high modulation index, one-phase leg is mainly clamped to the top/bottom points of the dc link to reduce switching loss. While it is mainly clamped to the NP with a low modulation index.

The black dashed lines $i_{n\_\max}$ and $i_{n\_\min}$ represent the corresponding average NP currents of DPWMP and DPWMN in one fundamental period, respectively, which are defined as

$$i_{n\_\mathrm{av}} = \frac{\int_0^{2\pi} i_n dt}{2\pi}. \tag{8}$$

Apparently, $i_{n\_\max}$ and $i_{n\_\min}$ are the maximum and minimum values of the average NP current that the rectifier can provide under normal operation, respectively.

TABLE IV
PARAMETERS OF SIMULATIONS AND EXPERIMENTS

Parameters	Values
Input line voltage (rms) e_x	138/77V(50Hz)
DC-link voltage V_{dc}	250V
DC-link capacitor C_1/C_2	1200μF
FC voltage V_{xf}	62.5V
FC	560μF
L-filter	2.2mH
Carrier frequency	20kHz
Control frequency	10kHz
DC loads (R_1, R_2)	(12Ω, 12Ω)/ (10Ω, 15Ω)/ (21Ω, 21Ω)/ (30Ω, 15Ω)

Neglecting the power loss, according to the power conservation between the ac side and dc side of the rectifier, it can be expressed as

$$1.5V_m I_m = 0.5V_{\mathrm{dc}}(i_1 + i_2) \tag{9}$$

where V_m, i_1, and i_2 are the peak value of the input ac voltages, upper dc current, and lower dc current, respectively. The modulation index m equals $2V_m/V_{\mathrm{dc}}$. And it also exists $i_2 = i_1 + i_{n\_\mathrm{av}}$ on the dc side. i_1 can be solved as $0.75mI_m - 0.5i_{n\_\mathrm{av}}$.

The unbalanced power degree γ is defined as

$$\gamma = \frac{P_1 - P_2}{P_1 + P_2} = \frac{0.5V_{\mathrm{dc}}i_1 - 0.5V_{\mathrm{dc}}i_2}{0.5V_{\mathrm{dc}}i_1 + 0.5V_{\mathrm{dc}}i_2} = \frac{-i_{n\_\mathrm{av}}}{2i_1 + i_{n\_\mathrm{av}}} = \frac{-i_{n\_\mathrm{av}}}{1.5mI_m} \tag{10}$$

where P_1 and P_2 are the upper and lower powers, respectively. Apparently, γ is directly related to i_{n_av} if the modulation index m is determined. Under balanced loads ($R_1 = R_2$), γ equals 0. Hence, the permissible range of γ can be solved by substituting $i_{n\_\max}$ and $i_{n\_\min}$ into (10). When m equals 0.9 and 0.5, the ranges of γ are solved as (−0.28,0.28) and (−0.72, 0.72), respectively. Permissible ranges under other modulation indices can be analyzed by the same way.

Fig. 7 shows the permissible range of the unbalanced power degree γ within the overall modulation range, providing a reference for industrial applications. When $\varphi = 0.05$, m cannot exceed 1.06, according to (5). Some conclusions can be drawn. 1) When m<0.62, the permissible range of γ is identical and reaches maximum (−0.72–0.72). 2) When m>0.62, the maximum of γ decreases gradually with the increase of m. To expand the unbalanced power range, the modulation index should not be too large. However, in order to improve the dc voltage utilization, m should be as high as possible. There is a tradeoff between them. The four purple coordinates (m, γ) in Fig. 7 are chosen and further verified by simulations and experiments in Section IV.

IV. SIMULATIONS AND EXPERIMENTS

Simulations using MATLAB/Simulink tool and experiments are carried out to verify the validity and performance of the

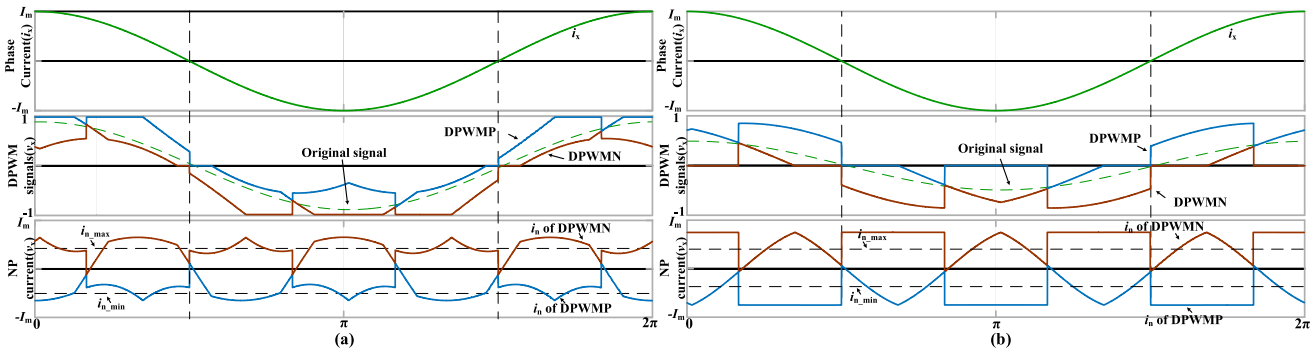

Fig. 6. Waveforms of DPWM signals and NP currents. (a) $m = 0.9$. (b) $m = 0.5$.

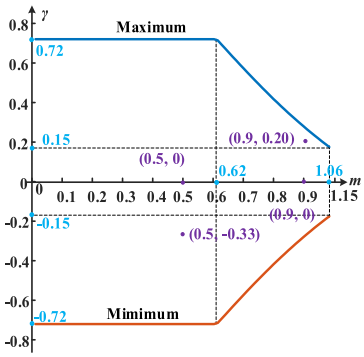

Fig. 7. Relationship of the unbalanced degree γ and modulation index m ($\varphi = 0.05$).

proposed method. Table IV presents the main system parameters. Two cases of different modulation indices are considered as follows.

Case 1($m = 0.9$): The line voltage V_{ab} (rms) and total dc voltage $V_{\rm dc}$ are kept at 138 V and 250 V, respectively, with resistive loads (12 Ω, 12 Ω)/(10 Ω, 15 Ω).

Case 2($m = 0.5$): The line voltage V_{ab} (rms) and total dc voltage $V_{\rm dc}$ are kept at 77 V and 250 V, respectively, with resistive loads (21 Ω, 21 Ω)/(30 Ω, 15 Ω).

A. Simulation Results Analysis

Fig. 8 shows the simulation results in case 1. The line voltage behaves like typical nine-level waveforms with superior harmonic performance (THDi = 1.4% and 1.2%) at a high modulation index. And it can be obviously observed that there is always one-phase reference signal clamped to −1, 0, or 1. Correspondingly, one-phase leg is clamped to the three points of the dc link with no switching transitions. The overall efficiency is improved. Due to the existence of redundant clamping modes, the proposed scheme has NP voltage balancing capability and can provide a certain NP current. Under balanced condition (12 Ω, 12 Ω), as shown in Fig. 8(a), the average NP current $i_{n\_\rm av}$ is near to zero by alternately switching positive and negative clamping modes. The number of positive and negative clamping modes used in a fundamental period is approximately equal. It can be seen that the time intervals of three-phase DPWM signals clamped to 1 and −1 are approximately equal. While, under unbalanced condition (10 Ω, 15 Ω), as shown in Fig. 8(b), the NP needs to provide −4.2 A current for keeping the dc-link balanced. More negative clamping modes are used in a fundamental period. Obviously, the signals are clamped to 1 for more time intervals than they are clamped to −1.

Fig. 9 shows the corresponding waveforms in case 2. Phase currents remain perfectly sinusoidal with low harmonics (THDi = 0.8% and 0.7%). Due to the low modulation index, the line voltage only contains five levels. Different from case 1, the reference signals are clamped to the NP to reduce the switching transitions. At any instant, there always exist one-phase reference signal clamped to 0. Correspondingly, the phase leg is clamped to the NP for avoiding switching transitions. With balanced loads (21 Ω, 21 Ω), as shown in Fig. 9(a), the NP current is kept at zero by selecting positive/negative clamping modes back and forth. The positive and negative clamping modes occupy approximately equal time intervals within a fundamental period. With unbalanced loads (30 Ω, 15 Ω), as shown in Fig. 9(b), there is about 4.2 A current flowing across the NP to keep the dc-link balanced. More positive clamping modes are used in a fundamental period to provide the NP current. The time intervals where the reference signals are negative are obviously more.

Fig. 10 shows the NP voltage ripple comparison. A smaller err band is set ($\Delta_{\rm band}$ = 1 V). The proposed DPWM is compared with the existing DPWM (E-DPWM) in [27]. Unidirectional rectifiers have the inherent constraint that the terminal voltage is related to the polarity of the phase current. Hence, for mitigating the current distortions near the zero points, the E-DPWM directly clamps one-phase reference signal to zero near the zero points of phase currents. When one-phase leg is clamped to the positive and negative points of the dc link near the current peak, there are opposite currents flowing across the NP. Thus, correspondingly, NP voltage balancing can be realized by clamping one-phase signal to 1 or −1, as shown in Fig. 10. However, near the zero-crossing points, due to which one-phase reference signal is clamped to 0, the NP voltage is uncontrollable, causing large NP voltage ripple, as shown in Fig. 10. On the contrary, this article detailedly analyzes the five-level space-vector diagram of the 5L-FC rectifier and finds

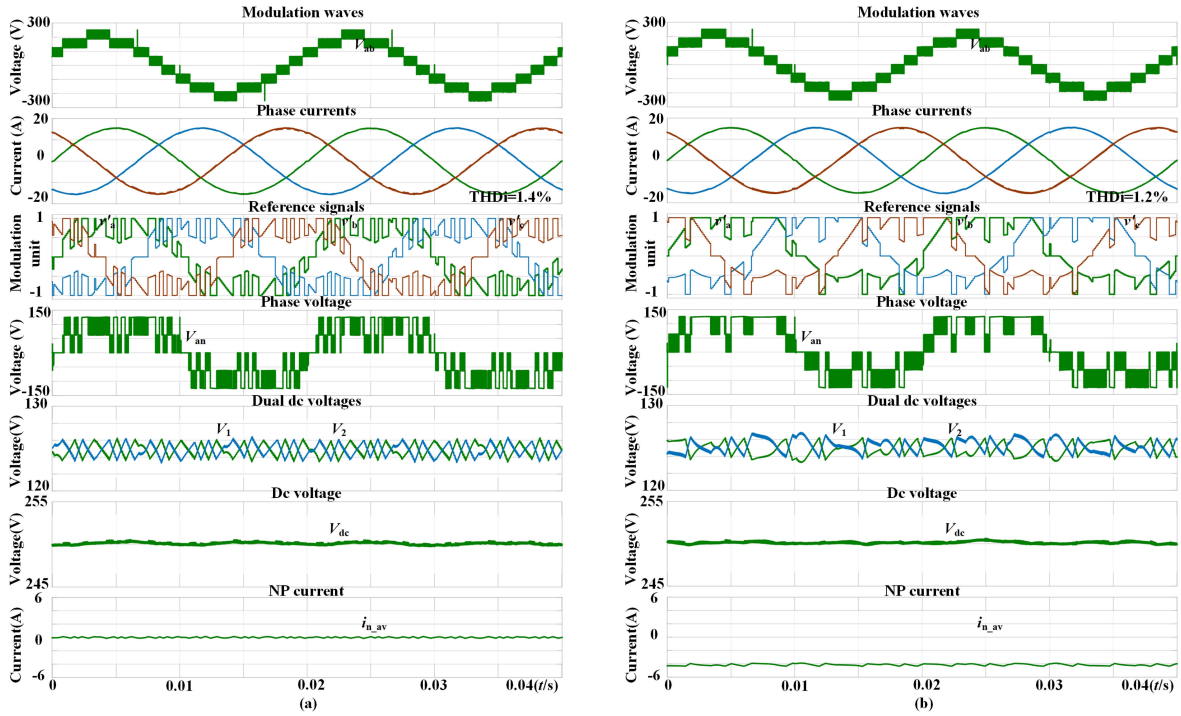

Fig. 8. Simulation waveforms with $m = 0.9$ ($\Delta_{\text{band}} = 2$ V). (a) Balanced loads ($R_1 = 12\ \Omega$ and $R_2 = 12\ \Omega$). (b) Unbalanced loads ($R_1 = 10\ \Omega$ and $R_2 = 15\ \Omega$).

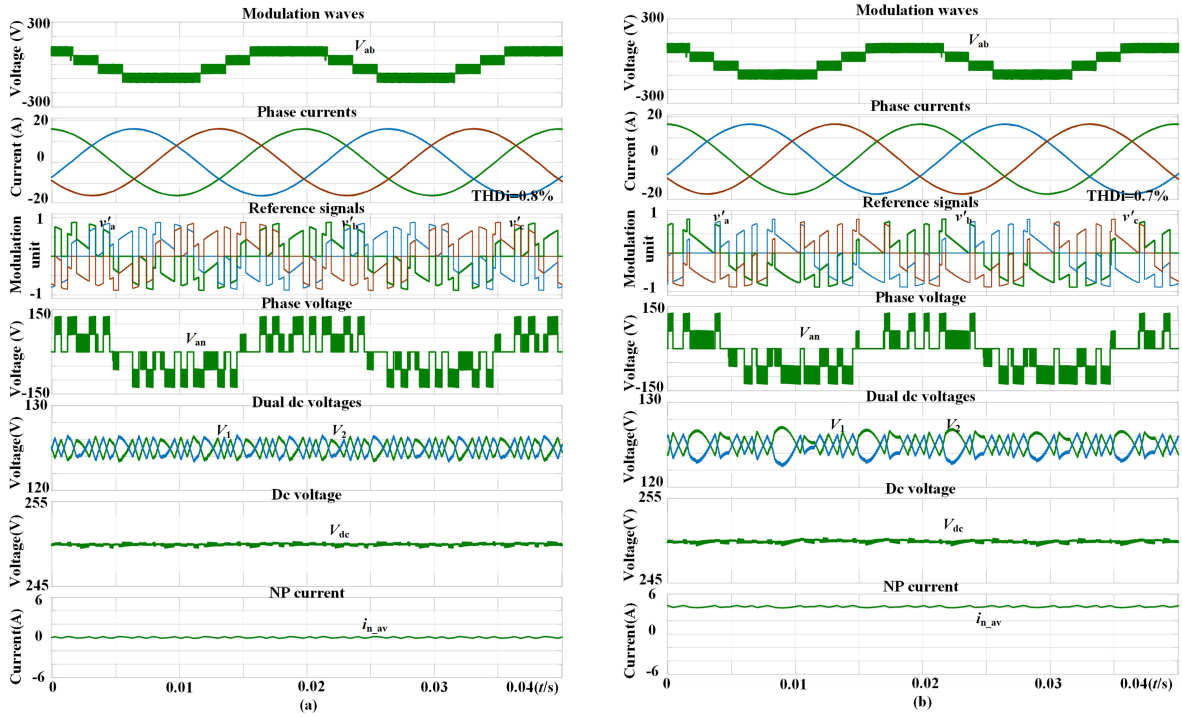

Fig. 9. Simulation waveforms with $m = 0.5$ ($\Delta_{\text{band}} = 2$ V). (a) Balanced loads ($R_1 = 21\ \Omega$ and $R_2 = 21\ \Omega$). (b) Unbalanced loads ($R_1 = 30\ \Omega$ and $R_2 = 15\ \Omega$).

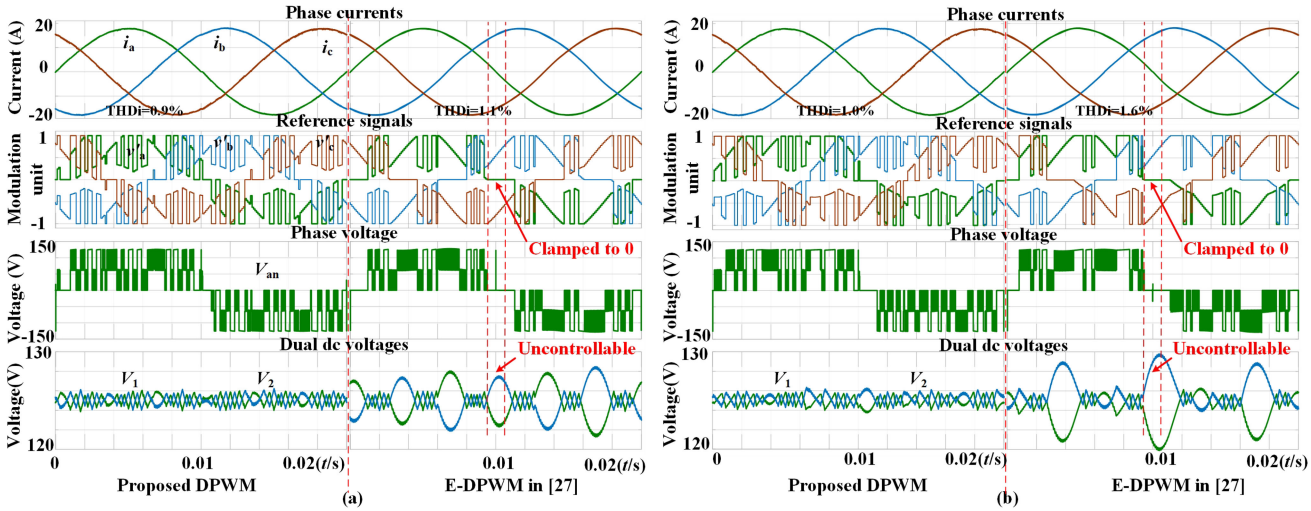

Fig. 10. NP voltage ripple comparison ($V_{\rm ab} = 120$ V, $V_{\rm dc} = 250$ V, and $\Delta_{\rm band} = 1$ V). (a) Balanced loads ($R_1 = R_2 = 12\ \Omega$). (b) Unbalanced loads ($R_1 = 10\ \Omega$ and $R_2 = 15\ \Omega$).

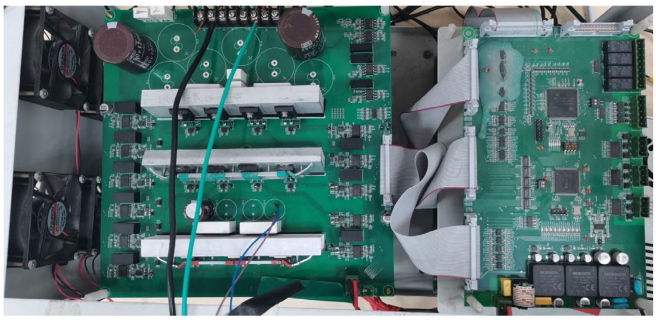

Fig. 11. Experimental platform of the 5L-FC rectifier.

that there is always a pair of redundant clamping modes with opposite effects on the NP voltage by analyzing the five-level space-vector diagram. Then, a carrier-based DPWM method is proposed based on the equivalence between carrier-based modulation and space-vector modulation. Therefore, the NP voltage is fully controllable during the whole fundamental period by adopting the proposed DPWM. It can be clearly seen that the proposed DPWM has better NP voltage control ability with smaller NP voltage ripple, even with unbalanced dc loads.

B. Experimental Results Analysis

The performance of the proposed scheme is further verified in the experimental platform, as shown in Fig. 11. The rectifier is controlled by using a digital-signal processor (TMS320F28377D) and a field-programmable gate array (10M16SAE144). The experimental parameters and operating conditions are kept the same as those in simulations. Notably, the waveform of the reference signal v'_a is observed by the digital-to-analog converter of the controller.

Fig. 12 shows the steady-state experimental waveforms of key parameters under two cases, including phase currents, line voltage, phase voltage, dc voltages, and reference signals. The line voltage V_{ab} contains nine levels and five levels under $m = 0.9$ and 0.5, respectively. There always exist some time intervals when v'_a is clamped to 1, -1, 0. Correspondingly, the phase A leg voltage V_{an} is fixed at 125 V, 0 V, and -125 V, respectively, in these time intervals with no switching actions, which significantly reduces the switching loss. With balanced loads in Fig. 12(a) and (c), the NP current is near zero by alternating switching positive/negative clamping modes. The waveforms of v'_a and V_{an} are symmetrical. With unbalanced loads in Fig. 12(b) and (d), more negative and positive clamping modes are selected to provide negative and positive NP currents, respectively, for dual loads to keep the dc-link balanced. The waveforms of v'_a and V_{an} are no longer symmetrical. Three-phase currents always behave as perfect sinusoidal waveforms with low harmonics (THDi = 2.3%, 2.4%, 2.5%, and 2.3%) by adopting the proposed scheme. The experimental results are consistent with the previous simulations.

Fig. 13 shows the waveforms of dynamic FC voltage regulation. Initially, the FC voltage of Phase A is controlled at 80 V in Fig. 13(a) and 40 V in Fig. 13(b), respectively. After a few tens of milliseconds, the reference value is suddenly changed to $0.25V_{\rm dc}$ (62.5 V). It can be clearly seen that the FC voltage takes about one fundamental period to reach the set value, and no obvious current distortions occur during the dynamic regulation. The experimental results verified the strong FC voltage balancing capability of the proposed scheme.

Fig. 14 verifies the dynamic performance of the proposed scheme under sudden load change. At initial, the dc loads are balanced. Hence, the average NP current is zero. Suddenly, R_2 jumps from 21 to 16 Ω in Fig. 14(a) and R_1 jumps from 21 to 15 Ω in Fig. 14(b), lead to the NP current jumping to 1.9 A and -2.4 A, respectively. Redundant clamping modes with different effects on the NP are chosen according to the upper

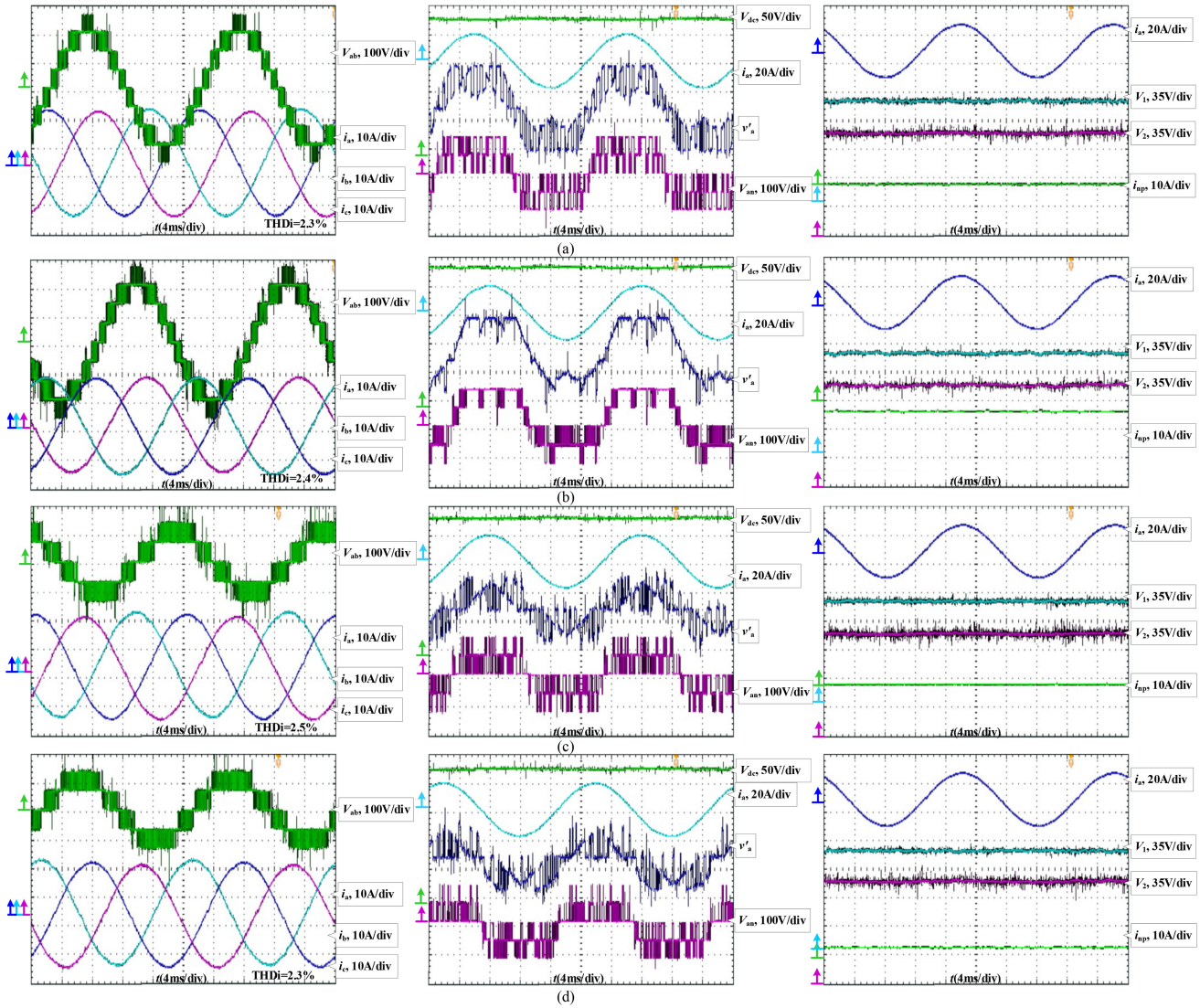

Fig. 12. Various steady-state experimental waveforms ($\Delta_{\rm band} = 2$ V). (a) $m = 0.9$ with balanced loads ($R_1 = R_2 = 12\ \Omega$). (b) $m = 0.9$ with unbalanced loads ($R_1 = 10\ \Omega$ and $R_2 = 15\ \Omega$). (c) $m = 0.5$ with balanced loads ($R_1 = R_2 = 21\ \Omega$). (d) $m = 0.5$ with unbalanced loads ($R_1 = 30\ \Omega$ and $R_2 = 15\ \Omega$).

voltage deviation ΔV_1. It can be clearly seen that V_1 is always stable at the set value regardless of the sudden change in R_1 or R_2, and V_2 decreases at first and then gradually returns to the set value. After a dozen fundamental periods, V_2 is rebalanced.

To verify the efficiency advantage of the proposed carrier-based DPWM scheme intuitively, Table V presents the efficiency comparison of the proposed DPWM scheme and the CPWM scheme based on zero-sequence injection in [32] under different load conditions. It can be obviously observed that the efficiency of the proposed scheme is higher regardless of whether the dual dc loads are balanced or not. Experiments fully verified the high-efficiency characteristic of the proposed scheme.

The execution times of different parts are also measured, as shown in Table VI. Proportional–integral (PI) controller and proportional–resonant (PR) controller are, respectively, used for the outer voltage loop and inner current loop in this article. It can be clearly seen that the proposed carrier-based DPWM method does not take up much of the microcontroller's execution time (about 16 μs), which is totally acceptable.

TABLE V
EFFICIENCY COMPARISON OF TWO MODULATION METHODS UNDER DIFFERENT LOAD CONDITIONS

(R_1, R_2)	V_{ab}=100V, V_{dc}=250V		(R_1, R_2)	V_{ab}=140V, V_{dc}=250V	
	Proposed DPWM	CPWM in [32]		Proposed DPWM	CPWM in [32]
(24Ω,24Ω)	90.6%	89.2%	(18Ω,18Ω)	92.4%	92.1%
(27Ω,27Ω)	91.8%	90.6%	(21Ω,21Ω)	93.3%	92.8%
(30Ω,30Ω)	92.8%	91.8%	(24Ω,24Ω)	94.6%	94.2%
(27Ω,21Ω)	90.5%	90.1%	(15Ω,21Ω)	92.0%	91.5%
(30Ω,24Ω)	91.4%	90.3%	(18Ω,27Ω)	94.0%	93.3%
(33Ω,21Ω)	90.7%	90.1%	(21Ω,30Ω)	95.1%	94.3%
(27Ω,33Ω)	92.9%	91.7%	(27Ω,18Ω)	93.7%	93.6%
(24Ω,30Ω)	91.6%	90.5%	(24Ω,15Ω)	92.4%	91.8%
(27Ω,30Ω)	92.3%	91.1%	(30Ω,18Ω)	94.0%	93.9%

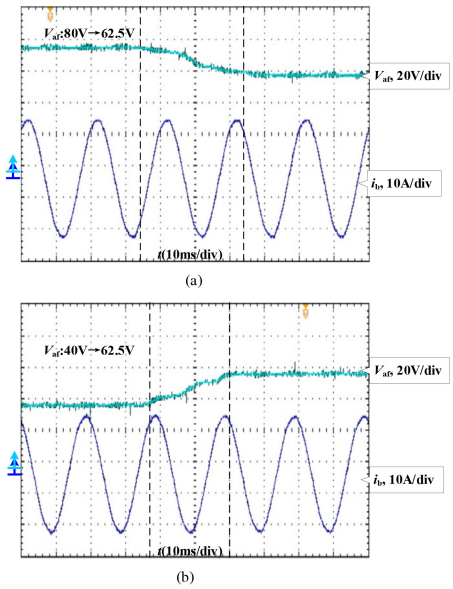

Fig. 13. Experimental waveforms of dynamic FC voltage regulation ($V_{ab} =$ 138 V(rms) and $V_{\rm dc} = 250$ V). (a) $V_{af} = 80$ V→62.5 V. (b) $V_{af} = 40$ V→62.5 V.

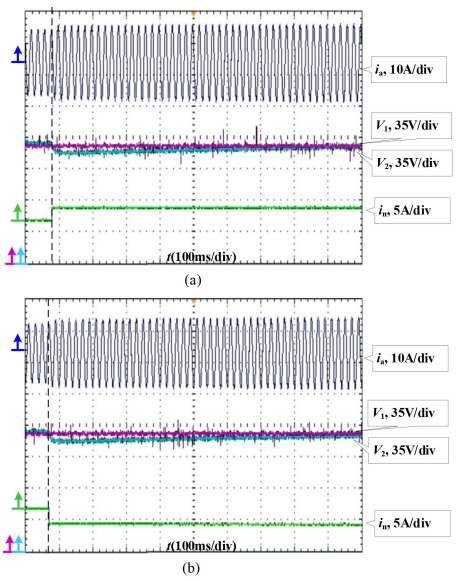

Fig. 14. Experimental waveforms with sudden load change. (a) ($V_{ab} = 110$ V(rms), $V_{\rm dc} = 250$ V, $R_1 = 21\ \Omega$, and R_2: 21 Ω→16 Ω). (b) ($V_{ab} = 120$ V(rms), $V_{\rm dc} = 250$ V, R_1: 21 Ω→15 Ω, and $R_2 = 21\ \Omega$).

TABLE VI
EXECUTION TIMES OF DIFFERENT PARTS

Different parts	AD sampling	Outer voltage loop (PI)	Inner current loop (PR)	Proposed carrier-based DPWM scheme	Total time
Execution time	8.6μs	0.9μs	3.8μs	16μs	29.3μs

V. CONCLUSION

A carrier-based DPWM scheme with optimal PWM sequences is presented in this article to reduce the switching losses and balance capacitor voltages for 5L-FC rectifiers. Since there is always one pair of redundant switching modes in each region, the NP voltage is fully controllable during the whole fundamental period, even with unbalanced dc loads, further expanding the application scenarios. The PWM sequences are also optimally redistributed for minimal switching transitions. Besides, the permissible range of unbalanced loads is investigated in detail, providing a reference for industrial applications. Simulation and experimental results firmly validated the improvement of efficiency and reliability under the proposed DPWM scheme. As the proposed scheme is realized by directly injecting the clamping compensation component, it is relatively easy to implement with low calculation burden compared with the traditional space-vector-based schemes. And in order to expand the allowable range of unbalanced loads in practical applications, the modulation index should be reserved for a certain margin.

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