A Bidirectional Five-Level Buck PFC Rectifier With Wide Output Range for EV Charging Application

Anekant Jain, *Member, IEEE*, Krishna Kumar Gupta, *Member, IEEE*, Sanjay K. Jain, *Member, IEEE*, and Pallavee Bhatnagar, *Senior Member, IEEE*

***Abstract*—AC-to-DC conversion is integral to the two-stage charging interface of electric vehicle (EV) batteries. For such chargers, the use of multilevel rectifiers (MLRs) reduces voltage ratings of power switches, while achieving a high-quality input voltage waveform. Balancing of capacitors in MLRs, however, is an important challenge. In this work, a power factor correction (PFC) five-level rectifier with self-balanced switched capacitors is proposed. Each leg of the presented topology comprises five power switches and one switched capacitor, where the voltage ratings of power switches are equal to the output dc voltage. It does not require an additional filter capacitor on the dc side, as the load appears in parallel always with a switched capacitor of one of the legs. The five-level operation with continuous conduction leads to the elimination of the capacitive filter on the ac-side and inductive filter on the dc-side. This article presents the operating principle, modulation strategy, closed-loop control, and design aspects of the proposed rectifier. The proposed topology is validated through experimental results and a comparison is made with other topologies. Following three features of the proposed topology make it suitable for EV battery charging applications—buck operation with a wide output regulation, the possibility of bidirectional flow of power needed for vehicle-to-grid systems, and easy realization of its three-phase version by simply adding one more leg. These features too have been demonstrated with experimental results.**

***Index Terms*—Buck rectifier, electric vehicle (EV) charging, multilevel converter, multilevel rectifier, power factor correction (PFC), switched capacitors, vehicle to grid (V2G).**

I. Introduction

THIS section summarizes a brief literature review and highlights the research motivation and objectives. For better readability and understanding, this part has been categorized into different sections.

Manuscript received 27 October 2021; revised 1 March 2022 and 26 May 2022; accepted 13 June 2022. Date of publication 23 June 2022; date of current version 26 July 2022. The work was supported in part by the Ministry of Electronics and Information Technology (MeitY), Govt. of India under the National Mission on Power Electronics Technology (NaMPET-III) Project NaMPET-III/SP25/NH-EXP-05 and in part by Thapar Institute of Engineering and Technology (TIET), Patiala under Grant TU/DORSP/57/7215 Recommended for publication by Associate Editor D. Zhang. *(Corresponding author: Anekant Jain.)*

Anekant Jain, Krishna Kumar Gupta, and Sanjay K. Jain are with the Thapar Institute of Engineering and Technology, Patiala 147004, India (e-mail: ajain_phd19@thapar.edu; kk_mact@rediffmail.com; skjain@thapar.edu).

Pallavee Bhatnagar is with the IES College of Technology, Bhopal 462008, India (e-mail: pallaveebhatnagar9@gmail.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3185239.

Digital Object Identifier 10.1109/TPEL.2022.3185239

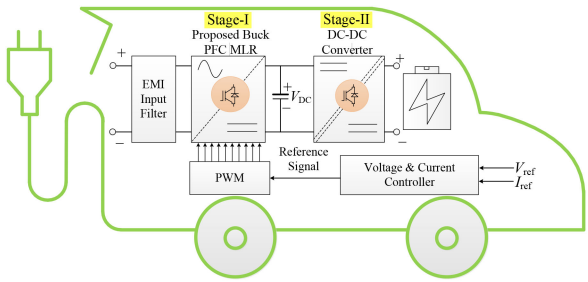


Fig. 1. Basic block diagram of level-2 on-board charging.

A. AC-to-DC Conversion in Emerging Interfaces for Electrical Vehicle Charging

The power electronics interface of an electric vehicle (EV) charging system generally comprises two stages: a power factor correction (PFC) rectifier stage, followed by a dc-to-dc converter [1]. The PFC stage aims at synthesizing sinusoidal input current in-phase with the supply voltage and performs ac-to-dc conversion to obtain a regulated output [2]. The dc-to-dc converter is used to regulate the current supply for the EV battery corresponding to its state-of-charge (SoC) and to match the dc-link and the EV battery voltages [1]. Many a times, an electromagnetic interference (EMI) input filter is also required between the ac source and the PFC stage [3]. All these constituents of the charging systems (viz., power converters and filters) can be integrated into the vehicle itself, leading to an on-board charging system, or they can be placed in a specially designed EV charging station as an off-board system [4]. Standards such as IEC61851 and IS17017 offer guidelines on power levels and voltages for such EV charging systems [1]. Depending on the power requirements, these charging systems are fed with single-phase or three-phase ac power [5]. For example, in the level-2 on-board EV battery charging (exemplified in Fig. 1 in a simplistic manner), a single-phase ac supply is used for the charging power ranging between 2 and 8 kW (typically rated at 32 A), while three-phase ac supply is used for a charging power of 19.2 kW (typically rated at 80 A) [5]. Similarly, three-phase systems are employed for off-board charging systems based on the power needs [6]. Thus, the conceptualization of the power converter for the PFC stage begins with the consideration of the ac supply, whether it is single-phase or three-phase.

Also at the PFC stage in EV charging systems, buck-type rectifiers are being increasingly advocated to achieve a wider control-range for the output voltage and to reduce the step-down

requirement in the dc-to-dc conversion stage [7]. Buck-rectifiers also enable the usage of low voltage power switches in the downstream dc-to-dc converter, leading to an increased efficiency and better design flexibility, especially when galvanic isolation is to be employed [8]. Another important consideration nowadays has been to impart the capability of bidirectional power flow to the charging interface so as to allow both G2V and V2G modes [9]. V2G systems can provide additional opportunities for grid operators [10], including reactive power support, active power regulation, load-balancing [11], peak shaving, and current harmonic filtering. They can also improve the technical performance of the grid in areas such as efficiency, stability, and reliability [12]. Hence, at the hindsight, it can be said that in the contemporary EV charging interfaces, the most desirable characteristics for a PFC rectifier topology are the following: 1) it should achieve buck operation; 2) it should allow bidirectional flow of power; and 3) its structure should be easy to extend for a three-phase ac input.

B. Emergence of Multilevel PFC Rectifiers

Now, numerous PFC rectifier topologies have been proposed and reviewed at length [13]–[16], including those which are targeted for application-specific needs, such as on-board EV chargers [17], electric drives [18], data centres [19], lighting [20], etc. These rectifiers are normally categorized into major groups, namely, PFC boost rectifiers, PFC buck rectifiers, and PFC buck–boost rectifiers [21].

1) PFC Boost Rectifiers: "Boost" here refers to the fact that in this class of rectifiers, the magnitude of the output dc voltage is greater than the peak value of the input ac voltage [22], [23]. The resulting dc voltage, in general, is too high to directly feed the dc-bus of EV battery, and hence either a subsequent step-down dc–dc converter is employed at the dc side, or a step-down transformer is introduced at the ac side. Both these approaches, however, add to the volume, costs and power losses in the system. At the same time, to provide a constant output dc voltage and UPF operation at the input, boost PFC rectifiers do not require bulky filters either at the ac side or the dc side.

2) PFC Buck Rectifiers: "Buck" here refers to the fact that in this class of rectifiers, the magnitude of the output dc voltage is lower than the peak value of the input ac voltage. Buck-type rectifiers provide a wider control range for the output dc voltage, as compared to the boost-type rectifier topologies [7], [8]. PFC buck rectifiers, however, generally exhibit discontinuous conduction mode (DCM), due to which the regulation of output voltage becomes difficult. Moreover, DCM makes the regulation of output voltage dependent on the load impedance, and thus, necessitates large filters on the dc side.

3) PFC Buck–Boost Rectifiers: "Buck-boost" type of rectifiers can operate in buck as well boost mode [24]. Many a times, they employ a low number of semiconductors and integrate the magnetic elements to reduce the total size and volume of the converter [25], [26]. Newly proposed topologies, such as the Ferdowsi rectifiers [25], use a low number of controlled switches to achieve low total-harmonic-distortion (THD) in the input current. In many cases, however, bridge-less buck–boost rectifiers do not offer the possibilities of bidirectional power flow and easy extension to three-phase ac systems [24]–[26].

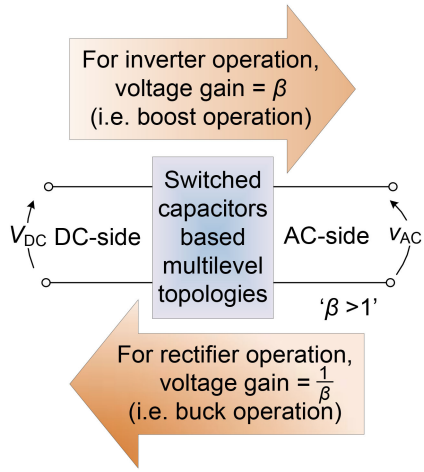


Fig. 2. Role reversal in switched capacitors-based multilevel topologies.

Another categorization of PFC rectifiers is in terms of the number of levels of the input side voltage waveform. This is due to the fact that a grid-connected voltage source rectifier synthesizes a voltage in order to control the grid current, and hence if the synthesized voltage is improved by increasing the number of voltage levels, the grid current can be consequently improved [17]. These rectifiers are known as "multilevel rectifiers (MLRs)." As compared to the nonmultilevel rectifiers, MLRs offer attractive advantages, such as lower voltage ratings of power switches, much better harmonic profile of the input waveform, reduced dv/dt stress, possibility of fault-tolerant operation, and so on. The conventional MLRs (viz., neutral point clamped, flying capacitors and Vienna rectifiers) operate as boost-rectifiers [22], [23], [27], [28], though some novel MLRs operate as buck rectifiers, as discussed in the next section.

C. Multilevel Bidirectional PFC Rectifiers With Buck Characteristics

To the best of the authors' knowledge, very limited literature is available on multilevel buck rectifiers [29]–[31]. These rectifiers operate in continuous-conduction mode (CCM) and generate a multilevel voltage waveform at the input. Due to CCM operation, commonly used ac-side capacitive and dc-side inductive filters are removed. The buck rectifier proposed in [30] is based on the cascaded H-bridge (CHB) topology and provides multiple dc outputs. For the CHB structure, on the ac side, each module must interact with the others to obtain an almost sinusoidal current in phase with the grid voltage. On the dc side, each capacitor's voltage must be stable and controlled. Balancing the capacitor output voltage requires multiple voltage sensors and a complex control strategy. In [29], Vahedi *et al.* have presented a five-level buck rectifier, which is bidirectional in nature. In order to balance the voltages of the two capacitors, two voltage sensors are needed to implement a complex control methodology. Moreover, it requires power switches of high voltage ratings equal to twice the output dc voltage. In addition, the topology in [29]

cannot be directly extended to its three-phase version. Another buck topology proposed in [31] is a nine-level converter, which is primarily based on the original inverter topology described in [32]. The control methodology in [31] is such that the structure does not utilize the switched-capacitors principle, and hence, voltage balancing of capacitors becomes challenging. In [31], the authors use finite switching set mode predictive control to regulate the dc voltages and to track the desired reference of the input ac current. This requires four voltage sensors and four current sensors to balance the capacitor voltage and improve the PFC. Another drawback of the topology in [31] is the requirement of high voltage rated power switches and difficulty in extension to three-phase version. Hence, both these rectifiers of [29] and [31] are characterized by three important limitations—voltage ratings of the switches are different and higher, balancing of voltages is extremely complex (involving multiple sensors and cumbersome real-time computation), and three-phase extensions are not possible directly.

D. Motivation and Objectives of the Work Proposed in This Article

In the light of the previous discussions, it can be concluded that there remains an ample scope of conceptualizing novel topologies for EV charging applications with following features: 1) to achieve buck operation along with power factor correction and wide range of output voltage; 2) synthesis of multilevel voltage at the ac side; 3) ability for bidirectional flow of power; 4) easy balancing of capacitors' voltages; and 5) possibility of easy extension for three-phase application.

In order to achieve these objectives, the authors propose to examine the features of the so-called "switched capacitors-based multilevel topologies" [33], which have been hitherto proposed as inverters [34]. These topologies use switched-capacitors to synthesize additional voltage levels at the output of the inverter, while at the same time, they enable an inherent voltage gain greater than one, and thereby achieving a "boost" operation as inverter. This is so because a switched capacitor is charged by bringing it in parallel with the input dc source. Thereafter, another switching combination brings it in series with the dc source, while they are connected to the ac load. Hence, these topologies offer the advantages of multilevel inverters, while providing additional advantages of inherent boost and self-balanced capacitors. Consider a simple single-phase system with V_{DC} as the dc side voltage and V_{AC} as the ac side multilevel voltage, with the voltage gain as β (see Fig. 2). Then, the peak value of the fundamental component of the multilevel voltage would be given as [35] and [36]

$$v_{\mathrm{AC},1}^{\max} = M.\beta.V_{\mathrm{DC}} \tag{1}$$

where M is the modulation index with $0.5 \leq M \leq 1$.

Now, for a rectification system based on the switched-capacitors, the peak value of the grid voltage ($v_{\mathrm{g}}^{\max}$) will replace $v_{\mathrm{AC},1}^{\max}$, while the output dc voltage (V_{DC}) can be expressed using (1) as

$$V_{\mathrm{DC}} = \frac{v_{\mathrm{g}}^{\max}}{M.\beta}. \tag{2}$$

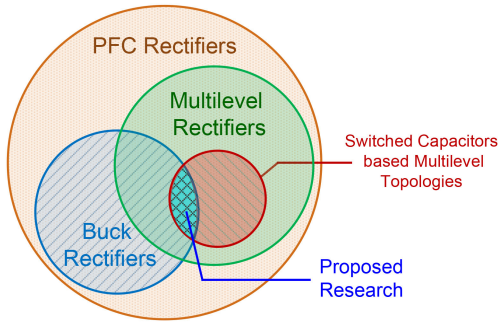


Fig. 3. Pertaining to the research proposed in this work.

The above expression indicates that for $\beta > 1$, the output dc voltage would be less than the peak value of the grid voltage, thereby allowing the ac-to-dc conversion to be of buck nature. This expression also indicates that in the conventional multilevel topologies where the voltage gain is unity (i.e., $\beta = 1$), the output dc voltage is greater than the peak value of the grid voltage, and hence, they act as boost rectifiers.

Based on (2), it can be said that when operated as a PFC rectifier, switched capacitors-based multilevel topologies should perform buck operation and can be called as "switched capacitors-based multilevel rectifiers (SCMLRs)." Some of the switched capacitors-based multilevel inverters (SCMLIs) [37], [38] can perform rectification, only if the diodes are replaced with controlled switches. Moreover, most of the SCMLI topologies cannot be easily extended to their three-phase version, as described in detail in [37]. While many others, which can be bidirectional and extended to three-phase versions, have limitations in terms of large peak-inverse-voltage (PIV) of power switches [39], large number of semiconductor devices, and large total-standing-voltage [39], [40]. Therefore, in this work, a novel SCMLR is conceptualized with the following features.

1) It works as a buck rectifier with power factor correction, while providing a wide output range.
2) It synthesizes five levels at the input side, thereby greatly improving the harmonic profile of the waveform. For all the switching states, one of the switched capacitors is in parallel with the load terminals and hence, no additional filter capacitor is required at the dc output.
3) It requires power switches of equal voltage ratings, because the PIV rating of all the power switches is equal to the output dc voltage.
4) It does not require any additional balancing circuitry since the capacitors are self-balanced. Moreover, the voltage of only one of the switched capacitors is required to be sensed to implement a closed loop control.
5) It operates in continuous conduction mode (CCM) as buck rectifier, thereby eliminating the bulky filters.
6) It allows bidirectional flow of power, and hence it can be employed to implement a V2G interface for EV charging.
7) It can be easily extended to a three-phase version.
8) It acts as a boost rectifier for low modulation indices ($<$ 0.5). Although in this case, it synthesizes only three levels at the input terminals.

The proposed research is summarized in Fig. 3, mainly to emphasize that the switched capacitors-based topologies are a special class of multilevel structures, which are being explored here for the purpose of achieving multilevel buck rectification.

E. Organization of This Article

This rest of this article is organized as follows. Section II presents the proposed topology, Section III deals with the control scheme, and Section IV deals with the converter design. Thereafter, Section V deals with a detailed comparison with other topologies. Section VI summarizes the experimental investigations for possible applications. Finally, Section VII concludes this article.

II. Proposed Five-Level Buck Rectifier

The proposed rectifier topology is shown in Fig. 4, wherein two legs "A" and "B" are shown. The ac input voltage is given at the terminals "a" and "b," while the dc output voltage is obtained between the terminals "p" and "n," with "p" being the higher potential terminal. The output voltage is shown as "$V_{\rm DC}$." Each leg has five active switches and one capacitor, which is maintained at a voltage equal to $V_{\rm DC}$. The pole voltages ("$V_{\rm an}$" and "$V_{\rm bn}$"), thus, have three voltage levels: $+2\,V_{\rm DC}$, $+V_{\rm DC}$ and 0. Of the five switches in a leg, say the leg A, the pairs $(A_1, \overline{A_1})$ and $(A_2, \overline{A_2})$ are complementary, while the switch A_3 operates simultaneously with $\overline{A_2}$. That is, if "1" corresponds to "ON" state and "0" corresponds to "OFF" state of a switch

$$\begin{aligned} \overline{A_1} &= 1 - A_1 \\ \overline{A_2} &= 1 - A_2 = A_3. \end{aligned} \tag{3}$$

The voltage $V_{\rm ab}$ can, thus, be expressed as

$$V_{\rm ab} = V_{\rm an} - V_{\rm bn}. \tag{4}$$

Since the pole voltages $V_{\rm an}$ and $V_{\rm bn}$ have three levels, the line voltage $V_{\rm ab}$ manifests five levels viz., $\pm 2\,V_{\rm DC}$, $\pm\,V_{\rm DC}$ and 0.

In this proposed SC-based rectifier, the value of β is 2. From (2) the output dc voltage can therefore be express as

$$V_{\rm DC} = \frac{v_{\rm g}^{\rm max}}{2M}. \tag{5}$$

Equation (5) suggests that the output dc voltage will be equal to the peak grid voltage $v_{\rm g}^{\rm max}$ for $M = 0.5$. The value of $V_{\rm DC}$ will be less than $v_{\rm g}^{\rm max}$ for M greater than 0.5, and therefore the proposed converter will perform buck rectification. During over modulation, where M exceeds unity, the output voltage will approximate a square waveform, where-in the fundamental ac side waveform acquires a maximum value of $(4/\pi)$ times the peak dc side voltage (i.e., $2V_{\rm DC}$) [36], indicating that $V_{\rm DC}$ can achieve a maximum value equal to $(\pi/8)$ times $v_{\rm g}^{\rm max}$. It is observed that $V_{\rm DC}$ exceeds $v_{\rm g}^{\rm max}$ during under modulation ($M < 0.5$) thereby performing boost operation. As described later, it will be seen that only three levels will be synthesized for $M < 0.5$, in which the voltage $V_{\rm ab}$ manifests the levels viz., $\pm V_{\rm DC}$ and 0, and hence, acts as three-level boost rectifier. The above discussion can be summarized as following results for the output voltage $V_{\rm DC}$:

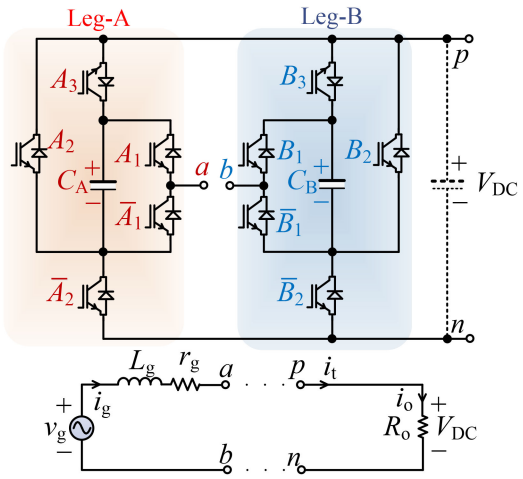


Fig. 4. Proposed five-level PFC rectifier topology (single-phase).

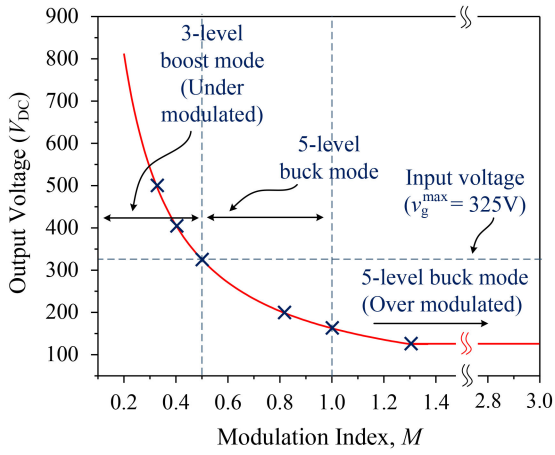


Fig. 5. Variation of the output voltage with respect to modulation index.

$$\frac{v_{\rm g}^{\rm max}}{2} \le V_{\rm DC} \le v_{\rm g}^{\rm max} \tag{6}$$

for $0.5 \le M \le 1$, five-level buck operation

$$\frac{\pi v_{\rm g}^{\rm max}}{8} < V_{\rm DC} < \frac{v_{\rm g}^{\rm max}}{2} \tag{7}$$

for $M > 1$, five-level buck operation (overmodulation) and

$$V_{\rm DC} > v_{\rm g}^{\rm max} \tag{8}$$

for $M < 0.5$, three-level boost operation.

Output voltage variation in terms of modulation index is shown in Fig. 5, for input rms ac voltage of 230 V (i.e., peak value of 325 V).

TABLE I
SWITCHING STATES OF THE PROPOSED FIVE-LEVEL RECTIFIER

State	i_g	Leg-A			Leg-B			$V_{ab} = V_{an} - V_{bn}$	Capacitors	
		Switches		$V_{an} = (A_1 + A_2)V_{DC}$	Switches		$V_{bn} = (B_1 + B_1)V_{DC}$			
		A_1	A_2		B_1	B_1			C_A	C_B
St_1	$i_g > 0$	1	1	$+2V_{DC}$	0	0	0	$+2V_{DC}$	C	C
St_2	$i_g > 0$	1	0	$+V_{DC}$	0	0	0	$+V_{DC}$	C	D
St_3	$i_g \geq 0$	0	0	0	0	0	0	0	D	D
St_4	$i_g \leq 0$	0	0	0	0	0	0	0	D	D
St_5	$i_g < 0$	0	0	0	1	0	$+V_{DC}$	$-V_{DC}$	D	C
St_6	$i_g < 0$	0	0	0	1	1	$+2V_{DC}$	$-2V_{DC}$	C	C

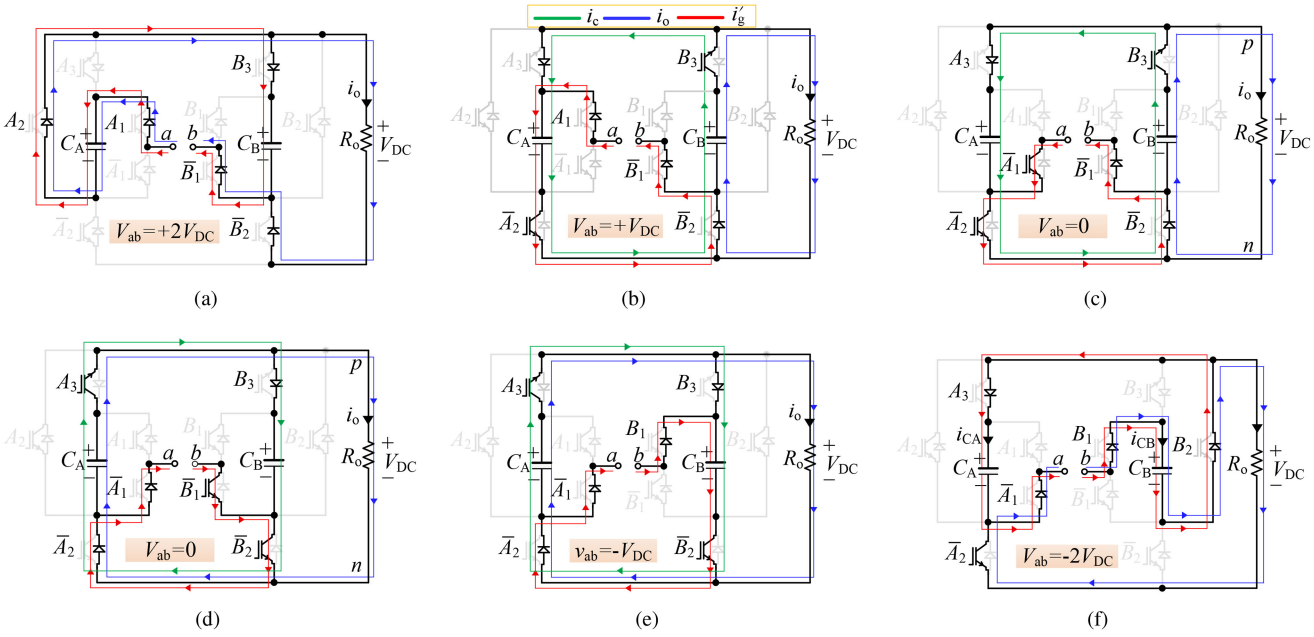


Fig. 6. Switching states for the proposed five-level buck rectifier. (a) State St_1. (b) State St_2. (c) State St_3. (d) State St_4. (e) State St_5. (f) State St_6.

A. *Description of Five-Level Buck Mode (0.5 < M < 1)*

All the valid operating states for the proposed rectifier are summarized in Table I, where ON and OFF states of a power switch are shown with "1" and "0," respectively, and charging and discharging states of the capacitors are shown with "C" and "D," respectively. There in, conduction paths of three currents are shown: i_o is the load current, i_c is the intercapacitors current and i'_g is the ac component drawn from the grid. These currents are, respectively, shown in blue, green, and red colors. Various switching states for the proposed rectifier are described herewith.

1) State St_1 ($V_{ab} = +2\,V_{DC}$): During this state, in the positive half cycle, the switches A_1, A_2, $\overline{B_1}$, $\overline{B_2}$, and B_3 are simultaneously turned ON, so as to achieve two simultaneous conduction paths as shown in Fig. 6(a). In the path shown with red, it can be seen that the $V_{ab} = +2\,V_{DC}$. Both the capacitors get charged from the ac source.
2) State St_2 ($V_{ab} = +V_{DC}$): During this state, in the positive half cycle, the switches A_1, $\overline{A_2}$, A_3, $\overline{B_1}$, $\overline{B_2}$, and B_3 are simultaneously turned ON, so as to achieve three simultaneous conduction paths as shown in Fig. 6(b). The capacitor C_A is in charging state and the capacitor C_B is in parallel with the load. Both the capacitors too are in parallel due to which an inter-capacitors current flows to balance their voltages.
3) State St_3 and St_4 ($V_{ab} = 0$): During this state, in the positive and negative half cycle, the switches $\overline{A_1}$, $\overline{A_2}$, A_3, $\overline{B_1}$, $\overline{B_2}$, and B_3 are simultaneously turned ON, so as to achieve three simultaneous conduction paths as shown in Fig. 6(c) and (d). In these states, $V_{ab} = 0$. For the positive half cycle, capacitor C_B is in parallel with the load, while during the negative half cycle, capacitor C_A is in parallel with the load. Once again, in both the states, the intercapacitors current balances the voltages of the two capacitors.
4) State St_5 ($V_{ab} = -V_{DC}$): During this state, in the negative half cycle, the switches $\overline{A_1}$, $\overline{A_2}$, A_3, B_1, $\overline{B_2}$, and B_3 are simultaneously turned ON, so as to obtain $V_{ab} = -V_{DC}$. As shown in Fig. 6(e), the capacitor C_B is in charging state and the capacitor C_A is in parallel with the load. The

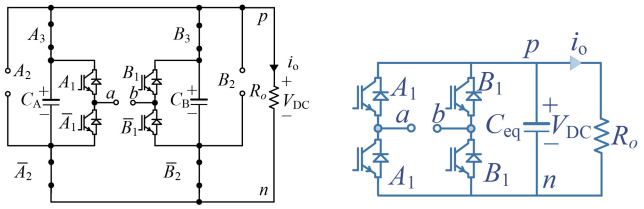


Fig. 7. Equivalent circuits of the proposed rectifier for boost mode of operation ($M < 0.5$).

voltages of the capacitors are balanced by the intercapacitors current.

5) State St_6 ($V_{ab} = -2\,V_{DC}$): During this state, in the negative half cycle, the switches $\overline{A_1}$, $\overline{A_2}$, A_3, B_1, and B_2 are simultaneously turned ON, so as to obtain $V_{ab} = -2\,V_{DC}$. As shown in Fig. 6(f), both the capacitors are in the charging state.

In this range of modulation index ($0.5 < M < 1$), the proposed topology operates in buck mode and generates five voltage levels at the input terminals of the rectifier.

B. Description of Three-Level Boost Mode ($M < 0.5$)

While the proposed topology is primarily a buck converter, it can perform boost operation as well, albeit with the synthesis of three levels instead of five. This warrants a discussion, especially from the point of view of switching states. The equivalent circuit for the boost mode of operation is shown in Fig. 7.

For $M < 0.5$, the states $\pm 2\,V_{DC}$ are not synthesized at the input terminals. This is so, because only switches A_1, $\overline{A_1}$, B_1, $\overline{B_1}$ operate, while switches A_2 and B_2 are permanently OFF and switches $\overline{A_2}$, $\overline{B_2}$, and A_3, B_3 are permanently ON, as shown in Fig. 6(b)–(e). Here, C_A, C_B are in parallel with an equivalent capacitance of C_{eq}. It can be observed that the operating states for boost-mode are similar to the operation of the H-bridge rectifier. Boost mode of operation generates a three-level voltage at the input of the rectifier viz., $+V_{DC}$, 0, and $-V_{DC}$. Operating states of this mode are same as $St_2 - St_5$.

III. Control and Modulation Technique

A. Multicarrier Pulsewidth Modulation (PWM) Technique

For the modulation of MLRs, different techniques have been used, including high switching frequency techniques (such as multicarrier PWM and space vector PWM) and low switching frequency methods (such as active harmonic elimination, selective harmonic elimination and nearest level control) [41]. The proposed MLR can be modulated with any of these techniques with appropriate adaptation. In the proposed work, a level-shifted PWM (LSPWM) scheme is employed for the gating signal generation, as shown in Fig. 8. A reference waveform (V_{ref}) of frequency (f_{ref}) is taken as the reference signal which is generated by the voltage controller and its absolute value $|V_{ref}|$ is compared with the two high-frequency triangular carrier waveforms v_{cr1} and v_{cr2}.

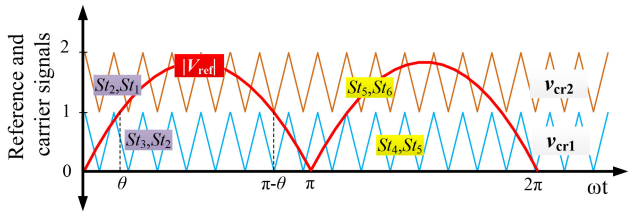


Fig. 8. Level-shifted modulation scheme for the proposed rectifier.

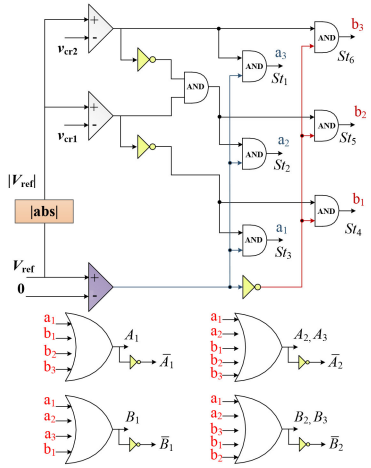


Fig. 9. Logic gates-based generation of switching signals.

During $0 \le \omega t \le 2\pi$, requirements of various operating states are shown in Fig. 8. During $0 \le \omega t \le \pi$, when v_{cr1} is compared with $|V_{ref}|$, the input voltage levels are (0 and V_{DC}) which are to be obtained by generating signals for states St_3 and St_2. Similarly, when v_{cr2} is compared with $|V_{ref}|$, the input voltage levels are V_{DC} and $2\,V_{DC}$, which are to be obtained by generating signals for states St_2 and St_1. For the remaining half cycle, during $\pi \le \omega t \le 2\pi$, the states for the negative half cycle are to be generated. When v_{cr1} and v_{cr2} are compared with $|V_{ref}|$, the output voltage levels are 0, $-V_{DC}$ and $-V_{DC}$, $-2\,V_{DC}$, which are to be obtained by generating signals for states St_4, St_5 and St_5, St_6, respectively. Logic gates-based switching pulse generation is shown in Fig. 9.

B. Controller Design

In a rectifier circuit, using hysteresis current controller, the grid current is shaped into a sine wave. By using this controller, switching complications occurs like large and variable switching frequency which increases power losses [42], [43]. For the proposed rectifier topology, a simple controller including two cascaded loops is designed for the generating the switching pulses. The inner loop is used for grid-current control and the outer loop is for regulating the output voltage. Primarily, the ac grid average current is shown in [28], [44], and [45]

$$L_g \frac{di_g}{dt} = v_g - r_g i_g - V_{ab} = v_g - r_g i_g - DV_{DC} \tag{9}$$

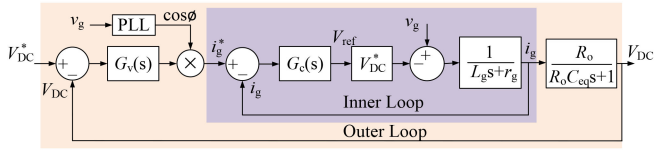


Fig. 10. Inner and outer loops for voltage and current controllers.

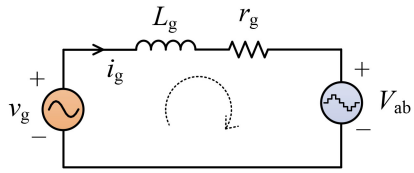


Fig. 11. Model of the conversion system for inductive filter design.

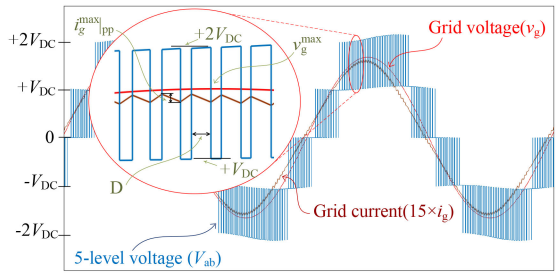


Fig. 12. Waveforms pertaining to the design of filter inductor.

where L_g is the grid inductor and r_g is that inductor parasitic resistance, and D is the buck rectifiers duty cycle. The small-signal model of (9) can be converted into Laplace domain by assuming a constant value of grid voltage (v_g), and averaged value of grid current and duty cycle

$$L_g s i_g = -i_g r_g - D V_{DC}^*. \tag{10}$$

As the inner loop should be faster than the outer loop, it is appropriate to consider the outer loop value, which is the dc voltage, to be constant. The following transfer function is obtained for the grid-connected rectifier inner loop using a dc voltage reference value V_{DC}^*, indicating that the dc voltage output, inductive filter value, and line impedance affect the grid ac current

$$\frac{i_g}{D} = \frac{-V_{DC}^*}{L_g s + r_g}. \tag{11}$$

Fig. 10 shows the inner and outer loops of the controller. Where, in the inner loop, current controller $G_c(s)$ can be either a simple gain as a proportional controller or a proportional integral (PI) controller. It should be noted that the inner loop should have a faster dynamics than the outer loop. Therefore, in the case of a sinusoidal input current signal using a PI controller, the integral gain of that PI should be minimal enough not to change the inner loop's speed. However, the use of a PI compensator on a sinusoidal signal creates some steady-state errors that can be seen as a dc component in the current harmonic spectrum. A proportional resonant (PR) controller with an infinite gain at the grid frequency (f_{ref}), which shows zero steady-state error, is one alternative for such situation [46]. Furthermore, another loop should be added to the controller to regulate the output dc voltage. Equations from the dc side of the rectifier should be examined to obtain the system model for the outer loop

$$i_g = i_{c_{eq}} + i_o C_{eq} \frac{dV}{dt} = i_g - \frac{V_{DC}}{R_o} \tag{12}$$

where the capacitors are parallel equivalent to C_{eq} and load current is i_o. The following transfer function for the outer loop will be accomplished by small-signal modeling of (12) conversion to s-domain. The relationship between the output dc voltage, value of the load resistance and dc capacitor value is shown by transfer function

$$\frac{V_{DC}}{i_g} = \frac{R_o}{R_o C_{eq} s + 1}. \tag{13}$$

The voltage controller can be considered the outer loop due to the relationship between i_g and V_{DC} as (13). Such loops deliver the idea of a cascaded controller in which an input for the inner loop is the output of the outer loop. As there is no frequency in the dc signal, a PI compensator with a $G_v(s)$ transfer function is used to control the voltage at the desired level. The voltage control system controls the output dc voltage at V_{DC}^*, as shown in Fig. 10, and provides the reference current peak value as an input to the inner loop. Due to its low complexity and adequate accuracy, the controller shown in Fig. 10 can be easily implemented with real-time controllers.

IV. Design Parameters, Component Ratings, Total Stored Energy, and Loss Analysis

A. Design Parameters

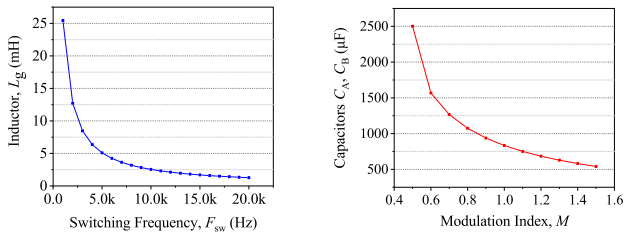
1) Filter Inductor (L_g) for the Input Side: Inductive filter is modeled as a series connection of an inductor L_g and equivalent series resistance r_g. As filter inductor bears the grid current i_g, the value of L_g mainly depends on the allowable maximum input current ripple, Δi_g^{max}. The maximum input current ripple (Δi_g^{max}) is limited to 20% of the rated current [47]. In the system under consideration, the input voltage to the proposed rectifier, designated as V_{ab}, is a five-level voltage (comprising the voltage levels 0, $\pm V_{DC}$, $\pm 2V_{DC}$). For the purpose of filter design, the system is modeled as shown in Fig. 11. The governing equation can be written as

$$L_g \frac{di_g}{dt} = v_g - r_g i_g - V_{ab}. \tag{14}$$

For a given switching cycle of period T_{sw} and duty-ratio D, the above equation is approximated as

$$L_g \frac{\Delta i_g}{D.T_{sw}} = v_g - r_g i_g - V_{ab}. \tag{15}$$

To determine the minimum required value of L_g, a limiting scenario may be considered, as depicted in Fig. 12, with the grid voltage at its maximum value (v_g^{max}), V_{ab} being equal to V_{DC} (since V_{ab} undergoes transitions between $2V_{DC} \leftrightarrow V_{DC}$ when v_g is in the region of its peak value), duty ratio being 50% and the resistance of the filter as negligible. Accordingly, the ripple on the inductor is maximum, with its peak-to-peak value being



(a) (b)

Fig. 13. Designing of passive components. (a) Variation of filter inductance with change in switching frequency. (b) Variation of capacitance with modulation index.

$\Delta i_{\rm g}^{\rm max}|_{\rm pp}$ and the value of $L_{\rm g}$ can be obtained as

$$L_{\rm g} = \frac{(v_{\rm g}^{\rm max} - V_{\rm DC}).T_{\rm sw}}{2\Delta i_{\rm g}^{\rm max}|_{\rm pp}} \tag{16}$$

where, in terms of the modulation index M, $V_{\rm DC}$ is expressed as (8)

$$L_{\rm g} = \frac{v_{\rm g}^{\rm max}(1 - \frac{1}{2M})}{2.F_{\rm sw}\Delta i_{\rm g}^{\rm max}|_{\rm pp}}. \tag{17}$$

Variation of filter inductance (for $v_{\rm g}^{\rm max}$ =325 V, $V_{\rm DC} = 200$ V) with different switching frequencies is shown in Fig. 13(a).

B. Designing of Switched Capacitors

The proposed rectifier is working on the principle of switched-capacitor ($C_{\rm X}$, X ∈ A, B) to maintain the voltage of capacitor $C_{\rm X}$ at $V_{\rm DC}$. When this capacitor discharges to load, voltage ripples should not exceed 10% of the appropriate capacitor voltage, which are decided by discharging time and load current. Through the switching states as shown in Fig. 6, it is clear that, capacitor $C_{\rm X}$ experiences the maximum continuous discharge in 0 output level occurring from 0 to θ. The maximum discharge for the load $R_{\rm o}$ can be articulated as

$$\Delta Q_{C_{\rm X}} = C_{\rm X}.\Delta V_{C_{\rm X}} = \int_0^{\theta} \frac{V_{\rm DC}}{2R_{\rm o}}\, d(\omega t). \tag{18}$$

Solving

$$\Delta Q_{C_{\rm X}} = \frac{V_{\rm DC}}{\omega.R_{\rm o}}\theta \tag{19}$$

where

$$\theta = sin^{-1}\left(\frac{1}{2M}\right). \tag{20}$$

If 10% of maximum ripple are allowed

$$\frac{100\Delta V_{C_{\rm X}}}{V_{\rm DC}} \leq 10. \tag{21}$$

Using these equations, we have

$$C_{\rm X} \geq \frac{10}{2\omega.R_{\rm o}}.sin^{-1}\left(\frac{1}{2M}\right). \tag{22}$$

This equation is valid for $M > 0.5$ and variation of capacitors values is shown in Fig. 13(b) with different modulating indexes and $R_{\rm o}$ is taken as 20 Ω.

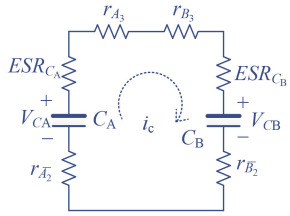


Fig. 14. Pertaining to the determination of intercapacitors current.

C. Component Ratings

The procedure for determination of voltage and current ratings of power switches is summarized below.

1) Voltage Ratings of Power Switches: All the power switches need to bear a maximum voltage equal to the output dc voltage. A summary table of the voltages blocked by all the power switches during various states corresponding to Fig. 6 is shown in Table II.

2) Current Ratings of Power Switches: It can be seen from various states (see Fig. 6) that the conduction paths for the following three currents are manifested in a state: 1) load current $i_{\rm o}$; 2) ac component drawn from the grid $i_{g'}$; and 3) intercapacitors current, $i_{\rm c}$ (see Fig. 14). For each working state, the total current in a power switch is determined. A summary table describing these currents is shown in Table II. Peak values of these currents are

$$i_{\rm o} = \frac{V_{\rm DC}}{R_{\rm o}} \tag{23}$$

where $i_{\rm o}$ is the output current, $V_{\rm DC}$ output voltage, and $R_{\rm o}$ is the load resistance

$$i_{\rm g}^{'\rm max} = \frac{v_{\rm g}^{\rm max}}{|\overline{\rm Z}|} \tag{24}$$

$$|\overline{\rm Z}| = \sqrt{r_{\rm g}^2 + (x_{\rm L} - x_{\rm c})^2} \tag{25}$$

where $r_{\rm g}$ is parasitic resistance of the inductor, and $x_{\rm L}$ and $x_{\rm c}$ are the inductive reactance and capacitive reactance values

$$i_{\rm c}^{\rm max} = \frac{\text{Specified } V_{\rm CA} - \text{Lowest possible } V_{\rm CB}}{R_{\rm eq}} \tag{26}$$

$$i_{\rm c}^{\rm max} = \frac{V_{\rm DC} - 0.9V_{\rm DC}}{R_{\rm eq}} \tag{27}$$

where

$$R_{\rm eq} = r_{\overline{A_2}} + r_{A_3} + r_{\overline{B_2}} + r_{B_3} + ESR_{C_A} + ESR_{C_B}. \tag{28}$$

Based on these equations and Table II, the maximum current for a given power switch is described, and hence, the current rating are determined.

D. Stored Energy in Passive Components

The values of passive components (viz., inductors and capacitors) greatly determine the size of the power converters, which are primarily governed by the maximum current ripples and maximum voltage ripples, respectively [47]. The values of

TABLE II
CURRENT AND VOLTAGE FOR THE POWER SWITCHES DURING VARIOUS STATES OF THE PROPOSED TOPOLOGY

Voltage level	i_{A1},V_{A1}	i_{A2},V_{A2}	i_{A3},V_{A3}	$i_{\overline{A1}},V_{\overline{A1}}$	$i_{\overline{A2}},V_{\overline{A2}}$	i_{B1},V_{B1}	i_{B2},V_{B2}	i_{B3},V_{B3}	$i_{\overline{B1}},V_{\overline{B1}}$	$i_{\overline{B2}},V_{\overline{B2}}$
$+2V_{DC}$	$i_o+i'_g$,0	$i_o+i'_g$,0	0,V_{DC}	0,V_{DC}	0,V_{DC}	0,V_{DC}	0,V_{DC}	i'_g,0	$i_o+i'_g$,0	i_o,0
$+V_{DC}$	i'_g,0	0,V_{DC}	i_c,0	0,V_{DC}	i'_g+i_c,0	0,V_{DC}	0,V_{DC}	i_c+i_o,0	i'_g,0	$i'_g+i_c+i_o$,0
0	0,V_{DC}	0,V_{DC}	i_c,0	i'_g,0	i'_g+i_c,0	0,V_{DC}	0,V_{DC}	i_c+i_o,0	i'_g,0	$i'_g+i_c+i_o$,0
0	0,V_{DC}	0,V_{DC}	i_c+i_o,0	i'_g,0	$i'_g+i_c+i_o$	0,V_{DC}	0,V_{DC}	i_c,0	i'_g,0	i'_g+i_c,o
$-V_{DC}$	0,V_{DC}	0,V_{DC}	i_c+i_o,0	i'_g,0	$i'_g+i_c+i_o$,0	i'_g,0	0,V_{DC}	i_c,0	0,V_{DC}	i'_g+i_c, 0
$-2V_{DC}$	0,V_{DC}	0,V_{DC}	i'_g,0	$i_o+i'_g$,0	i_o,0	$i_o+i'_g$,0	$i_o+i'_g$,0	0,V_{DC}	0,V_{DC}	0,V_{DC}

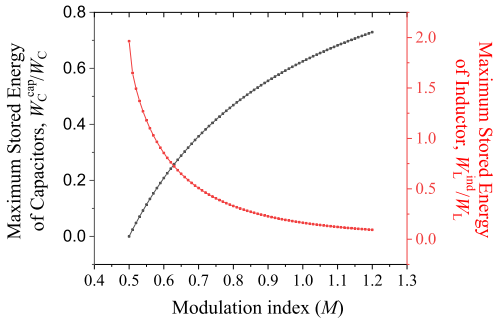


Fig. 15. Total maximum stored energy of inductor and capacitors in the proposed PFC rectifier and that proposed in [29].

stored energies are, respectively, given by [48]

$$W_L^{ind} = \frac{1}{2} L_g (i_g^{max})^2 \tag{29}$$

$$W_C^{cap} = \frac{1}{2} (C_A + C_B)(V_{Cx}^{max})^2 \tag{30}$$

where the maximum voltage across capacitors $V_{Cx}^{max} = V_{DC}$. Designing of the inductor for the proposed topology and that of [29] is the same as both are operated for five-level buck mode with 0.5 gain as seen from (17). Similarly, the capacitances too are same because the charging and discharging duration of the capacitors are the same as seen from (22). The maximum stored energy of an inductor and capacitor can be calculated by substituting (17) and (22) into (29) and (30)

$$W_L^{ind} = \frac{5}{4}\left(1 - \frac{1}{2M}\right).W_L \tag{31}$$

$$W_C^{cap} = \frac{5}{2}\sin^{-1}\left(\frac{1}{2M}\right).W_C \tag{32}$$

where

$$W_L = \frac{v_g^{max}.i_g^{max}}{F_{sw}} \tag{33}$$

$$W_C = \frac{(v_g^{max})^2}{\omega.R_o}. \tag{34}$$

The maximum stored energies for the proposed rectifier and that of [29] are plotted in Fig. 15. The total maximum stored energy of the inductor in the proposed PFC rectifier and those in [29] are the same, as illustrated in Fig. 15. It significantly decreases for the proposed buck converter, especially for the higher modulation index. Fig. 15 also shows that the total maximum stored energy of the capacitors C_A and C_B of both the converters increases when the gain increases. Therefore, the results presented in Fig. 15 imply that the size of energy-storing components of the proposed converters is the same as the buck PFC rectifier proposed in [29].

E. Switching Device Power (SDP)

As described in [49], each switching device in a PFC rectifier system must be chosen on the basis of the maximum blocking voltage across the switches and the peak and average currents passing through it. A rectifier system's voltage and current stresses are quantified in terms of the so-called switching device power (SDP) [50]. The product of voltage stress and current stress is the SDP of a switching device. A rectifier's total SDP equals the sum of the SDPs of all the switching devices in the power circuit. The overall SDP is a cost indicator for a rectifier system since it estimates the total semiconductor device need [49]. These definitions are summarized as follows:

$$SDP_{pk} = \sum_{i=1}^{N_s} V_i^{pk} I_i^{pk} \tag{35}$$

$$SDP_{avg} = \sum_{i=1}^{N_s} V_i^{pk} I_i^{avg} \tag{36}$$

where N_s is the number of semiconductors and V_i^{pk} and I_i^{pk} are their peak voltage and current stresses, respectively. The total peak and average switching device powers (SDP_{pk} and SDP_{avg}) are discussed at length in [50]. To quantify the voltage and current ratings of the switches, Table II is to be considered, which shows the voltage stress and current stress across each switch for a given state. According to [49], SDP_{pk} is used to determine the cost of converters, whereas SDP_{avg} is used to determine the semiconductors' thermal requirements and conversion efficiency.

Both SDP_{pk} and SDP_{avg} are also calculated for the topology proposed in [29]. Then, assuming the same output power for both the rectifiers, SDPs are plotted in Fig. 16 against the modulation index. As seen from Fig. 16, for $M < 1$ (i.e., buck mode of operation of the proposed rectifier), SDP_{pk} of the proposed converter is considerably higher than that of [29]. From Section II and Fig. 7, for $M > 1$, boost mode of operation takes place, and the utilization of power switches is greatly reduced because the

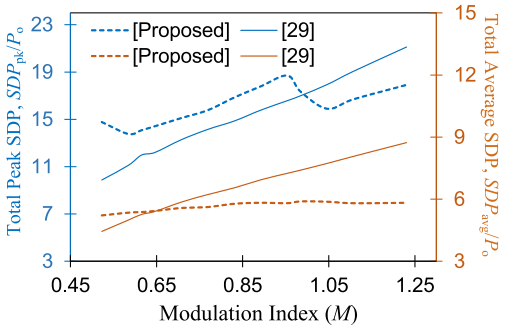


Fig. 16. Total peak and average SDP for the proposed PFC rectifier and that proposed in [29].

topology effectively behaves as an H-bridge converter. In the boost mode of operation, the SDP_{pk} of the proposed converter is considerably lower than that of [29]. Also, SDP_{avg} calculated for the proposed converter, is lower than [29] in a wide range of modulation indexes. Thus, though the number of power switches in the proposed rectifier is a bit higher as compared to that of [29], the SDPs are found to be comparable.

F. Loss Analysis

The efficiency of the rectifier can be expressed as

$$\eta = \frac{P_{\text{o}}}{P_{\text{in}}} = \frac{P_{\text{o}}}{P_{\text{o}} + P_{\text{loss}}} \tag{37}$$

where P_{o}, P_{in}, and P_{loss} correspond to output power, input power, and total power losses, respectively. The total power losses are due to the following: 1) capacitor power losses; 2) switching power losses; and 3) conduction power losses. These are covered briefly below.

1) Capacitor Power Losses: Voltage ripples, that are resulted in a switched capacitor with current $I_{C_{\text{x}}}$, (x∈ A, B) in every working state of the rectifier [38] are expressed as

$$\Delta V_{C_{\text{X}}} = \frac{1}{C}\int_{t_a}^{t_b} I_{C_X}\, dt \tag{38}$$

where $(t_b - t_a)$ represents the time span of discharge during the state under consideration. If f_{ref} is the grid frequency, the power losses caused by voltage ripple are given by

$$P_{\text{loss}}^{\text{ripple}} = \frac{f_{\text{ref}}}{2} C_{\text{x}} (\Delta V_{C_{\text{x}}})^2. \tag{39}$$

Power losses also take place in a capacitor due to its ESR (R_{ESR}). It is expressed as

$$P_{\text{loss}}^{\text{ESR}} = \frac{R_{\text{ESR}} \cdot f_{\text{ref}}}{2} \int_{t_a}^{t_b} I_{C_{\text{X}}}^2\, dt. \tag{40}$$

Thus, the total losses in a capacitor during operation are calculated by adding (39) and (40).

2) Switching Losses: The switching losses are resulted in power switches during transitions. These losses are calculated for a switch based on the overlap of the current and voltage waveforms during transitions [51] as

$$P_{\text{loss}}^{\text{sw}} \approx \frac{1}{2} V_{bv} I_{con} (t_{on} + t_{off}) F_{\text{sw}} \tag{41}$$

where t_{on} and t_{off} are the ON and OFF timings of switch, F_{sw} is the switching frequency, I_{con} is the conduction current, and V_{bv} is the blocking voltage across the switches.

3) Conduction Losses: As discussed in [51], the power losses due to conduction in a switch ($P_{\text{loss}}^{\text{con,sw}}$) and a power diode ($P_{\text{loss}}^{\text{con,D}}$) are expressed as

$$P_{\text{loss}}^{\text{con,sw}} \approx V_{\text{on}}^{\text{sw}} I_{\text{avg}}^{\text{sw}} + R_{\text{on}}^{\text{sw}} (I_{\text{RMS}}^{\text{sw}})^2 \tag{42}$$

$$P_{\text{loss}}^{\text{con,D}} \approx V_{\text{on}}^{D} I_{\text{avg}}^{D} + R_{\text{on}}^{D} (I_{\text{RMS}}^{D})^2 \tag{43}$$

where $V_{\text{on}}^{\text{sw}}$, $R_{\text{on}}^{\text{sw}}$, $I_{\text{on}}^{\text{sw}}$, and $I_{\text{RMS}}^{\text{sw}}$ correspond to voltage drop, resistance, average current, and rms current through the transistor part, respectively. While, V_{on}^{D}, R_{on}^{D}, I_{on}^{D}, and I_{RMS}^{D} correspond to voltage drop, resistance average current, and rms current across diode part, respectively. The overall power losses are obtained by adding (42) and (43).

V. Comparison With Other Topologies

The proposed topology combines multiple dimensions, viz., (buck ac-to-dc conversion) + (multilevel power conversion) + (switched capacitors principle). And therefore, carrying out a comparison with various other PFC topologies may not be very straight forward, as they employ one or two of the aforementioned dimensions. And hence, in this section, separate comparisons of the proposed topology with following topologies have been presented:

1) comparison with switched-capacitors-based multilevel topologies (single- and three-phase) (summarized in Table III);
2) comparison with conventional multilevel topologies (summarized in Table IV);
3) comparison with bridge-less multilevel buck PFC rectifiers (which do not employ the switched capacitors principle) (summarized in Table IV);
4) comparison with some nonmultilevel buck–boost PFC rectifiers (summarized in Table V)

Though switched-capacitors-based multilevel topologies have been studied for many years now, they have been proposed for dc-to-ac conversion. Some of the recent such topologies (both single- and three-phase) are described in [52]–[54], which were originally presented as inverters but can be employed as rectifiers based on (2). Table III shows the comparison of the proposed topology with those presented in [34], [39], [40], and [55]–[59] in terms of crucial parameters such as [33]: number of levels (N_{L}), number of power switches (N_{s}), number of capacitors (N_{c}), number of diodes (N_{D}), peak inverse voltage (PIV), voltage gain (β), and efficiency. Moreover, some other features are also discussed, such as the requirements of the dc bus capacitor, split-capacitors, and possibility of extension to three phases. As can be seen from Table III, the topologies presented in [55]–[57] synthesize five levels with lesser number of power switches than that of the proposed structure, but those in [55], [56] require power switched of high PIV (twice the dc voltage), while an additional dc link capacitor is required in [55] and [57]. Topologies presented in [39], [40], [55], [58], and [59] employ split-capacitors (two connected capacitors in

TABLE III
COMPARISON OF THE PROPOSED TOPOLOGY WITH SOME OTHER SWITCHED CAPACITORS-BASED MULTILEVEL TOPOLOGIES

Topologies	N_L	N_s	N_c	PIV^{**}_{pu}	Voltage gain (β)	Requirement of dc bus capacitor(s)	Presence of split capacitors	Efficiency [%]
Single-phase								
[56]	5	8	2	2	2	Yes	Yes	96.80
[57]	5	9	2	2	2	No	No	98.00
[58]	5	8	2	1	2	Yes	No	97.91
[40]	7	12	2	2	3	Yes	Yes	97.70
[39]	7	12	4	4	4	Yes	Yes	97.62
[34]	7	10	2	3	3	Yes	No	96.07
[59]	9	12	2	1	2	Yes	Yes	80.61
[60]	9	11	2	1	2	Yes	Yes	NA*
Proposed	5	10	2	1	2	No	No	97.50
Three-phase								
[53]	9	36	12	4	4	Yes	Yes	98.60
[54]	13	30	8	1.5	1	yes	Yes	97.00
[55]	17	36	9	4	4	Yes	Yes	97.70
Proposed	5	15	3	1	2	No	No	98.10

*Not available, **PIV is with respect to the dc side voltage, V_{DC}

TABLE IV
COMPARISON OF THE PROPOSED TOPOLOGY WITH MULTILEVEL RECTIFIERS (SINGLE-PHASE)

Parameters	Boost topologies			Buck topologies			
	HB [22]	NPC [28]	FC [27]	CHB [30]	[29]	[31]	Proposed
N_L	3	5	5	5	5	9	5
N_s	4	8	8	8	6	8	10
N_D	0	4	0	0	0	0	0
N_C	1	2	3	2	2	3	2
PIV^{*}_{pu}	1	1	1	1	2	3	1
Voltage Gain ($1/\beta$)	1	1	1	0.5	0.5	0.25	0.5
N_{VS}	2	2	2	3	3	4	2
N_{CS}	1	1	1	1	1	4	1
Phase modularity	Yes	Yes	Yes	Yes	No	No	Yes

*PIV is with respect to the dc side voltage V_{DC}

TABLE V
COMPARISON OF THE PROPOSED TOPOLOGY WITH SOME NON-MULTILEVEL PFC BUCK–BOOST RECTIFIERS

Parameters	[24]	[25]	[26]	[61]	[62]	Proposed
N_s	2	2	2	2	1	10
N_D	4	2	4	5	6	0
N_{ind}	3	3	3	3	3	1
N_C	3	3	3	3	2	2
N_M	2	2	1	3	3	0
Voltage stress*	High	High	High	High	High	Low
THD of grid current, i_g	2.60	2.00	6.55	9.70	15.80	2.90
Efficiency [%]	96.80	95.70	92.35	95.20	95.85	97.50
Bidirectional power flow	No	No	No	No	No	Yes
Easy extension to three-phase	No	No	No	No	No	Yes

*Voltage stress across switches with respect to the dc side voltage V_{DC}

a T-type fashion), which increases the complexity of balancing the voltages of these capacitors, especially in the rectification operation, requiring additional voltage sensors [12]. Topologies presented in [34], [39], [40] and [58], [59], respectively, synthesize seven and nine levels, but are characterized by high PIV and requirement of additional dc bus capacitors. Of these, [39], [40], [55], [58], and [59] also need split-capacitors, leading to voltage balancing issues. These topologies are difficult to extend directly to three-phase structures [38]. In contrast, the proposed topology is characterized by low PIV power switches and does not require split capacitors and dc link capacitors. Also, it can be easily extended to its three-phase version by adding a leg. Thus, it shows better structural features. A comparison of the three-phase version of the proposed topology has also been shown with other three-phase switched capacitors-based multilevel topologies in Table III. It can be seen that, as compared to topologies presented in [52]–[54], the proposed topology has a low requirement of components. Also, the presence of split-capacitors and dc bus capacitors in the topologies of [52]–[54] increases the controller complexity and number of voltage sensors.

In Table IV, a comparison of the proposed topology with the conventional multilevel rectifiers, viz., H-bridge (HB) [22], neutral point clamped [28], and flying capacitors [27], has been shown. As compared to the proposed rectifier, the component requirement is significantly less in these topologies, but it must be noted here that these topologies offer a unity voltage gain, and hence they function as boost rectifiers, and not buck rectifiers. Multilevel buck rectifiers have been proposed in [29]–[31], and

they too are included in Table IV. MLRs are classified with respect to the output voltage, i.e., buck and boost. A comparative analysis is done in terms of different parameters such as; N_{L}, N_{s}, N_{D}, N_{c}, PIV, in addition to the number of voltage sensors (N_{VS}), number of current sensors (N_{CS}), phase modularity and efficiency. Topology in [29] requires power switches with PIV equal to twice the output dc voltage and more number of voltage sensors. Similar is the case with topology in [31], which requires power switches with PIV equal to four times of the output dc voltage and a significantly large number of voltage and current sensors. Both these topologies possess similar limitations: difficulty in balancing of capacitors' voltages and difficulty in extension to three-phase configuration. Hence, the proposed topology manifests superior characteristics.

Table V summarizes the comparison of the proposed topology with some buck–boost PFC rectifiers [24]–[26], [60], [61] including the recently proposed Ferdowsi rectifiers [25]. The proposed work is based on employing capacitors to attain multilevel buck rectification, whereas the nonmultilevel topologies proposed in [24]–[26], [60], and [61] employ magnetic core(s). The comparison is carried out using the parameters of N_{s}, N_{c}, and N_{D}, in addition to the number of magnetic cores (N_{M}), number of the inductors (N_{ind}), input current THD, and efficiency. Some other features are also discussed such as voltage stress across the switches, bidirectional capability, and possibility of extension to a three-phase system. In the magnetic core-based-buck rectifiers proposed in [24]–[26], [60], and[61], voltage stress in terms of output dc voltage is very high though they require lesser number of active switches. However, the requirement of other components is significantly high in these topologies. Moreover, these topologies do not allow bidirectional flow of power and do not offer an easy possibility of implementation in three-phase systems. Hence, it can be safely concluded that the topology proposed in this work is highly competent with the considerations of buck PFC operation, bidirectional power flow, three-phase extension, voltage ratings of power switches, and ease of voltage balancing of capacitors.

VI. Experimental Verification With Possible Applications

In this section, results of experimental studies are presented in steady and dynamic states. Additional results are presented with the perspective of application to EV charging.

A. Results and Discussion

For the validation of the proposed five-level rectifier and the closed loop control scheme, a laboratory setup was developed using discrete power switches (MOSFETs SiHG47N60) with Si82071AB-IS for gate driving. Hall effect-based voltage sensor (LEM LV25-P) and current sensor (HE025T01) are used to sense the output voltage and input current. A labeled photograph of the setup is shown in Fig. 17.

OPAL-RT OP4510 was used to generate the real time control pulses for the power switches, which was interfaced with the hardware using MATLAB/Simulink on the host computer. The controller and switching process are implemented with a

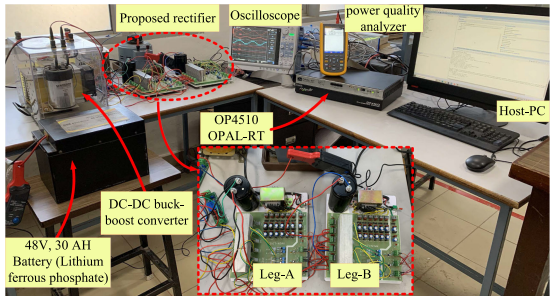


Fig. 17. Photograph of laboratory set-up for validation of the proposed rectifier.

TABLE VI
Various Parameters/ Items for the Experimental Setup

Parameters	Value
Input voltage (v_{g})	230 VRMS
Grid frequency (f_{ref})	50 Hz
Output dc voltage (V_{DC})	200V
Switching frequency (F_{sw})	10 kHz
Switched capacitor (C_{A}, C_{B})	1600 uF
Filter inductor (L_{g})	4 mH
Semiconductor switches	MOSFETs SiHG47N6
Gate driver IC	Si82071AB-IS
Voltage sensor	LEM LV25-P
Current sensor	HE025T01
EV battery details	48V, 30AH, Lithium ferrous phosphate type
Oscilloscope	Yokogawa DL950 with 10:1 probes

sampling time of 10 μs. Input ac is obtained from the grid as single-phase 230 VRMS, while the output dc voltage is set to 200 V in buck mode of operation. Various parameters for the experimental studies are summarized in Table VI. Values of capacitors and inductor are chosen as per the design consideration described previously. The performance of the system is tested for both steady state and dynamic conditions (which include variations in the operating conditions, such as sudden change in dc load, sudden change in the input ac source voltage, and change in the output reference voltage).

The steady-state results are captured when the rectifier converts 325 V peak ac to 200 V dc (in buck mode) and supplies it to the dc load, as shown in Fig. 18. It can be seen that the input current (i_{g}) is sinusoidal and is in the same phase with the input grid voltage (v_{g}), indicating that the input power factor is maintained at unity. The figure also shows a five-level voltage waveform at the rectifier input with low harmonic voltage, positively impacting grid current THD. A 20Ω load is connected on the dc side and the reference output voltage is set to 200 V, which is satisfactorily obtained with a tolerable voltage ripple. The voltages of capacitors C_{A} and C_{B} are balanced at 200 V each, resulting in a five-level voltage waveform of V_{ab} with levels of 0, $\pm$200 V, and $\pm$400 V.

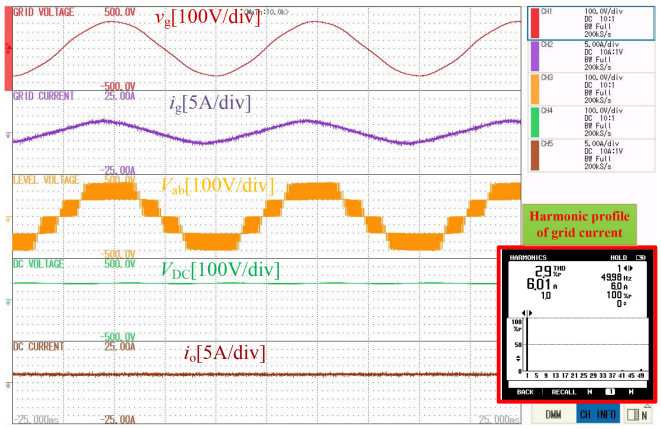


Fig. 18. Waveforms pertaining to the steady-state operation of proposed rectifier.

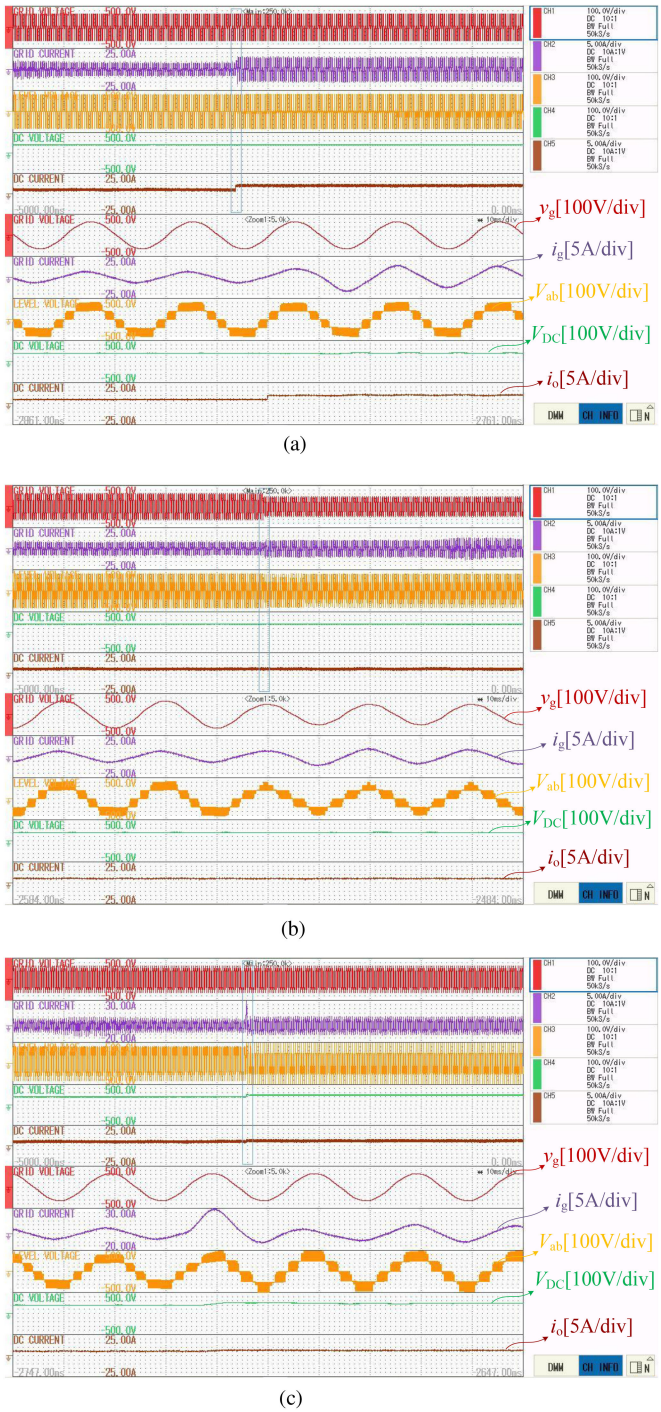


Fig. 19. Experimental results for dynamic performance. (a) When the load is suddenly changed. (b) When the input ac source voltage is varied. (c) During 20% rise in the output dcC voltage reference.

Results related to dynamic performance are shown in Fig. 19. As can be seen in Fig. 19(a), when the output current is increased suddenly by 50% (by changing the load resistance from 40 to 20Ω), the load voltage quickly stabilizes at 200 V and the rectifier is still in unity power factor mode. In another instance, the dc side power consumption ($V_{DC}.i_o$) is not changed, but v_g is suddenly decreased, and it is seen that the grid current ig is increased proportionally and unity power factor is maintained, as shown in Fig. 19(b). When the ac grid voltage is suddenly decreased by 25% without any change in load, then the current drawn from the grid stabilizes instantaneously to a proportionate value. The voltages of dc capacitors are not affected by the voltage sag in the grid. In another scenario, shown in Fig. 19(c), when the output dc reference voltage is changed by 20%, it causes V_{DC} and i_o to change and the load voltage stabilizes at 240 V as desired. These results also validate the tracking accuracy of the controller. Under increased output voltage, the converter continues to operate with a unity power factor and with five voltage levels at the input of the rectifier. The voltage waveforms across the switches are shown in Fig. 20 and as expected, it can be seen that they are limited to a value equal to the output dc voltage.

The steady-state results are also captured when the rectifier converts 325 V peak ac to 400 V dc (in boost mode) and supplies it to the dc load, as shown in Fig. 21. It can be seen that the input current (i_g) is sinusoidal and is in the same phase with the input grid voltage (v_g), indicating that the input power factor is maintained at unity. Fig. 21 also shows a three-level voltage waveform at the rectifier input.

The efficiency, THD, and PF are calculated for the proposed work and comparisons are made with the topology proposed in [29], which has been previously discussed to be a five-level rectifier. The operating conditions for obtaining the efficiency curves for both the topologies are same, viz., input ac voltage of 325 $v_g^{\max}$, output dc voltage 200 V, and carrier frequency 10 kHz. Now, it can be noticed from Fig. 22 below that the proposed topology shows slightly lesser efficiency, but at the same time, if a further comparison is carried out in terms of THD (versus power) [see Fig. 23(a)] and power factor (PF) (versus power) [see Fig. 23(b)] for the topologies, then the proposed topology exhibits much better performance on these parameters. Thus, the peak efficiencies are differing slightly, which are 97.5% and 98%, respectively, for the proposed topology and [29] (mainly due to intercapacitor currents in the proposed topology and lower number of power devices in [29]). It is observed that proposed rectifier yields lower THD and higher PF as compared to [29].

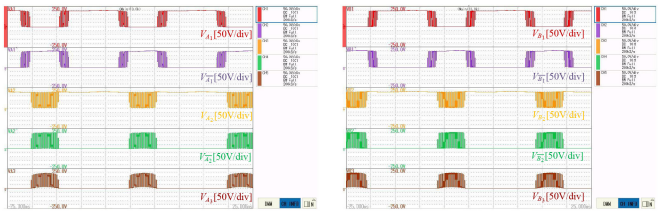


Fig. 20. Waveforms of voltages across the power switches when the output voltage is 200 V.

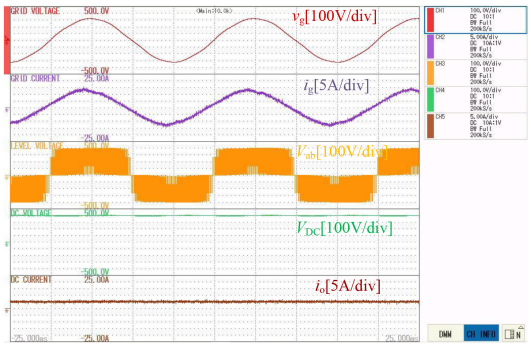


Fig. 21. Experimental waveforms for steady-state boost mode of operation of the proposed rectifier.

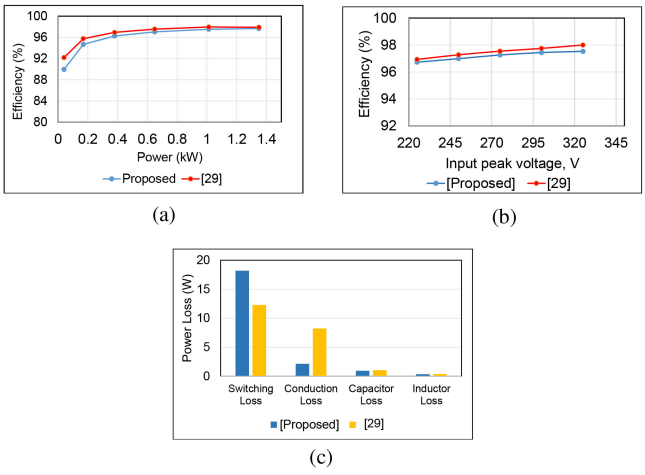


Fig. 22. Efficiency comparison with [29]. (a) Curves with respect to power. (b) Curves with respect to input voltage. (c) Comparison of distribution of power losses with [29].

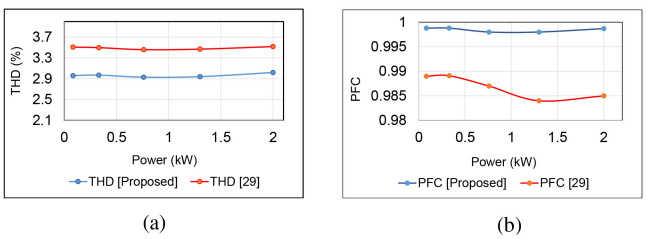


Fig. 23. Comparison with [29]. (a) THD curves with respect to power. (b) PFC curves with respect to power.

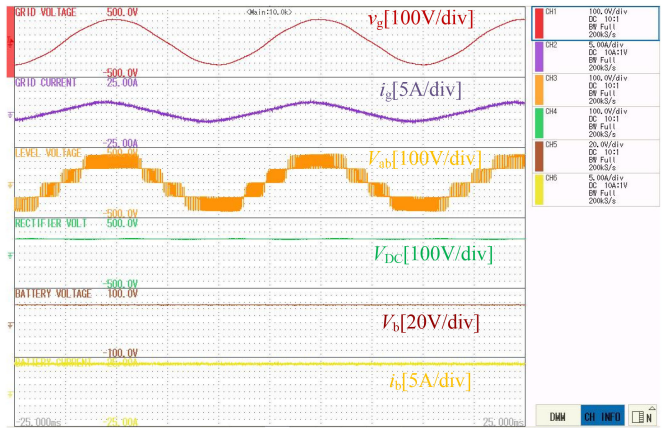


Fig. 24. Experimental waveforms for single-phase battery charging application for 1 kW system.

B. Possible Applications

Although the proposed SC-based PFC MLR can perform both buck and boost operations, the number of levels at the input side are five and three, respectively. And, hence this work focuses on the buck operation due to better quality of waveform synthesized. Since the output voltage can be regulated in a wide range, the proposed rectifier can be employed in a variety of applications such as EV charging, LED drives, lamp ballasts, motor drives, telecom power supplies, etc. However, all the advantages of the topology can be fully tapped when it is used for EV charging application. These major advantages are buck output with wide range, bidirectional flow of power, and easy extension to three-phase systems. Accordingly, relevant experimental results are presented, as discussed below.

1) Single-Phase EV Charging: For the purpose of demonstration of implementation in single-phase charging, a power electronics interface is developed comprising of the proposed PFC rectifier and a conventional buck–boost dc-to-dc converter, as shown in Fig. 17. The ratings are considered as input voltage 230 VRMS, 50 Hz, rectifier output dc voltage being 200 V. The rated power is 1 kW. Battery voltage (V_b) and current (i_b), 48 V and 20 A, respectively. The waveforms are shown in Fig. 24, and it can be seen that the grid voltage and current are in phase and achieve five-voltage level at the input terminal of the rectifier. Output voltage of rectifier regulates to 200 V dc which is further regulates to battery voltage 48 V by dc–dc converter.

2) Three-Phase EV Charging: Due to phase modular structure of the proposed topology, it can be easily extended to its three-phase version. This is achieved by adding a third leg which too carries a switched capacitor and five power switches, as shown in Fig. 25.

Here too, a buck output voltage is obtained with unity power factor operation at the input. Experimental results for the three-phase MLR are shown in Fig. 26(a), with the input ac voltage of 120 VRMS, 50 Hz, and the output dc voltage being 100 V. The rated power is 1 kW. Fig. 26(b) shows the line voltages with five levels (of step size 100 V) corresponding to the phases a, b, and c with 120° phase shift, and also the three-level pole

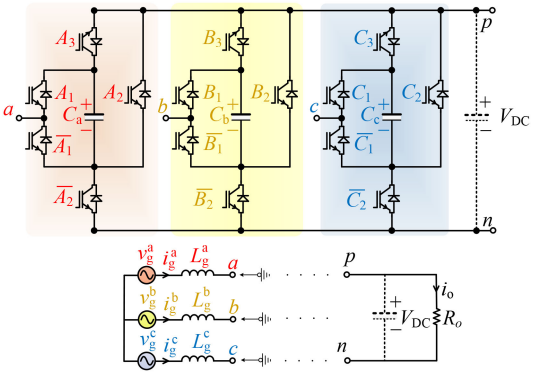
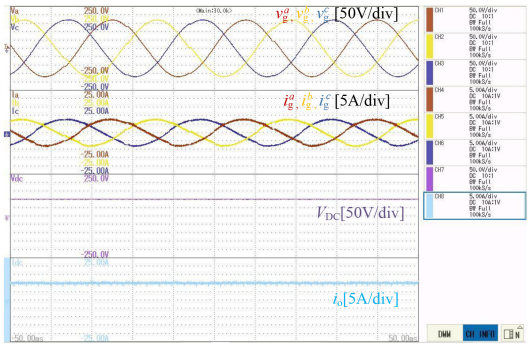
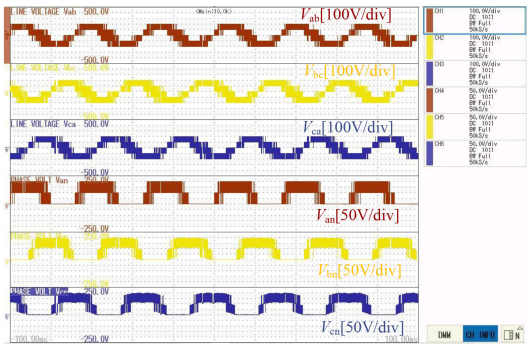


Fig. 25. Three-phase version of the proposed buck PFC rectifier.



(a)



(b)

Fig. 26. Experimental waveforms for the proposed three-phase buck rectifier. (a) Grid voltage, grid current, dc voltage, and current. (b) Line voltages and pole voltages.

voltages which too are phase-shifted from one another by 120°. This phase voltage generates five-level as a line voltage.

3) Bidirectional Power Flow to Enable Vehicle-to-Grid (V2G) Compatibility: The V2G mode facilitates the injection of battery energy back to the grid. That is to say, an EV can respectively act as a load or a generator in grid-to-vehicle (G2V) charging and vehicle-to-grid (V2G) discharging modes. A V2G mode requires capability of bidirectional flow of power in the interface. Such possibility is offered by the proposed topology, both in the single- and three-phase versions. Fig. 27 shows experimental results for both modes (G2V and V2G) of operation. It can be seen that when a sudden change in the flow of battery current is commanded, the battery current is reversed. In this case, the grid current is 180° out-of-phase with the grid voltage.

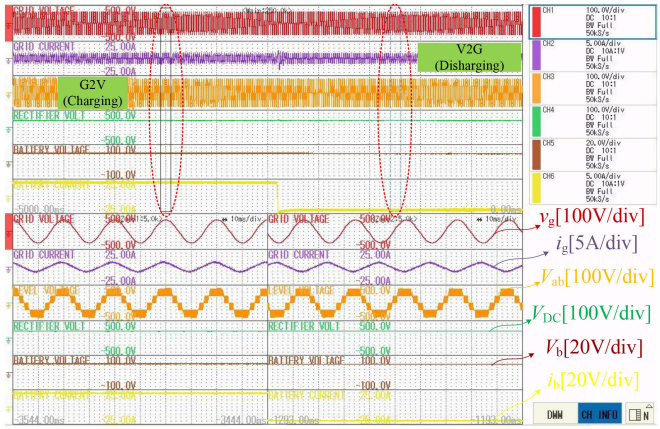


Fig. 27. Experimental waveforms pertaining to bidirectional flow of power with the proposed five-level topology.

VII. Conclusion

In this work, a novel topology is proposed which utilizes the switched capacitors principle to achieve five-level buck rectification. This topology can be realized in single-phase as well as three-phase applications. With the help of experimental results, it is demonstrated that the proposed five-level rectifier achieves power factor correction at the ac side and a wide control range at the output dc side. In addition, it is observed that the PIV of all the power switches is within the output dc voltage, and hence, low voltage-rated switches can be employed. The capability of presented topology for bidirectional flow of power is also established with experimental results. A comparison with other PFC buck rectifiers establishes that the proposed topology is highly modular and offers easy balancing of capacitors. One of the limitations of the proposed rectifier is that if operated in boost mode, it synthesizes only three levels instead of five as some switches of the proposed rectifier become redundant and hence are less utilized.

References

[1] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[2] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part I: A topological review," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, Feb. 2015.

[3] I. F. Kovačević, T. Friedli, A. M. Muesing, and J. W. Kolar, "3-D electromagnetic modeling of EMI input filters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 231–242, Jan. 2014.

[4] A. Kuperman, U. Levy, J. Goren, A. Zafranski, and A. Savernin, "High power Li-Ion battery charger for electric vehicle," in *Proc. 7th Int. Conf.-Workshop Compat. Power Electron.*, 2011, pp. 342–347.

[5] M. R. Khalid, I. A. Khan, S. Hameed, M. S. J. Asghar, and J.-S. Ro, "A comprehensive review on structural topologies, power levels, energy storage systems, and standards for electric vehicle charging stations and their impacts on grid," *IEEE Access*, vol. 9, pp. 128069–128094, 2021.

[6] J. Y. Yong, V. K. Ramachandaramurthy, K. M. Tan, and J. Selvaraj, "Experimental validation of a three-phase off-board electric vehicle charger with new power grid voltage control," *IEEE Trans. Smart Grid*, vol. 9, no. 4, pp. 2703–2713, Jul. 2018.

[7] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Design and implementation of a three-phase buck-type third harmonic current injection PFC rectifier SR," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1608–1621, Apr. 2013.

[8] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Swiss rectifier - A novel three-phase buck-type PFC topology for electric vehicle battery charging," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 2617–2624.

[9] S. H. Hosseini, R. Ghazi, and H. Heydari-Doostabad, "An extendable quadratic bidirectional DC-DC converter for V2G and G2V applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4859–4869, Jun. 2021.

[10] M. C. Kisacikoglu, M. Kesler, and L. M. Tolbert, "Single-phase on-board bidirectional PEV charger for V2G reactive power operation," *IEEE Trans. Smart Grid*, vol. 6, no. 2, pp. 767–775, Mar. 2015.

[11] M. Yilmaz and P. T. Krein, "Review of benefits and challenges of vehicle-to-grid technology," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 3082–3089.

[12] M. C. Kisacikoglu, B. Ozpineci, and L. M. Tolbert, "Examination of a PHEV bidirectional charger system for V2G reactive power compensation," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 458–465.

[13] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[14] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.

[15] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A survey," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749–755, May 2003.

[16] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three-phase PWM AC–AC converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011.

[17] V. Monteiro, J. G. Pinto, A. A. N. Meléndez, and J. L. Afonso, "A novel single-phase five-level active rectifier for on-board EV battery chargers," in *Proc. IEEE 26th Int. Symp. Ind. Electron.*, 2017, pp. 582–587.

[18] V. Bist and B. Singh, "PFC Cuk converter-fed BLDC motor drive," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 871–887, Feb. 2015.

[19] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, "99% efficient three-phase buck-type SiC MOSFET PFC rectifier minimizing life cycle cost in DC data centers," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 1, pp. 47–58, 2017.

[20] J. Garcia, M. A. Dalla-Costa, A. L. Kirsten, D. Gacio, and A. J. Calleja, "A novel flyback-based input PFC stage for electronic ballasts in lighting applications," *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 769–777, Mar./Apr. 2013.

[21] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: State of the art," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 5–22, Feb. 2005.

[22] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1% efficient 10 kV SiC-based medium-voltage ZVS bidirectional single-phase PFC AC/DC stage," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 779–797, Jun. 2019.

[23] J.-S. Lee, U.-M. Choi, and K.-B. Lee, "Comparison of tolerance controls for open-switch fault in a grid-connected T-type rectifier," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5810–5820, Oct. 2015.

[24] M. Pourmahdi, H. Heydari-doostabad, R. Ghazi, and T. O'Donnell, "Buck-boost common ground bridgeless PFC (CGBPFC) rectifies with positive/negative output," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1272–1282, Feb. 2022.

[25] S. Sharifi, M. Monfared, and M. Babaei, "Ferdowsi rectifiers-single-phase buck-boost bridgeless PFC rectifiers with low semiconductor count," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9206–9214, Nov. 2020.

[26] M. Mahmoodsaleh and E. Adib, "Soft-switching bridgeless buck-boost PFC converter using single magnetic core," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5704–5711, Jul. 2021.

[27] C. A. Teixeira, D. G. Holmes, and B. P. McGrath, "Single-phase semi-bridge five-level flying-capacitor rectifier," *IEEE Trans. Ind. Appl.*, vol. 49, no. 5, pp. 2158–2166, Sep./Oct. 2013.

[28] Y. Xu, Y. Zou, C. Wang, W. Chen, and B. Liu, "A single-phase high-power-factor neutral-pointer clamped multilevel rectifier," in *Proc. 7th Int. Conf. Power Electron. Drive Syst.*, 2007, pp. 1487–1491.

[29] H. Vahedi and K. Al-Haddad, "A novel multilevel multioutput bidirectional active buck PFC rectifier," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5442–5450, Sep. 2016.

[30] A. Dell'Aquila, M. Liserre, V. G. Monopoli, and P. Rotondo, "Overview of PI-based solutions for the control of DC buses of a single-phase H-bridge multilevel active rectifier," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 857–866, May/Jun. 2008.

[31] M. Babaie and K. Al-Haddad, "A novel single-phase triple-output active buck rectifier using nine-level packed E-cell converter," in *Proc. Int. Conf. Smart Energy Syst. Technol.*, 2021, pp. 1–6.

[32] F. Sebaaly, M. Sharifzadeh, H. Y. Kanaan, and K. Al-Haddad, "Multilevel switching-mode operation of finite-set model predictive control for grid-connected packed E-cell inverter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6992–7001, Aug. 2021.

[33] P. Bhatnagar, A. K. Singh, K. K. Gupta, and Y. P. Siwakoti, "A switched-capacitors-based 13-level inverter," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 644–658, Jan. 2022.

[34] A. Khodaparast, M. J. Hassani, E. Azimi, M. E. Adabi, J. Adabi, and E. Pouresmaeil, "Circuit configuration and modulation of a seven-level switched-capacitor inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7087–7096, Jun. 2021.

[35] K. K. Gupta and P. Bhatnagar, *Multilevel Inverters: Conventional and Emerging Topologies and Their Control*. New York, NY, USA: Academic, 2017.

[36] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. Hoboken, NJ, USA: Wiley, 2003.

[37] Y. Ye, W. Peng, and Y. Yi, "Analysis and optimal design of switched-capacitor seven-level inverter with hybrid PWM algorithm," *IEEE Trans. Ind. Inform.*, vol. 16, no. 8, pp. 5276–5285, Aug. 2020.

[38] Y. Ye, S. Chen, R. Sun, X. Wang, and Y. Yi, "Three-phase step-up multilevel inverter with self-balanced switched-capacitor," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7652–7664, Jul. 2021.

[39] L. He, J. Sun, Z. Lin, and B. Cheng, "Capacitor-voltage self-balance seven-level inverter with unequal amplitude carrier-based APODPWM," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14002–14013, Dec. 2021.

[40] M. D. Siddique, S. Mekhilef, N. M. Shah, J. S. M. Ali, and F. Blaabjerg, "A new switched capacitor 7L inverter with triple voltage gain and low voltage stress," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 67, no. 7, pp. 1294–1298, Jul. 2020.

[41] M. Rao A and K. Sivakumar, "A fault-tolerant single-phase five-level inverter for grid-independent PV systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7569–7577, Dec. 2015.

[42] B.-R. Lin and T.-L. Hung, "High-power-factor single-phase switch clamped rectifier," in *Proc. Power Convers. Conf.*, 2002, pp. 25–30.

[43] H. Vahedi, E. Pashajavid, and K. Al-Haddad, "Fixed-band fixed-frequency hysteresis current control used in APFs," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, 2012, pp. 5944–5948.

[44] H. Hafezi, E. Akpinar, and A. Balikci, "Cascade PI controller for single-phase STATCOM," in *Proc. Int. Power Electron. Motion Control Conf. Expo.*, 2014, pp. 88–93.

[45] M. Andrey Freitas de Souza Kohler and D. Flores Cortez, "Single-phase five-level flying-capacitor rectifier using three switches," *IEEE Open J. Power Electron.*, vol. 1, pp. 383–392, Sep. 2020.

[46] J. Zhang, L. Li, D. G. Dorrell, and Y. Guo, "Modified PI controller with improved steady-state performance and comparison with PR controller on direct matrix converters," *Chin. J. Elect. Eng.*, vol. 5, no. 1, pp. 53–66, 2019.

[47] T. Lahlou, M. Abdelrahem, S. Valdes, and H.-G. Herzog, "Filter design for grid-connected multilevel CHB inverter for battery energy storage systems," in *Proc. Int. Symp. Power Electron. Elect. Drives Autom. Motion*, 2016, pp. 831–836.

[48] S. Sharifi, M. Monfared, and A. Nikbahar, "Highly efficient single-phase direct AC-to-AC converter with reduced semiconductor count," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1130–1138, Feb. 2021.

[49] S. Sharifi, M. Monfared, M. Babaei, and A. Pourfaraj, "Highly efficient single-phase buck-boost variable-frequency AC–AC converter with inherent commutation capability," *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 3640–3649, May 2020.

[50] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," in *Proc. Power Electron. Transp.*, 2004, pp. 125–132.

[51] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.

[52] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.

[53] L. He and C. Cheng, "A flying-capacitor-clamped five-level inverter based on bridge modular switched-capacitor topology," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7814–7822, Dec. 2016.
[54] S. S. Lee, Y. Bak, S.-M. Kim, A. Joseph, and K.-B. Lee, "New family of boost switched-capacitor seven-level inverters (BSC7LI)," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10471–10479, Nov. 2019.
[55] M. Saeedian, S. M. Hosseini, and J. Adabi, "A five-level step-up module for multilevel inverters: Topology, modulation strategy, and implementation," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2215–2226, Dec. 2018.
[56] B. Shaffer, H. A. Hassan, M. J. Scott, S. U. Hasan, G. E. Town, and Y. Siwakoti, "A common-ground single-phase five-level transformerless boost inverter for photovoltaic applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 368–374.
[57] N. Sandeep, J. S. M. Ali, U. R. Yaragatti, and K. Vijayakumar, "A self-balancing five-level boosting inverter with reduced components," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6020–6024, Jul. 2019.
[58] S. S. Lee, "Single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8204–8207, Oct. 2018.
[59] J. S. Mohamed Ali and V. Krishnasamy, "Compact switched capacitor multilevel inverter (CSCMLI) with self-voltage balancing and boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4009–4013, May 2019.
[60] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New bridgeless DCM sepic and Cuk PFC rectifiers with low conduction and switching losses," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 873–881, Mar./Apr. 2011.
[61] B. R. Ananthapadmanabha, R. Maurya, and S. R. Arya, "Improved power quality switched inductor Cuk converter for battery charging applications," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9412–9423, Nov. 2018.

Anekant Jain (Member, IEEE) received the B.E. degree in electronics and communication engineering from the Oriental College of Technology, Bhopal, India in 2014, and the M.Tech. degree in digital communication from the RGPV, Bhopal, India, in 2018, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the Thapar Institute of Engineering and Technology, Patiala, India.

He is currently a Teaching Assistant with the Thapar Institute of Engineering and Technology. His current research interests include electric vehicle charging, multilevel converters, communication methodologies, and cyber-physical systems.

Krishna Kumar Gupta (Member, IEEE) received the B.Tech. degree in electrical engineering, the M.Tech. degree in power systems, and the Ph.D. degree in electrical engineering from the Maulana Azad National Institute of Technology, Bhopal, India, in 2005, 2007, and 2014, respectively.

He is currently with the Department of Electrical and Instrumentation Engineering, Thapar Institute of Engineering and Technology, Patiala, India. He has coauthored two books *Multilevel Inverters*, (Academic Press, Elsevier) and *Modeling and Control of Power Electronics Converter System for Power Quality Improvements*, (Academic Press, Elsevier). He is the Inventor of cross-connected sources based multilevel inverter and holds a patent on it. His research interests include power electronics for renewable energy, multilevel inverters, and electric vehicle charging.

Dr. Gupta was the recipient of the Young Scientist Award conferred upon by the Government of M.P., India, in 2015 and Confederation of Indian Industry for his contribution in teaching.

Sanjay K. Jain (Member, IEEE) received the B.E. degree in electrical engineering from SGSITS, Indore, India, in 1992, the M.E. degree in power systems from the University of Roorkee, Roorkee, India, in 1995, and the Ph.D. degree in power system from IIT Roorkee, Roorkee, India, in 2001.

In 2000, he joined the Thapar Institute of Engineering and Technology, Patiala, India, where he is currently a Full Professor. His research interests include power system operation and control, power system optimization, data analytics, and renewable energy systems.

Pallavee Bhatnagar (Senior Member, IEEE) received the B.E. degree in electrical engineering from the Lakshmi Narain College of Technology, Bhopal, India, in 1998, and the Ph.D. degree from the Department of Electrical Engineering, Maulana Azad National Institute of Technology, Bhopal, India, in 2015.

From 1999 to 2001, she was an Assistant Engineer with All India Radio, Bhopal. From 2001 to 2005, she was the Head (Product Development) of Nucleus Electro-Enterprises Limited, Bhopal. In 2005, she joined the National Thermal Power Corporation of India as an Engineer. Thereafter, she took up teaching and has now taught for more than a decade. In 2019, she was a Research Scientist with the Skoltech Center for Energy Science and Technology, Skolkovo Institute of Science and Technology, Moscow, Russia. She is currently the Dean (Academics) of the IES College of Technology, Bhopal, and a Postdoctoral Fellow with the Sustainable Energy Research Center, Sultan Qaboos University, Muscat, Oman. She has coauthored a book *Multilevel Inverters* (Academic Press, Elsevier). Her research interests include power converters, photovoltaic systems, LED-based lighting, and electric vehicle charging infrastructure.