Parallel-Hybrid Converter Based STATCOM: Operating Principles and Capacitor Voltage Control Using Fundamental Frequency Zero-Sequence Voltage

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***Abstract*—The parallel-hybrid converter (PHC) based high-voltage dc (HVdc) plant (PHC-HVdc) mandates the injection of additional harmonic-voltage components into its chain-links (CLs) to regulate its output voltage/modulation index (MI). However, these harmonic voltages are restricted to have limited magnitude and their zero crossings must coincide with the respective output voltages of converter. Hence, the operating range of MI for the PHC-HVdc has narrow limits. This article explores the reactive power compensating capabilities of the PHC based static compensator (PHC-STATCOM), which is relieved from the fixed dc source and is free to operate at any MI without requiring any additional efforts. Two degrees of freedom inherent with PHC-STATCOM are discovered, which proves that PHC is utilized to its maximum when applied for reactive compensation. The capacitor voltages of the PHC-STATCOM belonging to different CLs divert from desired value under unbalanced grid/load conditions. By the virtue of degrees of freedom associated with PHC-STATCOM, a capacitor voltage control technique is proposed using fundamental-frequency zero-sequence voltage (FFZSV). The generalized expression of the reference FFZSV is derived, which regulates the capacitor voltages. The loci planes indicating the maximum range of load unbalance that the PHC-STATCOM can compensate with specific grid voltage conditions is obtained and plotted. The working principles and proposed capacitor control are verified using experimental studies. A detailed comparative study is presented to substantiate the advantages of the proposed topology.**

***Index Terms*—Chain-link (CL), cluster (CR) power, constraints, degrees of freedom, fundamental-frequency zero-sequence voltage (FFZSV), modulation index (MI), multilevel converter, parallel-hybrid converter (PHC), static compensators (STATCOM), third harmonic voltage components (THVCs), unbalanced grid.**

I. Introduction

THE parallel-hybrid converter (PHC) proposed in [1]–[3] for high-power high-voltage dc transmission (HVdc) applications offers several benefits over the modular multilevel converter (MMC) [4]–[8]. The PHC requires smaller sized capacitors, lower number of switching and energy storing devices, and has lower switching losses than the MMC [1], [10]–[11], [24]. Therefore, the PHC is specifically suited for applications where smaller footprint and high efficiency are the major requirements. The MMC configuration is also utilized for the static compensation applications where it is classified as double star chopper cells (DSCCs) [12]–[16] and double star bridge cells (DSBCs) [12], [16]. The present-day power system demands efficient and compact-sized static compensators (STATCOMs) for improving its power quality. Hence, this article intends to utilize the PHC configuration as a STATCOM and explores its working and control principles, whereas exchanging positive and negative sequence reactive powers with the grid.

The PHC proposed in [1]–[3] consists of a series connection of three chain-links (CLs) fed by a dc-link voltage source for exchanging active power with the grid. The three CLs consist of half-bridge submodules (SMs) that generate rectified sine wave voltages, which are unipolar and are 120° apart from each other. Each CL voltage is unfolded into a bipolar sine wave with the help of an H-bridge connected across the respective CL. The application of PHC that necessitates a dc voltage source at its input is termed as PHC-HVdc in this article. The PHC-HVdc has two constraints that prevent it from providing reactive power support to the ac grid, which are mentioned as constraint-1 and constraint-2 in this article. The average value of the sum of its CL voltages must remain constant and equal to the dc-link voltage source (Kirchhoff's voltage law), which acts as constraint-1. To exchange reactive power with the grid, a converter must be able to generate a flexible output voltage. Nevertheless, any variation in one or more CL voltages of the PHC-HVdc, which might be required to exchange reactive power, would no longer hold their average sum at the constant dc-link value. Hence, the PHC-HVdc cannot generate flexible desired output voltage and thus the modulation index (MI) of the PHC-HVdc remains fixed at rated value [1]. To deal with this issue of fixed MI in the PHC-HVdc, equal and unequal quantities of third harmonic voltage components (THVCs) are injected into their CLs during balanced and unbalanced grid conditions, respectively [1]–[2]. With the injection of THVCs, the average sum of the CL voltages remains constant. However, the amplitude of the injected THVCs must be limited and their zero crossings must always

Manuscript received December 11, 2021; revised March 26, 2022; accepted April 27, 2022. Date of publication May 16, 2022; date of current version June 24, 2022. Recommended for publication by Associate Editor B. Singh. *(Corresponding author: Anshuman Shukla.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3175321.

Digital Object Identifier 10.1109/TPEL.2022.3175321

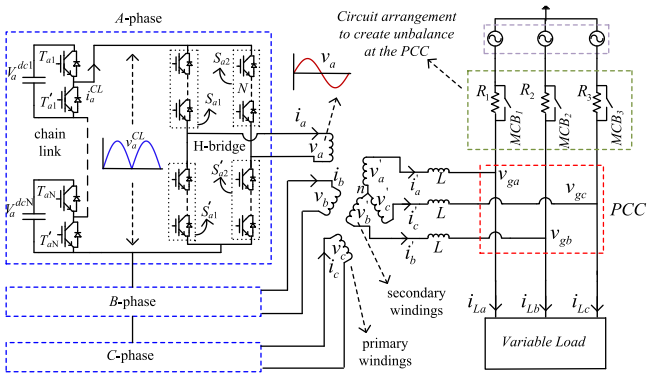

Fig. 1. Circuit Configuration of PHC-STATCOM.

coincide with the corresponding output voltages of the converter, which forms the constraint-2. The reason for the same is well described in Section-II-B. With the imposition of constraint-2, the PHC-HVdc can regulate the MI only within a narrow limit [2]–[3]. The regulation of MI in the PHC-HVdc by injecting THVCs in the CLs also demands a bulkier sized dc side inductor and thereby, increases the cost and size [24].

Under unbalanced grid voltage conditions, each CL of the PHC-HVdc delivers unequal active power to the grid. Subsequently, the capacitor voltages of different CLs of PHC-HVdc stray away from the rated value [2]–[3]. In this circumstance, unequal quantities of THVCs are injected into each CL, which not only satisfies constraint-1 but also regulates the capacitor voltages at their rated value. Nonetheless, the main disadvantage in this method lies in the fact that these unequal THVCs enter into the three-phase grid and distort it further. Moreover, due to the imposition of constraint-2 in PHC-HVdc, as mentioned earlier, the control over the capacitor voltages is restricted to limited magnitudes (less than 5%) of unbalance in the grid voltages. Also, the procedure involved in calculating the amplitude and phase angles of these unequal THVCs includes a large number of complex mathematical steps, which are quite difficult to be implemented in a real-time application [2].

The PHC configuration presented in this article, referred to as PHC-STATCOM in Fig. 1, is primarily designed to provide reactive power support to the grid and hence does not require a fixed dc-link source at its input. The PHC-STATCOM is not bound by any of the abovementioned constraints and hence provides two extra degrees of freedom of control. First degree of freedom: the average value of the sum of the CL voltages need not remain fixed at a particular value, and hence the CL voltages can be varied in a desirable manner to provide reactive power support to the three-phase grid. The PHC-STATCOM no longer requires any harmonic injection techniques to vary its MI both during balanced and unbalanced grid conditions. The PHC-STATCOM can vary its MI from 0 to the designed voltage rating of the converter, without any external dedicated control, and hence can exchange desired reactive power with the grid. However, when it compensates reactive power to an unbalanced grid or load connected at the point of common coupling (PCC), the capacitor voltages of the PHC-STATCOM belonging to different CLs get disturbed and diverge from their desired value. This issue is addressed here as the "capacitor voltage imbalance" problem of PHC-STATCOM. The capacitor voltage imbalance arises because of uneven average active powers associated with each CL, termed as cluster (CR) power. These CR powers are formed due to the interaction between the nonidentical sequence components of converter voltage and current, which are described in good detail in Section III-B. Nevertheless, the capacitor voltages belonging to a particular CL remain equal to each other, due to the capacitor voltage sorting technique [17].

The application of PHC for reactive power compensation applications (PHC-STATCOM) was first proposed in [18], where the negative sequence current injection technique was utilized to solve the capacitor voltage imbalance problem during unbalanced grid conditions. The reference negative sequence currents generated to maintain the capacitor voltages also gets exchanged into the grid at the PCC. However, these negative sequence currents are unwanted to the grid. This may increase the intensity of voltage unbalance in the grid. Moreover, the negative sequence current components of the converter are utilized as tools to regulate the capacitor voltages. Hence, the negative sequence current can no longer be used to compensate the unbalanced load. Also, constraint-2 of PHC-HVdc and second degree of freedom associated with PHC-STATCOM were not explored and discussed in [18].

This article proposes the PHC-STATCOM with a new capacitor voltage control technique using the fundamental-frequency zero-sequence voltage (FFZSV), where the converter can simultaneously compensate for the unbalance in the grid or load. The overall control structure presented in this article yields three-phase sinusoidal reference voltage signals that need to appear across the primary windings of transformers of PHC-STATCOM. These reference primary winding voltages consist of an FFZSV component in addition to the positive and negative sequence voltages. Each CL of the PHC-STATCOM is commanded to generate rectified version of these reference primary winding voltages. The proposed control regulates the magnitude and zero crossings/phase angle of this FFZSV in a manner that the uneven CR powers of the CLs get neutralized, which eventually solves the capacitor voltage imbalance issue of PHC-STATCOM. Except for being limited by the converter voltage rating, the FFZSV is free to possess any magnitude and phase angle. This is the second degree of freedom in the PHC-STATCOM as compared against constraint-2 of PHC-HVdc. The FFZSV appears across both the primary and secondary windings of all three single-phase transformers of the PHC-STATCOM but does not enter the grid since the neutral point, n, remains ungrounded.

The circuit configuration of the PHC-STATCOM is described in Section II. In Section III, the power analysis of the PHC-STATCOM is performed where the expressions of the CL voltage and currents are established to formulate the average CL power. In addition, the capacitor voltage divergence issue of the PHC-STATCOM during unbalanced network conditions is explained in detail in Section III using the generalized power equations. Section IV deals with the overall control structure of the PHC-STATCOM including the proposed capacitor voltage control technique. The expression for the reference FFZSV

required to resolve the capacitor voltage imbalance issue is derived using the analysis presented in Section IV. In Section V, the "constraints of the PHC-HVdc and the degrees of freedom of PHC-STATCOM" are demonstrated using the simulated waveforms. This section illustrates that the PHC is utilized to its best when applied for reactive power compensation applications. In Section V, a three-phase hardware prototype of the PHC-STATCOM is built in the laboratory and is operated under balanced and unbalanced network conditions in order to demonstrate the working and proposed control principles. This article also obtains and plots the well-defined boundaries indicating the maximum range of load unbalance the PHC-STATCOM can compensate under specific grid voltage conditions, as considered in the hardware studies, while the proposed controller regulates the capacitor voltages. Moreover, the advantages of the proposed capacitor technique are compared with the traditional technique presented in [18] using the hardware results. A detailed comparative study is presented in Section VI to prove that the proposed topology requires fewer components (switches and capacitors) and hence it has lower size, weight, and footprint. Hence, the PHC-STATCOM can be a viable option for all such application like offshore and city-infeed, where low converter size and footprint are major requirements. The inferences obtained are summarized in the conclusion section.

II. Parallel-Hybrid Converter STATCOM

A. Description of the PHC STATCOM Configuration

The circuit configuration of the PHC-STATCOM is presented in Fig. 1. It is void of the fixed dc-link source, unlike the PHC-HVdc. The PHC-STATCOM comprises three CLs, where each CL consists of *N* number of identical half-bridge SMs. Each SM further incorporates a dc capacitor and a complementary pair of IGBT switches T_{kj} and T'_{kj}, where, $k = (a, b, \text{and } c)$ represents a particular phase and $j = (1 \text{ to } N)$ represents the SM number. The capacitor of an SM can either be inserted into or by-passed from a CL by switching ON/OFF T_{kj} and switching OFF/ON T'_{kj}. y_k number of capacitors are inserted in a CL at a given instant in order to generate a full-wave rectified sine voltage as shown in Fig. 1, where, $y_k = (0 \text{ to } N)$ depends on the instantaneous value of the reference voltage signal associated with that CL. The rectified sine wave voltages appear across the dc input terminals of the respective H-bridges linked to each CL.

The H-bridges constitute two complementary pairs of switches (S_{k1} & S'_{k1}) and (S_{k2} & S'_{k2}), which are also termed as director switches (DSs). The switching operations of these DSs are governed by the positive and negative zero-crossing instants of the reference voltage signal. During the positive duration of this reference voltage/modulation signal, the switches $S_{k1}$and S'_{k2} are ON, leading the dc input terminal voltages of the H-bridges to appear directly across its ac output terminals. Whereas, during the negative half duration of the reference voltage signal, the switches $S'_{k1}$and S_{k2} are ON, leading the dc input terminal voltages to appear in its inverted form across the ac output terminals of the H-bridges. This kind of operation generates a complete sine wave voltage across the primary windings of the three single-phase transformers of the PHC-STATCOM. Hence, the switches of the H-bridge undergo zero-voltage switching (ZVS) mode of operation at the fundamental frequency. The corresponding secondary windings of the PHC-STATCOM are connected to the grid at the PCC as shown in Fig. 1. *L* represents the equivalent leakage inductance on the secondary side of the transformers.

It is also worth mentioning that the transformer terminals of the PHC-STATCOM shall exhibit common mode voltage stress. Other series-connected VSC-HVdc topologies, such as the PHC-HVdc [1], series-connected MMC (SC-MMC) [32], series bridge converter (SBC) [33], [34], and enhanced SBC [35], use similar transformer arrangements. Furthermore, high-common-mode-stress transformers are used in various real-world high-voltage applications [36]–[38]. Design of such transformers is an established and well-known technology [34], [36]–[38]. In addition, whereas a conventional MMC-HVdc system can employ a single three-phase transformer, series-connected converters such as the SC-MMC and SBC require three single-phase transformers. However, this is not a disadvantage of series-connected topologies because three single-phase transformers are favored over a single three-phase transformer for high-voltage applications [1], [39]. This is primarily due to the fact that single-phase transformers are easier to be transported and lower the amount of spare storage required at converter stations. These are extremely crucial and critical elements in high-voltage applications, like HVdc [1], [39]. It is also worth noting here that the PHC-STATCOM does not suffer from the leakage current problem due to the isolation provided by the transformers between the grid ground and the terminals of the primary windings.

Each DS of PHC-STATCOM consists of *N* IGBTs connected in series to withstand the voltage imposed by the CL (if the same voltage rating of IGBTs is considered in the half-bridge SMs and DSs). The use of series connection of IGBTs to realize a high-voltage switch is a well-known approach that is used in a variety of high-power applications [1], [24], [33] and [40]–[46]. High-voltage switches implemented with series-connected IGBTs are also used in several of the recently proposed significant hybrid topologies, such as the alternative arm converter (AAC) [42], [43], PHC-HVdc [1], HSC [24], SBC [33], [47], and H-bridge hybrid modular converter [46]. In addition, gate driver designs for DSs provided in [48], [49] can be readily be implemented in PHC-STATCOM. It is also worth mentioning that the DSs of PHC-STATCOM operate in ZVS mode. The ZVS operation decreases switching losses and allows simple gate driver designs for DSs to be used. The power analysis of the PHC-STATCOM is described in the next section.

III. Power Analysis of the Proposed PHC-STATCOM

A. Derivation of Generalized Expressions of the CL Voltage and CL Current of the PHC-STATCOM

The three-phase grid voltage at the PCC is defined as v_{gk}. The positive sequence components of grid voltage (v^p_{gk}), depicted in form of vectors, (V^p_{gk}), in Fig. 2(a), are considered as reference phasors for synchronizing the output voltages of the PHC-STATCOM with that of the grid, which is the phase-locked loop [25]–[26]. The voltage across the secondary windings of the transformers after considering the leakage inductance

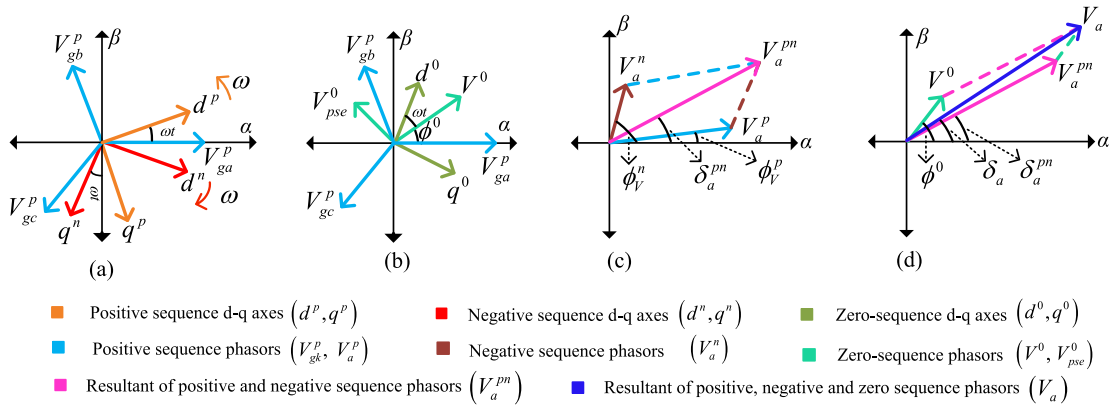

Fig. 2. (a) Decoupled double synchronous reference frames. (b) Zero-sequence voltage vectors and its *d-q* components. (c) Resultant voltage vector formed from positive and negative sequence components across primary winding "*a*" phase. (d) Resultant voltage vector diagram formed from positive, negative, and zero-sequence voltage components across primary winding of "*a*" phase.

drop is referred as v'_k. The transformation ratios of the three single-phase transformers are denoted as γ. The generalized expressions of the primary winding voltages (v_k) , as generated by the PHC-STATCOM, are expressed in (1). In (1), V^p, V^n, and V^0 are the peak values and ϕ^p_V , ϕ^p_V, and $\phi^0$are the phase angles associated with the positive, negative, and FFZSV components of v_k, respectively. And $\theta_u = (0°, 120°, \text{and } -120°)$ for $k = (a, b, \text{and } c)$

$$v_k = \underbrace{V^p \sin(\omega t - \theta_u - \phi^p_V)}_{v^p_k} + \underbrace{V^n \sin(\omega t + \theta_u - \phi^n_V)}_{v^n_k} + \underbrace{V^0 \sin(\omega t - \phi^0)}_{v^0}. \quad (1)$$

To proceed with the analysis, a pseudo-zero-sequence voltage phasor with a peak value of V^0_{pse} and phase lag of 90° with respect to the actual FFZSV vector (V^0), is introduced as shown in Fig. 2(b). The voltage vectors V^0 and V^0_{pse} are transformed into d^0 and q^0components $(V^0_d \text{ and } V^0_q)$ in (2) and (3), respectively, using the *Park* transformation matrix [26], [27]

$$V^0_d = V^0 \cos(\omega t) + V^0_{\text{pse}} \sin(\omega t) \quad (2)$$

$$V^0_q = V^0 \sin(\omega t) - V^0_{\text{pse}} \cos(\omega t). \quad (3)$$

Now, from Fig. 2(b), the actual FFZSV v^0 can be expressed as in (4). It can be inferred from (4) that the magnitude and phase angle of the voltage v^0 can be regulated by setting V^0_d and V^0_q to appropriate values

$$v^0 = V^0_d \cos(\omega t) + V^0_q sin(\omega t). \quad (4)$$

The positive $(V^p_d,\ V^p_q)$ and negative $(V^n_d,\ V^n_q)$sequence components of the primary wining voltages are obtained using the decoupled double synchronous reference frames (DDSRF) [26], [28] (d^p, q^p) and (d^n, q^n), respectively, as shown in Fig. 2(a). These DDSRF components of primary winding voltages along with the obtained V^0_d and V^0_q are employed to represent the primary winding voltages, v_k as

$$v_k = \underbrace{V^p_d \cos(\omega t - \theta_u) + V^p_q \sin(\omega t - \theta_u)}_{v^p_k} + \underbrace{V^n_d \cos(\omega t + \theta_u) - V^n_q \sin(\omega t + \theta_u)}_{v^n_k} + \underbrace{V^0_d \cos(\omega t) + V^0_q \sin(\omega t)}_{v^0}. \quad (5)$$

The expression for the peak value of the primary winding voltage associated with "*a*" phase (V_a) and its positive zero-crossing time instant $t_a$are obtained from the resultant vector diagrams shown in Fig. 2(c) and (d) and are presented in (6), shown at the bottom of the next page and (9), respectively. Similarly, the expressions of the peak values V_b and V_c are also obtained and presented in (7) and (8) shown at the bottom of the next page , respectively. The positive zero-crossing time instants t_b and t_c are given by (10) and (11), respectively. The phase angles $(2\pi - \delta_a)$, $(\pi + \delta_b)$, and $(\pi - \delta_c)$ in (9)–(11), shown at the bottom of the next page, represent the angular position of the positive zero-crossing instants of v_a, v_b, and v_c, respectively. In (6)–(11), V^{pn}_a, V^{pn}_b, and V^{pn}_c are the peak values and $(2\pi - \delta^{pn}_a)$, $(\pi + \delta^{pn}_b)$, and $(\pi - \delta^{pn}_c)$ are the angular positions of the positive zero-crossing instants of the voltage phasors, which are formed from the vector sum of only the positive and negative sequence voltage components across primary windings $(v_a - v^0, v_b - v^0, \text{and } v_c - v^0)$. The expressions of $V^{pn}_k$and δ^{pn}_k can be obtained from derivations [18]

The negative zero-crossing instants of the primary winding voltages, v_k, is expressed as

$$t'_k = \frac{\pm\pi}{\omega} + t_k. \quad (12)$$

The rectified version of the primary winding voltages yields the respective CL voltages. Hence, the three CL voltages are functions of the primary winding voltages, v_k, and their positive

and negative zero-crossing instants $(t_k\ ,\ t'_k)$ as expressed as

$$v_k^{\mathrm{CL}} = \begin{cases} \begin{pmatrix} V_d^p\cos(\omega t-\theta_u)+V_q^p\sin(\omega t-\theta_u) \\ +V_d^n\cos(\omega t+\theta_u)-V_q^n\sin(\omega t+\theta_u) \\ +V_d^0\cos(\omega t)+V_q^0\sin(\omega t) \end{pmatrix},\ t_k\le t\le t'_k \\ -\begin{pmatrix} V_d^p\cos(\omega t-\theta_u)+V_q^p\sin(\omega t-\theta_u) \\ +V_d^n\cos(\omega t+\theta_u)-V_q^n\sin(\omega t+\theta_u) \\ +V_d^0\cos(\omega t)+V_q^0\sin(\omega t) \end{pmatrix},\ t'_k\le t\le t'_k+\frac{\pi}{\omega}. \end{cases} \tag{13}$$

The primary winding currents consist of only positive and negative sequence components as

$$i_k = I^p\sin(\omega t-\theta_u-\phi_V^p-\phi_I^p)+I^n\sin(\omega t+\theta_u-\phi_V^n-\phi_I^n) \tag{14}$$

where $I^p$and I^n represent the peak values and ϕ_I^p and ϕ_I^p represent the phase angles of the positive and negative sequence components of the primary winding currents. Using the DDSRF [Fig. 2(a)], i_k is represented as

$$\begin{aligned} i_k = &\left(I_d^p\cos(\omega t-\theta_u)+I_q^p\sin(\omega t-\theta_u)\right. \\ &\left.+I_d^n\cos(\omega t+\theta_u)-I_q^n\sin(\omega t+\theta_u)\right). \end{aligned} \tag{15}$$

The CL currents are expressed as follows as a function of the respective primary winding currents, i_k and the positive and negative zero-crossing instants of the primary winding voltages $(t_k\ ,\ t'_k)$:

$$i_k^{CL} = \begin{cases} \begin{pmatrix} I_d^p\cos(\omega t-\theta_u)+I_q^p\sin(\omega t-\theta_u) \\ +I_d^n\cos(\omega t-\theta_y)-I_q^n\sin(\omega t-\theta_y) \end{pmatrix},\ t_k\le t\le t'_k \\ -\begin{pmatrix} I_d^p\cos(\omega t-\theta_u)+I_q^p\sin(\omega t-\theta_u) \\ +I_d^n\cos(\omega t-\theta_y)-I_q^n\sin(\omega t-\theta_y) \end{pmatrix},\ t'_k\le t\le t'_k+\frac{\pi}{\omega}. \end{cases} \tag{16}$$

The generalized equations of the CL voltages and currents are utilized to perform the power analysis in the following subsection, which are further utilized in Section IV, to develop the proposed capacitor voltage control principle. The expressions for the peak values of the primary winding voltages, as derived in (6)–(8), are employed in Section VI to attain the maximum load unbalance compensation ability of the PHC-STATCOM.

B. Power Analysis

1) Active Power Associated With CLs: The average active power associated with each CL, $(\overline{P_k^{\mathrm{CL}}})$, can be determined by integrating the instantaneous CL power as

$$\overline{P_k^{\mathrm{CL}}} = \frac{\omega}{\pi}\int_{t_k}^{\left(t_k+{}^{\pi}/_{\omega}\right)} v_k^{\mathrm{CL}} * i_k^{\mathrm{CL}}dt,\ (k=a,b,c)\,. \tag{17}$$

The CL voltages and currents from (13) and (16), respectively, are substituted into (17), to obtain the generalized expressions for the average active power of each CL, which are presented in (18), shown at the bottom of the next page. The sum of these average active CL powers yields the total active power that is withdrawn from the grid to compensate for the losses occurring in the CLs of the PHC-STATCOM, which are represented as $\overline{P_{\mathrm{losses}}^{\mathrm{CL}}}$ in (19). Each of the three CLs of the PHC-STATCOM contributes equally to $\overline{P_{\mathrm{losses}}^{\mathrm{CL}}}$. Hence, the active power loss in each CL is given by $\overline{P_{\mathrm{losses}}^{\mathrm{CL}}}/3$

$$\overline{P_{\mathrm{losses}}^{\mathrm{CL}}} = \sum_{k=a,\,b,\,c}\overline{P_k^{\mathrm{CL}}} = 1.5\left(V_d^pI_d^p+V_q^pI_q^p+V_d^nI_d^n+V_q^nI_q^n\right). \tag{19}$$

The average active CL powers in (18) are classified into three matrices (matrix-1, 2, and 3). However, the expression of the total active power loss occurring in the CLs, as in (19), is constituted of only the terms present in matrix-1 of (18). This indicates that the matrix-2 and 3 portions of $\overline{P_k^{\mathrm{CL}}}$ do not contribute to the active power losses and instead, just stay associated with each CL. The terms involved with matrix-2 and matrix-3 of (18) are termed as CR powers, $\overline{P_k^{\mathrm{CR}}}$, which are represented in (20) shown at the bottom of the next page. Since each CL contributes equally

$$V_a = \sqrt{(V_a^{pn})^2+(V_d^0)^2+\left(V_q^0\right)^2+2V_a^{pn}V_q^0\cos(\delta_a^{pn})-2V_a^{pn}V_d^0 sin(\delta_b^{pn})} \tag{6}$$

$$V_b = \sqrt{(V_b^{pn})^2+(V_d^0)^2+\left(V_q^0\right)^2-2V_b^{pn}V_q^0\cos(\delta_b^{pn})-2V_b^{pn}V_d^0\sin(\delta_b^{pn})} \tag{7}$$

$$V_c = \sqrt{(V_c^{pn})^2+(V_d^0)^2+\left(V_q^0\right)^2-2V_c^{pn}V_q^0\cos(\delta_c^{pn})+2V_c^{pn}V_d^0\sin(\delta_c^{pn})} \tag{8}$$

$$t_a = \frac{(2\pi-\delta_a)}{\omega} = \frac{1}{\omega}\left(2\pi-\delta_a^{pn}-\tan^{-1}\left\{\frac{-V_d^0\cos(\delta_a^{pn})-V_q^0\sin(\delta_a^{pn})}{V_a^{pn}+V_q^0\cos(\delta_a^{pn})+V_d^0\sin(\delta_a^{pn})}\right\}\right) \tag{9}$$

$$t_b = \left(\frac{\pi+\delta_b}{\omega}\right) = \frac{1}{\omega}\left(\pi+\delta_b^{pn}+\tan^{-1}\left\{\frac{-V_d^0\cos(\delta_b^{pn})+V_q^0\sin(\delta_b^{pn})}{V_b^{pn}-V_q^0\cos(\delta_b^{pn})+V_d^0\sin(\delta_b^{pn})}\right\}\right) \tag{10}$$

$$t_c = \left(\frac{\pi-\delta_c}{\omega}\right) = \frac{1}{\omega}\left(\pi-\delta_c^{pn}+\tan^{-1}\left\{\frac{-V_d^0\cos(\delta_c^{pn})-V_q^0\sin(\delta_c^{pn})}{V_c^{pn}-V_q^0\cos(\delta_c^{pn})-V_d^0\sin(\delta_c^{pn})}\right\}\right). \tag{11}$$

to the total active power loss, the *CR* powers can also be obtained by evaluating (21).

The CR power expressions of each CL in (20) constitute only the cross-coupling terms of voltage and current components belonging to different sequences. Hence, the values of $\overline{P_k^{\mathrm{CR}}}$ remain equal to zero when the PHC-STATCOM feeds a balanced network since the system deals only with the positive sequence parameters of voltage and current. Conversely, while dealing with an unbalanced network, the $\overline{P_k^{\mathrm{CR}}}$ have a finite value that depends on the type and intensity of unbalance in the grid or load. However, the sum of the three CR powers always remains equal to zero irrespective of balance and unbalanced conditions, as is represented in (22). From (22), it is reconfirmed that the CR powers do not contribute to the active losses of the converter

$$\overline{P_k^{\mathrm{CR}}} = \overline{P_k^{\mathrm{CL}}} - \overline{P_{\mathrm{loss}}^{\mathrm{CL}}}\Big/3 \tag{21}$$

$$\sum_{k=a}^{c} \overline{P_k^{\mathrm{CR}}} = 0. \tag{22}$$

As can be observed from (20), under unbalanced network conditions, the CR powers of different CLs remain unequal to each other, i.e., $\overline{P_a^{\mathrm{CR}}} \neq \overline{P_b^{\mathrm{CR}}} \neq \overline{P_c^{\mathrm{CR}}}$. Due to the unequal nature of these CR powers, the capacitor voltages of different CLs of the PHC-STATCOM stray away from their desired value. This is the capacitor voltage divergence/imbalance issue, which is symbolically represented as $(V_a^{\mathrm{dc}j} \neq V_b^{\mathrm{dc}j} \neq V_c^{\mathrm{dc}j})$. The consequences that may follow with the inter CL capacitor voltage divergence is that the PHC-STATCOM shall not be able to regulate its primary winding and CL currents at their anticipated value and hence desired reactive power cannot be exchanged with the grid. This necessitates developing a control technique to hold the capacitor voltages at desired reference even when the PHC-STATCOM compensates for an unbalanced network. The detailed working of the proposed control is presented in Section IV.

2) Reactive Power Exchanged by the PHC-STATCOM: The instantaneous reactive power (q_k) delivered from each primary wining of the PHC-STATCOM into the PCC is obtained as follows [26], [31]:

$$q_k = \left((v_k^p)_{\perp} + (v_k^n)_{\perp} + \left(v_k^0\right)_{\perp}\right) i_k = \left(\left(v_{k+1}^p - v_{k+2}^p\right) + \left(v_{k+1}^n - v_{k+2}^n\right) + \left(v_{k+1}^0 - v_{k+2}^0\right)\right) i_k \tag{23}$$

where $(v_k^p)_{\perp}$ and $(v_k^n)_{\perp}$ are the orthogonal component of v_k^p and v_k^n, respectively; and if suppose k represents a phase, then $k{+}1$ and $k{+}2$ represent b and c phases, respectively. In (23), the FFZSV being a common mode component gets canceled and hence may not be considered for procuring q_k. The average reactive power associated with each phase $(\overline{Q_k})$ of PHC-STATCOM can be evaluated from (24), shown at the bottom of the next page. Subsequently, the total average reactive power delivered at the PCC $(\overline{Q_{\mathrm{Total}}})$ is represented in (25)

$$\overline{Q_k} = \frac{1}{2\pi}\left(\int_{-\varphi_V^p-\frac{\pi}{2}-\theta_u}^{-\varphi_V^p+\frac{3\pi}{2}-\theta_u} \left(v_{k+1}^p - v_{k+2}^p\right) i_k d(\omega t) + \int_{-\varphi_V^n+\frac{\pi}{2}+\theta_u}^{-\varphi_V^n+\frac{5\pi}{2}+\theta_u} \left(v_{k+1}^n - v_{k+2}^n\right) i_k d(\omega t)\right) \tag{24}$$

$$\begin{bmatrix} \overline{P_a^{\mathrm{CL}}} \\ \overline{P_b^{\mathrm{CL}}} \\ \overline{P_c^{\mathrm{CL}}} \end{bmatrix} = \underbrace{\frac{1}{2}\begin{bmatrix} V_d^p & V_q^p & V_d^n & V_q^n \\ V_d^p & V_q^p & V_d^n & V_q^n \\ V_d^p & V_q^p & V_d^n & V_q^n \end{bmatrix}\begin{bmatrix} I_d^p \\ I_q^p \\ I_d^n \\ I_q^n \end{bmatrix}}_{\text{matrix}-1} + \underbrace{\frac{1}{4}\begin{bmatrix} 2I_d^p + 2I_d^n & 2I_q^p - 2I_q^n \\ -I_d^p - \sqrt{3}I_q^p - I_d^n - \sqrt{3}I_q^n & -I_q^p + \sqrt{3}I_d^p + I_q^n - \sqrt{3}I_d^n \\ -I_d^p + \sqrt{3}I_q^p - I_d^n + \sqrt{3}I_q^n & -I_q^p - \sqrt{3}I_d^p + I_q^n + \sqrt{3}I_d^n \end{bmatrix}\begin{bmatrix} V_d^0 \\ V_q^0 \end{bmatrix}}_{\text{matrix}-2}$$
$$+ \underbrace{\frac{1}{4}\begin{bmatrix} 2V_d^n & -2V_q^n & 2V_d^p & 2V_d^p \\ \sqrt{3}V_q^n - V_d^n & \sqrt{3}V_d^n + V_q^n & \sqrt{3}V_q^p - V_d^p & \sqrt{3}V_d^p + V_q^p \\ -\sqrt{3}V_q^n - V_d^n & -\sqrt{3}V_d^n + V_q^n & -\sqrt{3}V_q^p - V_d^p & -\sqrt{3}V_d^p + V_q^p \end{bmatrix}\begin{bmatrix} I_d^p \\ I_q^p \\ I_d^n \\ I_q^n \end{bmatrix}}_{\text{matrix}-3} \tag{18}$$

$$\begin{bmatrix} \overline{P_a^{\mathrm{CR}}} \\ \overline{P_b^{\mathrm{CR}}} \\ \overline{P_c^{\mathrm{CR}}} \end{bmatrix} = \underbrace{\frac{1}{4}\begin{bmatrix} 2I_d^p + 2I_d^n & 2I_q^p - 2I_q^n \\ -I_d^p - \sqrt{3}I_q^p - I_d^n - \sqrt{3}I_q^n & -I_q^p + \sqrt{3}I_d^p + I_q^n - \sqrt{3}I_d^n \\ -I_d^p + \sqrt{3}I_q^p - I_d^n + \sqrt{3}I_q^n & -I_q^p - \sqrt{3}I_d^p + I_q^n + \sqrt{3}I_d^n \end{bmatrix}\begin{bmatrix} V_d^0 \\ V_q^0 \end{bmatrix}}_{\text{matrix}-2}$$
$$+ \underbrace{\frac{1}{4}\begin{bmatrix} 2V_d^n & -2V_q^n & 2V_d^p & 2V_d^p \\ \sqrt{3}V_q^n - V_d^n & \sqrt{3}V_d^n + V_q^n & \sqrt{3}V_q^p - V_d^p & \sqrt{3}V_d^p + V_q^p \\ -\sqrt{3}V_q^n - V_d^n & -\sqrt{3}V_d^n + V_q^n & -\sqrt{3}V_q^p - V_d^p & -\sqrt{3}V_d^p + V_q^p \end{bmatrix}\begin{bmatrix} I_d^p \\ I_q^p \\ I_d^n \\ I_q^n \end{bmatrix}}_{\text{matrix}-3} \tag{20}$$

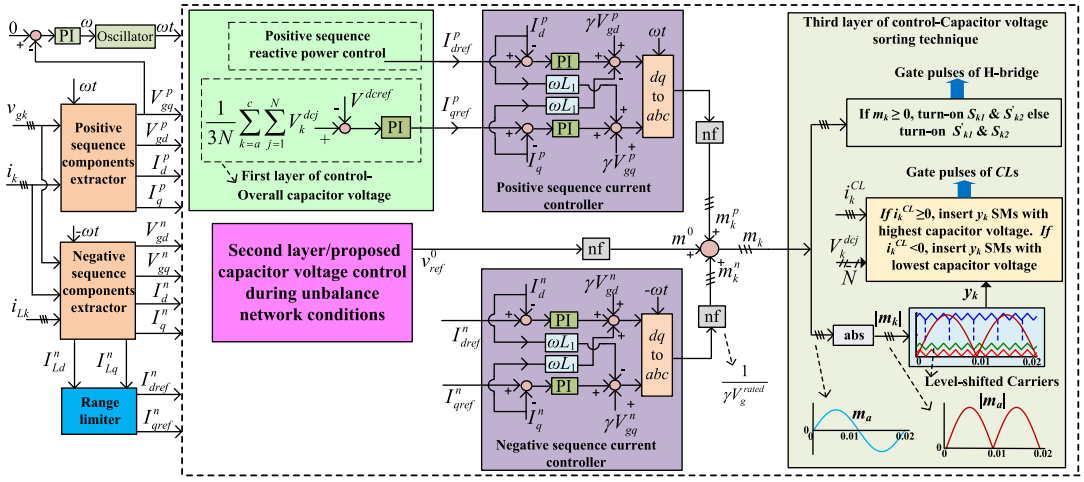

Fig. 3. Overview layout of the global control block diagram for the PHC-STATCOM.

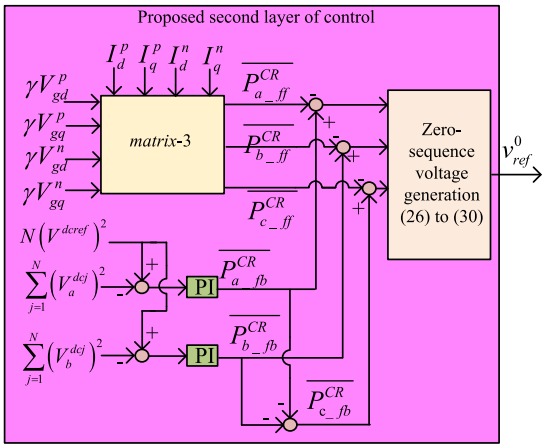

Fig. 4. Proposed capacitor voltage control or the second layer of control.

$$\overline{Q_{\text{Total}}} = \sum_{k=a}^{c} \overline{Q_k} = \underbrace{V_d^p I_q^p - V_q^p I_d^p}_{\overline{Q_{\text{Total}}^p}} + \underbrace{V_d^n I_q^n - V_q^n I_d^n}_{\overline{Q_{\text{Total}}^n}}. \quad (25)$$

The $\overline{Q_{\text{Total}}}$ is constituted of positive and negative sequence powers $(\overline{Q_{\text{Total}}^p})$ and $(\overline{Q_{\text{Total}}^n})$, respectively, is also represented in (25). The regulation of the positive and negative sequence reactive current components besides the proposed capacitor voltage control technique and generation of switching signals is explained in the subsequent section.

IV. Proposed Control Scheme of the PHC-STATCOM

The block diagram of the global control structure of the PH-STATCOM is depicted in Fig. 3. It is divided into three layers of control, the *first*, *second,* and *third* layers. The *first layer* deals with the overall capacitor voltage control and reactive power control. The *second layer* generates the FFZSV components that are used to regulate the capacitor voltages during unbalance compensation. The *third layer* is the process involved in generating gate pulses to the switches in SMs present in the CLs of the PHC-STATCOM. The first and third layers are depicted in detail in Fig. 3, whereas the second layer is just depicted as a block generating reference FFZSV. For a better understanding of the proposed control technique, the detailed procedure of establishing the reference FFZSV is shown separately in Fig. 4. The positive and negative sequence current control blocks that regulate the primary winding currents of the PHC-STATCOM are also shown in Fig. 3.

The grid voltages, primary winding current of the transformers, and the load currents are first sensed using the sensing boards (Fig. 8). The sensed signals are fed into the digital signal processor (DSP), where the sensed grid voltages and primary winding currents are decomoposed into their respective positive and negative sequence components using the method discussed in [25]–[26]. The positive sequence quadratue axis component of the grid voltage is used to obtain the grid synchronizing angle (ωt) as also displayed in Fig. 3. The extracted sequence components in addition to the sensed capacitor voltages are fed as input to the aforementioned control layers to execute their respective functionalities. The functionalities of each control layer are described as follows.

A. First Layer of Control

The *first* layer of control deals in the generation of the reference current component that is utilized to compensate for the active power losses occurring in the PHC-STATCOM. The quadrature component of the positive sequence current present in the primary winding, I_q^p, determines the active power flow in the PHC-STATCOM. To compensate for the active losses of the converter, it is essential to regulate the component I_q^p at the desired reference value, $I_{q\text{ref}}^p$. The value of $I_{q\text{ref}}^p$ is obtained by comparing the average of the capacitor voltages of all the three CLs with the reference capacitor voltage, V^{dcref} and then passing the error signal through a PI controller [28]–[30] as shown in Fig. 3. Once the current component I_q^p is set at $I_{q\text{ref}}^p$,

the converter withdraws necessary active power from the grid and compensates the losses as expressed in (19).

The *first* layer also governs the quantity of $\overline{Q^p_{\text{Total}}}$ required to be exchanged with the grid. The direct axis component of the positive sequence current of the primary winding, I^p_d determines $\overline{Q^p_{\text{Total}}}$ traded by the PHC-STATCOM. The reference current, $I^p_{d\text{ref}}$ can be generated by regulating the actual $\overline{Q^p_{\text{Total}}}$ to a reference power or by simply assigning a value to $I^p_{d\text{ref}}$, which corresponds to a particular amount of reactive power [21]–[23]. This article chooses the latter option and assigns a value to $I^p_{d\text{ref}}$ as shown in the *first layer of the control* block of Fig. 3.

The actual components I^p_q and I^p_d are regulated at the attained reference components $I^p_{q\text{ref}}$ and $I^p_{d\text{ref}}$, respectively, using the conventional PI controllers as shown in the *positive sequence current control* block of Fig. 3 [26], [28]. This generates the positive sequence constituents of the modulation signals, m_k.

B. Second Layer Proposed Capacitor Voltage Control Technique During Unbalanced Load/grid Conditions

This layer of control describes the proposed control technique to restore the inter CL capacitor voltages of the PHC-STATCOM while compensating for an unbalanced network. The CR powers in (20) must be neutralized in order to hold the capacitor voltages of the CLs at their reference value. The negative sequence current components of the primary winding current, I^n_q and I^n_d, are responsible for compensating the negative sequence reactive power ($\overline{Q^n_{\text{Total}}}$) at the PCC. Hence, the FFZSV components V^0_d and V^0_q are the only free parameters that can be set to particular values $V^0_{d\text{ref}}$ and $V^0_{q\text{ref}}$ such that the CR powers in (20) become equal to zero (indirectly, the magnitude and phase angle of v^0 are regulated).

Theoretically, the values of $V^0_{d\text{ref}}$ and $V^0_{q\text{ref}}$ can be obtained from (20) by just replacing $\overline{P^{\text{CR}}_k}$ with zeroes. However, to ensure that the capacitor voltages do not divert from the reference in a real-time or practical system, the $\overline{P^{\text{CR}}_k}$ in (20) is replaced by the feedback terms $\overline{P^{\text{CR}}_{k\_fb}}$. The sum of square of the capacitor voltages of a particular CL is compared with $N(V^{\text{dcref}})^2$ to obtain the feedback term $\overline{P^{\text{CR}}_{k\_fb}}$ as shown in the proposed *second layer of control* block in Fig. 4. In addition to the considered feedback terms, the elements present in matrix-3 of (20) behave as the feed-forward terms $\overline{P^{\text{CR}}_{k\_ff}}$, as also shown in Fig. 4. Henceforth, the CR power expression in (20) is reframed as (26) shown at the bottom of the next page.

As stated in (22), the sum of the CR powers always remains equal to zero, and hence it can be assumed that the sum of CR powers represented in (26) also remains at zero. Therefore, the Clarke transformation [27] is applicable to (26), which breaks it into two variables and two equations format as

$$\begin{bmatrix} \frac{3\overline{P^{\text{CR}}_{a\_fb}}-2\overline{P^{\text{CR}}_{a\_ff}}+\overline{P^{\text{CR}}_{b\_ff}}+\overline{P^{\text{CR}}_{c\_ff}}}{3} \\ \frac{\overline{P^{\text{CR}}_{a\_fb}}+2\overline{P^{\text{CR}}_{b\_fb}}-\overline{P^{\text{CR}}_{b\_ff}}+\overline{P^{\text{CR}}_{c\_ff}}}{\sqrt{3}} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} I^p_d+I^n_d & I^p_q-I^n_q \\ -I^p_q-I^n_q & I^p_d-I^n_d \end{bmatrix}\begin{bmatrix} V^0_{d\text{ref}} \\ V^0_{q\text{ref}} \end{bmatrix}. \tag{27}$$

To obtain the expressions for the reference FFZSV components $V^0_{d\text{ref}}$ and $V^0_{q\text{ref}}$, the feed-forward terms $\overline{P^{\text{CR}}_{k\_ff}}$ in (27) are first substituted by the elements of matrix-3 and are then solved to yield (28) and (29) shown at the bottom of the next page. Subsequently, the actual reference FFZSV (v^0_{ref}) is acquired by substituting $V^0_{d\text{ref}}$ and $V^0_{q\text{ref}}$ for V^0_d and V^0_q, respectively, in (4) as represented in (30). The zero-sequence component of the net modulation signal, m^0 is generated by normalizing v^0_{ref} as illustrated in (31), where V^{rated}_g denotes the rated grid voltage per phase

$$v^0_{\text{ref}} = V^0_{d\text{ref}}\cos(\omega t) + V^0_{q\text{ref}}\sin(\omega t) \tag{30}$$

$$m^0 = \frac{v^0_{\text{ref}}}{\gamma V^{\text{rated}}_g}. \tag{31}$$

To evaluate the reference components $V^0_{d\text{ref}}$ and $V^0_{q\text{ref}}$in a practical application, the voltages V^p_d, V^p_q, V^n_d, and V^n_q in (28) and (29) can be replaced with, γV^p_{gd}, γV^p_{gq}, γV^n_{gd}, and γV^n_{gq}, respectively.

As stated earlier in this subsection and as can also be observed from (25), the negative sequence reactive power delivered/compensated at the PCC depends on I^n_q and I^n_d, respectively. Hence, the sensed components I^n_q and I^n_d are compared with their reference values $I^n_{q\text{ref}}$ and $I^n_{d\text{ref}}$ and are then passed through PI controllers to obtain the negative sequence modulation signals (m^n_k) as represented in the *negative sequence current control* block [26], [28] in Fig. 3. The net modulation signal (m_k) is then obtained by adding the positive, negative, and zero-sequence components, i.e., $m_k = m^p_k + m^n_k + m^0$. This net modulation signal is the reference primary winding voltage expressed in per-unit form.

Considering a case of an unbalanced load connected at the PCC, the negative sequence reference components $I^n_{q\text{ref}}$ and $I^n_{d\text{ref}}$ depend on the intensity of unbalance in the load, which is modeled as I^n_{Lq} and I^n_{Ld} (negative sequence components of the load current, I_{Lk}). However, the values of $I^n_{q\text{ref}}$ and $I^n_{d\text{ref}}$ cannot be assigned directly as such to I^n_{Lq} and I^n_{Ld}, respectively. The range of $I^n_{q\text{ref}}$ and $I^n_{d\text{ref}}$ should be restricted in a manner that the corresponding v^0_{ref} (30), required to restore the capacitor voltages, must not force the CLs to generate voltage exceeding its ratings.

$$\begin{bmatrix} \overline{P^{\text{CR}}_{a\_fb}} \\ \overline{P^{\text{CR}}_{b\_fb}} \\ \overline{P^{\text{CR}}_{c\_fb}} \end{bmatrix} - \underbrace{\begin{bmatrix} \overline{P^{\text{CR}}_{a\_ff}} \\ \overline{P^{\text{CR}}_{b\_ff}} \\ \overline{P^{\text{CR}}_{c\_ff}} \end{bmatrix}}_{\text{matrix}-3} = \underbrace{\frac{1}{4}\begin{bmatrix} 2I^p_d+2I^n_d & 2I^p_q-2I^n_q \\ -I^p_d-\sqrt{3}I^p_q-I^n_d-\sqrt{3}I^n_q & -I^p_q+\sqrt{3}I^p_d+I^n_q-\sqrt{3}I^n_d \\ -I^p_d+\sqrt{3}I^p_q-I^n_d+\sqrt{3}I^n_q & -I^p_q-\sqrt{3}I^p_d+I^n_q+\sqrt{3}I^n_d \end{bmatrix}\begin{bmatrix} V^0_{d\text{ref}} \\ V^0_{q\text{ref}} \end{bmatrix}}_{\text{matrix}-2}. \tag{26}$$

In other words, the maximum value among the positive peaks of the voltages required across CLs or primary windings, $V_k^{\max}$ should be less than or equal to NV^{dcref}as illustrated in (32). This article obtains the locus plane of negative sequence components, such that any operating point (I^n_{qref}, I^n_{dref}) on the considered locus does not mandate the CLs to exceed its voltage limits to regulate the capacitor voltages using the proposed control technique. The values of I^n_{qref} and I^n_{dref} can be assigned directly to the I^n_{Lq} and I^n_{Ld} , respectively, only when the negative sequence components of the load current lie inside the obtained locus plane, which is represented as *range limiter* block in Fig. 3. The process involved in obtaining the locus plane of negative sequence components is explained in experimental case studies for better understanding

$$(V_k^{\max} = \max(V_a, V_b, V_c)) \leq NV^{\text{dcref}}. \tag{32}$$

C. Third Layer of Control-Capaitor Voltage Sorting and Generation of Switching signals

The third and final layer of control is the capacitor voltage sorting technique [17], which controls the intra CL capacitor voltages during both balanced and unbalanced network conditions. The net modulation signal, m_k, which is a fundamental frequency signal, is fed as the reference signal for the ZVS operation of the DSs present in the H-bridges of the PHC-STATCOM. Since the CLs synthesize only unipolar voltage, the designed controller obtains the absolute value of the net modulation signal, $|\mathrm{m_k}|$, as shown in the "third layer control block" of Fig. 3. The absolute/rectified version of the modulation signal is then compared with *N* level shifted triangular carrier waves to obtain the number of SMs to be inserted in a particular CL at a given instant, y_k. Now, it is necessary to select the specific y_k SMs to be inserted in the CL out of *N* available SMs. A standard capacitor voltage sorting technique is used to accompolish it as discussed in [11], [17]. The algorithm selects y_k SMs with highest/lowest capacitor voltages when the direction of the CL current is positive/negative.

In the next section, the various constraints of the PHC-HVdc are compared against the degrees of freedom associated with the PHC-STATCOM.

V. Constraints in PHC-HVdc vs Degrees of Freedom in PHC-STATCOM

In this section, three different case studies are analyzed in Fig. 5 to describe the *constraints* and *first degree of freedom* associated with the PHC-HVdc and PHC-STATCOM, respectively. The major model parameters utilized to obtain the three simulation case studies of Fig. 5 of the revised article are listed in Table I. This simulation case study is provided to establish the advantages of the proposed converter over PHC-HVdc. The waveforms of the various converter parameters shown in Fig. 5 are generated in the MATLAB platform with the following assumptions: the leakage inductance drop of the transformer is neglected and the losses occurring in the converter are neglected. Fig. 5 presents the ideal primary winding and CL voltages in per-unit system, while the PHC is subjected to different symmetric grid voltage conditions [1 pu from 0.2 to 0.225 s, followed by a three-phase voltage swell of 12.5% (1.125 pu) and 33% (1.33 pu) during 0.225–0.25 s and 0.25–0.275 s, respectively]. The maximum swell in the grid voltage is considered to be 1.33 pu for the simulation case studies since the developed experimental model is designed for this rating. Throughout this article, MI is defined as the ratio of the peak value of the fundamental component of operating CL voltage to the product of peak nominal grid voltage and turns ratio of the transformer.

Case-I: The waveforms of the voltages appearing across the primary windings of the transformers of the PHC (v_k) corresponding to the considered grid conditions are shown in Fig. 5(a), where $k = a$, *b,* and *c* phases. The zero crossings of the same voltage v_k are utilized as reference signals for the ZVS operation of the H-bridges of the PHC. Hence, the absolute value of v_k yields the CL voltage waveforms (v_k^{CL}) as shown in Fig. 5(b). The instantaneous sum of the CL voltages ($\sum v_k^{\text{CL}}$) and its average ($V_{\text{avg}}^{\text{CL}}$) are represented in Fig. 5(c). The average of the CL voltages $V_{\text{avg}}^{\text{CL}}$ is 1.91 pu under normal grid voltage conditions, as shown in Fig. 5(c), between the time instants of 0.2 and 0.225 s. However, for different grid voltage swell conditions the value of $V_{\text{avg}}^{\text{CL}}$ varies from its nominal value (1.91 pu) as can be observed from Fig. 5(c) during 0.225–0.25 s and 0.25–0.275 s. The PHC-HVdc would fail to operate during 0.225–0.275 s due to the violation of *constraint*-1 (the average of the *CL* voltages must remain fixed and equal to the fixed dc source). Therefore,

$$V^0_{\text{dref}} = \frac{\begin{pmatrix} 2\overline{P^{\text{CR}}_{a-fb}}\left(I^p_d - I^n_d + \left(I^n_q - I^p_q\right)/\sqrt{3}\right) + 4\overline{P^{\text{CR}}_{b-fb}}\left(I^n_q - I^p_q\right)/\sqrt{3} \\ +V^p_d\left((I^n_d)^2 - (I^n_q)^2 - I^p_d I^n_d + I^p_q I^n_q\right) + V^p_q\left(I^p_d I^n_q - 2I^n_d I^n_q + I^p_q I^n_d\right) \\ +V^n_d\left((I^p_q)^2 - (I^p_d)^2 - I^p_q I^n_q + I^p_d I^n_d\right) + V^n_q\left(2I^p_d I^p_q - I^p_q I^n_d - I^p_d I^n_q\right) \end{pmatrix}}{\left((I^p_d)^2 + (I^p_q)^2 - (I^n_d)^2 - (I^n_q)^2\right)} \tag{28}$$

$$V^0_{\text{qref}} = \frac{\begin{pmatrix} 2\overline{P^{\text{CR}}_{a-fb}}\left(I^p_q + I^n_q + (I^n_d + I^p_d)/\sqrt{3}\right) + 4\overline{P^{\text{CR}}_{b-fb}}(I^n_d + I^p_d)/\sqrt{3} \\ -V^p_d\left(I^p_q I^n_d + 2I^n_d I^n_q + I^p_d I^n_q\right) + V^p_q\left((I^n_q)^2 - (I^n_d)^2 - I^p_d I^n_d + I^p_q I^n_q\right) \\ -V^n_d\left(2I^p_d I^p_q + I^p_q I^n_d + I^p_d I^n_q\right) + V^n_q\left((I^p_q)^2 - (I^p_d)^2 + I^p_q I^n_q - I^p_d I^n_d\right) \end{pmatrix}}{\left((I^p_d)^2 + (I^p_q)^2 - (I^n_d)^2 - (I^n_q)^2\right)} \tag{29}$$

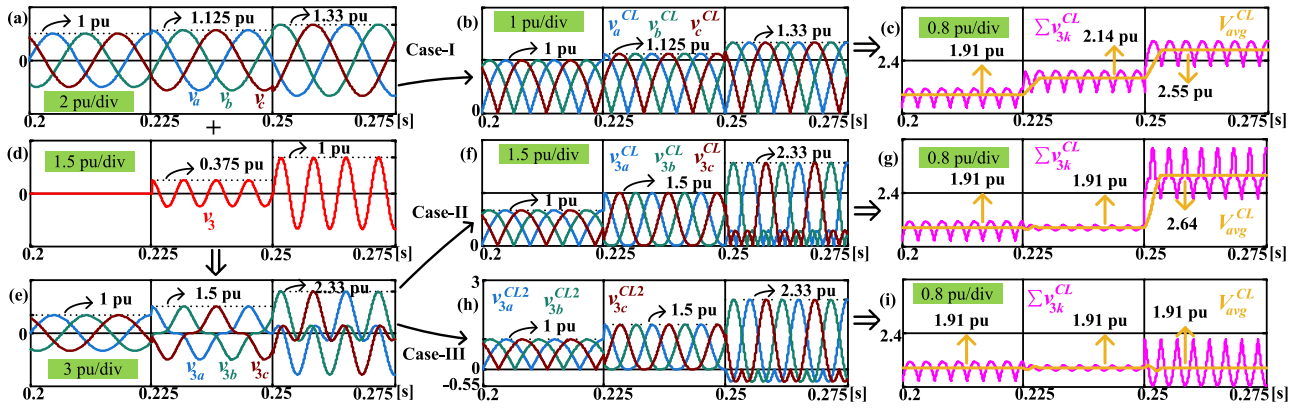

Fig. 5. Case-I: (a) Primary winding voltages of PHC under different grid voltage swell conditions without THIM. (b) Desired CL voltages without THIM (when switches of H-bridges operate at zero crossings of waveforms shown in (a). (c) Sum of the CL voltages of (b) and its average. (d) Required third harmonic voltage to regulate MI of PHC-HVdc. (e) Primary winding voltages with THIM. Case-II: (f) Desired CL voltages with THIM (when switches of H-bridges operate at zero crossings of waveforms shown in (e). (g) Sum of the CL voltages of (f) and its average. Case-III: (h) Desired CL voltages with THIM (when switches of H-bridges operate at zero crossings of waveforms shown in (a). (i) Sum of CL voltages of (h) and its average.

TABLE I
SIMULATION MODEL PARAMETERS AND STUDY CASES

Parameters for all three case studies shown in Fig. 5			
Time duration	0.2 to 0.225 s	0.225 to 0.25 s	0.25 to 0.275 s
Grid voltage, v_{gk}	1 pu	1.125 pu	1.33 pu
Leakage inductance	Neglected		
Transformation ratio	1:1 (since parameters are measured in per-unit system)		
No. of SMs in each *CL*	Infinitely large number of SMs are assumed to be present in PHC such that the *CL*s generate ideal desired voltage so as to simplify the analysis of the case-studies		
Main test conditions associated with individual cases of Fig. 5			
Cases	Case-I	Case-II	Case-III
Assumed voltages across primary windings of the transformers of PHC	Same as grid voltage, since inductance drop is neglected [shown as v_k in Fig. 5(a)]	Grid voltage along with additional third harmonic voltage component [shown as v_{3k} in Fig. 5(e), where $v_{3k} = v_k + v_3$]	
Reference voltages considered for the switching operation of H-bridges	(v_k), grid voltage Fig. 5(a)	(v_{3k}), grid voltage along with additional third harmonic voltage component Fig. 5(e)	(v_k), the grid voltage Fig. 5(a)
Chain-link voltage	Chain-link voltage =primary winding voltage (during positive half cycle of reference voltage considered for H-bridge switching). Chain-link voltage =−1*primary winding voltage, (during negative half cycle of reference voltage considered for H-bridge switching)		
Aim of the cases	To demonstrate 1. *Constraint-1* of PHC- HVdc 2. First *degree of freedom* of PHC-STATCOM	To obtain the maximum range of MI in the PHC-HVdc	To demonstrate the *constraint-2* of PHC-HVdc

the MI of the PHC-HVdc remains fixed at unity under nominal grid voltage conditions (0.2 to 0.225 s) and cannot be varied without additional control efforts. However, due to the absence of a fixed input dc source, the PHC-STATCOM does not mandate $V_{\text{avg}}^{\text{CL}}$, to be constant, which defines the *first degree of freedom* associated with the PHC-STATCOM.

In [1], a third harmonic injection method (THIM) is proposed to regulate the MI of the PHC-HVdc converter operating under varying grid voltages. Considering the exact grid voltage swelling conditions of Case-I, the required THVC (v_3) is calculated using the method presented in [1] and shown here in Fig. 5(d). The resultant primary winding voltages (v_{3k}) of the PHC-HVdc with the injected third harmonics are shown in Fig. 5(e), which are obtained by adding v_3 to the voltage waveforms of Fig. 5(a), i.e., v_k. The further analysis of the ability of the PHC-HVdc to control its MI with additional THIM technique can be divided into two different cases as follows:

Case-II: In this case study, the voltage across the primary windings of the transformers of the PHC-HVdc is considered to be v_{3k} as shown in Fig. 5(e). The zero-crossing instants of voltages v_{3k} are utilized as reference signals for the ZVS operation of the H-bridges of the PHC-HVdc. Hence, the absolute value of v_{3k} yields the required voltage waveforms across each CL (v_{3k}^{CL}) as shown in Fig. 5(f). The instantaneous sum of these CL voltages ($\sum v_{3k}^{\text{CL}}$) and its average ($V_{3\text{avg}}^{\text{CL}}$) are represented in Fig. 5(g). This average voltage $V_{3\text{avg}}^{\text{CL}}$ is maintained at its nominal value (1.91 pu) under both nominal and 12.5% swell in grid voltage conditions as can be observed during the time duration 0.2–0.225 s and 0.225–0.25 s, respectively, in Fig. 5(g). Thus, the PHC-HVdc satisfies *constraint*-1 and hence can feed the grid undergoing a voltage swell of 12.5% without failure. Nonetheless, under a grid voltage swell of 33%, the average value $V_{3\text{avg}}^{\text{CL}}$ does not remain intact at its nominal value even with the THIM technique as shown during the time duration 0.25–0.275 s of Fig. 5(g). The average value of the CL voltages $V_{3\text{avg}}^{\text{CL}}$ cannot be maintained at its nominal value if the grid voltage swell is beyond 12.5% (33% swell for the considered case). Hence, the maximum MI that can be achieved by the PHC-HVdc

with additional THIM is 1.125. Similarly, the minimum value of the MI possible with the PHC-HVdc is 0.75 [1], [3].

However, the operating range of MI in the PHC-STATCOM is not bounded between any scaled limits, except being limited by the converter voltage ratings. Moreover, the PHC-STATCOM eliminates the need of using any THIM technique to regulate its MI. The range of MI of the PHC-STATCOM can flexibly vary between 0 and 1.33 for the considered experimental study.

Case-III: In this case study, the voltage across the transformers primary windings of the PHC-HVdc is also considered to be v_{3k} as shown in Fig. 5(e). However, the zero-crossing instants of the voltages v_k shown in Fig. 5(a) are utilized as reference signals for the switching operation of the H-bridges of PHC-HVdc. Subsequently, the desired voltages that are required to be synthesized across the CLs are obtained as shown in Fig. 5(h). The instantaneous sum of these CL voltages $(\sum v_{3k}^{\mathrm{CL2}})$ and its average $(V_{3\mathrm{avg}}^{\mathrm{CL2}})$ are represented in Fig. 5(i). The average voltage $V_{3\mathrm{avg}}^{\mathrm{CL2}}$ is maintained at its nominal value (1.91 pu) under all the considered grid voltage conditions as shown in Fig. 5(i). Hence, it seems that the PHC-HVdc can satisfy *constraint*-1 during all the grid voltage conditions with the THIM technique However, in practice, *constraint*-1 can never be satisfied when the swell in the grid voltage is more than 12.5% (33% swell for the considered case) since the CLs need to produce a negative polarity voltage as can be observed during 0.25–0.275 s [Fig. 5(h)]. Due to the fact that the CLs cannot generate negative polarity of voltage, the amplitude of the third harmonic voltage injected in the CLs of the PHC-HVdc must be limited, which forms the basis of *constraint*-2.

The PHC-HVdc system can eliminate the requirement of generating negative voltage by its CLs and simultaneously satisfy *constraint*-1 only when the following conditions are satisfied:

1) The peak magnitude of injected third harmonic voltage v_3 must be less than or equal to 1/3$^{\mathrm{rd}}$ of the peak of v_k, which is the fundamental component of voltage across primary winding and the corresponding swell in the grid voltage must be less than 12.5%. As observed during 0.225–0.25 s from Fig. 5(d), the peak magnitude of $v_3$is equal to 0.375 pu, which is 1/3$^{\mathrm{rd}}$ of the maximum primary winding voltage (1.125 pu) in Fig. 5(a).
2) The zero crossings of v_3 must always coincide with that of v_k, irrespective of the degree of swell in the grid voltage. If the zero-crossings of v_3 and v_k do not coincide, then the PHC-HVdc shall again demand its CLs to generate negative voltage to satisfy *constraint*-1, which is not possible.

The conclusions drawn from the above case studies in respect to the PHC-HVdc are as follows: It cannot be utilized for exchanging reactive power with the grid since it has a narrow limit of operating MI even with the THIM technique. Also, as can be observed between 0.225 and 0.25 s from Fig. 5(e), the PHC-HVdc should be rated to 1.5 pu to achieve a maximum MI of 1.125. During unbalanced network conditions, the PHC-HVdc injects unequal quantities of third harmonics in its CLs, which may enter into the grid and further degrade the quality of the power system [3]. In addition, depending on the intensity of unbalance in the grid, the operating range of MI of PHC-HVdc gets further narrower [2].

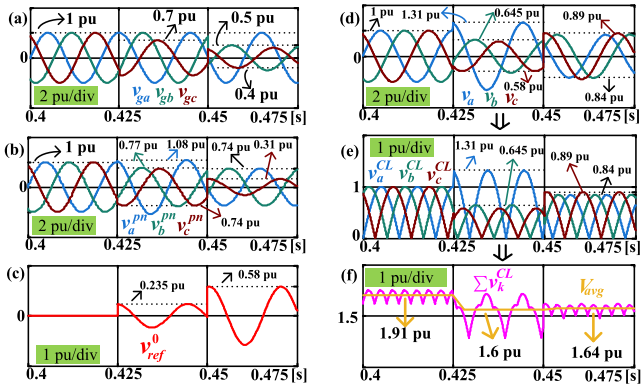

Fig. 6. Waveforms related to PHC-STATCOM. (a) Primary winding voltages without FFZSV. (b) Reference FFZSV. (c) Primary winding voltages with FFZSV. (d) Desired CL voltages. (e) Sum of CL voltages and its average.

It can hence be concluded from the above case studies that the PHC-STATCOM can flexibly vary its MI (0 to 1.33) without any additional control efforts both during balanced and unbalanced grid conditions. This also shows wide range of reactive power exchange capability of PHC-STATCOM. As stated in the introduction, the PHC-STATCOM has a capacitor imbalance issue during unbalanced network conditions. The proposed capacitor voltage control of PHC-STATCOM demands each CL to generate a rectified version of the reference primary winding voltage, which in turn consists of an FFZSV component in addition to positive and negative sequence voltages. This FFZSV has no restrictions on its amplitude and does not require maintaining the same zero-crossings with any of the converter output voltage (primary winding voltage). This is the second degree of freedom of the PHC-STATCOM, which is also illustrated using the waveforms shown below in Fig. 6.

The following grid voltage conditions are assumed as shown in Fig. 6(a). During 0.4–0.425 s, balanced grid voltages exist at nominal voltage (1 pu). During 0.425–0.45 s, the "*c*" phase experiences voltage unbalance of 30% in magnitude and 45° in phase (lead). In the duration 0.45–0.5 s, the "*c*" phase undergoes an unbalance of 60% in magnitude and 180° in phase (lead), while the "*b*" phase experiences an unbalance of 50% in magnitude and 90° in phase (lag).

It is considered that the PHC-STATCOM feeds a balanced grid from 0.4 to 0.425 s at which the *c* phase of the grid experiences a magnitude unbalance of 30% and a phase unbalance of 45° (lead) till 0.45 s. Moreover, at 0.45 s, both the "*b*" and "*c*" phases of the grid undergo voltage unbalance. During 0.45–0.5 s, the "*c*" phase experiences a magnitude unbalance of 60% and a phase unbalance of 180° (lead), while the "*b*" phase experiences a magnitude unbalance of 50% and a phase unbalance of 90° (lag). The corresponding primary winding voltages of transformers of PHC-STATCOM without FFZSV are shown in Fig. 6(b). Thus, the primary winding voltages in Fig. 6(b) are constituted of only positive and negative sequence components, v_k^{pn}. The reference

TABLE II
EXPERIMENTAL PARAMETERS

Parameters	Value	Parameters	Value
Line-line grid voltage	400 V	Transformer turns ratio	1:1.3
Reactive power	3 kVAr	Leakage inductance	2.8 mH
Sub module voltage	111 V	External inductance, L	3 mH
No. of *SM*s/*CL*	3	Sub module capacitance	3.3 mF

FFZSV determined from (28) to (30) for the considered unbalanced grid voltage conditions is shown in Fig. 6(c). In order to obtain the reference FFZSV [Fig. 6(c)], the feedback power terms $P^{\mathrm{CR}}_{k\_fb}$ in (28)–(30) are neglected since they tend to zero in the steady state. In addition, the system losses and the leakage drop are also neglected for ease of calculation of the reference FFZSV. The FFZSV in Fig. 6(c) possesses a magnitude of 0.235 and 0.58 pu during the time instants 0.425–0.45 s and 0.45–0.5 s, respectively. In contrast, the amplitude of the injected third harmonic voltage in the PHC-HVdc is only limited to 0.375 pu as demonstrated in Case-III study associated with Fig. 5. [If the amplitude of injected harmonics in PHC-HVdc exceeds 0.375 pu, then the CLs shall be forced to generate negative polarity voltage to satisfy *constraint*-1 as shown in Fig. 5(h), which is not possible.]

The resultant primary winding voltages of the PHC-STATCOM along with the reference FFZSV are shown in Fig. 6(d). The zero crossings of the resultant primary winding voltages of Fig. 6(d) are utilized as the reference signal for the ZVS operation of H-bridges of PHC-STATCOM. Therefore, the absolute value of the waveforms of Fig. 6(d) fetches the required CL voltages as depicted in Fig. 6(e). The instantaneous sum of the CL voltages of Fig. 6(e) and its average are shown in Fig. 6(f). Even though the magnitude of the FFZSV reaches 0.58 pu (which is greater than 0.375 pu), it can be seen from Fig. 6(e) that the CLs of the PHC-STATCOM do not need to generate negative polarity voltage to satisfy *constraint*-1, unlike the PHC-HVdc [referring to Case-III study of Fig. 5(h)]. This illustrates that the reference FFZSV can possess any magnitude and phase angle as generated by the proposed controller, which is the second degree of freedom of PHC-STATCOM. The amplitude and phase of reference FFZSV must be only limited in a manner such that the maximum voltage required to be generated across each CL [Fig. 6(e)] should not exceed its rating, which is 1.33 pu for the considered experimental case studies. The various control principles of the PHC-STATCOM are verified through experimental case studies in the Section VI.

VI. EXPERIMENTAL VERIFICATION RESULTS

A seven-level scaled-down hardware prototype of the PHC-STATCOM is developed in the laboratory as shown in Fig. 7. The basic experimental parameters are listed in Table II. The operating and proposed control principles of the converter as explained above are verified and demonstrated using the hardware results obtained from the developed experimental setup. The three control layers of the converter are implemented in the DSP TMS320F28335. The DSP generates the gate pulses,

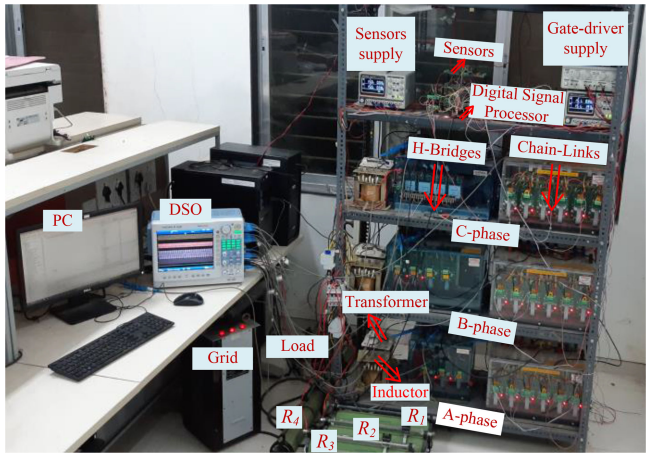

Fig. 7. Experimental prototype of the PHC-STATCOM.

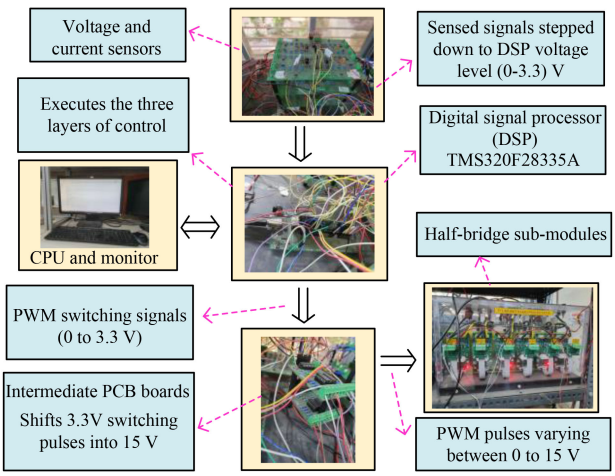

Fig. 8. Block diagram of generation of gate signals in experimental setup.

TABLE III
COMPARISON TABLE

STATCOMS	SDBC	DSCC	DSBC	AAC	PHC-STATCOM
Power exchanged with the grid	S_n	S_n	S_n	S_n	S_n
Line-line voltage of the grid at the PCC (rms)	$\frac{\sqrt{3}V_g^{rated}}{\sqrt{2}}$	$\frac{\sqrt{3}V_g^{rated}}{\sqrt{2}}$	$\frac{\sqrt{3}V_g^{rated}}{\sqrt{2}}$	$\frac{\sqrt{3}V_g^{rated}}{\sqrt{2}}$	$\frac{\sqrt{3}V_g^{rated}}{\sqrt{2}}$
Required number of capacitors	$3\sqrt{3}N$	12N	$12N$	$6N$	$3N$
Required number of switching devices	$12\sqrt{3}N$	$24N$	$48N$	$30N$	$18N$
High-frequency switches	$12\sqrt{3}N$	$24N$	$48N$	$24N$	$6N$
ZVS devices	0	0	0	$6N$	$12N$
Nominal voltage rating of each switching device (peak)	$\frac{V_g^{rated}}{N}$	$\frac{V_g^{rated}}{N}$	$\frac{V_g^{rated}}{N}$	$\frac{V_g^{rated}}{N}$	$\frac{V_g^{rated}}{N}$
Number of voltage levels in the line-line ac output	$2\sqrt{3}N+1$	$4N+1$	$4N+1$	$4N+1$	$4N+1$

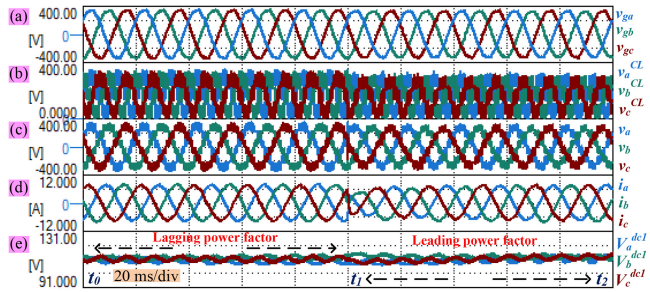

Fig. 9. (a) Grid voltages at the PCC. (b) Chain-link voltages. (c) Primary winding voltages. (d) Primary winding currents. (e) Capacitor voltages.

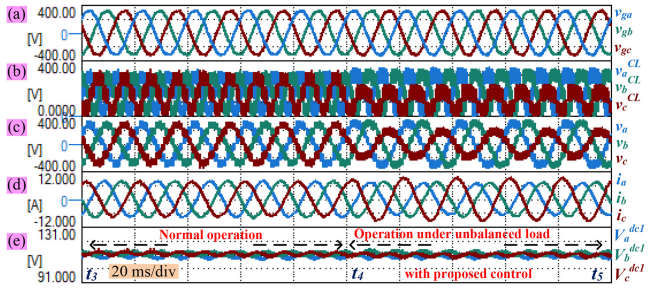

Fig. 10. (a) Grid voltages at the PCC. (b) Chain-link voltages (c) Primary winding voltages. (d) Primary winding currents. (e) Capacitor voltages.

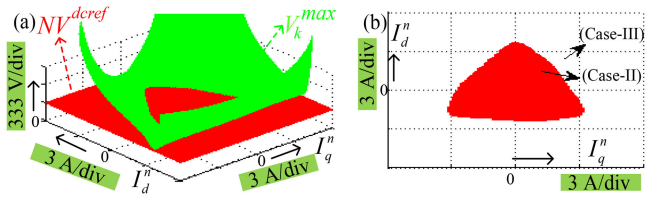

Fig. 11. (a) Plot of the maximum value among the required peaks of the chain-link voltages with varying I_q^n and I_d^n. (b) Locus plane indicating maximum range of I_q^n and I_d^n that can be compensated by the PHC-STATCOM for the case study-II.

which is amplified from 3.3 to 15 V and applied to the gate driver as shown in Fig. 8. The hardware results are categorized into five different case studies, which are explained individually as follows:

The test conditions prevailing with each of the case studies are described as follows:

Case-I: The reactive power compensating capability of the PHC-STATCOM under balanced grid voltage is verified.

During ($t_0 \leq t < t_1$): $I^p_{\text{dref}} = -7.5$ A (lagging reactive current). During ($t_1 \leq t < t_2$): $I^p_{\text{dref}} = 7.5$ A (leading reactive current).

Case-II: The proposed capacitor voltage control technique is verified, while the converter compensates an unbalanced load. Three phase balanced grid voltage exists at PCC (400 V line)

During ($t_3 \leq \text{t} < t_4$): $I^p_{\text{dref}} = -7.5$ A. During ($t_4 \leq \text{t} < t_5$): $I^p_{\text{dref}} = 7.5$ A, $I^n_{\text{dref}} = 1.25$ A and $I^n_{\text{qref}} = 1.25$ A.

Case-III: The truthfulness of the locus plane shown in Fig. 11(b) is verified. Three-phase balanced grid voltage exists at PCC (400 V line).

During ($t_6 \leq \text{t} < t_7$): $I^p_{\text{dref}} = -7.5$ A. During ($t_7 \leq \text{t} < t_8$): $I^p_{\text{dref}} = 7.5$ A, $I^n_{\text{dref}} = 2.25$ A and $I^n_{\text{qref}} = 2.25$ A.

Case-IV: The proposed capacitor voltage control technique is verified under an unbalanced grid. The reference reactive current component is $I^p_{\text{dref}} = -7.5$ A.

During ($t_9 \leq t < t_{10}$): Three-phase balanced grid voltage exists at PCC (400 V line). During ($t_{10} \leq t < t_{11}$), the "c" phase of the grid, at the PCC, experiences a magnitude unbalance of 30% and phase unbalance of 30°.

Case-V: The traditional capacitor voltage control technique discussed in [18] is demonstrated in this case. The test conditions remain same as that of case-IV. The advantages of the proposed method over the one presented in [18] are presented.

The detailed narrations of the individual case studies are given as follows:

Case-I: The ability of the developed experimental setup of the PHC-STATCOM to exchange lagging to leading reactive power with the three-phase grid is verified in this case study and the corresponding waveforms are shown in Fig. 9. The three miniature circuit breakers (MCBs) shown in Fig. 1, MCB_1, MCB_2, and MCB_3 remain ON in this case study. Hence, balanced grid voltage appears at the PCC. The line–line voltage at the PCC is maintained at 420 V (rms) as shown in Fig. 9(a). The reference reactive current is altered from $I^p_{\text{dref}} = -7.5$ A (lagging) to 7.5 A (leading) at the time instant t_1. The converter exactly responds to the reference command, which can be verified from the waveforms of primary winding currents shown in Fig. 9(d). A maximum of three SM capacitors get inserted in each CL [Fig. 9(b)] resulting to a seven-level voltage waveform appearing across each of the primary windings as shown in Fig. 9(c). The waveforms of the capacitor voltages are presented in Fig. 9(e), which are maintained at their reference value of 111 V.

Case-II: The efficacy of the proposed capacitor voltage control technique while the developed PHC-STATCOM compensates an unbalanced load is demonstrated using the waveforms shown in Fig. 10. The converter feeds balanced three-phase currents ($I^p_{\text{dref}} = -7.5$ A) to the grid (400 V) between the instants t_3 and t_4 as shown in Fig. 10(d). However, at time instant t_4, the converter is demanded to compensate negative sequence current given by $I^n_{\text{dref}} = 1.25$ A and $I^n_{\text{qref}} = 1.25$ A in addition to the positive sequence reactive current of $I^p_{\text{dref}} = -7.5$ A. The designed controller senses the unbalance in the converter currents and activates the second layer/proposed capacitor voltage control immediately after the instant t_4. Subsequently, the converter generates required FFZSV across each of the primary windings, which are given by its components $V^0_d = -64$ V and $V^0_q = 40$ V as obtained from (28) and (29). The waveforms of primary winding voltages comprising of the generated FFZSV are illustrated between the time instants t_4 to t_5 of Fig. 10(c). The corresponding CL voltages are shown in Fig. 10(b). The PHC-STATCOM feeds both the desired positive and negative sequence currents to the grid, at the PCC (t_4 to t_5 of Fig. 10(d)) while maintaining the capacitor voltages around its reference of 111 V [Fig. 10(e)]. This proves the authenticity of the proposed control and the derived expressions of the FFZSV components present in (28) and (29).

According to *first degree of freedom*, the PHC-STATCOM is not bound by fixed MI (unlike PHC-HVdc) and each CL can generate desired voltage. The virtue of *first degree of freedom*

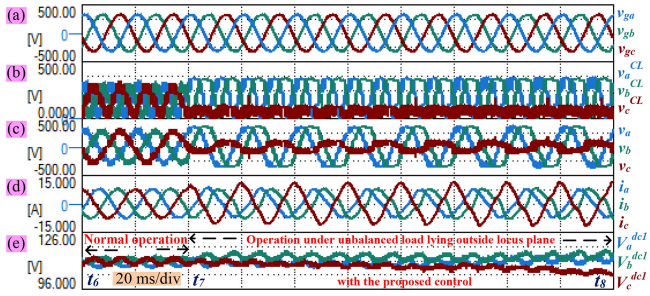

Fig. 12. (a) Grid voltages at the PCC. (b) Chain-link voltages. (c) Primary winding voltages. (d) Primary winding currents compensating unbalanced load located outside locus plane of Fig. R1.3(b). (e) Capacitor voltages.

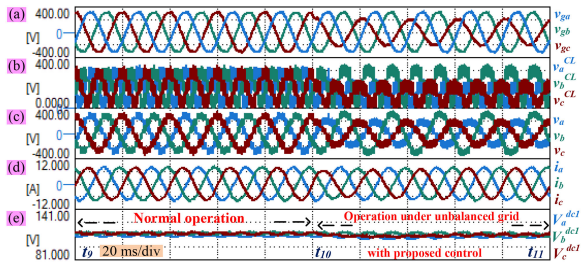

Fig. 13. (a) Grid voltages at the PCC with single-phase unbalance. (b) Chain-link voltages. (c) Primary winding voltages. (d) Primary winding currents. (e) Capacitor voltages.

can be verified physically from Fig. 10(b) where variable voltage levels are generated across the "*c*" phase CL. According to the *second degree of freedom*, the FFZSV required to regulate the capacitor voltages during unbalanced network conditions are free to possess any phase angle and magnitude. For the considered case study, the required FFZSV possess the following components: $V_d^0 = -64$ V and $V_q^0 = 40$ V , which are obtained from the proposed control. This verifies the *second degree of freedom*.

The negative sequence current components compensated by the converter in the above case study ($I^n_{\text{dref}} = 1.25$ A and $I^n_{\text{qref}} = 1.25$ A) are manifested onto a point on the locus plane of Fig. 11(b) and is marked as "case-II." The plane represents the set of points (I_d^n, I_q^n) that can be compensated by the PHC-STATCOM under the considered grid voltage and positive sequence current as that of case-II, while maintaining the capacitor voltages with the help of proposed control. In order to obtain the locus plane, first a range of negative sequence current components are chosen ($-6\text{A} \le I_d^n \le 6\text{A}$), ($-6\text{A} \le I_q^n \le 6\text{A}$) as also shown in Fig. 11(a). For all the feasible values of (I_d^n, I_q^n) within the chosen range, the FFZSV components (V^0_{dref}, V^0_{qref}) required to regulate capacitor voltage are obtained from (28) and (29). These FFZSV components are substituted in (6)–(8) to synthesize the positive peak values of voltage required across each CL. The maximum value among the obtained positive peaks, $V_k^{\max}$, is plotted (in green) as shown in Fig. 11(a). However, the maximum voltage that can be generated by a CL remains less than or equal to 333 V (three SMs and each SM voltage equal 111 V). Hence, the negative sequence current components corresponding to the portion of $V_k^{\max}$, which lies below the sheet of 333 V [in red Fig. 11(a)], procures the locus plane shown in Fig. 11(b). The obtained set of points inside the locus plane forms the unbalanced load compensation zone of the PHC-STATCOM.

Case-III: In this case study also, the PHC-STATCOM is commanded to feed positive sequence reactive current $I^p_{\text{dref}} = -7.5$ A to the balanced grid operating at 400 V between the time instants t_6 and t_7 as shown in Fig. 12(c) and (a), respectively (same operating conditions as that of preceding case between instants t_3 and t_4). However, at time instant t_7, the PHC-STATCOM requires to feed negative sequence current components $I^n_{\text{dref}} = 2.25$ A and $I^n_{\text{qref}} = 2.25$ A in addition to $I^p_{\text{dref}} = -7.5$ A. The considered negative sequence reference current components lie outside the boundary of the obtained locus plane of Fig. 11(b). Hence, the capacitor voltages no longer remain regulated and start diverting from reference value after t_7 as shown in Fig. 12(e). Subsequently, the PHC-STATCOM fails to deliver the desired positive and negative sequence currents to the grid as illustrated between the time instants t_7 and t_8 of Fig. 12(d).

In order to compensate any negative sequence current components that lies outside the zone of the locus plane, as is demanded in this case study, the required value of $V_k^{\max}$ becomes greater than NV^{dcref}, which does not satisfy inequality (32). The CLs of the PHC-STATCOM fail to generate a voltage more than its rating, which can be observed from the CL and primary winding voltage waveforms between the time instants t_7 and t_8 of Fig. 12(b) and (c), respectively.

Case-IV: The ability of the developed hardware structure (Fig. 7) to exchange desired positive sequence reactive power with an unbalanced grid while maintaining its capacitor voltages at their reference with the help of proposed control is demonstrated using the waveforms shown in Fig. 13. Throughout this case study, the converter is demanded to trade only positive sequence reactive current with the grid, which is given by $I^p_{\text{dref}} = -7.5$ A. The line–line voltage of the three-phase grid is maintained at 400 V between t_9 and t_{10}. At the instant t_{10}, the "*c*" phase of the grid experiences a magnitude unbalance of 30% and phase unbalance of 30° as can be observed from Fig. 13(a). The voltage unbalance at the PCC is created by turning OFF the MCB_3 shown in Fig. 1 (MCB_1 and MCB_2 remain ON). The resistance R_3 connected across the MCB_3 causes the voltage unbalance at the PCC as shown in Fig. 13(a). The control system senses the unbalance in the voltage and activates the proposed second layer capacitor voltage control. It can be observed from Fig. 13(d) that the PHC-STATCOM keeps exchanging desired reactive current with the grid even after t_{10} while maintaining its capacitor voltages at its reference [Fig. 13(e)]. The waveforms of the CL voltages and primary winding voltages consisting the generated FFZSV components ($V_d^0 = -38.5$ V and $V_q^0 = -24$ V) are depicted in Fig. 13(b) and (c), respectively, between t_{10} and t_{11}.

The locus plane indicating the load compensation zone of the converter for case-IV is represented in Fig. 14(b). In order to obtain the images of Fig. 14(b), the same procedure is followed, which was used for generating Fig. 11. In both the case studies (II and IV), the converter cannot compensate the unbalance in the load entirely if the latter demands any negative current components, which lies outside the zone of the locus plane

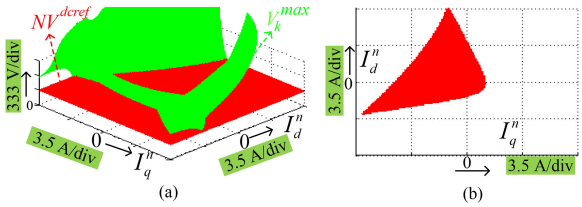

Fig. 14. (a) Plot of the maximum value among the required peaks of the chain-link voltages with varying I_q^n and I_d^n. (b) Locus plane indicating maximum range of I_q^n and I_d^n that can be compensated by the PHC-STATCOM for the case study-IV.

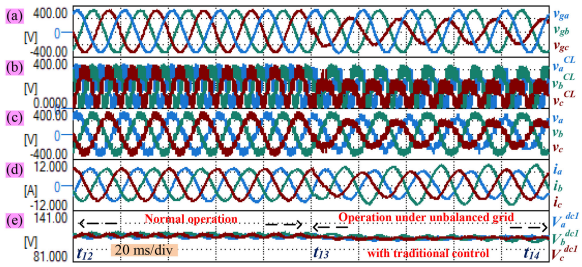

Fig. 15. (a) Grid voltages at the PCC with single-phase unbalance. (b) Chain-link voltages. (c) Primary winding voltages. (d) Primary winding currents. (e) Capacitor voltages controlled with traditional control technique presented in [18].

of Figs. 11(b) and 14(b), respectively. However, under these circumstances, the converter can partially compensate for the unbalanced load by injecting negative sequence currents equal to $I_{\text{dref}}^n = z_1 * I_{Ld}^n$ and $I_{\text{qref}}^n = z_1 * I_{Lq}^n$. z_1 is a positively signed iterative parameter whose value is less than unity and keeps declining with each iteration. This iterative procedure keeps yielding new sets of reference negative sequence current components until they lie inside the well-defined boundaries of the locus planes or satisfy the inequality given in (32). The iterative method involved in obtaining the desired value of $z_1$is not discussed in this article.

Case-V: The traditional capacitor voltage control method discussed in [18] is utilized in this case to regulate the capacitor voltages of the PHC-STATCOM during unbalanced grid voltage conditions. The experimental waveforms are shown in Fig. 15. The test conditions are maintained same as that of the case-IV. The PHC-STATCOM is commanded to feed only positive sequence reactive current ($I_{\text{dref}}^p = -7.5$) to the grid at the PCC throughout the duration t_{12} to t_{14}. The three-phase balanced grid voltage is maintained at the PCC (400 V) till the time instant t_{13}. At the instant t_{13}, a voltage unbalance at the PCC in the "c" phase of the grid is created as in case-IV. The unbalance grid voltage at the PCC can be observed between t_{13} and t_{14} of Fig. 15(a). The traditional capacitor voltage controller [18] is also activated simultaneously at t_{13} instant. In the presence of unbalanced grid voltage, the traditional controller generates reference negative sequence current components to hold the capacitor voltages of the converter at desired reference [18]. The reference negative sequence currents as obtained from [18] for the considered test conditions are given by ($I_{\text{dref}}^n = 1.31$ A and $I_{\text{dref}}^n = -1.66$ A). Now, the primary winding currents comprise of the reference negative sequence current components in addition to the positive sequence component, $I_{\text{dref}}^p = -7.5$ as can also be observed between the time instants t_{13} to t_{14} in Fig. 15(d). The capacitor voltages remain around desired reference as shown in Fig. 15(e). The corresponding CL and primary winding voltage waveforms are also shown in Fig. 15(b) and (c), respectively. The traditional control in [18] regulated the capacitor voltages around 111 V.

A. *Comparison of the Traditional Capacitor Voltage Method in* [18] *With the Proposed Method*

In Case-V, the converter was commanded to feed only positive sequence reactive current to the grid, as stated in beginning of the case. However, as seen in Fig. 15(d), the converter also feeds the generated reference negative sequence currents into the grid. The reference negative sequence currents regulate the capacitor voltages of the converter but are unwanted by the grid. Moreover, the traditional method cannot be utilized to compensate an unbalanced load since, the negative sequence current components of the converter are utilized to control the capacitor voltages.

However, as demonstrated in Case-IV, the converter exchanges only the desired positive sequence current with the grid [Fig. 14(d)] even under unbalanced grid conditions, while the capacitor voltages also remain at reference with the proposed capacitor voltage control. The negative sequence current components of the PHC-STATCOM can be commanded to compensate an unbalanced load since the capacitor voltages are regulated through FFZSV. The capacitor voltage control of the converter with the proposed FFZSV method, under the presence of unbalanced load is demonstrated in Case-II.

From the above comparisons of the experimental results, it is clear that the proposed method is advantageous over the traditional capacitor control technique presented in [18].

B. *Comparative Analysis*

The PHC-STATCOM is compared with the popular existing STATCOM configurations such as SDBC [19]–[23], DSCC [12]–[16], DSBC [12], [16] and AAC [42], [43] in terms of required number of switching devices and capacitors and are listed in Table III. The comparison is done by taking into count the same output apparent power (S_n), line-to-line grid voltage $\sqrt{3}V_g^{\text{rated}}/\sqrt{2}$, and voltage rating of the switching device. The following assumptions are incorporated to generalize and to ease the process of comparison: the balanced grid conditions are considered, the turns-ratio of the transformers are assumed to be unity, the leakage inductance drop of the transformer is neglected, and the MI is unity. Furthermore, the nominal voltage rating of switching device associated with each SM of the PHC-STATCOM (V_g^{rated}/N) is considered as the basic building switch for all the topologies under consideration. It can be concluded from the comparison table that the PHC-STATCOM requires least number of SM capacitors and switching devices than all the popular STATCOM topologies, besides generating same number of levels in its line-to-line output ac voltage, as that of the other considered topologies. Hence, compared to the existing topologies, the proposed PHC-STATCOM will have least size, weight, and footprint for a given power rating.

VII. Conclusion

This article has proposed the PHC-STATCOM which is able to regulate the MI to any desired value without any additional dedicated control, unlike the PHC-HVdc. It is due to the first degree of freedom associated with the proposed converter. In addition, a generalized power analysis of the proposed converter is performed, which reveals that the CLs retain unequal CR powers while feeding an unbalanced network. This creates the capacitor voltage imbalance issue in the PHC-STATCOM. A control method is proposed in this article using the FFZSV components to regulate the capacitor voltages. The generalized expressions for the reference FFZSV components ($V^0_{d\text{ref}}$and $V^0_{q\text{ref}}$) required to neutralize the CR powers are derived. These components are free to possess any required value (indirectly controlling the magnitude and phase angle of the FFZSV) in order to resolve the capacitor voltage imbalance problem. This is the second degree of freedom in the proposed converter. The FFZSV components should be limited such that the required voltage across the CLs does not exceed its rating. The positive and negative sequence current components of the converter compensate the reactive power and unbalance in the load, while the FFZSV control the capacitor voltages. The FFZSV components utilized in the proposed scheme do not reflect in the grid voltage. On the other hand, the unequal harmonic voltages injected in the PHC-HVdc to control capacitor voltage appear in the grid voltage. A detailed analysis is presented to compare the degrees of freedom associated with the PHC-STATCOM against the PHC-HVdc, proving that the PHC structure is utilized more proficiently when applied for the reactive power compensation applications.

The working principles of the PHC-STATCOM and the proposed capacitor voltage control technique are verified by the experimental studies. In the supervision of the proposed capacitor voltage control, the maximum range of load unbalance that the PHC-STATCOM can compensate for the considered experimental case studies are derived and plotted on loci planes. The advantages of the proposed capacitor voltage control over one of the existing control methods are demonstrated by using experimental studies. Furthermore, a comparative study is carried out to substantiate that the proposed converter requires lesser number of SMs, switching devices, and capacitors than the existing STATCOM configurations such as SDBC, DSCC, DSBC, and AAC for a given output power, line voltage, and voltage rating of switches.

Acknowledgement

This publication is an outcome of the R&D work undertaken in a project under the SERB Technology Translation Award (SERB-TETRA) scheme of the Department of Science and Technology, Government of India.

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