Modular Model Predictive Control of a 15-kW, Kilo-to-Mega-Hertz Variable-Frequency Critical-Soft-Switching Nonisolated Grid-Tied Inverter With High Efficiency

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***Abstract*—A variable-frequency critical-soft-switching (VF-CSS) model predictive control method is developed combining with a modified nonisolated inverter to improve the efficiency. A two-level control structure is developed, including 1) the central-level grid-side inductor current control and zero-sequence voltage control; and 2) the local-level per-phase power module control of VF-CSS model predictive controller with state estimator. Two VF-CSS controllers are proposed, including variable-continuous-frequency critical-soft-switching controller and variable-discrete-frequency critical-soft-switching, to achieve critical soft-switching operation for high efficiency. The combination of MPC and VF-CSS guarantees a complete critical soft-switching operation at full period range of varying frequency and especially during transient. The state estimator provides sampling noise rejection and accurate switch-side inductor current estimations for MPC and VF-CSS. Also, with the help of state estimator, the current sensor cost is reduced by 50%. Meanwhile, the estimator contributes to a more accurate switch-side inductor current reading for MPC implementation with variable continuous frequency controller, especially when the critical soft switching requires huge inductor current ripple. With the proposed control strategies and topology, medium-frequency (>200 kHz, 45 μH) and high-frequency (>1 MHz, 4.5 μH) test benches are validated experimentally. The efficiency is above 99% at a rated power of 15 kW. A power density of more than 10.4 kW/L is achieved.**

***Index Terms*—Critical soft switching (CSS), model predictive control (MPC), state estimator, variable switching frequency control.**

I. Introduction

With the increasing demands of high efficiency, high power density, and better dynamic/steady-state performance in the application of power electronics, more advanced control techniques and circuitry topologies have been studied to improve the performance of power converters. To achieve high power density with low volume, the size of passive magnetic components needs to be reduced. Thus, it is necessary to increase the switching frequency for maintaining reasonable current/voltage ripples on the inductor/capacitor [1], [2]. However, higher switching frequency brings more switching losses and inductor losses, which could influence the efficiency of the power conversion system. Thus, there exists a typical trade-off between efficiency and power density for balancing [3]. For the dynamic performance of power converters, besides a careful hardware design, more advanced control techniques can contribute to the transient behavior. Model predictive control (MPC) has been studied to have better dynamic performance than the traditional method of proportional and integral (PI) control [4].

First, for the trade-off between high efficiency and high power density, soft-switching techniques can be applied to achieve both targets with less compromise [5]. The switching losses are mainly caused by the overlapping of voltage and current across the switch during turn-ON and turn-OFF transients. Soft-switching techniques are generally aimed at minimizing the overlapping area of switch voltage and current in transients. Zero-voltage switching (ZVS) and zero-current switching (ZCS) are the two main soft-switching methods [6], [7]. ZVS focuses on reducing the voltage across the switch and ZCS can minimize the current flowing through the switch during the turn-ON or turn-OFF transients [8], [9]. The soft switching can be achieved by adding auxiliary circuit. Typically, extra inductor, capacitor, and switch are needed to form the buffer circuit for the implementation of soft switching [10], [11]. This will bring extra cost and control complexity. Another method to achieve ZVS is by replacing the higher turn-ON loss with lower turn-OFF loss. This strategy can be realized by controlling the switch-side inductor current ripple to be bidirectional during switching transients [12]. To control the peak/valley inductor current for ZVS, the simplest way is varying the switching frequency for the adjustment of inductor current ripple [13]. A variable frequency soft-switching method is proposed in this article in combination with MPC and state estimator to reduce the switching losses without introducing auxiliary circuit.

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Second, for the improvement of dynamic performance, advanced control techniques can be applied. Different from the conventional PI control method, MPC has the advantages in the aspects of rising time, overshoot, and disturbance rejection [14]. The MPC is typically implemented by optimizing the tracking error between the measurement and reference in the desired future steps to predict the duty cycle for the modulation [15]. Some recent MPC techniques have been published to improve the performance of inverter control [16]–[19]. Specifically, [16] leveraged joint voltage vector for the Quazi-Z-Source inverter MPC control to suppress the current ripple. Aragon *et al.* [17] developed the constrained MPC algorithm based on large-signal model for microgrid inverter. Nam *et al.* [18] proposed a voltage-sensorless MPC for grid-connected inverter. And Guo *et al.* [19] enabled the MPC control with inductance online identification capability and improved phase-locked loop (PLL). The MPC can perform a high tracking speed with less transient oscillation, especially during load or reference variations [20]. This characteristic can be combined with the variable frequency soft-switching technique to reduce the oscillation caused by the switching frequency variation. This article leverages the advantages of MPC in dynamic performance to mitigate the oscillation and stability issue caused by the variable frequency soft-switching operation.

Third, for the accuracy of state parameter acquisition, the state estimation techniques have been developed to improve the quality of sampling information and reduce the sensor cost. The recent publications are introduced as follows. Specifically, in the power electronics field, Cheng *et al.* [21] developed a state and disturbance observer for grid-connected inverter under non-ideal conditions. Mondal *et al.* [22] proposed a robust observer algorithm for voltage and frequency control of a doubly fed induction generator. Wang *et al.* [23] applied an extended-state observer estimation method for LCL inverter to improve the observation dynamics. Tran *et al.* [24] studied the resonant extended state observer for grid voltage estimation of LCL inverter.

The contributions of this article can be concluded in four main aspects. First, the combination of MPC with variable-frequency critical-soft-switching (VF-CSS) control improves the efficiency of grid-connected inverter. The unexpected hard switching power loss from the oscillation caused by the time-varying switching frequency is attenuated by the MPC due to the robust transient performance. Second, two variable-frequency techniques, variable-continuous-frequency critical-soft-switching (VCF-CSS) and variable-discrete-frequency critical-soft-switching (VDF-CSS), are proposed to achieve the full grid period soft switching. A Luenberger observer is designed to be integrated with VCF-CSS for a more accurate inductor current estimation and soft-switching boundary calculation. Both VCF-CSS and VDF-CSS do not need extra sensor circuits, e.g., [25], to sample the averaged inductor current for soft switching. Third, the zero-sequence voltage control method combined with the modified inverter topology enables the nonisolated circuitry application with low leakage current. Fourth, compared with the typical prototypes, the designed inverter achieves the Pareto optimal points in the parameters of frequency-power and efficiency-power density.

The article is organized as follows. First, a modified nonisolated grid connected inverter topology is introduced. The modified topology is composed based on a fundamental power module for each phase. The power module includes upper/lower switches, switch-side inductor, and two output capacitors to be connected to the upper/lower dc bus terminals. Three power modules can be connected to form a modified three-phase nonisolated inverter with the capability to stabilize the zero-sequence voltage and attenuate the leakage current. Then, based on the power module, a critical soft-switching technique is introduced to reduce the large turn-ON loss with small turn-OFF loss for the improvement of efficiency. Third, the control strategies are proposed, including three parts: 1) central level of grid current control/zero-sequence voltage control cascaded with local level of per-phase power module modular MPC; 2) two types of VF-CSS controllers including VCF-CSS and VDF-CSS to achieve highly efficient critical soft-switching operation by adjusting switching frequency and inductor current ripple; 3) state estimator for per-power module to estimate the switch-side inductor current, output capacitor voltage, and grid-side inductor current with the sampling values of output capacitor voltage and grid-side inductor current. The combination of MPC and VF-CSS guarantees a complete critical soft-switching operation at full period range of varying frequency and especially during transient. The estimator provides noise rejection and accurate switch-side inductor current estimations for MPC and VF-CSS. Three controllers can be combined to achieve a high efficiency, good dynamic/steady-state performance nonisolated grid-tied inverter with low leakage current. Finally, two cases of prototype are built with medium frequency/medium inductance ($>$200 kHz, 45 μH) and high frequency/small inductance ($>$1 MHz, 4.5 μH) to validate the effectiveness of the proposed methods. The efficiency is above 99% at a rated power of 15 kW. A power density of more than 10.4 kW/L is achieved.

II. System Modeling

The proposed control methods are based on a modified non-isolated grid-tied LCL inverter. Different from the conventional L and LCL types of nonisolated inverters in Fig. 1, the proposed topology is shown in Fig. 2, which consists of three power module units and three grid-side inductors, L_{fg}. The per-phase power module unit is composed of upper/lower switches, M_1 and M_2, switch-side inductor, L_{fs}, and two output capacitors connected to the upper/lower dc bus terminals, $C_{f,\text{up}}$ and $C_{f,\text{lo}}$. The modification of nonisolated topology contributes to the stabilization of common mode voltage leveraging the proposed control methods and the proposed VF-CSS methods, VCF-CSS and VDF-CSS, are based on the per-phase power module unit. As is shown in Fig. 2, the local-level control is implemented at each of the power module independently for MPC, estimator, and VF-CSS to improve the efficiency and dynamic/steady-state performance.

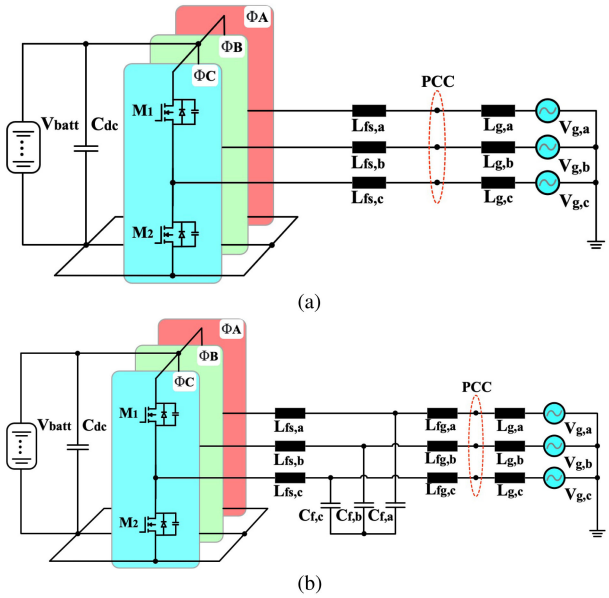

Fig. 1. Conventional (a) L and (b) LCL types of nonisolated inverters. (a) Conventional L type of nonisolated inverter. (b) Conventional LCL type of nonisolated inverter.

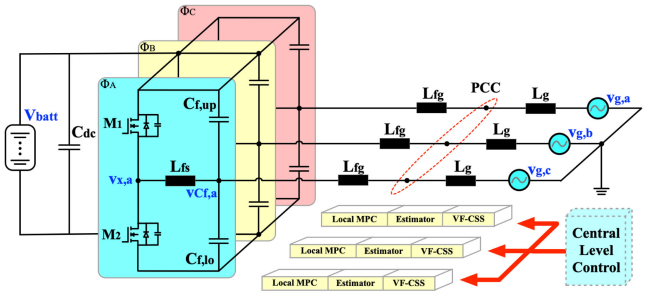

Fig. 2. Proposed modified nonisolated inverter composed of per-phase power modules.

A. Nonisolated Topology Modeling

The modified nonisolated topology is composed of three power modules (upper/lower switches, switch-side inductor, upper/lower capacitors), grid-side inductors, and dc bus capacitor, as is shown in Fig. 2. With the help of the power module units labeled in colored blocks in Fig. 2, the upper/lower common points of three-phase output capacitors are connected to the positive/negative dc bus terminals, respectively. This topological modification allows the zero-sequence capacitor voltage to be stabilized as constant and the leakage current to be bypassed from flowing into the grid. To combine the proposed topology with control strategy and stabilize the zero-sequence voltage, the modeling of the proposed converter needs to be transformed from abc to $dq0$ reference frame.

1) abc Reference Frame: The state-space equations in abc system can be expressed as

$$\dot{i}_{Lfs,abc} = \frac{1}{L_{fs}}\mathrm{I}v_{x,abc} - \frac{1}{L_{fs}}\mathrm{I}v_{Cf,abc} \tag{1a}$$

$$\dot{v}_{Cf,abc} = \frac{1}{C_f}\mathrm{I}i_{Lfs,abc} - \frac{1}{C_f}\mathrm{I}i_{Lfg,abc} \tag{1b}$$

$$\dot{i}_{Lfg,abc} = \frac{1}{L_{fg}}\mathrm{I}v_{Cf,abc} - \frac{1}{L_{fg}}\mathrm{I}v_{g,abc} \tag{1c}$$

where L_{fs}, C_f, and L_{fg} are the switch-side inductor, capacitor, and grid-side inductor, respectively, for the LCL filter. $v_{x,abc}$, $i_{Lfs,abc}$, $v_{Cf,abc}$, $i_{Lfg,abc}$, and $v_{g,abc}$ are the switch leg output voltage, switch-side inductor current, lower output capacitor voltage, grid-side current, and grid voltage in abc reference frame, respectively. And the upper dot represents the differential calculation. Also, it is worth noting that only one voltage sensor is required in each phase for the lower output capacitor voltage. Since the dc voltage source is constant, only the negative dc bus terminal is needed as the reference for the zero-sequence voltage stabilization. $\mathbf{I} \in \mathbb{R}^{3\times3}$ is the identity matrix.

2) $dq0$ Reference Frame: For the zero-sequence voltage stabilization and leakage current attenuation, the circuit model needs to be transformed from abc to $dq0$ reference frame. Traditional three-phase grid-tied inverter control only considers dq components, as is shown in Fig. 1. The proposed topology in Fig. 2 connects the common points of output capacitors to the positive/negative dc bus terminals, which allows the zero-sequence voltage to be controlled constant as half of dc bus. Thus, the zero-sequence current to the grid can be mitigated accordingly. Leveraging the Clarke and Park transformations, the abc components can be converted to $\alpha\beta0$ and then to $dq0$ for the control purpose.

The state-space equations in $dq0$ reference frame can be expressed as

$$\dot{i}_{Lfs,dq0} = \frac{1}{L_{fs}}\mathrm{I}v_{x,dq0} - \frac{1}{L_{fs}}\mathrm{I}v_{Cf,dq0} - \omega\mathrm{G}i_{Lfs,dq0} \tag{2a}$$

$$\dot{v}_{Cf,dq0} = \frac{1}{C_f}\mathrm{I}i_{Lfs,dq0} - \frac{1}{C_f}\mathrm{I}i_{Lfg,dq0} - \omega\mathrm{G}v_{Cf,dq0} \tag{2b}$$

$$\dot{i}_{Lfg,dq0} = \frac{1}{L_{fg}}\mathrm{I}v_{Cf,dq0} - \frac{1}{L_{fg}}\mathrm{I}v_{g,dq0} - \omega\mathrm{G}i_{g,dq0} \tag{2c}$$

where ω is the angular velocity of the grid in rad/s. G is the matrix for the coupling terms resulted from the transformation

$$\mathrm{G} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}. \tag{3}$$

$i_{Lfs,dq0}$, $v_{Cf,dq0}$, $i_{Lfg,dq0}$ and $v_{x,dq0}$ are the switch-side inductor current, capacitor voltage, grid-side current and grid voltage in $dq0$ reference frame, respectively.

With the Clarke and Park transformations, the three-phase abc components of switch-side inductor current, capacitor voltage, and grid-side inductor current can be converted to $dq0$ reference frame for control. The zero-sequence voltage can be stabilized to be half of dc bus voltage with MPC controller and the leakage current will be bypassed within the power modules in Fig. 2.

B. Critical Soft-Switching Analysis

To reduce the switching losses of the power module, a critical soft-switching method is introduced in this section. The critical

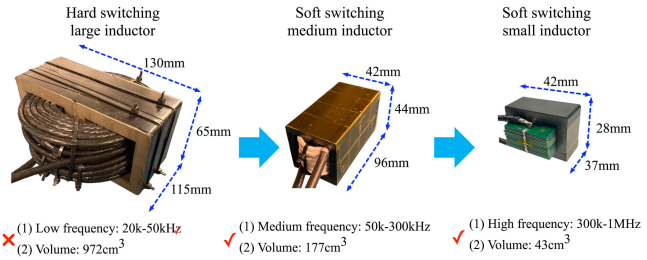

Fig. 3. Three inductor size comparison for implementing low-, medium-, and high-frequency converters.

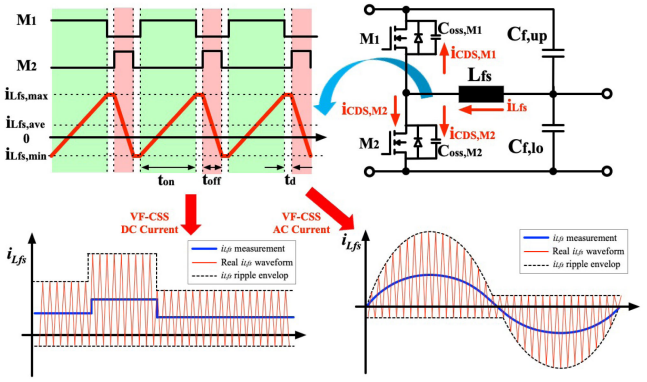

Fig. 4. Critical soft-switching working principles for dc and ac current modes.

soft-switching technique is aimed at improving the power density and efficiency at the same time. It permits to increase the switching frequency by a factor of 3–5 and reduce the required inductance by a factor of 10–20. As is shown in Fig. 3, three sets of inductors are compared in size and volume with the inductance of 450, 45, and 4.5 μH, respectively. From left to right of the three inductors, the inductance are decreased by a factor of 10 in sequence, and the volume is decreased by the factors of 5.5 and 4.1 in sequence, respectively. For the inductor design perspective considering the area product, losses, and current ripple saturation, the desired operating frequencies are increased by a factor of 3–5 from left to right in sequence. Thus, instead of using a bulky 450-μH inductor on the left side of Fig. 3 for hard switching, the critical soft-switching technique enables smaller inductors on the middle and right sides of Fig. 3 with lower inductance/switching losses and higher switching frequency/power density.

The working principle diagram of critical soft switching is shown in Fig. 4 with dc and ac current modes for each of the proposed power module. The core idea of critical soft-switching method is to replace the large turn-ON loss of the upper switch with small turn-OFF loss of the lower switch in the power module. For a typical SiC MOSFET, C3M0021120 K, at a certain dc voltage of 800 V, the turn-ON, turn-OFF, and total switching losses of energy are been plotted in Fig. 5 with the drain–source current, which shows that the turn-ON loss is four times larger than the turn-OFF loss. The methodology of critical soft switching is to ensure that the peak point and valley point of the switch-side inductor current should be positive and negative, respectively.

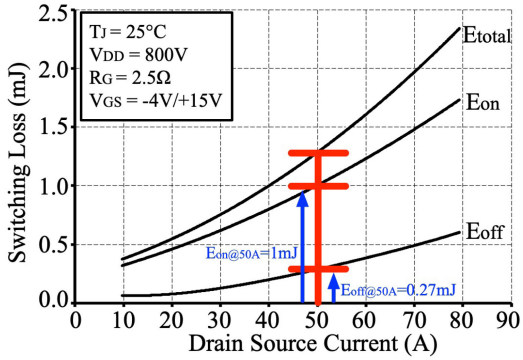

Fig. 5. Turn-ON and turn-OFF loss comparison of typical SiC MOSFET C3M0021120 K.

And the absolute values of positive peak point and negative valley point should be above a threshold current level to ensure the complete soft switching. The threshold current and dead time define the boundary condition of critical soft switching. As is shown in Fig. 4, in the turn-ON transient of upper switch, a negative inductor current can discharge the upper switch output capacitor, $C_{\text{oss},M1}$. The zero-voltage turn-ON of upper switch will be achieved if $C_{\text{oss},M1}$ is fully discharged before it turns ON. Similarly, a positive inductor current is needed to fully discharge the lower switch output capacitor, $C_{\text{oss},M2}$, before it turns ON. The critical soft switching deals with the boundary condition of zero-voltage soft turn-ON for the required threshold current and dead time to fully discharge the output capacitors of upper and lower switches before they turn ON. The dc and ac current modes of switch-side inductor current waveforms are shown at the bottom of Fig. 4, where the dashed lines of current ripple envelope demonstrate the required threshold current for critical soft-switching operation at certain dead time.

The switch-side inductor current peak/valley point values, $i_{Lfs,\max/\min}$, for critical soft-switching operation can be expressed by the drain–source current through the upper and lower switches, $i_{\text{DS},M1}$ and $i_{\text{DS},M2}$, and the current through the upper and lower switch output capacitance, $i_{\text{CDS},M1}$ and $i_{\text{CDS},M2}$. And the $i_{\text{CDS},M1}$ and $i_{\text{CDS},M2}$ are the derivative functions of upper/lower switch output capacitors, $C_{\text{DS},M1}$ and $C_{\text{DS},M2}$, and drain–source voltages, $v_{\text{DS},M1}$ and $v_{\text{DS},M2}$. Then, with the integral calculation in each switching dead time period, t_d, the required $i_{Lfs,\max/\min}$ at specific dead time can be further expressed by the discharge, $Q_{\min}$ and $Q_{\max}$, of upper/lower switch output capacitors, which have been provided by the MOSFET manuals

$$\tfrac{1}{2} i_{Lfs,\min} t_d \le Q_{\min} \le 0 \tag{4a}$$

$$\tfrac{1}{2} i_{Lfs,\max} t_d \ge Q_{\max} \ge 0. \tag{4b}$$

Then, the model of critical soft-switching method can be expressed with the function image in Fig. 6, where the light green regions are the feasible soft-switching range based on (4) and the peak/valley inductor current can be controlled with the developed methods in the following sections.

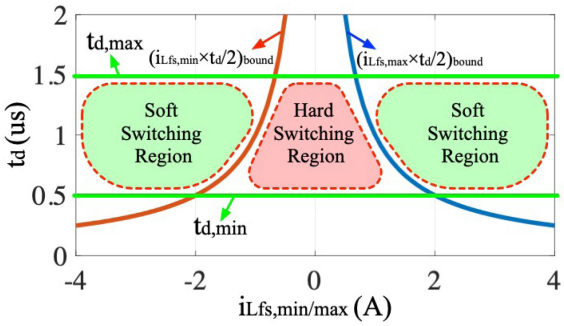

Fig. 6. Critical soft-switching operation regions for different devices.

III. Control

The proposed control strategies of the modified nonisolated converter include two layers of control: 1) Central-level grid-side inductor current control and zero-sequence voltage MPC control to generate the references for the per-phase power module local control; 2) local-level per-power module MPC, state estimator, and VF-CSS control. The combination of MPC and VF-CSS guarantees a complete critical soft-switching operation at varying frequency and even transient. The state estimator provides noise rejection and more accurate switch-side inductor current estimations for MPC and VF-CSS.

A. Central-Level Grid Current/Zero-Sequence Voltage Control

As is shown in the left block of Fig. 7, the central-level control layer is composed of PLL, Park/Clarke transformations, grid current control, and zero-sequence voltage control. Two main targets are achieved with central-level grid current and zero-sequence voltage control: 1) provide the three-phase capacitor voltage references for local-level power module MPC control; and 2) stabilize the zero-sequence voltage and attenuate the leakage current for the modified nonisolated topology.

1) Grid-Side Inductor Current Control: The three-phase grid-side inductor currents are transformed from abc to $dq0$ reference frame with PLL and Clarke/Park transformations. Two PI controllers are designed to regulate the d and q components of grid current, $i_{Lfg,d}$ and $i_{Lfg,q}$, respectively. The outputs of dq grid current controllers are configured as the dq output capacitor voltage references, $V^*_{c,d}$ and $V^*_{c,q}$, respectively. Then, $V^*_{c,d}$ and $V^*_{c,q}$ are transformed to abc reference frame as $V^*_{c,a}$, $V^*_{c,b}$, and $V^*_{c,c}$ for the tracking purpose of per-phase local power module MPC control.

2) Zero-Sequence Voltage Control: Based on the proposed topological modification in Fig. 2 to connect three-phase output capacitors common points with positive/negative dc bus terminals, the zero-sequence capacitor voltage is controlled to be half of dc bus voltage, as is shown in Fig. 7. In central-level control layer, the zero-sequence output capacitor voltage reference is configured to be half of dc bus voltage and allocated to the local level per-phase MPC controller. Thus, the local MPC can stabilize the zero-sequence capacitor voltage to attenuate the leakage current. Since the controlled three-phase output capacitor voltages, $v_{Cf,abc}$, are measured with respect to the dc bus negative terminal and the upper/lower capacitors are connected to the dc bus positive/negative terminals, the output capacitor voltage waveforms will be ranged within 0–$V_{\rm dc}$ and centered at $V_{\rm dc}/2$. Thus, the reference of zero-sequence voltage controller is configured as $V_{\rm dc}/2$ for the common mode voltage stabilization.

In the conventional topologies, the zero-sequence capacitor voltage is not controlled to be constant, which causes the leakage current to be flowing into the grid. However, in the proposed modified circuit, the zero-sequence capacitor voltage is stabilized by MPC to be half of dc bus. Thus, the zero-sequence current will be bypassed to be only flowing through the switch-side inductors. The leakage current will be prevented from injecting into the grid. The definition of leakage current to the grid can be expressed as

$$i_{Lfg,0} = C_p \frac{dv_{c,0}}{dt}. \tag{5}$$

Thus, the zero-sequence capacitor voltage stabilization by MPC can attenuate the grid-side leakage current.

B. Local-Level Model Predictive Control

For the purpose of improving the dynamic performance especially when the controller is combined with variable-frequency operations, an explicit MPC method is designed for the per-phase switch-side capacitor voltage and inductor current control by solving the *constrained finite-time optimal control* problem. As is shown in Fig. 7 of the control diagram, the three-phase capacitor voltages are controlled in abc frame to follow the references from the cascaded grid current controller's outputs. The switch-side inductor currents are also regulated with the MPC by adjusting the weighing factor between $i_{Lfs,abc}$ and $v_{Cf,abc}$. The benefits to configure the MPC per-phase in abc frame can be concluded as follows: 1) The state-space matrix of *LC* per-phase is simpler than dq system to implement the offline piecewise affine (PWA) optimization code in a less costly digital signal processor (DSP) controller; (2) the time-varying angular speed term, ω, in (2) can be omitted in the explicit MPC state-space matrix for the offline optimization calculation; (3) per-phase MPC for *LC* is more flexible for a modular design perspective to extend the paralleled phase number and other topologies, e.g., dc/dc, single-phase dc/ac converters.

For the MPC implementation, in every control period, the MPC controller receives the measured switch-side inductor current, $i_{Lfs,abc}$, output lower capacitor voltage, $v_{Cf,abc}$, grid current, $i_{Lfg,abc}$, from analog-to-digital converter (ADC) and capacitor voltage reference, and $v^*_{Cf,abc}$ from the grid current controller. An offline generated PWA search tree is applied to derive the optimal duty cycle for the explicit MPC. The equivalent circuit for each power module is shown in Fig. 8 with the variables to derive the state-space equation for MPC. The state equations of switch-side *LC* filter can be expressed as

$$i_{Lfs}(k+1) = i_{Lfs}(k) - \frac{T_s}{L_{fs}} v_{Cf}(k) + \frac{v_{\rm dc} T_s}{L_{fs}} d(k) \tag{6a}$$

$$v_{Cf}(k+1) = \frac{T_s}{C_f} i_{Lfs}(k) + v_{Cf}(k) - \frac{T_s}{C_f} i_{Lfg}(k). \tag{6b}$$

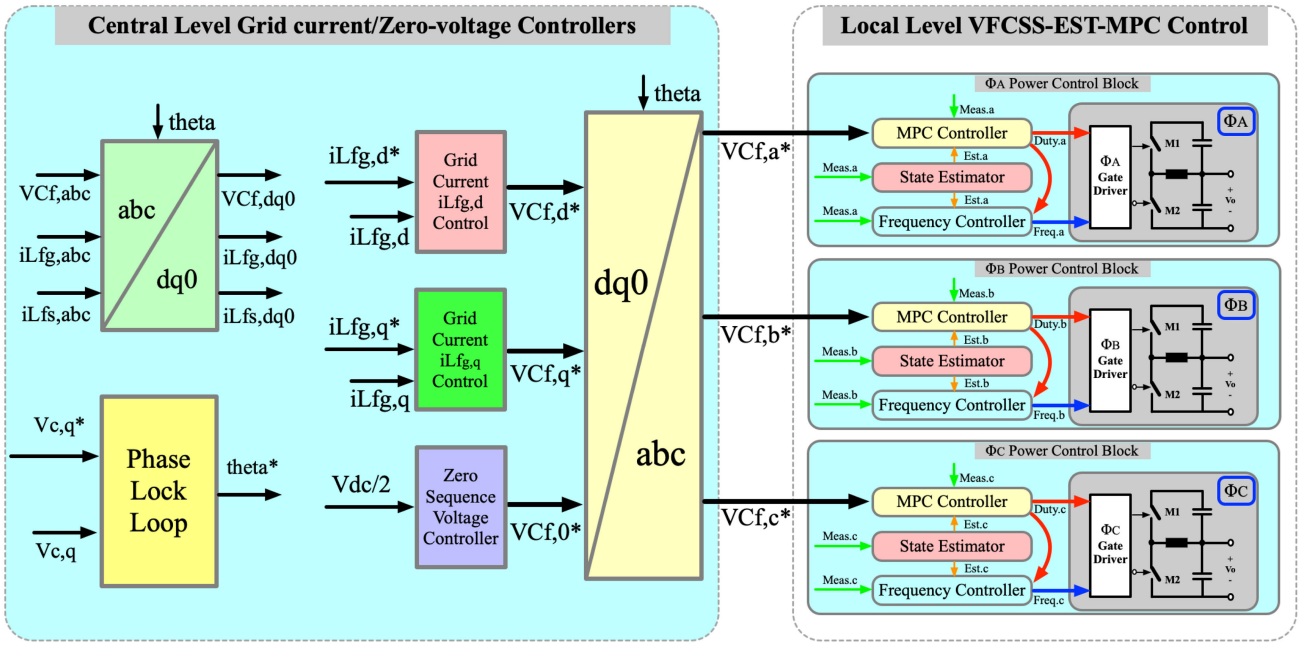

Fig. 7. Proposed control diagram.

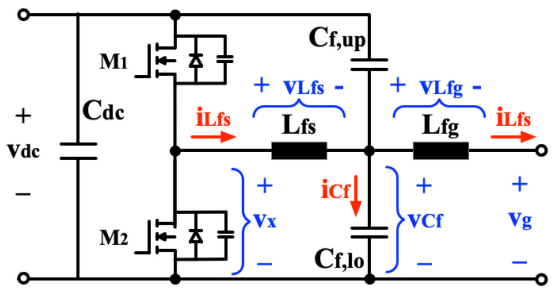

Fig. 8. Equivalent circuit for state-space equation.

For the flexibility of implementing the explicit MPC and the convenience of experimentally adjusting the dc bus voltage during test, the last term of (6), $v_{\rm dc}d(k)$, can be replaced by the switch leg output voltage, $v_x(k)$. The state-space model for MPC can be expressed in standard matrix format of

$$X_{k+1} = A_C X_k + B_C u_k + E_C e_k \tag{7}$$

where the variables and matrices for MPC control represent

$$A_C = \begin{bmatrix} 1 & -\frac{T_s}{L_{fs}} \\ \frac{T_s}{C_f} & 1 \end{bmatrix}, B_C = \begin{bmatrix} \frac{T_s}{L_{fs}} \\ 0 \end{bmatrix}, E_C = \begin{bmatrix} 0 \\ -\frac{T_s}{C_f} \end{bmatrix}, \tag{8a}$$

$$X_k = \begin{bmatrix} i_{Lfs}(k) \\ v_{Cf}(k) \end{bmatrix}, u_k = \begin{bmatrix} v_{\rm dc} d(k) \end{bmatrix}, e_k = \begin{bmatrix} i_{Lfg}(k) \end{bmatrix}. \tag{8b}$$

In the MPC formulation, the inductor current/capacitor voltage references can be defined as $\bar{X}$ and the tracking errors between the measurement and the references are expressed as $\tilde{X}$, which are composed of

$$\bar{X}_k = \begin{bmatrix} i_{Lfs,ref}(k) \\ v_{Cf,ref}(k) \end{bmatrix}, \tilde{X}_k = \begin{bmatrix} i_{Lfs,ref}(k) - i_{Lfs}(k) \\ v_{Cf,ref}(k) - v_{Cf}(k) \end{bmatrix}. \tag{9}$$

Thus, the cost function includes two terms

$$\min \sum_{k=0}^{N_c} \tilde{X}_k^T Q_C \tilde{X}_k + \sum_{k=0}^{N_p-1} \triangle u_k^T R_C \triangle u_k. \tag{10}$$

For the penalties of the MPC cost function, Q_C and R_C represent the weighing factor matrices that are implemented on the state values and input values, respectively.

The constraints of the MPC controller can be expressed as

$$\tilde{X}_{k+1} = A\tilde{X}_k + Bu_k + Ee_k \in \mathcal{X} \tag{11}$$

$$\triangle u_k = u_k - u_{k-1} \in \mathcal{U} \tag{12}$$

$$\begin{bmatrix} -I_{Lfs,\max} \\ 0 \end{bmatrix} \le X_k \le \begin{bmatrix} I_{Lfs,\max} \\ v_{\rm dc} \end{bmatrix} \tag{13}$$

$$\begin{bmatrix} 0 \end{bmatrix} \le u_k \le \begin{bmatrix} v_{\rm dc} \end{bmatrix} \tag{14}$$

$$\begin{bmatrix} -I_{Lfg,\max} \end{bmatrix} \le e_k \le \begin{bmatrix} I_{Lfg,\max} \end{bmatrix}. \tag{15}$$

Since the application of the MPC is kilo-to-mega-Hertz switching frequency, the execution efficiency of the algorithm should be high. Thus, an explicit method is developed to relieve the online MPC implementation burden. Specifically, based on the state-space model, cost function and the corresponding constraints of the power module, a PWA function is derived with computer and the related C code is configured in the DSP controller memory for the online implementation. The internal operation principle of the MPC is shown in Fig. 9, where the flowchart of MPC implementing process is demonstrated. The PWA function is reflected on the C code as n sections of active regions, H_n and K_n, with the corresponding feedback law, F_n and G_n. And the colored areas in Fig. 9 represent different regions. A binary search tree is configured to quickly find the

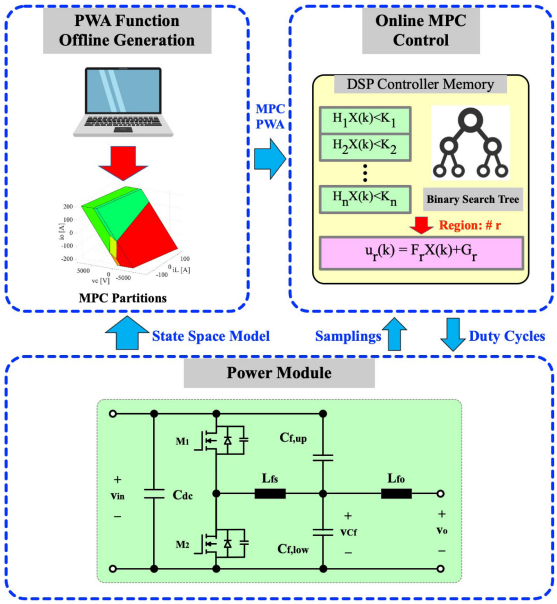

Fig. 9. MPC optimization search tree implementing process.

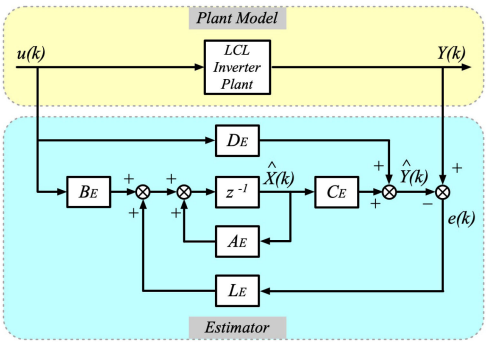

Fig. 10. Diagram of the state estimator.

active region, r, and the related feedback law, F_r and G_r, for the derivation of the optimal duty cycle.

During the control interrupt period, the binary search tree finds the active region, r, based on the ADC samplings/estimations of inductor current, capacitor voltage, output current, and the tracking references. Then, the corresponding feedback law, F_r and G_r, will calculate the optimal duty cycle for pulse-width modulation (PWM) modulation. This simplified explicit process avoids the online MPC optimization and is suitable for the developed high-frequency inverter control design.

C. Local-Level Luenberger Observer

A state estimator is designed for per-phase power module to provide more accurate switch-side inductor current estimation and noise rejection, as is shown in Fig. 10. Since the VF-CSS controller needs an accurate inductor current sampling for peak/valley ripple current calculations, especially when the current ripple is huge ($\geq 200\%$), a state estimator is desired to predict the inductor current with capacitor voltage and grid current samplings. The main purposes of the state estimator are 1) avoid inaccuracy of inductor current sampling with high current ripple for VF-CSS; 2) improve the antinoise capability for better control performance; and 3) reduce the sensor cost.

The Luenberger observer is designed to estimate the switch-side inductor current, $\hat{i}_{Lfs}$, capacitor voltage, $\hat{v}_{Cf}$, and grid-side inductor current, $\hat{i}_{Lfg}$, with the samplings of capacitor voltage, v_{Cf}, and grid-side inductor current, i_{Lfg}. The state-space equations for the discrete-time state estimator can be expressed in standard matrix format of

$$\hat{X}_{k+1} = A_E\hat{X}_k + B_E u_k + L_E(Y_k - \hat{Y}_k) \tag{16a}$$

$$\hat{Y}_{k+1} = C_E\hat{X}_k + D_E u_k \tag{16b}$$

where the variables and matrices for Luenberger observer represent

$$A_E = \begin{bmatrix} 0 & -\frac{1}{L_{fs}} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ 0 & 0 & 0 \end{bmatrix}, B_E = \begin{bmatrix} \frac{1}{L_{fs}} \\ 0 \\ 0 \end{bmatrix} \tag{17a}$$

$$C_E = \begin{bmatrix} 0\,1\,0 \\ 0\,0\,1 \end{bmatrix}, D_E = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{17b}$$

$$\hat{X}_k = \begin{bmatrix} \hat{i}_{Lfs}(k) \\ \hat{v}_{Cf}(k) \\ \hat{i}_{Lfg}(k) \end{bmatrix}, \hat{Y}_k = \begin{bmatrix} \hat{v}_{Cf}(k) \\ \hat{i}_{Lfg}(k) \end{bmatrix}. \tag{17c}$$

L_E is a 3×2 observer gain matrix that can be tuned to achieve minimal estimation errors. The diagram of the state estimator is shown in Fig. 10. The state observer minimizes the estimation error, $e(k)$, with a dynamic equation of

$$e_{k+1} = (A_E - L_E C_E)e_k. \tag{18}$$

The estimation gain can be derived by

$$L_E^T = RM^{-1} \tag{19}$$

where R is composed of tuning factors and M is determined by solving the Sylvester equation

$$A_E^T M - M\Lambda = C_E^T R \tag{20}$$

in which Λ is a matrix with the desired eigenvalues.

D. Local-Level Variable Frequency Control

For the local level per-phase VF-CSS control, two control strategies are proposed, including VCF-CSS and VDF-CSS. Two frequency controllers are implemented to achieve critical soft-switching operation for high efficiency with different types of frequency. The VCF-CSS derives a continuous switching frequency based on the critical soft-switching boundary conditions and then directly implements the frequency value to the PWM with the help of state estimator to collect the switch-side inductor current value. On the other hand, VDF-CSS discretizes the calculated switching frequency with multiple times of the sampling frequency for PWM which does not need the state estimator to derive an accurate switch-side inductor current value. Fig. 11(a) and (b) shows the switch-side inductor current waveforms for VCF-CSS and VDF-CSS, respectively. The envelopes of VCF-CSS and VDF-CSS are smooth and discretized due to the varying types of switching frequency. Both methods

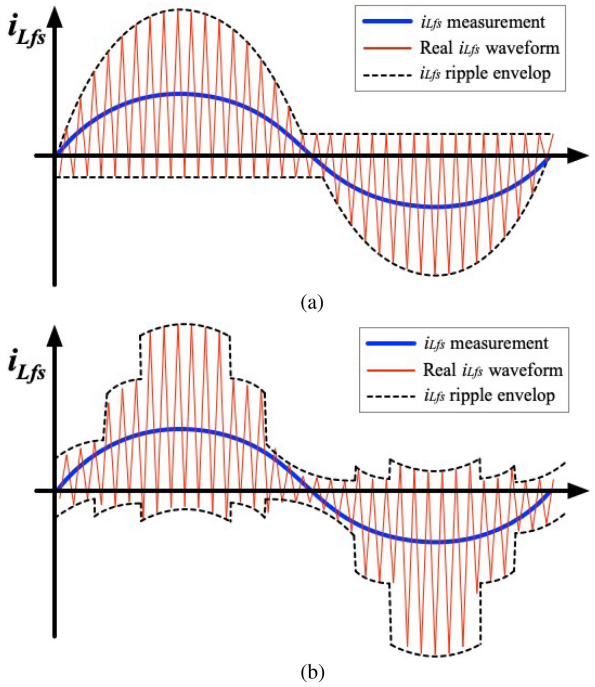

Fig. 11. (a) VDF-CSS and (b) VCF-CSS ac current ripple.

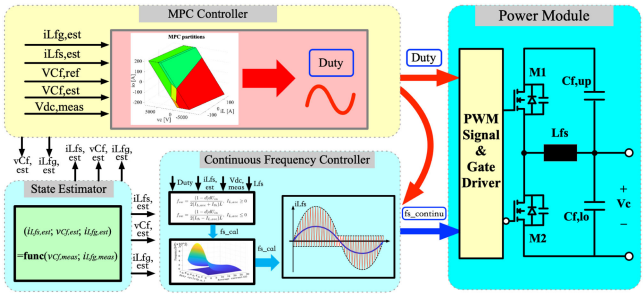

Fig. 12. Control diagram of power module with VCF-CSS, MPC, and estimator.

can achieve critical soft-switching operation for the improvement of efficiency. Since both the VCF-CSS and VDF-CSS are combined with MPC to deal with the time-varying switching frequency, the transient performance is improved by MPC with less oscillation and spikes even for the discretized frequency. And the corresponding di/dt stress on the switches is low.

1) VCF-CSS: VCF-CSS is designed to calculate the desired continuous switching frequency based on the peak/valley switch-side inductor current and the critical soft-switching boundary conditions in (4). The control diagram of the per-phase power module with VCF-CSS and MPC is shown in Fig. 12, which includes MPC controller, state estimator, and VCF-CSS controller. For the VCF-CSS controller, the continuously varying switching frequency, $f_{s,\text{cal}}$, is derived based on the threshold current, I_{th}, of critical soft-switching boundary conditions in (4). The switch-side inductor current ripple, Δi_{Lfs}, can be calculated as

$$\Delta i_{Lfs} = \frac{d(1-d)v_{\text{dc}}}{f_s L_{fs}}. \tag{21}$$

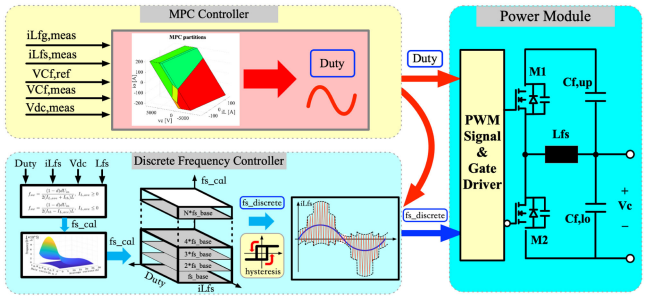

Fig. 13. Control diagram of power module with VDF-CSS and MPC.

And the critical soft-switching boundary conditions require the peak/valley inductor current values to be higher than I_{th} and lower than -I_{th}, respectively. Thus, the calculation of the continuously varying switching frequency, $f_{s,\text{cal}}$, can be expressed as

$$f_{s,\text{cal}} = \frac{(1-d)dv_{\text{dc}}}{2(i_{Lfs,\text{ave}} + I_{th})L_{fs}},\ i_{Lfs,\text{ave}} \geq 0 \tag{22a}$$

$$f_{s,\text{cal}} = \frac{(1-d)dv_{\text{dc}}}{2(I_{th} - i_{Lfs,\text{ave}})L_{fs}},\ i_{Lfs,\text{ave}} \leq 0 \tag{22b}$$

where $i_{Lfs,\text{ave}}$ is the average value of switch-side inductor current without considering the high current ripple for critical soft-switching calculation. The $i_{Lfs,\text{ave}}$ is also plotted as the blue sine waveform lines in Fig. 11.

As is shown in Fig. 12, the VCF-CSS receives the estimated values of $i_{\text{Lfs,est}}$, $v_{\text{Cf,est}}$, and $i_{\text{Lfg,est}}$ from the state estimator and optimal duty cycle value from MPC controller to calculate the desired switching frequency, $f_{s,\text{cal}}$, and applies to the PWM. The state estimator contributes to providing a more accurate switch-side inductor current value for frequency calculation compared with the direct sampling value since the sampling frequency and control frequency are both constant. The varying switching frequency could result in a deviation of sampling from the true averaged inductor current value, especially when the current ripple is large for critical soft switching. This deviation error can be solved by the state estimator.

2) VDF-CSS: Another frequency controller is designed as VDF-CSS to further discretize the calculated switching frequency in (22). The local per-phase power module control with VDF-CSS is shown in Fig. 13. The continuously varying switching frequency in (22) is further discretized into predefined frequency bandwidth sections, which is designed as integral multiple of the fundamental sampling frequency, $f_{s,\text{base}}$. Thus, the discretized varying switching frequency for PWM signals could be n times of $f_{s,\text{base}}$ ($n \in \mathbb{Z}$). To ensure the soft-switching operation, the multiple value of n is rounded down during the discretization by choosing a relatively lower switching frequency section. The implementation of the frequency controller is shown in the left bottom block of Fig. 13. The relationship of PWM switching carrier signals and sampling signals are shown in Fig. 14, with a varying switching frequency from $4f_{s,\text{base}}$ to $2f_{s,\text{base}}$ then to $f_{s,\text{base}}$. The process of frequency discretization

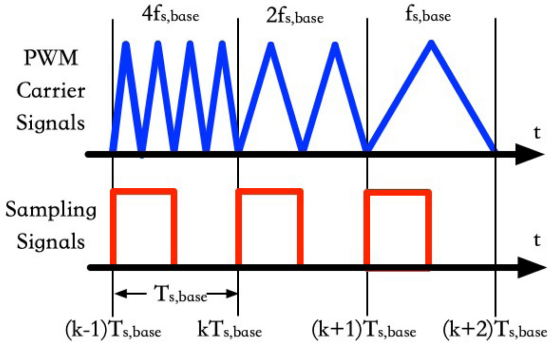

Fig. 14. Relationship of PWM carriers and fundamental sampling signals for VDF-CSS.

can be expressed as

$$f_{s,\text{discrete}} = n f_{s,\text{base}} = \text{floor}\left(\frac{f_{s,\text{cal}}}{f_{s,\text{base}}}\right) f_{s,\text{base}}. \tag{23}$$

The discretized frequency may be ringing back and forth by the oscillation of sampling noise during frequency-changing transients. A hysteresis loop is configured after the frequency discretization process to eliminate the frequency oscillation. Then, the discretized frequency will be implemented to the PWM for soft-switching operation.

Compared with the VCF-CSS, the VDF-CSS discretizes the switching frequency to be multiple times of the fundamental sampling frequency. Thus, the switch-side inductor current will be sampled exactly at the average points of the current ripple without deviation from the accurate values, as is shown in Fig. 14. Thus, even without the state estimator for the estimation of i_{Lfs}, the inductor current sampling can be accurate for the critical soft-switching calculation at high current ripple.

IV. Results

The proposed VF-CSS MPC methods with state estimator for zero-sequence stabilized nonisolated grid-connected inverter have been validated experimentally with carefully designed litz wire inductors and power converter board. The control strategies and modified topology are applied to both medium frequency of 40–240 kHz with 45-μH switch-side inductor and high frequency of 360 kHz–1.08 MHz with 4.5-μH switch-side inductor, respectively. The maximum efficiency at rated power of 15 kW is reaching 99%. The power densities of 8.14 and 10.4 kW/L are achieved for medium and high frequencies, respectively. The detailed performances of the proposed control methods on the modified nonisolated inverter are shown as follows.

A. Hardware Setup

The testbench is shown in Fig. 15, including the power converter board in Fig. 15(b) and switch-side medium inductor in Fig. 15(c) and small inductor in Fig. 15(d). The DSP control card, TMS320F28388D, is plugged on side of the power converter board. The Cree SiC MOSFET, C3M0032120 K, is chosen for the power switch in the middle area of the power board covered by the heat sink and cooling fan. For the switch-side LCL

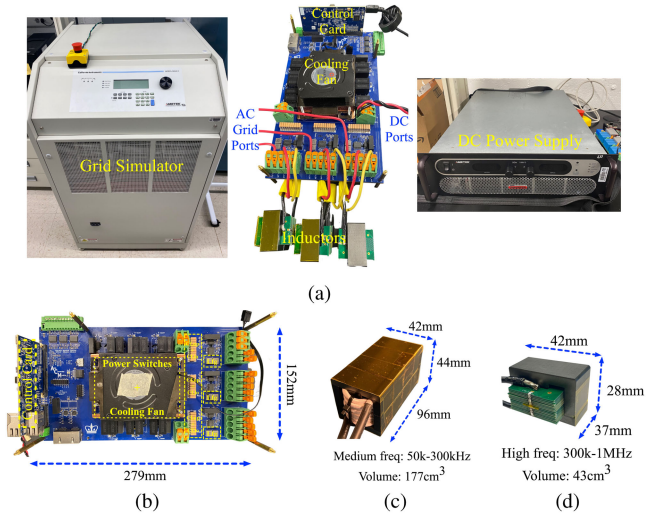

Fig. 15. Hardware prototypes of (a) integrated prototype, (b) power board, (c) medium-frequency inductor, and (d) high-frequency inductor.

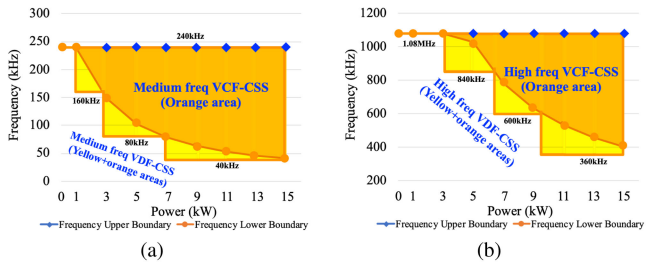

Fig. 16. Switching frequency of VCF-CSS and VDF-CSS for (a) medium-frequency and (b) high-frequency applications.

inductors, two types of inductors with 45 and 4.5 μH are designed at rated power for the medium frequency of 40–240 kHz and high frequency of 360 kHz–1.08 MHz operations, respectively. The switching frequency as functions of output power for high/medium frequencies VCF-CSS/VDF-CSS are also shown in Fig. 16. The dead time is configured as 80 ns for the safety consideration. Thus, the maximal modulation indexes for the medium- and high-frequency inductor applications are calculated as 0.98 for 240 kHz and 0.91 for 1.08 MHz, respectively.

For the medium inductor in Fig. 15(c), air-gaped E-E core is designed with E42/21/20-3F3 from Ferroxcube to be combined with litz wire winding (equivalent gauge 10). For the small inductor in Fig. 15(d), air-gaped E-I core is designed with E42/21/20-3F3 from Ferroxcube to be combined with litz printed circuit board (PCB) winding for the purpose of saving window space to reduce the inductor volume as has been designed in [26].

For the output capacitors, each phase has three 2.5-μF upper caps and three 2.5-μF lower caps in parallel, all from TDK FA10 to be integrated on the power board. The grid-side inductor is composed of two 1 μH in series for each each phase on the board.

For the parameters design of output capacitance and grid-side inductance, the principles are based on the minimum output capacitor voltage ripple, $v_{Cf,\text{ripple}}$ and the resonant frequency of the LCL filter, ω_{res}. Specifically, the minimum capacitance is

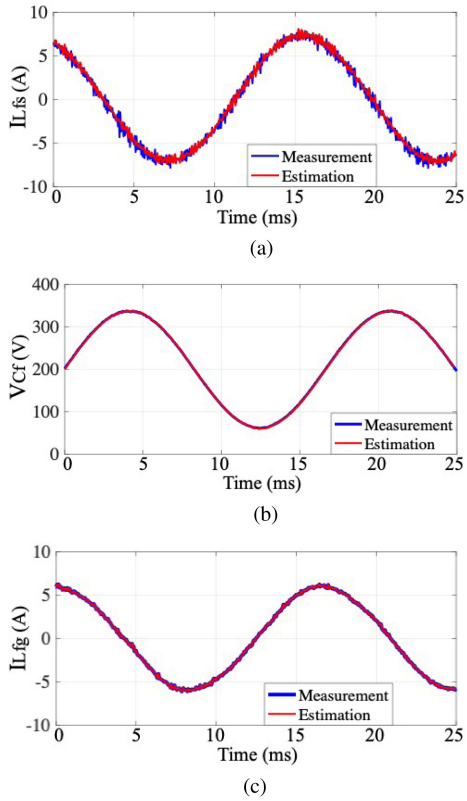

Fig. 17. Captured experimental readings of sampling measurement in blue lines and estimation in red lines of (a) switch-side inductor current, (b) capacitor voltage, and (c) grid-side inductor current.

determined by the output voltage ripple, which is expressed as

$$C_{f,\min} = \frac{1 - d_{\min}}{8 L_{fs} v_{Cf,\text{ripple}}[\%] f_{sw}^2}. \tag{24}$$

Then, from the minimum available $C_{f,\min}$, the value of grid inductance can be adjusted to determine the resonant frequency of LCL filter system, as is shown in

$$\omega_{\text{res}} = \sqrt{\frac{L_{fs} + L_{fg}}{L_{fs} L_{fg} C_f}}. \tag{25}$$

B. State Estimation Results

The state estimation method is validated in the modified nonisolated LCL grid-connected inverter to be combined with the VCF-CSS and MPC. One purpose of the estimator is to provide accurate switch-side inductor current readings, i_{Lfs}, for both the calculation of optimal soft-switching frequency and MPC implementation with fixed control frequency at high current ripple. Another purpose is to reduce the sampling noise from the sensors for a better steady-state performance.

The observer estimates the switch-side inductor current, $\hat{i}_{Lfs}$, capacitor voltage, $\hat{v}_{Cf}$, and grid-side inductor current, $\hat{i}_{Lfg}$, with the ADC measurements of capacitor voltage, v_{Cf}, and grid-side inductor current, i_{Lfg}. Fig. 17 shows the experimental readings from DSP of the estimated $\hat{i}_{Lfs}$, $\hat{v}_{Cf}$, $\hat{i}_{Lfg}$ in blue lines and the measured i_{Lfs}, v_{Cf}, i_{Lfg} in red lines. The observer accurately

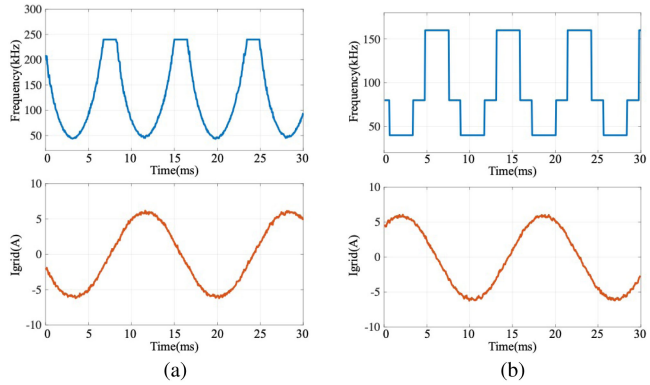

Fig. 18. Captured experimental readings of switching frequency in blue lines and grid-side inductor current in red lines of (a) VCF-CSS and (b) VDF-CSS at medium frequency of 40–240 kHz with 45-μH switch-side inductor.

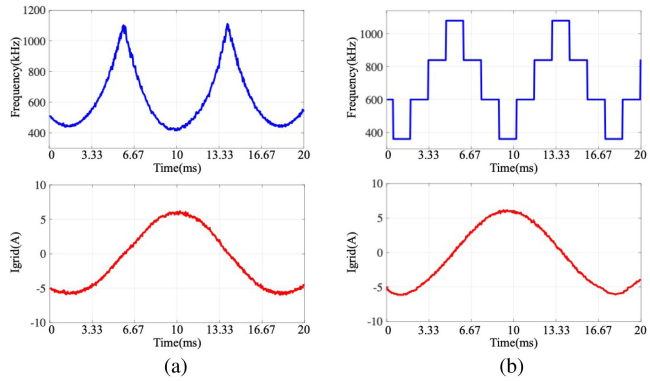

Fig. 19. Captured experimental readings of switching frequency in blue lines and grid-side inductor current in red lines of (a) VCF-CSS and (b) VDF-CSS at high frequency of 360 kHz–1.08 MHz with 4.5-μH switch-side inductor.

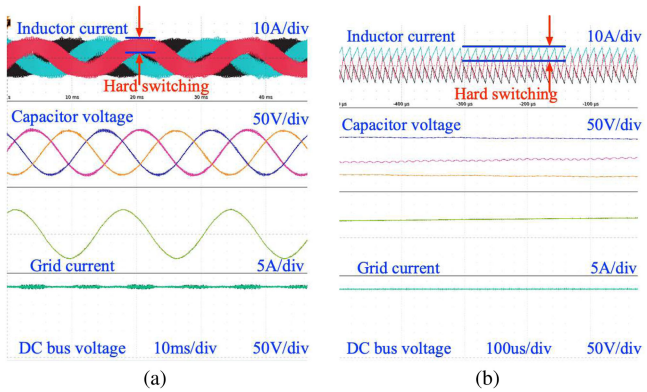

Fig. 20. (a) Inductor current, capacitor voltage, grid current, and dc bus voltage with constant switching frequency and (b) zoomed waveforms.

estimates the measurements of LCL system. And the sampling noises from the measurements are reduced with observer to provide cleaner and smoother current/voltage information for VCF-CSS and MPC.

C. Steady-State Results

The steady-state experimental results of VCF-CSS and VDF-CSS with MPC and estimator are shown in this section to

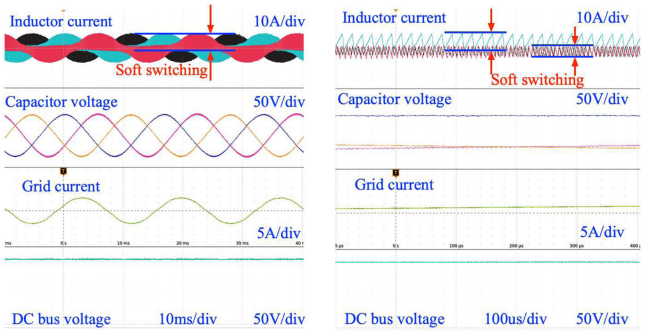

Fig. 21. Medium frequency of 40–240 kHz with 45-μH switch-side inductor. (a) VCF-CSS. (b) Zoomed steady-state waveforms of inductor current, capacitor voltage, grid current, and dc bus voltage.

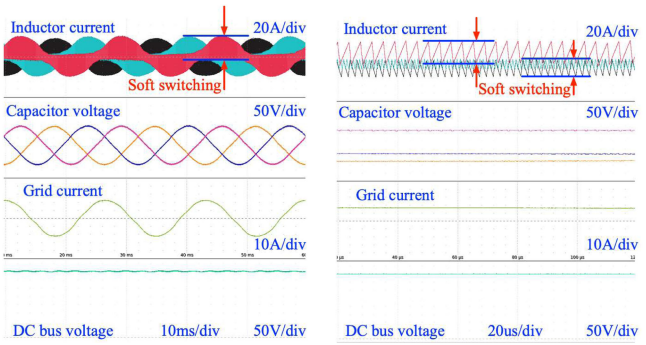

Fig. 22. High frequency of 360 kHz–1.08 MHz with 4.5-μH switch-side inductor. (a) VCF-CSS. (b) Zoomed steady-state waveforms of inductor current, capacitor voltage, grid current, and dc bus voltage.

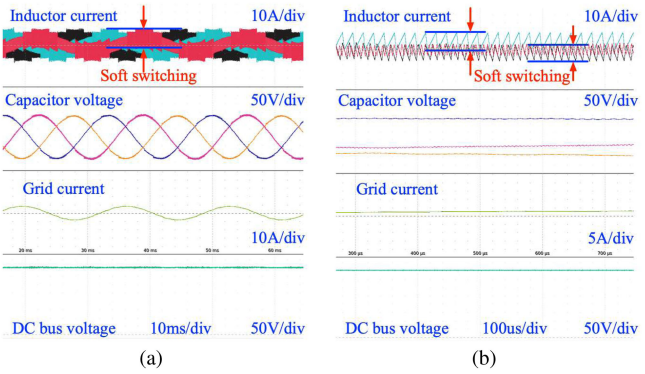

Fig. 23. Medium frequency of 40–160 kHz with 45-μH switch-side inductor. (a) VDF-CSS. (b) Zoomed steady-state waveforms of inductor current, capacitor voltage, grid current, and dc bus voltage.

demonstrate the critical soft-switching performance for both medium frequency (40–240 kHz, 45 μH) and high frequency (360 kHz–1.08 MHz, 4.5 μH) testing setups.

Fig. 18 shows the captured data of switching frequency and the corresponding ac current with medium frequency ranged at 40–240 kHz on the 45-μH inductor test bench. Specifically, Fig. 18(a) captures the VCF-CSS data of switching frequency and ac current based on the control method in Fig. 12 and (22).

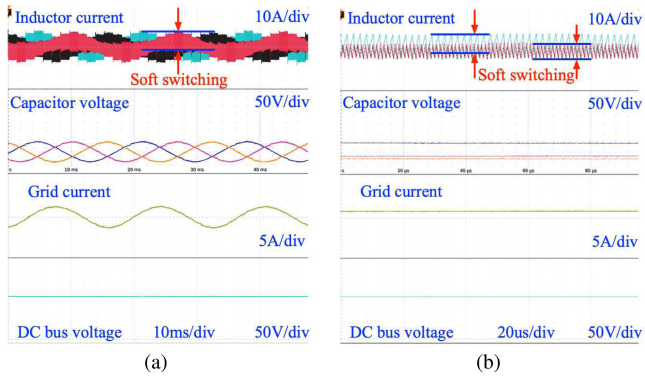

Fig. 24. High frequency of 360 kHz–1.08 MHz with 4.5-μH switch-side inductor. (a) VDF-CSS. (b) Zoomed steady-state waveforms of inductor current, capacitor voltage, grid current, and dc bus voltage.

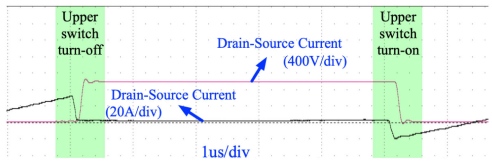

Fig. 25. Drain–source voltage and current across the upper switch for soft-switching operation.

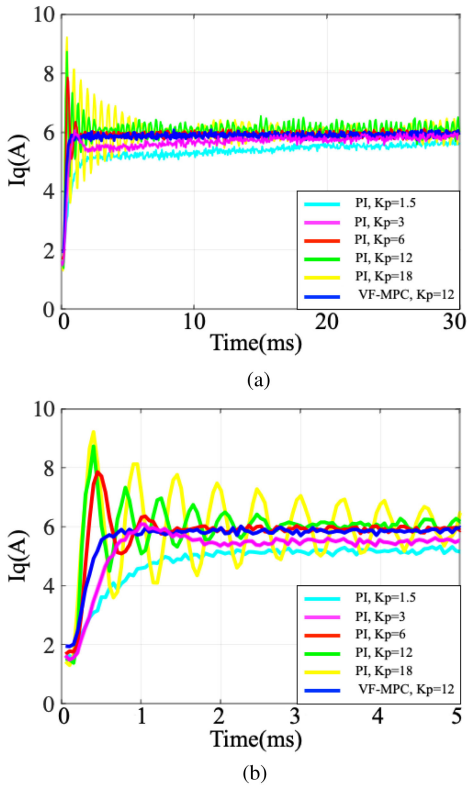

Fig. 26. Comparison of transient performance for MPC control with high gain of 12 and conventional PI control with the gains ranged from 1.5 to 18 by capturing ADC readings with current steps (a) from 2 to 6 A and (b) the corresponding zoomed waveforms.

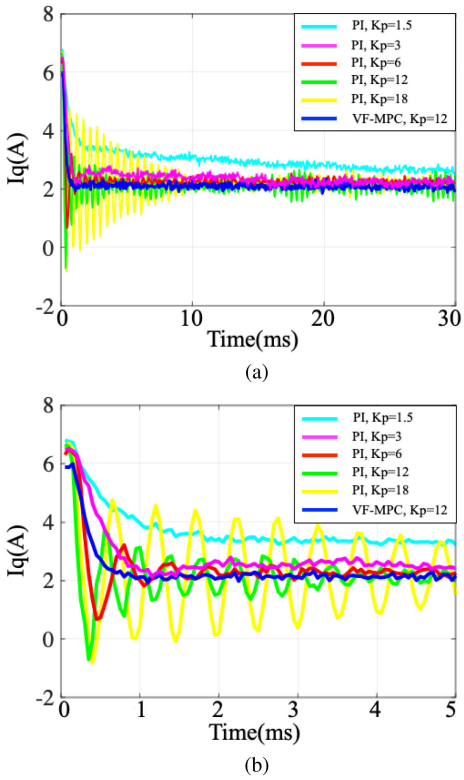

Fig. 27. Comparison of transient performance for MPC control with high gain of 12 and conventional PI control with the gains ranged from 1.5 to 18 by capturing ADC readings with current steps (a) from 6 to 2 A and (b) the corresponding zoomed waveforms.

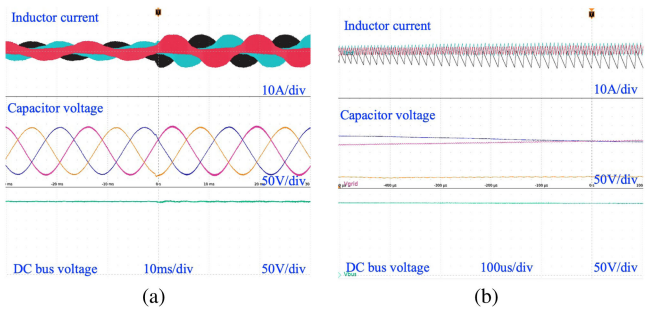

Fig. 28. (a) VCF-CSS. (b) Zoomed transient waveforms of inductor current, capacitor voltage, and dc bus voltage with a current step of 4 A.

Fig. 18(b) captures the VDF-CSS data of switching frequency and ac current based on the control method in Fig. 13. The variable discrete frequency is separated into three discretized levels, including 40, 80, and 160 kHz, which are all multiple times of the fixed sampling frequency of 40 kHz. Thus, the switch-side inductor current can be sampled more accurately at high current ripple even without estimation.

Fig. 19 shows the captured data of switching frequency and the corresponding AC current with high frequency ranged at 360 kHz–1.08 MHz on the 4.5-μH inductor test bench. Specifically, Fig. 19(a) captures the VCF-CSS data of switching frequency and ac current based on the control method in Fig. 12 and (22). Fig. 19(b) captures the VDF-CSS data of switching

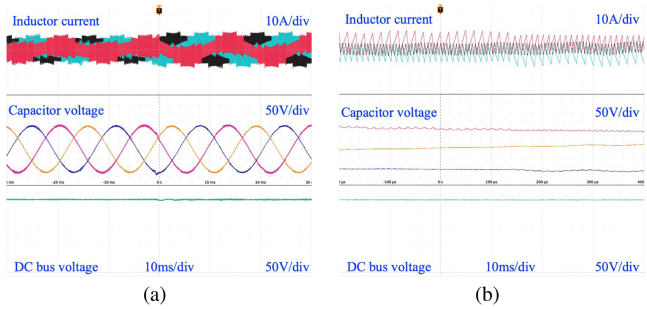

Fig. 29. (a) VDF-CSS. (b) Zoomed transient waveforms of inductor current, capacitor voltage, and dc bus voltage with a current step of 4 A.

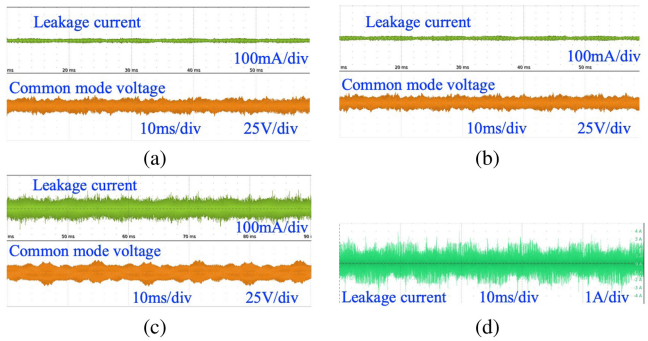

Fig. 30. Comparison of leakage current and common mode voltage (a) for the proposed VCF-CSS with zero-sequence voltage control, (b) for the proposed VDF-CSS with zero-sequence voltage control, (c) for the proposed VF-CSS without zero-sequence voltage control, and (d) for the traditional topology without zero-sequence voltage control.

frequency and ac current based on the control method in Fig. 13. The variable discrete frequency is separated into four discretized levels, including 360 kHz, 600 kHz, 840 kHz, and 1.08 MHz, which are all multiple times of the fixed sampling frequency of 120 kHz. Thus, the switch-side inductor current can be sampled more accurately at high current ripple even without estimation.

The experimental waveforms of switch-side inductor current, capacitor voltage, grid current, and dc voltage are compared between the hard switching and the proposed VCF-CSS and VDF-CSS in Figs. 20–24. Specifically, in Fig. 20, a fixed switching frequency of 80 kHz is implemented, which results in hard switching at the peak and valley points of the sinusoidal ac current waveforms. Figs. 21 and 22 show the VCF-CSS and zoomed waveforms at medium and high frequency, respectively. The critical soft-switching operations are maintained at the full ac current period. Figs. 23 and 24 show the VDF-CSS and zoomed waveforms at medium and high frequency, respectively. The critical soft-switching operations can also be maintained by the discretized frequency at the full ac current period. Since the main target of VF-CSS is to achieve soft-switching turn-ON of the upper switch, the detailed drain–source voltage and current waveforms across the upper switch for soft switching are shown in Fig. 25 to illustrate the ZVS operation.

D. Model Predictive Control Transient Results

The transient experimental results for the proposed MPC controller with state estimator are shown in this section to

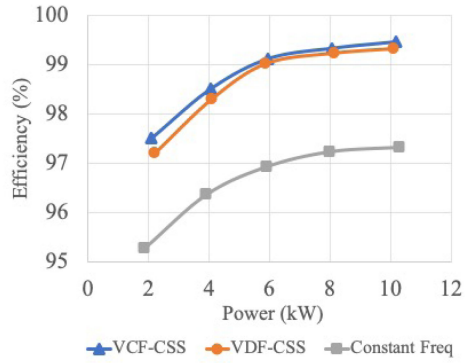

Fig. 31. Efficiency curves comparison of VCF-CSS, VDF-CSS, and constant frequency.

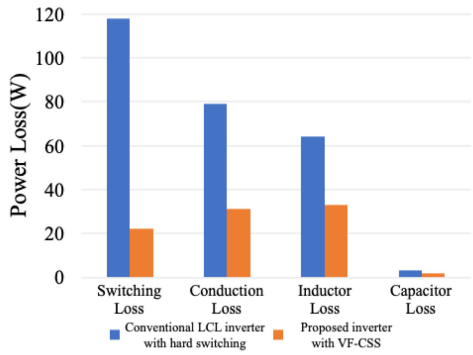

Fig. 32. Loss comparison between the conventional LCL inverter and the developed inverter with VF-CSS.

demonstrate the improved dynamic performance of the proposed MPC for the variable frequency operation and during current reference steps.

For the demonstration of the dynamic performance improvements, a conventional PI control method is taken as comparison with the proposed MPC method. Figs. 26 and 27 show the captured current ADC reading comparisons of VFCSS-MPC with a high K_p of 12 on the grid-side inductor current control and the conventional PI control with the K_p gain swept from 1.5 to 18 by implementing a current step from 2 to 6 A and 6 to 2 A, respectively. The rising time is within 1 ms for the proposed MPC at a high K_p gain of 12 and more than 20 ms for the conventional PI control at low K_p gain of 1.5. The overshoot of MPC is within 2%, which is negligible. Also, the results of conventional PI control at higher K_p gains of 3, 6, 12, and 18 are shown in Figs. 26 and 27, where the overshoot and oscillation are larger than the MPC method. The local cascaded inner loop MPC controller plays an active damping role and enables a high control bandwidth for outer loop to operate at a high gain without oscillation. Thus, the proposed MPC has faster tracking speed than conventional PI without overshoot or oscillation.

The transient experimental results and the zoomed waveforms for VCF-CSS-MPC and VDF-CSS-MPC are shown in Figs. 28 and 29, with a current step of 4 A, respectively. From the zoomed switch-side inductor current waveforms, the critical soft-switching operations are fully maintained during both the current step transients and switching frequency transition instants.

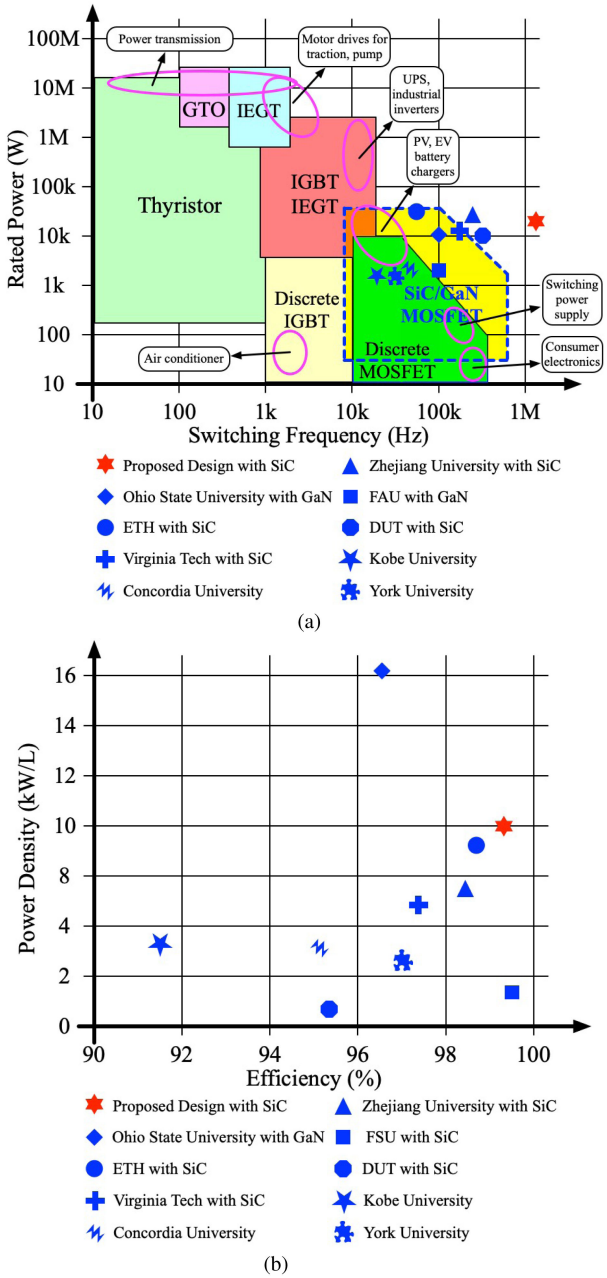

Fig. 33. (a) Power-frequency and (b) efficiency-power density diagrams of SiC- and GaN-based applications.

E. Zero-Sequence Stabilized Leakage Current Results

The zero-sequence voltage stabilization results for the leakage current attenuation of the modified nonisolated grid-tied inverter are shown in Fig. 30. The proposed MPC-based zero-sequence voltage control method maintains the common mode voltage constant at half of dc bus. The leakage current is restricted within 20 mA, which is compliant with the standard requirements, e.g., VDE 0126-1-1 for PV and IEC for EV. Specifically, the waveforms of leakage current and common mode voltage for

VCF-CSS-MPC and VDF-CSS-MPC are shown in Fig. 30(a) and (b), respectively. It is worth mentioning that the leakage current attenuation is resulted from the combination of MPC-based zero-sequence voltage control method and the modified topology in Fig. 2. For a more detailed comparison, the leakage current and common mode voltage of the modified topology without zero-sequence voltage control are shown in Fig. 30(c), which has two to three times higher leakage current due to the lack of zero-sequence voltage stabilized control. Finally, the conventional nonisolated topology leakage current is also shown in Fig. 30(d), which has 10–15 times higher leakage current than the proposed zero-sequence voltage-stabilized modified nonisolated inverter.

F. Efficiency and Power Density Results

The efficiencies of the proposed VCF-CSS and VDF-CSS control strategies have been tested up to the rated power, as is shown in Fig. 31. The efficiencies of above 99% are both achieved for the VCF-CSS and VDC-CSS, which are 2% higher than the hard switching operation. Also the loss breakdown comparison between the developed inverter with VF-CSS and the conventional LCL inverter with hard switching is shown in Fig. 32. With the proposed method, the switching loss is reduced by more than times. And with the high-frequency inductor and power board design in Fig. 15, a maximum power density of 10.4 kW/L is achieved. Several typical SiC/GaN converter designs are compared in Fig. 33 with the power-frequency and efficiency-power density plots [27]–[36]. The proposed design is labeled in red star and achieves the Pareto optimal points.

V. Conclusion

This article proposes VF-CSS MPC strategies to improve the efficiency and power density of a modified nonisolated grid-connected inverter. Also, a state estimator is developed to be combined with the variable frequency model predictive controller for the improvements of sampling accuracy and noise rejection. The leakage current is attenuated by the zero-sequence MPC and the modified nonisolated topology. Two types of variable frequency controllers are developed, including VCF-CSS and VDF-CSS, to achieve the CSS operation. A Luenberger observer is developed to be combined with the VCF-CSS for more accurate inductor current calculation of CSS and noise rejection. The proposed control methods and modified non-isolated topology have been validated on medium-frequency ($>$200 kHz, 45 μH) and high-frequency ($>$1 MHz, 4.5 μH) test benches, respectively. With the proposed CSS control strategies, the efficiency is above 99% at the rated power of 15 kW, and a power density of more than 10.4 kW/L is achieved.

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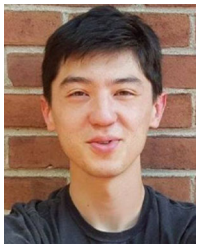

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