Modeling and Minimization of the Parasitic Capacitances of Single-Layer Toroidal Inductors

Florentin Salomez, Arnaud Videt, *Member, IEEE*, and Nadir Idir, *Member, IEEE*

***Abstract*—High-frequency power converters need electromagnetic interferences filters using common and differential mode chokes with low parasitic capacitance to comply with the electromagnetic compatibility standards. This article proposes a modeling method of this capacitance and ways to minimize it. The studied components are ring core inductors with magnetic materials considered as perfect conductors or with high permittivity, such as nanocrystalline material and most Mn-Zn ferrite materials. In comparison to other work in the literature, the proposed approach takes into account the curvature of the turn, in addition to the coating of the core and the insulation layer of the wire. The hypotheses, used in this article to simplify the real geometry, are compatible with two-dimensional (2-D) approaches to compute the parasitic interturns and turn–core capacitances. These capacitances are evaluated thanks to the 2-D finite element method. The obtained model allows accurate evaluation of the effect of turn–core space on the parasitic capacitance, and enables to reduce its value with a limited impact on the volume of the magnetic component.**

***Index Terms*—Common-mode chokes, electromagnetic compatibility (EMC), equivalent parallel capacitance (EPC), inductor, modeling, parasitic capacitance.**

I. Introduction

WIDE bandgap power transistors, made with silicon carbide (SiC) and gallium nitride (GaN), allow the development of high-frequency (up to megahertz ranges) static converters. However, these converters produce high-frequency noises, both conducted and radiated, which must be mitigated to respect the electromagnetic compatibility (EMC) standards [1], [2]. Among many other techniques [3], a passive filter is often used to change the propagation path of the conducted emissions, thus reducing the impact of the noise, produced by the converter, toward the grid [2], [4]. Since the bandwidth of the conducted EMC standards spans along several decades (hundreds of kilohertz–hundreds of megahertz), a good knowledge of the parasitics of the electromagnetic interference (EMI) filter is required to size it correctly [5]–[8]. In this article, the model of the equivalent parallel capacitance (EPC) of a ring core inductor is considered, along with means of reducing and tuning its value.

Manuscript received November 26, 2021; revised February 16, 2022 and April 25, 2022; accepted May 10, 2022. Date of publication May 24, 2022; date of current version June 24, 2022. This work was supported by the University of Lille, France. Recommended for publication by Associate Editor H. S. Krishnamoorthy. *(Corresponding author: Florentin Salomez.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3177642.

Digital Object Identifier 10.1109/TPEL.2022.3177642

In the literature, several models based on the finite element method (FEM) and on the modeling of the full geometry have been used to determine the value of the EPC for rode core [9], ring core [10], [11], and spiral inductors [12], [13]. But the difficulty with this numerical approach lays in the deduction of the relation between geometrical and material properties and the overall value of the EPC. To tackle this drawback and to decrease the computation cost of simulations for optimization purpose [4], several analytical models have been developed. Most works reviewed hereafter compute the EPC in the following two steps.

1) The evaluation of the elementary parasitic capacitive coupling between turns, between layer of turns, and between turns and core in the middle and at the periphery of the winding.
2) The resolution of the capacitance network.

For the first step, layers of winding can be assumed as equivalent cylinder capacitances, as described in [14]–[16]. These works were dedicated to multilayer winding transformers with straight core, but this approach was used in [17] to study the fractional winding scheme on ring core. Nevertheless, it is generally not accurate enough for loose winding made with round conductors. In the literature, this problem is solved with the image theory [18], equivalent segment or arc parasitic capacitances [19]–[22], a combination of the two previous methods [23], conformal transform [24], or two-dimensional (2-D) FEM [25], [26]. The latter approach will be used in this article, because it takes into account insulation layers, coating, interturn, and turn–core spaces.

Then, for the second step, the popular model developed by Massarini and Kazimierczuk [19] and the derived ones [22], [27] consider a pure capacitive network decoupled from the magnetic part of the component to compute the EPC. But as described in [25], the evolution of the EPC with the number of turns is not correctly reproduced. A more accurate hypothesis based on energy conservation and presented in several published works [14]–[16], [18], [25], [26], [28], [29], will be used here.

In addition to the modeling of the EPC, some articles propose ways to reduce it. Middelstädt *et al.* [23] identified the turn–core capacitance as the most important one in the total EPC and its dependence with the interturns space. Therefore, they suggest to keep the winding tight to avoid the increase of the parasitic capacitive coupling between turns and core, and thus to reduce the EPC (this has been confirmed in [18], [25], and [26]). According to them, for this same reason, the turn–core capacitance on the periphery of the winding cannot be neglected

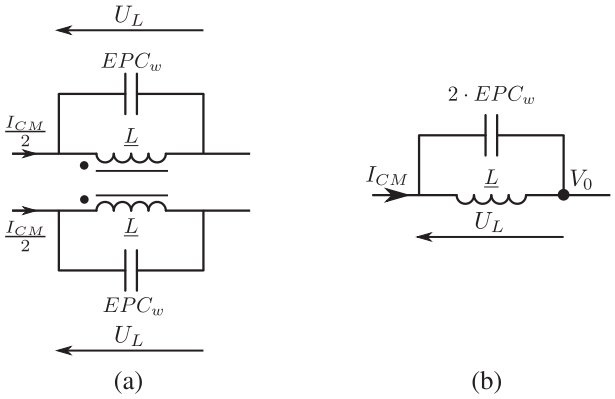

Fig. 1. Equivalent circuits of a common-mode inductor with EPC. (a) Two phases equivalent circuit. (b) Single-phase common-mode equivalent circuit.

in the total EPC. Another way to reduce the EPC is to increase the space between turns and core, or between layers, thanks to a plastic bobbin as proposed in [15] and [30], or by the wave-winding technique, as done by radio-frequency engineers in the 60s [31]. A last innovative solution was presented in [8], where the winding was shielded with aluminum foil to the ground to increase the coupling with it and reduce the coupling across the component. This solution is dedicated to common-mode chokes.

In this article, a modeling method of the parasitic capacitances to determine the EPC of inductors is proposed. In comparison to the previously reviewed works, the proposed method will focus on the assumptions required to approximate the curvature of both the turns and the coating thickness. In addition, it will take into account the turn–core and interturn spaces to evaluate the possibility to reduce the value of the EPC while keeping the impact on the volume low. The simplified 2-D geometry is then used as input of the 2-D FEM simulations of the parasitic capacitances. Furthermore, a novel method is proposed to evaluate the applicability of the model for a given magnetic material, notably for ferrite ones where core permittivity is a key parameter.

The rest of this article is organized as follows. Section II presents the models of the EPC and of the parasitic capacitances, with a focus on the compensation of the turn and coating curvatures in this article. Section III shows the experimental validations of the proposed model on conducting magnetic materials, such as nanocrystalline. Section IV explores applicability of the model to manganese-zinc (Mn-Zn) ferrite materials. Section V deals with the reduction of the EPC by tightening the winding and by the use of specific plastic spacers, and the extension of the model to take into account bigger turn–core spaces than conventional component without spacers is also presented. Finally, Section VI concludes this article.

II. Model of the EPC

First, in this section, the electrical couplings occurring in the winding and with the core are explained, and an EPC is determined as the one added to the circuit representation of a common-mode choke, as shown in Fig. 1(a), and called EPC_w,

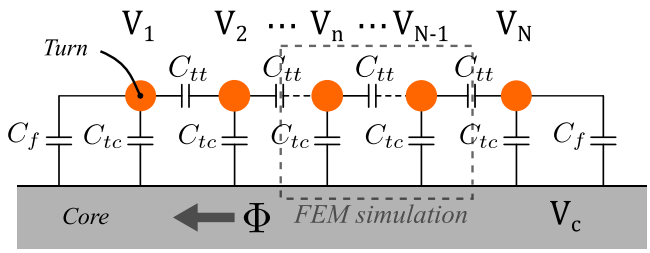

Fig. 2. Equivalent capacitive network of the winding.

where $\underline{L}$ is the inductance with its losses, I_{CM} is the common-mode current, and U_L is the voltage across the component. Second, the geometry of the component and the hypotheses used to transform it to a 2-D equivalent one are described in details. Last, the 2-D FEM simulation setups used to retrieve the values of the elementary parasitic capacitances are presented.

A. Capacitive Network of the Winding

Parasitic capacitance appears between two conductive surfaces at different potentials. For the inductor, those are the core and the wire. Each turn of the winding is considered as a monopotential closed loop; hence, a turn–core capacitance C_{tc} and a turn–turn capacitance C_{tt} are associated with each turn, as shown in Fig. 2. At the beginning and at the end of the winding, there is an additional coupling with the core due to the remaining space without winding, where electric field can further spread, modeled here by a fringe capacitance C_f.

The equivalent potential V_n of each n turn is defined as the mean potential across it, as presented in (1), where U_L is the total voltage across the component and V_0 is the reference potential. Each loop sees the same voltage drop because of the Lenz law, as discussed in [18], [25], [26], [32], and under the hypothesis that no propagation along the wire occurs at the considered frequencies. The core is floating, and according to the circuit theory, the symmetry of the capacitive network leads to a core potential V_c equal to the mean potential across the component, as defined in (2).

Knowing the voltage across each capacitance, one can find the total electrical energy stored in the winding. Then, by equalizing it to the energy held by an EPC across the component, as described in [14]–[16], [18], [25], [26], [28], [29], [32], one can deduce the expression of the winding capacitance EPC_w as a function of the total number of turns N and elementary capacitances $C_{\mathrm{tc}}, C_{\mathrm{tt}}$, and C_f, as described in (3). As shown in Fig. 1(b), for a two-winding components excited in common-mode, the overall EPC is simply two times the EPC_w.

$$1 \leq n \leq N, \quad V_n = \frac{2n-1}{2N} U_L + V_0 \tag{1}$$

$$V_c = \frac{U_L}{2} + V_0 \tag{2}$$

$$\mathrm{EPC}_w(N) = \frac{N-1}{N^2} C_{\mathrm{tt}} + \frac{1}{12} \frac{N^2-1}{N} C_{\mathrm{tc}} + \frac{1}{2} \left(\frac{N-1}{N} \right)^2 C_f. \tag{3}$$

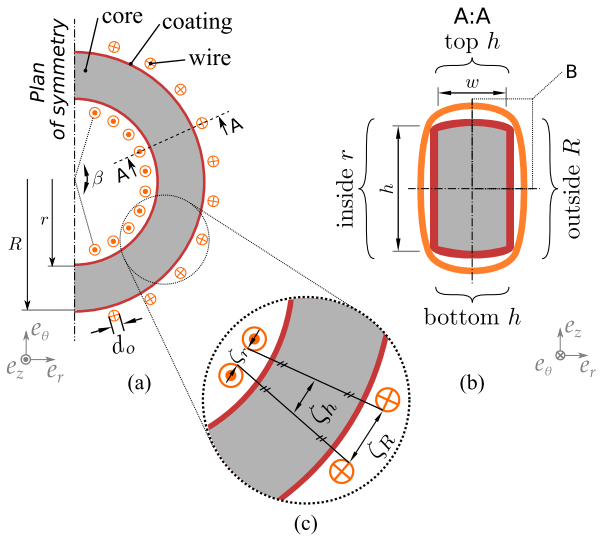

Fig. 3. Description of the geometry of the component. (a) Half-transversal cut of the component. (b) Section cut A:A with close-up B of a quarter of the section. (c) Close-up of a pair of turns.

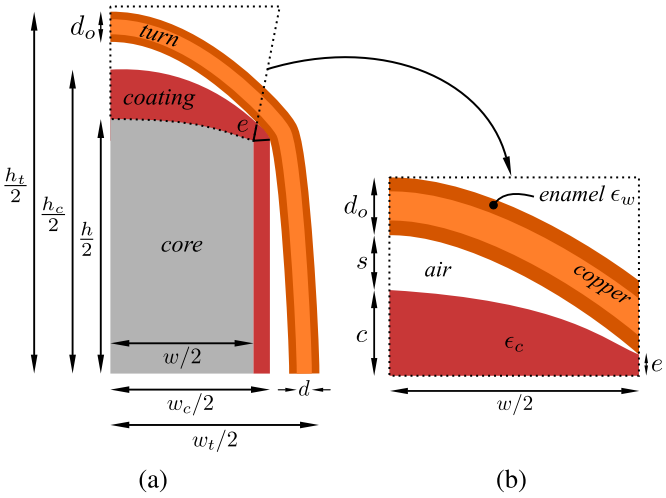

Fig. 4. Close-up on a quarter of section. (a) Quarter of section B from Fig. 3(b) with measured dimensions. (b) Details of the top face from the core surface with deduced dimensions.

In this article, the case of a coated ring core is studied. To retrieve the values of the elementary parasitic capacitances, the 2-D FEM simulations will be performed on a pair of turns, as shown in Fig. 2. But first, the turn and coating curvatures are compensated in the following section.

B. Preparation of the Geometry for 2-D FEM Simulations

1) Geometry of the Wound Component: Fig. 3 shows the geometry of the wound component with one winding. The half-transversal cut of the core, as shown in Fig. 3(a), presents the internal and external radii r and R, respectively, and the winding angle β covered by the N regularly spaced turns. The core section is defined by its width w and its height h, as shown in Fig. 3(b). The close-up B on one-quarter of the section is shown in Fig. 4. The distances between two adjacent turns are shown in Fig. 3 in the close-up (c), where ζ_r and ζ_R are the mean interturn distances on the internal and external surface of the core, respectively, and ζ_h is the mean interturn distance on the top and bottom surfaces. In order to compute the capacitances $C_{\text{tc}}, C_{\text{tt}}$, and C_f with a 2-D FEM approach, the presented geometry will be transformed. The retained hypotheses are described in details hereafter.

2) Focus on One Face of the Component: Fig. 4(a) shows a quarter of the section of the component along with the measured dimensions. The core dimensions h and w are given by the datasheet from the manufacturer. The coated dimensions h_c, and w_c are measured at the middle of each face using a caliper. And, the same is performed for the dimensions of the wound components h_t and w_t. The wire is assumed to touch the coated core on a small surface on the corner, at a distance e from the core corner due to coating, with relative permittivity ϵ_c. The impact of the corner is first neglected in this section. The area delimited by the edge of the iron surface and the position where the wire comes off the coated surface is considered for the following transformations, as shown in Fig. 4(b). The maximum turn–core space s and coating thickness c are deduced from the previous measurements. The interturn spaces, as shown in Fig. 3(c), are deduced from the measurements of the winding angle β, the geometry of the wound core R_t, r_t, the number of turns N, and the insulated wire diameter d_o as

$$\begin{cases} \zeta_R = \frac{\beta}{N-1}(R_t + d_o/2) - d_o \\ \zeta_r = \frac{\beta}{N-1}(r_t - d_o/2) - d_o \\ \zeta_h = \frac{1}{2}(\zeta_R + \zeta_r) \end{cases} . \tag{4}$$

3) Compensation of the Wire Insulation: The wire insulation is a thin layer of enamel ($30\,\mu$m, or 6%, of the wire copper diameter in our experiments) that requires a fine meshing in FEM simulation. A transformation of the conductor diameter is proposed to decrease the number of domains and elements and speed up the simulation time for optimization purpose. Fig. 5(a) shows a cross section of a pair of turns wound around the core, where d is the copper diameter of the wire, e_w is the insulation thickness, and ϵ_w is its relative permittivity. Given the small size of the wire diameter compared to the core radius, the curvature of the core is neglected. Considering the thinness of wire insulation layer, it can be assumed that electric field lines remain orthogonal to the enamel surfaces, such that the elementary capacitance of wire insulation $\mathrm{d}C_w$ (in series with the air one $\mathrm{d}C_a$) can be replaced by $\mathrm{d}C_{wc}$ made of air and of a smaller thickness in such way that $\mathrm{d}C_w = \mathrm{d}C_{wc}$, as demonstrated in Fig. 5(b). This leads to an equivalent wire without insulation, where copper diameter d is increased by two times the additional length δ_w. This gives corrected values of diameter d_c, interturn space ζ_c, turn–core space s_c, and turn–core distance at the edge s_e, as shown in Fig. 6 and given as

$$\begin{cases} \delta_w = e_w \times \left(1 - \frac{1}{\epsilon_w}\right) \\ d_c = d + 2\delta_w \\ \zeta_c = \zeta + 2\frac{e_w}{\epsilon_w} \\ s_c = s + \frac{e_w}{\epsilon_w} \\ s_e = \frac{e_w}{\epsilon_w} \end{cases} . \tag{5}$$

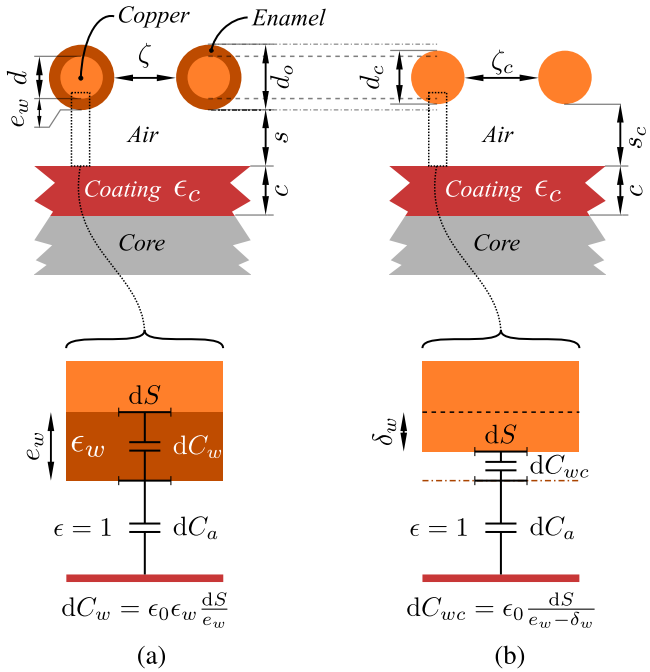

Fig. 5. Equivalent model of the wire insulation. (a) Before the compensation of the insulation layer is applied. (b) After the compensation of the insulation layer is applied.

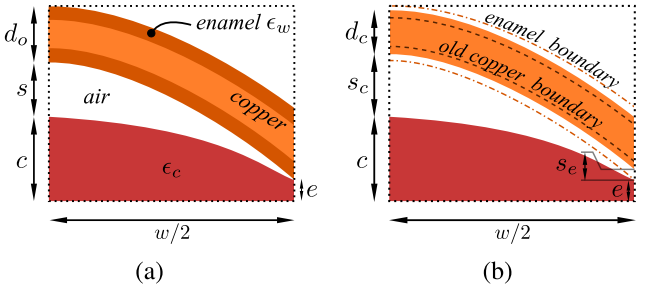

Fig. 6. Diagrams of the top surface of the component: (a) before and (b) after compensation of wire enamel.

4) Flattening of the Turn and Coating Curvatures: The thickness of the coating is not constant, and each turn follows a curve, as presented in Fig. 7(a). To simulate the parasitic capacitances in 2-D FEM, every distance of interest must be constant along the face considered, as shown in Fig. 7(b). Thus, the capacitive behavior of the curvated wire and coating over the considered width is modeled as series capacitances C_{air} and C_{coat} between flattened surfaces. Taking only the maximum distances s_c and c is a first-order approximation of the turn–core distance and coating thickness. But it will lead to an underestimation of the capacitances, as shown in the following section. A better approximation that conserves the value of the capacitances is proposed in the following paragraph, with a focus on C_{air}.

As a geometrical model of the curvature, the turn–coating distance is assumed to follow a parabola S, as defined in (6) and shown in Fig. 8(a). Assuming that $(s_c - s_e) \ll w/2$, a straight elementary capacitance per unit area $\mathrm{d}C$ is defined along a portion $\mathrm{d}x$ of the length $w/2$. One can express the average capacitance per unit area over the full width, as described in

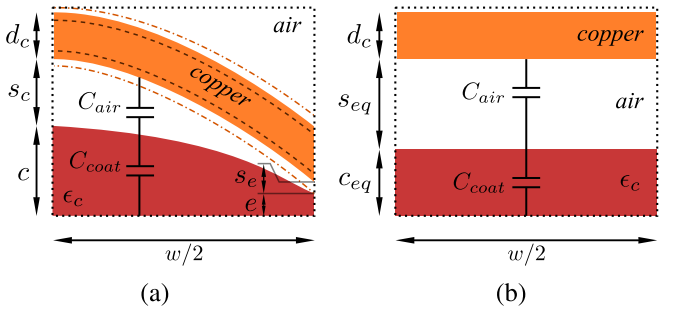

Fig. 7. Diagram of the top surface of the component. (a) Before flattening. (b) After flattening.

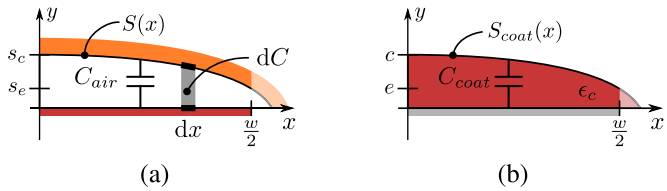

Fig. 8. Diagrams of the flattening of (a) wire curvature; and (b) coating curvature.

(7). By equalizing it to a constant capacitance per unit area defined between two straight surfaces, an equivalent turn–coating distance that gives the same overall capacitance value C_{air} is extracted. This distance, called s_{eq}, is retrieved from (7) and presented in (8). If the coating thickness is not constant on the considered face, as shown in Fig. 7(a) for the top face, the same approach is used by defining a second parabola S_{coat}, as shown in Fig. 8(b), and obtaining an equivalent thickness c_{eq} by applying (8).

$$S(x) = s_c - (s_c - s_e) \times \frac{x^2}{(w/2)^2} \tag{6}$$

$$\frac{2}{w}\int \mathrm{d}C = \frac{2}{w}\int_0^{w/2} \frac{\epsilon_0}{S(x)}\mathrm{d}x = \frac{\epsilon_0}{s_{\text{eq}}} \tag{7}$$

$$s_{eq} = \frac{2\sqrt{s_c \times (s_c - s_e)}}{\log\left(\frac{\sqrt{s_c}+\sqrt{s_c - s_e}}{\sqrt{s_c}-\sqrt{s_c - s_e}}\right)}. \tag{8}$$

Once all the previous transformations have been applied on each face, the geometry is ready for the 2-D FEM simulations of the parasitic capacitances C_{tc}, C_{tt}, and C_f along the considered face.

C. Simulations of the Elementary Parasitic Capacitances

The simulation setups of C_{tc}, C_{tt}, and C_f are shown in Fig. 9, they are all planar simulation of the same depth (depending on the simulated face, for example, h for the inside face), computed, thanks to *FEMM 4.2* [33]. The margin with the bounding boxes h_{box} and w_{box} are defined as ten times the characteristic distance of the setup (the maximum between the interturn and turn–core distances) to avoid strong coupling with the boundaries. Periodic boundary is used for Fig. 9(a) to avoid coupling with the boundary as shown by the mirror setup. Antiperiodic boundaries

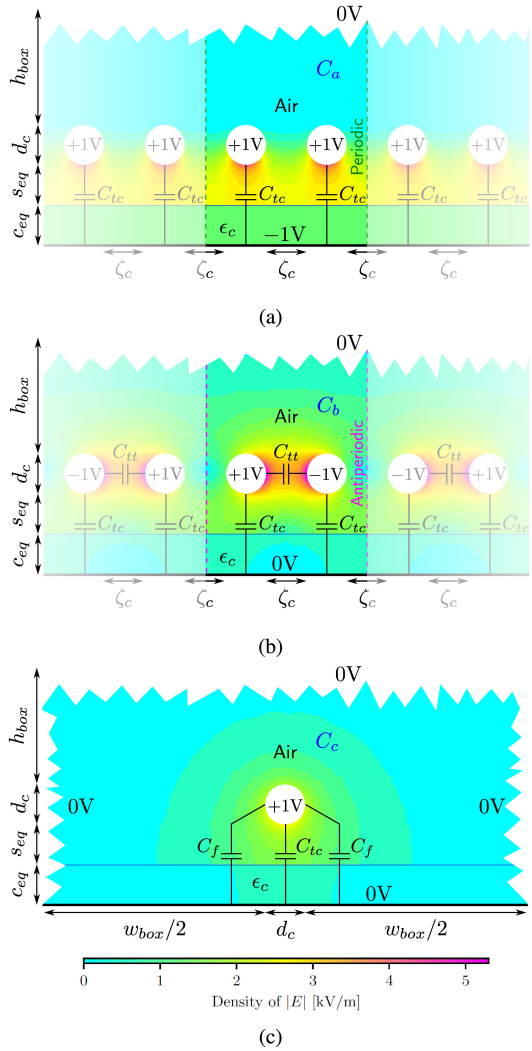

Fig. 9. Electric field map and its equivalent capacitances network for a pair of turn. (a) C_a for C_{tc} extraction. (b) C_b for C_{tt} extraction. (c) C_c for C_f extraction, the torn edges indicate that the simulation domain extends far beyond them.

are used in Fig. 9(b) for the same reason. In Fig. 9(a)–(c), the respective total capacitances C_a, C_b, and C_c are retrieved from the total energy. Then, the elementary capacitances of interest $C_{\text{tc}}, C_{\text{tt}}$, and C_f are computed, thanks to (9). This process is applied to each face of the core along the cross section shown in Fig. 3(b), involving a first set of elementary capacitances identified by the R subscript ($C_{\text{tc}R}, C_{\text{tt}R}, C_{fR}$) for the outside face, a second set C_{kr} for the inside face, and C_{kh} for both the top and bottom faces. Finally, totalized elementary capacitances are obtained by summing the results from each face as

$$\begin{cases} C_{\text{tc}} = \frac{C_a}{2} \\ C_{\text{tt}} = C_b - \frac{C_{tc}}{2} \\ C_f = \frac{C_c - C_{\text{tc}}}{2} \end{cases} \tag{9}$$

$$\forall k \in \{tc, tt, f\}, C_k = C_{kR} + C_{kr} + 2 \times C_{kh}. \tag{10}$$

In comparison to analytical formulations in the literature [18]–[22], the enamel insulation layer is taken into account, in addition to the coating of the core. Furthermore, the 2-D FEM setups are easier to implement and faster to compute than a full 3-D model of the component. The relevance of this method is further discussed in the following based on comparisons with non-FEM approaches.

TABLE I
INTERTURNS AND TURN–CORE SPACES FOR DIFFERENT WINDING CASES

	Cases			
	Tight	Loose ζ	Loose s_{eq}	Loose
ζ [mm]	0.1	1.0	0.1	1.0
s [mm]	0.1	0.1	1.0	1.0
Drawing				

D. Comparison of Methods for Determining Elementary Capacitances

The FEM simulations presented in the previous section for determining the elementary capacitances C_{tc} and C_{tt} are compared with analytical methods from the literatures [18] and [22]. The method described in [22] takes into account coating layer of the core and insulation layer of the wire, in addition to interturn and turn–core spaces. So this work is directly comparable to the proposed approach. On the contrary, the method described in [18] used the image theory method, but with the assumption of no insulation layers on the conductor and on the core, and the authors made no recommendations about how to take them into account. In order to make a fair comparison, three hypotheses will be used hereafter. The simplest ones are to replace any insulation layer with either air or conductor as described in (11) and (13), respectively. The more realistic one, called *intermediate*, is to replace only a part of insulation layer by conductor and the other part by air by using parallel plate capacitor approximation, as shown in Fig. 5 and specified in (12). The methods are tested on four winding cases derived from the geometry shown in Fig. 9 and described in Table I, while the remaining parameters are kept constant $d = 0.5, d_w = 0.56, \epsilon_w = 4, c_{\text{eq}} = 0.2\text{mm}$, and $\epsilon_c = 3$.

$$\begin{cases} d_{c,\text{air}} &= d \\ s_{\text{eq,air}} &= s_{\text{eq}} + e_w + c \\ \zeta_{c,\text{air}} &= \zeta + 2 \times e_w \end{cases} \tag{11}$$

$$\begin{cases} d_{c,\text{inter}} &= d_c \\ s_{\text{eq,inter}} &= s_{\text{eq}} + \frac{e_w}{\epsilon_w} + \frac{c}{\epsilon_c} \\ \zeta_{c,\text{inter}} &= \zeta_c \end{cases} \tag{12}$$

$$\begin{cases} d_{c,\text{cond}} &= d_w \\ s_{\text{eq,cond}} &= s_{\text{eq}} \\ \zeta_{c,\text{cond}} &= \zeta \end{cases}. \tag{13}$$

In this section, the methods are compared assuming that the 2-D hypotheses to take into account curvatures of wire are the same and have been applied to all the methods. The relevance of these hypotheses will be discussed in the following section. Only the turn–core capacitance is studied, because EPC is more sensitive to it according to (3).

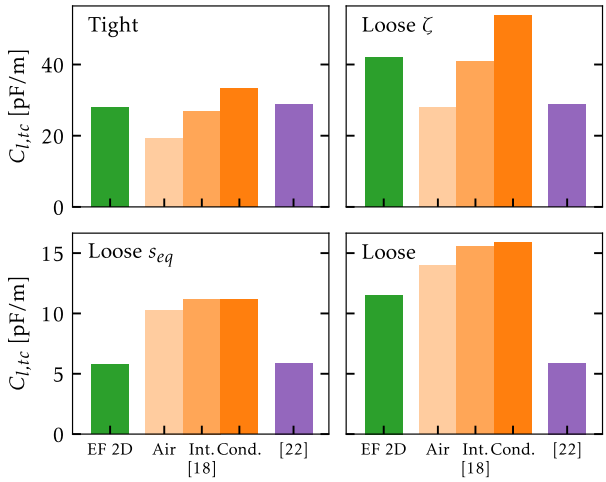

Fig. 10. Comparison of the analytical methods for determining $C_{l,\mathrm{tc}}$ capacitances for each case to the proposed 2-D FEM approach.

The breakdown of the results for the linear turn–core capacitance $C_{l,\mathrm{tc}}$ for each case and for each method from the literature are shown in the Fig. 10. From [22], there are some cases that results in the same value, for example, $C_{l,\mathrm{tc}}$ both *Tight* and *Loose* ζ are identical. However, this is expected since the method that computes $C_{l,\mathrm{tc}}$ is independent from ζ. According to these results, the work in [22] performed with a relative error of less than $\pm 3\%$ for cases with small ζ compared to d. When adjacent turns are far away from each other in comparison to d, the method gives only an order of magnitude and underestimates the value by at least 30%.

From [18] and both cases *Tight* and *Loose* ζ, the hypothesis regarding the insulation layers that leads to the best results is the *intermediate* one, with a relative error of less than $\pm 10\%$. For the last *Loose* cases with ζ big compared to d, the method always overestimates $C_{l,\mathrm{tc}}$.

This study shows that both analytical methods for determining the elementary capacitances [18], [22] are good compared to the proposed FEM method (relative errors less than $\pm 5\%$) for the *Tight* winding only and by considering specific hypotheses for the insulation layers with [18]. Yet, this article aims at a general method also suitable for *Loose* winding in the aim of EPC reduction in Section V. Thus, the proposed FEM method is applied hereafter for determining C_{tc} and C_{tt}. The accuracy of the method will be discussed with measurements of EPC in the following sections, based on two ring cores from different suppliers and different kind of materials.

III. Application to Conductive Magnetic Material

To validate the obtained model, a coated ring core called device under test 1 (DUT1) is chosen (*Vacuumschmelze: T60004-L2030 W911*). This core is made of the nanocrystalline material, which is a good conductor and fulfills the perfect conductor hypothesis. It is wound by hand with one winding made of copper wire of diameter 0.5 mm with an enameled insulation layer of thickness 30 μm and relative permittivity of 4 (at 1MHz, 60 °C according to [34]).

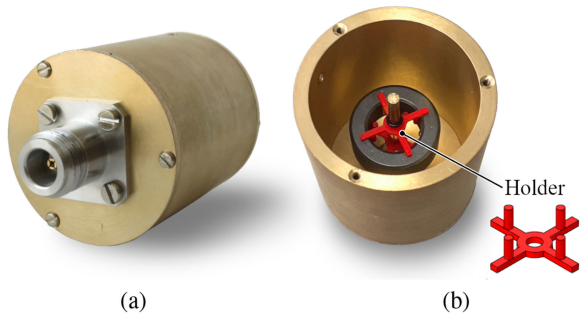

Fig. 11. Photographs of the one-turn equivalent brass device for the characterization of magnetic ring cores. (a) Outside with a loaded core. (b) Inside with a loaded core. The red crosses are 3-D printed plastic holders for the core.

A. EPC Measurements

To extract the EPC of a wound DUT, two measurements of complex impedance versus frequency f are performed.

The first one is done with a single-turn winding, called Z_{N1}, to characterize the core without parasitic and to obtain the ideal impedance of the choke without the EPC, called Z_{ideal}, as described in (14). To perform such measurements, a one-turn equivalent device has been designed and made of brass, as shown in Fig. 11. The core is maintained centered on the axis by a 3-D printed device in thermoplastic *Polylactic Acid* (PLA) called holder, as shown in Fig. 11(b). The self-impedance of the device without a core is subtracted from the measured impedance with the DUT inside it to retrieve the characteristic impedance of the core Z_{N1}. Parasitic capacitances of the core with the device are negligible for the cores studied here. The remaining parasitic capacitance of the device at no load has been cancelled out by the OPEN compensation of the impedance.

The second one is performed with the winding Z_{meas} to deduce the value of EPC. Indeed, the EPC is extracted by fitting the model impedance Z_{mod} that results from the paralleling of Z_{ideal} and EPC presented in (15) to the measured one Z_{meas}, with EPC as the design variable. In this way, the possible dispersion of the relative permeability among the samples and its decrease with high frequency do not impact the extracted EPC value of one specific core. The impedance measurements are carried out with an impedance analyzer *HP4294 A* equipped with the socket *16047E*. A space of 2 cm between the DUT and the socket is ensured to avoid direct coupling of the winding with the socket. According to the datasheets of the *HP4294 A* and the *16047E*, the relative error on the impedance module δ_Z in the frequency range of the fitting (10 kHz–20 MHz) is less than $\pm 3\%$. This leads to a similar maximum relative error $\delta_{\mathrm{EPC}} = -\delta_Z/(1+\delta_Z)$ on the extracted EPC of approximately $\pm 3\%$.

$$Z_{\mathrm{ideal}}(f) = N^2 Z_{N1}(f) \tag{14}$$

$$Z_{\mathrm{mod}}(f) = \frac{N^2 Z_{N1}(f)}{1 + j \times 2\pi f \times EPC \times N^2 Z_{N1}(f)}. \tag{15}$$

B. Validation on Impedance Measurements

To apply the model to the DUT1, its geometry is measured before and after winding with a caliper. The coating thickness

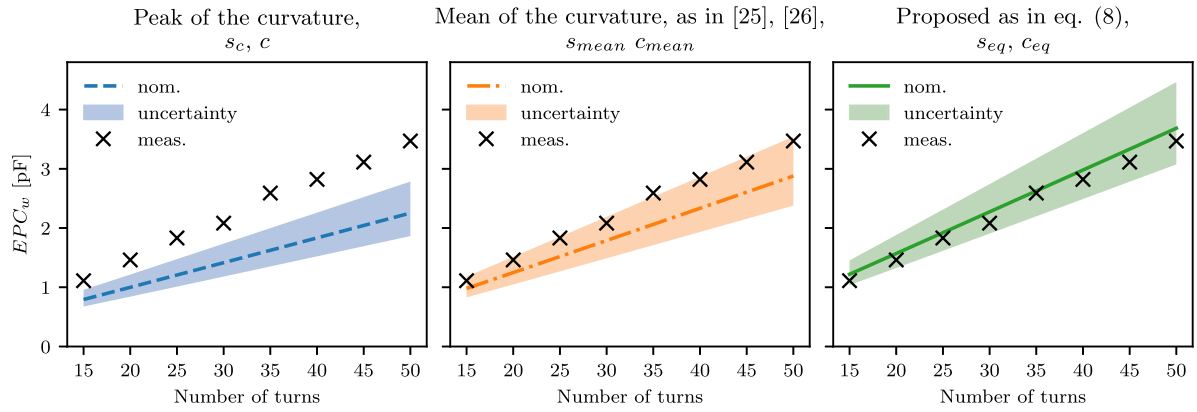

Fig. 12. Evolution of the EPC against the number of turns for the nanocrystalline core DUT1 with one winding, and comparison of the three hypotheses for the computation of the turn–core spaces s_{eq} and coating thickness c_{eq} regarding their curvature with worst cases min–max.

is deduced from the subtraction of the datasheet dimensions from the coated core measurements. Since the winding has some irregularities, each distance is measured at several angles on the component. In addition to the nominal case, two worst cases are computed to provide an interval of the modeled value due to uncertainties. The minimal case is defined by the maximum turn–core compensated distances s_c, maximum coating thicknesses c, and minimal coating relative permittivity. The opposite is performed to obtain the maximum case. Since the model considers only regular winding distribution, the worst cases give an overestimation of the interval around the nominal value. The resulted EPC is compared to the measured one in Fig. 12 for several hypotheses regarding the 2-D approximation of the turn and thickness curvature, as the maximum distances s_c and c, the mean distance under the core and thickness on the top and bottom of the core as proposed in [25] and [26], and the inverse of the mean inverse distances s_{eq} and c_{eq} according to (7) and (8). For the three hypotheses, the evolution of EPC with number of turns has the correct trend. This justifies the use in the three cases of the energetic approach to solve the capacitative network. The value of the EPC when using s_c underestimates the measured value by more than 30% for the nominal case, and the maximum value is below the measurement by 20%. It means that this hypothesis is not correct for the modeling of the EPC. The use of s_{mean} and c_{mean} gives better results. Indeed the relative error compared to the measurements is below 20%, and some measurements points are encompassed in the uncertainty area, though they remain near the upper bound of the interval. The last one that uses (8) as s_{eq} performs better than the previous one, its relative error for the nominal case is only 6% in average. This means that the model is able to give both the correct value and its evolution over the number of turns. Introducing the uncertainties, the model value is comprised in an interval of -15%–$+30\%$. As a consequence, even with some imperfections and uncertainties, the correct order of magnitude of the EPC is given by the proposed model. These measurements validate the 2-D hypotheses described earlier and the energetic approach used to solve the capacitive network. The comparison of the impedances in Fig. 13 shows that the proposed EPC model allows to extend the frequency range of the modeled impedance up to 20 MHz in this specific case.

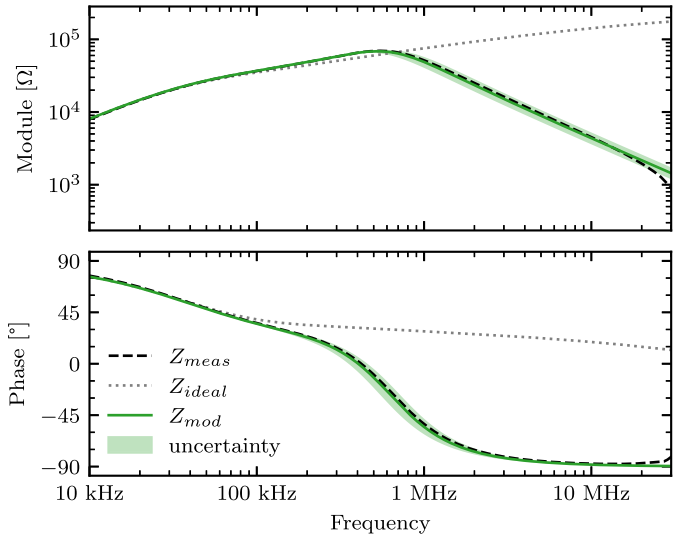

Fig. 13. Comparison of the measured and modeled impedance of the DUT1 with 50 turns.

IV. Application to High Permittivity Mn-Zn Material

The validity of the model regarding the hypothesis on the electric behavior of the magnetic material is studied for Mn-Zn ferrite materials commonly used in the EMI filter design.

A. Characterization of the Dielectric Behavior of the Magnetic Material

The model is applicable on any material that can be considered as a perfect conductor and on any material with a high permittivity, because it would cause a negligible voltage drop along the core. To verify this assumption, a simple and nondestructive test is performed on two cores of similar geometry and of different material: 1) Mn-Zn N30; and 2) nickel-zinc (Ni-Zn) 4F1. The proposed capacitive measurement will give an estimation of the dielectric properties of the core and its coating, and will help to decide whether the model is applicable or not on this material. In Fig. 14(a), copper tape of width γ (here, 5 mm) is used to build surface electrodes on the coated core, separated by an angle η

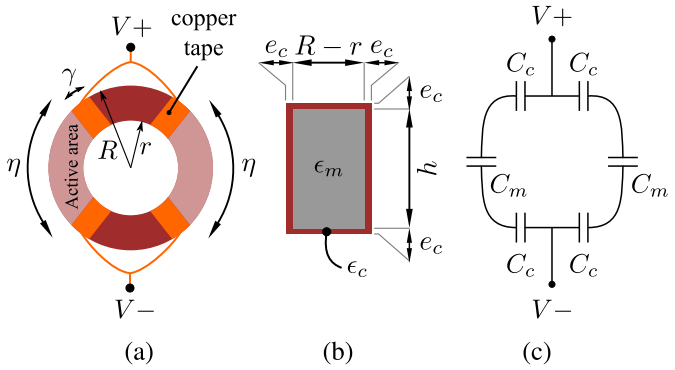

Fig. 14. Nondestructive test of the core relative permittivity ϵ_m. (a) Drawing of the core equipped with copper tape electrodes. (b) Section of the coated core. (c) Equivalent capacitive network.

and symmetrically duplicated in two branches, such that only the portions of the core comprised within the η angles undergo electrostatic excitation, called *active area*. Thus, the electric flux goes from one pair of electrode ($V+$) through a first layer of coating, then the core, and finally a second layer of coating to the other pair of electrodes ($V-$). An equivalent capacitive network of the measurement is shown in Fig. 14(c) with C_c the capacitance through the coating under one electrode and C_m the capacitance through the magnetic material. According to the diagram of the section of the core shown in Fig. 14(b), the coating capacitance can be estimated, as described in (16), where e_c is the mean thickness of coating. The material capacitance is assimilated to a plane capacitance in the active area as in (17). The resulting overall capacitance C_{eq} is expressed in (18).

$$C_c = \frac{\epsilon_0 \epsilon_c 2(R - r + h)\gamma}{e_c} \tag{16}$$

$$C_m = \frac{\epsilon_0 \epsilon_m (R - r)h}{\eta \times \frac{R+r}{2}} \tag{17}$$

$$C_{\text{eq}} = \frac{2C_m C_c}{C_c + 2C_m}. \tag{18}$$

Since C_m and C_c capacitances are in series, if the core permittivity ϵ_m is high so that $C_m \gg C_c$, then the voltage drop in the core remains negligible and $C_{\text{eq}} \approx C_c$ whatever is the interelectrode angle η. On the other hand, if low ϵ_m brings C_m to a comparable or lower value than C_c, then increasing η should reduce C_{eq} in (18), as a result of lower C_m in (17). Thus, Fig. 15 shows C_{eq} capacitance measurements for different angles on the two core materials: 1) DUT2 (Mn-Zn N30 of reference B64290L0632X830); and 2) DUT3 (Ni-Zn 4F1 of reference TX20/10/7). In addition, C_c is estimated at 15.3 pF from (16) (using $\epsilon_c = 3$ and $e_c = 125\ \mu$m from the measurements), so that the trend of C_{eq} is also plotted for different ϵ_m values. According to the localization of the measurement points in Fig. 15, it can be concluded that on the one hand, the Mn-Zn material *N30* has a high relative permittivity and the proposed model of the EPC can be readily applied, while on the other hand, the Ni-Zn material *4F1* has a low permittivity and the model is not applicable. Thus,

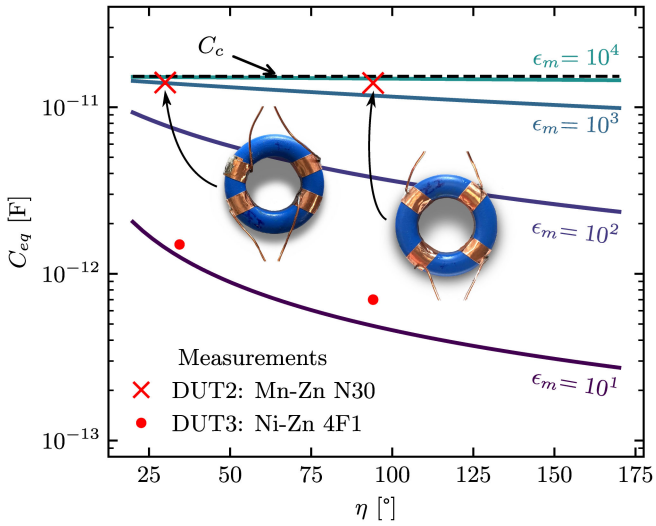

Fig. 15. Evolution of the equivalent capacitance as a function of core relative permittivity ϵ_m and angle η between electrodes.

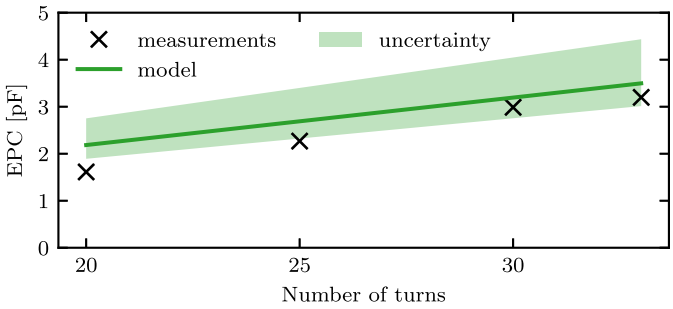

Fig. 16. Evolution of the EPC against the number of turns for one winding for the Mn-Zn core DUT4.

the test setup proposed in this section allows simple evaluation of the model applicability to a given ferrite core.

B. Experimental Validation With Impedance Measurements

DUT4 is a Mn-Zn *N30* core of reference *B64290L0618X830* and of similar size to DUT1. Direct application of the proposed model to this high-permittivity ferrite material is confirmed by the comparison of the extracted and measured EPC on the wound DUT4, as shown in Fig. 16. The evolution and the order of magnitude of the EPC is correctly reproduced, and the average relative error to the measurement is 20%. It should be noted that the geometry of the core DUT4 is slightly different than DUT1. The top and bottom sides are more bumpy. This could account for the bigger relative error than for DUT1.

V. Reduction of the EPC

The validated model to extract the EPC is used here to propose actions to reduce its value. According to (3), the main contributor is C_{tc}. To minimize its value, two methods can be used: 1) one based on the interturn spacing; and 2) the other on the turn–core spacing. For this section, the same core reference as DUT1 is

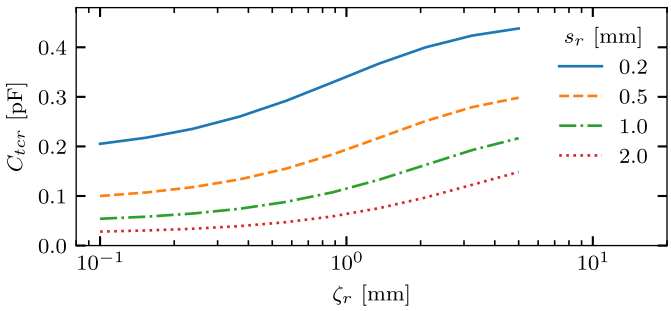

Fig. 17. Evolution of $C_{\mathrm{tc}r}$ as a function of s_r and ζ_r.

used, but with two windings to validate the model for common-mode inductors at the same time.

A. Small Interturn Spacing

According to 2-D FEM simulations (setups shown in Fig. 9) performed on the inside face of the component for different values of s_r and ζ_r and shown in Fig. 17, the interturn space ζ should be kept as small as possible to minimize C_{tc}. Indeed the electrical field lines can reach more surface of the core when two adjacent turns are far apart each other. Since keeping the winding tight is already performed on regular components to increase their power density, this design rule does not compete with existing ones.

B. Increase of the Turn–Core Spacing

As depicted in Fig. 17, C_{tc} is also inversely proportional to the turn–core spacing s. Thus specific devices called *spacers* are proposed to increase this space on all the faces of the component.

1) Design of the Spacers: The spacers are designed to increase the turn–core spaces while adding a minimum of dielectric material, thanks to their placement on the corners of the section. They are made of three parts built by additive manufacturing with the PLA material and glued together. Three wound components are shown in Fig. 18(a): one without spacer (named A1) and two others (A2 and A3) equipped with spacers shown in Fig. 18(b) with thickness 0.8 mm and (c) with thickness 1.6 mm, respectively.

2) Taking Into Account the Corners in the Model: Fig. 19(a) shows a close-up view of the corners of a turn, which were not taken into account so far. However, as the turn–core distance is increased, their contribution to overall C_{tc} may not be neglected. Thus, this small part is taken into account by increasing the domain simulation of the inside and outside faces, as shown in Fig. 19(b). The increase δ_h of the height h for the simulation, on the outside of the core, is equal to the path of the mean space under the corner s_{avg}, as defined in (19) and shown in Fig. 19(b). This is repeated on the other corner on the same side and on the two inside corners of the core. This new hypothesis is added to the model, and the resulting model is called extended model.

$$\delta_h = \frac{\pi}{2}\frac{s_{\mathrm{avg}}}{2} = \frac{\pi}{4}\frac{s_{\mathrm{eq}R} + c_R + s_{\mathrm{eq}h} + c_{\mathrm{eq}h}}{2}. \tag{19}$$

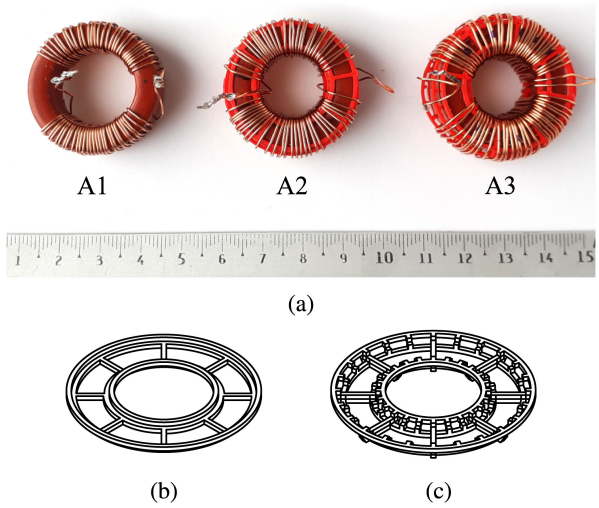

Fig. 18. Wound components series with different turn–core space. (a) Photograph of A1 without spacers. (b) Drawing of A2 and A3 equipped with spacers of thickness 0.8 mm. (c) Drawing of thickness 1.6 mm.

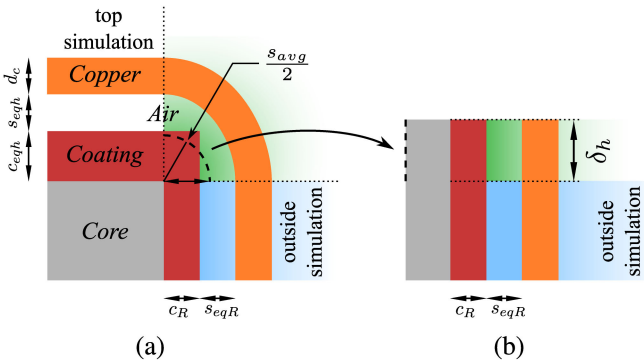

Fig. 19. Drawings of (a) outside top corner of a turn; and (b) its 2-D transformation.

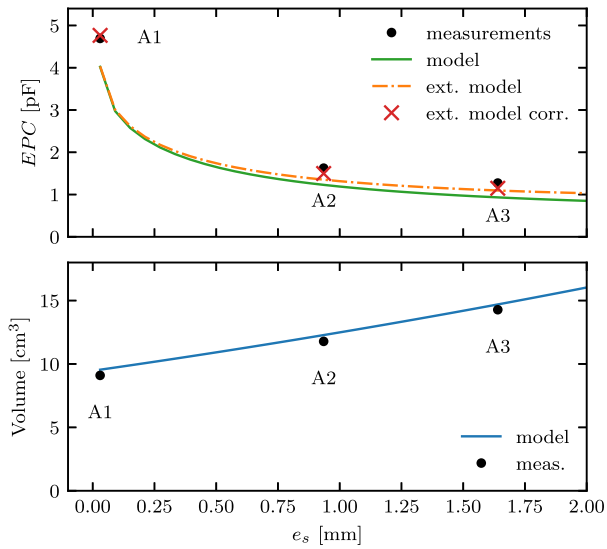

Fig. 20. Evolution of the EPC and cylinder volume against the spacer thickness e_s.

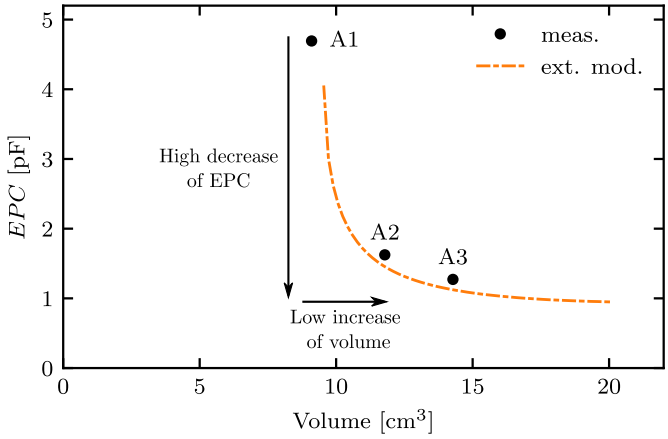

Fig. 21. Evolution of the EPC against the cylinder volume.

3) Experimental Validation: Fig. 20 shows the measured and modeled values of the EPC as a function of the spacer thickness e_s. To compute the modeled values, the following theoretical values have been applied to all faces: a constant space e_s on all the faces of the component, a maximum turn–core distance s defined as in (20) from empirical observations, and interturn distances ζ computed accordingly with (4) and estimated R_t and r_t.

$$s = e_s + \frac{2}{3}d_o. \tag{20}$$

As expected, the EPC decreases with bigger e_s. For instance, between A1 and A3 designs, the EPC has been reduced by 73%, while the cylinder volume of the wound component has been increased by 54% between *A1* and *A3* designs. It is worth pointing out that between *A1* and *A2* designs the decrease on the EPC is still significant (65%), while the impact on the volume is only $+37\%$. This behavior is explained by the fact that C_{tc} is approximately inversely proportional to e_s. This means that with a small increase in e_s, the EPC will drop fast with low volume penalty. This is emphasized in Fig. 21 where an area of low increase in volume and high decrease of EPC has been highlighted. In Fig. 20, the underestimation of the models to the measured value are at maximum 26.8% and 17.5%, respectively, for the base model and the extended one. This demonstrates that the corners play a relatively bigger role in the case of larger e_s. But the overall underestimation of EPC with both models shows that a discrimination of each face of the components and a precise knowledge of each distance on each face may be necessary to further improve accuracy. This is confirmed by the application of the extended model to the measured devices called *ext. model corr.* in Fig. 20, for which the relative error is reduced between -10% and 12.8%. The overestimation for A1 is consistent with previous results, and the underestimation for A2 and A3 might be due to the neglected PLA material of the spacers (such dielectric has relative permittivity of around 3 at the considered frequencies according to [35]), which represent roughly 20% of the perimeter of the section of DUT1. Nevertheless, even without the correction, the proposed model is able to give a robust and precise order of magnitude of the EPC as a function of the turn–core space, which can be beneficial to anticipate the high-frequency response of a coupled inductor at the design stage.

Finally, it has been checked that the differential mode inductance (leakage inductance) of the common-mode chokes does not increase with bigger turn–core spaces. It has even decreased of roughly 25% compared to the tight case A1 because of the increase of the angle covered by the windings. This behavior is confirmed and explained in [36].

VI. Conclusion

A model of the EPC of inductors due to parasitic capacitances of the winding was developed. The proposed 2-D FEM model is applicable to coated ring core, with one winding or two excited in common-mode, and is robust even for determining the elementary capacitances for loose windings. In addition to the classical interturn and turn–core capacitances, the contribution of the fringe and of the corner capacitances were integrated into the model. It is valid for magnetic material that can be considered as perfect conductor or with a high permittivity. In addition, a simple nondestructive test was proposed to help designers to determine whether the model is applicable or not to a specific magnetic material. The model gave the value of the EPC as a function of the number of turns with a satisfactory relative error of 15%, even for loose windings, thanks to accurate 2-D transformation of the curved turns and coating thickness. The assumption used was compared to simpler assumptions and found to be better. The model has been validated for different design parameters, including turn–core space, allowing to proposing a solution for the fine tuning and reduction of the EPC as a tradeoff with the total volume of the component. Hence, plastic spacers were used to increase the turn–core distance, and thus decrease the EPC. The perspectives of this work concern the extension of the proposed model regarding low permittivity magnetic material, such as Ni-Zn, and its application to EMI filters optimization. Indeed for magnetic material with low permittivity, the perfect conductor hypothesis might not hold and some revisions of the parasitic capacitances model are needed. To use the model as a fully predictive tool of the EPC, a model for the turn–core distance s as a function of the core geometry, the diameter of the wire, and the mechanical tension applied on the wire during the winding should be derived. Other winding shapes are also a perspective of this work. The case where turns are kept close to the core, thanks to plastic ties for cores with a big height compared to their radius, is a good example. A loss and thermal models of the component are also desirable to study the thermal advantages and drawbacks of the proposed solution to reduce the EPC, based on loose winding. Finally, the proposed model will be used in the optimization of the volume of the inductor under the constraints of the EMC standards for high-frequency power converters.

References

[1] A. K. Morya *et al.*, "Wide bandgap devices in AC electric drives: Opportunities and challenges," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 1, pp. 3–20, Mar. 2019.

[2] B. Zhang and S. Wang, "A survey of EMI research in power electronics systems with wide-bandgap semiconductor devices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 626–643, Mar. 2020.
[3] K. Mainali and R. Oruganti, "Conducted EMI mitigation techniques for switch-mode power converters: A survey," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2344–2356, Sep. 2010.
[4] B. Zaidi, A. Videt, and N. Idir, "Optimization method of CM inductor volume taking into account the magnetic core saturation issues," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4279–4291, May 2019.
[5] S. Wang, F. C. Lee, D. Y. Chen, and W. G. Odendaal, "Effects of parasitic parameters on EMI filter performance," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 869–877, May 2004.
[6] M. Hartmann, H. Ertl, and J. W. Kolar, "EMI filter design for a 1 MHz, 10 kW three-phase/level PWM rectifier," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1192–1204, Apr. 2011.
[7] X. Huang, J. Feng, F. C. Lee, Q. Li, and Y. Yang, "Conducted EMI analysis and filter design for MHz active clamp flyback front-end converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 1534–1540.
[8] J. Sun, W. Chen, and X. Yang, "EMI prediction and filter design for MHz GaN based LLC half-bridge converter," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 297–304.
[9] Q. Yu and T. W. Holmes, "A study on stray capacitance modeling of inductors by using the finite element method," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 1, pp. 88–93, Feb. 2001.
[10] M. Kovačić, S. Stipetić, Z. Hanić, and D. Žarko, "Small-signal calculation of common-mode choke characteristics using finite-element method," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 1, pp. 93–101, Feb. 2015.
[11] C. Cuellar and N. Idir, "Stray capacitances determination methods of EMI filter inductors," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 7040–7045.
[12] M. Bensetti *et al.*, "A hybrid finite-element method for the modeling of microcoils," *IEEE Trans. Magn.*, vol. 41, no. 5, pp. 1868–1871, May 2005.
[13] A. Chafi, N. Idir, A. Videt, and H. Maher, "Design method of PCB inductors for high-frequency GaN converters," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 805–814, Jan. 2021.
[14] L. Dalessandro, F. da S. Cavalcante, and J. W. Kolar, "Self-capacitance of high-voltage transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2081–2092, Sep. 2007.
[15] Z. Shen, H. Wang, Y. Shen, Z. Qin, and F. Blaabjerg, "An improved stray capacitance model for inductors," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11153–11170, Nov. 2019.
[16] H. Zhao *et al.*, "Physics-based modeling of parasitic capacitance in medium-voltage filter inductors," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 829–843, Jan. 2021.
[17] B. Liu, R. Ren, F. Wang, D. Costinett, and Z. Zhang, "Winding scheme with fractional layer for differential-mode toroidal inductor," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1592–1604, Feb. 2020.
[18] Y. Li and S. Wang, "Modeling and increasing the high-frequency impedance of single-layer Mn-Zn ferrite toroidal inductors with electromagnetic analysis," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6943–6953, Jun. 2021.
[19] A. Massarini and M. K. Kazimierczuk, "Self-capacitance of inductors," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 671–676, Jul. 1997.
[20] M. Kovacic, Z. Hanic, S. Stipetic, S. Krishnamurthy, and D. Zarko, "Analytical wideband model of a common-mode choke," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3173–3185, Jul. 2012.
[21] N. B. Chagas and T. B. Marchesan, "Analytical calculation of static capacitance for high-frequency inductors and transformers," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1672–1682, Feb. 2019.
[22] G. Dong, F. Zhang, Y. Liu, W. Meng, and C. Xu, "Analytical method for extraction of stray capacitance in single-layer CM chokes," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 3185–3191.
[23] L. Middelstädt, S. Skibin, R. Döbbelin, and A. Lindemann, "Analytical determination of the first resonant frequency of differential mode chokes by detailed analysis of parasitic capacitances," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, 2014, pp. 1–10.
[24] A. Massarini, "Analytical approach to the calculation of parasitic capacitance between winding turns," in *Proc. IEEE 4th Int. Forum Res. Technol. Soc. Ind.*, 2018, pp. 1–4.
[25] F. Salomez, A. Videt, and N. Idir, "Semi-analytical model of parasitic capacitance of inductor with conductive core," in *Proc. PCIM Europe Digit. Days; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2021, pp. 1–8.
[26] F. Salomez, A. Videt, and N. Idir, "Modelling and minimization of the parasitic capacitance of ring core inductors," in *Proc. 23rd Eur. Conf. Power Electron. Appl.*, 2021, pp. 1–10.
[27] S. W. Pasko, M. K. Kazimierczuk, and B. Grzesik, "Self-capacitance of coupled toroidal inductors for EMI filters," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 2, pp. 216–223, Apr. 2015.
[28] W. Tan, X. Margueron, and N. Idir, "Analytical modeling of parasitic capacitances for a planar common mode inductor in EMI filters," in *Proc. 15th Int. Power Electron. Motion Control Conf.*, 2012, pp. DS3f.2-1–DS3f.2-6.
[29] E. Snelling, *Soft Ferrites: Properties and Applications*. London, U.K.: Iliffe Books Ltd., 1969.
[30] M. Zdanowski, K. Kostov, J. Rabkowski, R. Barlik, and H.-P. Nee, "Design and evaluation of reduced self-capacitance inductor in DC/DC converters with fast-switching SiC transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2492–2499, May 2014.
[31] R. Clarke, "The wave winder," Accessed: Mar. 2007. [Online]. Available: http://info.ee.surrey.ac.uk/Workshop/advice/coils/winders/wave/index.html
[32] H. Zhao *et al.*, "Rethinking basic assumptions for modeling parasitic capacitance in inductors," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8281–8289, Jul. 2022.
[33] D. C. Meeker, *Finite Element Method Magnetics*. (ver. 4.2), Apr. 2019. [Online]. Available: https://www.femm.info
[34] S. Diaham and M.-L. Locatelli, "Dielectric properties of polyamide-imide," *J. Phys. D: Appl. Phys.*, vol. 46, no. 18, Apr. 2013, Art. no. 185302.
[35] J. Zechmeister and J. Lacik, "Complex relative permittivity measurement of selected 3D-printed materials up to 10 GHz," in *Proc. Conf. Microw. Techn.*, 2019, pp. 1–4.
[36] P.-E. Lévy, F. Costa, C. Gautier, and B. Revol, "Analytical calculation of the magnetic field radiated by a CM coil using conformal mapping methods," in *Proc. Int. Symp. Electromagn. Compat.*, 2014, pp. 246–251.

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