Modeling Turn-OFF Process of High-Power IGBT Based on Both Quasi Static and Nonquasi Static Assumptions

Xin Liu, Litong Wang, Guishu Liang, and Lei Qi

***Abstract*—The calculation for carrier distribution in the quasi-neutral base region is necessary for modeling the turn-OFF process of an insulated gate bipolar transistor (IGBT). The carrier distribution difference between quasi static (QS) and nonquasi static (NQS) conditions and its influences on turn-OFF characteristics of a high-power IGBT are worthy of further study. In this article, the carrier distribution differences between QS and NQS conditions in different turn-OFF stages are first analyzed. In addition, based on the derived conclusions, a novel method modeling the turn-OFF process of high-power IGBTs is further proposed. In the method, the turn-OFF process before the collector–emitter voltage increases to the direct current (dc) voltage is modeled under the QS condition. In contrast, after the collector–emitter voltage increases to the dc voltage, the turn-OFF process is modeled under the NQS condition. Subsequently, the method is verified by comparisons with popular models and experiments. By adopting both QS and NQS assumptions, the proposed method can simplify the calculation and avoid considering the two-dimensional carrier distribution effect in the base. The method is implemented into SABER circuit simulator with MAST language and shows a high accuracy and considerable calculation efficiency.**

***Index Terms*—Behavioral model, excess carrier distribution, finite differential method, high-power insulated gate bipolar transistor (IGBT), quasi static (QS) and nonquasi static (NQS) assumptions.**

I. Introduction

MODELING the high-power insulated gate bipolar transistor (IGBT) turn-OFF process is helpful for predicting the overvoltage problem, the turn-OFF loss, and EMC problem. Based on the modeling methods for IGBTs, the available models can be classified into three categories: behavioral model, mechanism model, and mixed model of behavior and mechanism [1].

The behavioral models produce the target device port characteristic waveforms under specific working conditions. Then, the electromagnetic disturbance or power dissipation problems in the application circuit can be predicted using the models [2]–[6]. The mechanism models are derived based on semiconductor physics. These models have relatively good accuracy and predictability, which has a good guiding significance for the design and application of the devices. Aimed at simplicity, the mixed models of behavior and mechanism are mainly based on semiconductor physics while combining behavioral models for some components [7].

Both the mechanism and mixed models need to calculate the carrier distribution in the quasi-neutral base region, which is governed by the ambipolar diffusion equation (ADE). There are three inevitable issues for the carrier distribution calculation in the turn-OFF process.

First, when calculating the carrier distribution during turn OFF, the existing models are mainly based on the nonquasi static (NQS) assumption [7]. That is to say, when the excess carrier change time cannot be ignored compared with the short switching time, the dynamic transition process of carrier change should be described.

Hefner compared and analyzed the differences between quasi static (QS) and NQS conditions in modeling the turn-OFF process, and concluded that the calculation should be performed under NQS condition [8]. The rapid change rate of the quasi-neutral base region width dW/dt is critical for the significant difference in carrier distributions between QS and NQS conditions [8]. Therefore, adopting QS assumption to model the transient process of IGBTs will lead to large errors. However, this conclusion is aimed at low-power IGBTs. High-power IGBTs have a large current conduction capacity and high withstand voltage. The chip structure shows some differences from that of low-power IGBTs. The active chip sizes in high-power IGBTs are larger than those of low-power IGBTs, which bring about larger capacitances between device terminals. The large capacitances will reduce the turn-OFF speed of high-power IGBTs. Therefore, the change rate of the quasi-neutral base region width dW/dt during turn OFF is far less than that of low-power devices. In addition, the excess carriers were swept out to the buffer layer quickly during turn OFF by introducing the buffer layer. Then, the excess carriers can recombine and disappear much more quickly, which also contributes to a relatively small difference in carrier distributions between NQS and QS conditions. Considering the chip structure differences between low-power and high-power IGBTs, it is necessary to discuss this conclusion further.

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Second, with the gate structure optimization in high-power IGBTs, the excess carrier capacity in high-power IGBTs is improved to enhance the conductivity modulation and increase the current conduction ability. As a result, at the beginning of the turn-OFF process, the depletion region expands around the gate region, and the carriers show a two-dimensional (2-D) distribution effect [10]–[14]. However, the accurate calculation for carrier 2-D distribution depends on the chip gate structure parameters, which increases the difficulty for device application engineering.

Last, during the working process of high-power IGBTs, the range of working current is extensive, and the variation range of excess carrier concentration in the quasi-neutral base region also increases. The modeling for high-power IGBTs needs to adapt to all injection levels.

In addition, modeling the carrier 2-D distribution and all injection levels for high-power IGBTs will significantly increase the amount of calculation, which also increases the difficulty for device application engineering.

The main methods in existing literature for modeling the carrier distribution can be classified into three main categories as follows:

1) Based on the results derived by the finite-element method, the carrier distribution is approximately described by specific functions [15]–[20]. The common functions include linear function, exponential function, trigonometric function, and hyperbolic function. This method is simple and computationally efficient, but it is more suitable for specific devices or specific working conditions and has limitations for all injection levels.
2) Fourier-series-based models: The excess carrier distribution is first discretized by the Fourier series shown in (1) [21], [22]. Then, the related coefficients in (1) are determined, and the carrier distribution is obtained by combining the ADE. The traditional Fourier-series-based model is only suitable for high injection levels, and it is improved for adapting to all injection levels [23]. However, these Fourier-series-based equations in [23] are too complex and not applicable to circuit simulation

$$\Delta p\,(x,t) = \Delta p_0\,(t) + \sum_{k=1}^{M-1} \Delta p_k\,(t) \cos\left[\frac{k\pi\,(x-x_1)}{x_2-x_1}\right] \tag{1}$$

where Δp is the excess hole concentration; x_1 and x_2 are the left and right boundary of the quasi-neutral base region, respectively; and Δp_k are the coefficients to be solved.

3) The excess carrier distribution is discretized by piecewise linearization. This method mainly includes the finite differential model [24], [25], the lumped-charge model [26]–[29], and the finite-element model [30]–[33].

The calculations for carrier distribution in the existing finite differential models are confined to 1-D and high-level injection conditions. The hole and electron current density equations and continuity equations, not the ADE, are directly solved in the lumped-charge model. This calculation method is convenient to realize circuit simulation, but has limitations for engineering applications because it puts high requirements for the model needed parameters, which are difficult to be extracted by existing methods. By comparison, the finite-element method aims at solving the ADE, which is the same as the 1) and 2), and is more widely used by some commercial software. However, after the finite-element method discretizes the ADE equation, the complex calculus involved in the discrete equations are usually solved based on numerical methods, which substantially increases the computational complexity.

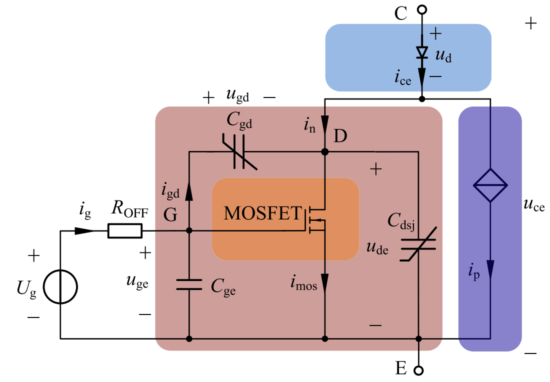

Fig. 1. Typical equivalent circuit model of an IGBT.

In light of these problems, we further study the turn-OFF process model of high-power IGBTs. In Section II, this article first analyzes the carrier distribution differences between QS and NQS conditions in different turn-OFF stages. It determines the applicable turn-OFF stages of QS and NQS assumptions. In Section III, based on the derived conclusions, a novel method for modeling the turn-OFF process of high-power IGBTs is proposed. In the method, the QS and NQS assumptions are both adopted to model different turn-OFF stages for the requirements of accuracy and simplification. In Section IV, the method is preliminarily verified by experiments. In addition, a further comparison with the popular high-power IGBT models is performed and the advantages of this method are proved. The proposed model can be a convenient tool to predict the turn-OFF characteristics of high-power IGBTs.

II. Analysis for Excess Carrier Distribution of High-Power IGBTs During Turn off

The typical equivalent circuit of an IGBT is shown in Fig. 1 [15], where a controlled current source i_p and a metal-oxide semiconductor field-effect transistor (MOSFET) are used to describe the hole and electron current, respectively. A diode is connected in series with the MOSFET, and its voltage u_d represents the voltage drop from collector to base; C, E, and G refer to the collector, emitter, and gate, respectively; D refers to the drain of the MOSFET; C_{gd} is the gate–drain nonlinear capacitance; C_{dsj} is the drain–emitter nonlinear capacitance; C_{ge} is the gate–emitter capacitance; R_{OFF} is the driving resistance when the IGBT turns OFF; u_{gd} is the gate–drain voltage; u_{ge} is the gate–emitter voltage; u_{de} is the drain–emitter voltage; u_{ce} is the collector–emitter voltage; U_g is the pulse driving voltage; i_n is the electron current; i_p is the hole current at emitter side; i_{ce} is the collector current; i_{mos} is the MOSFET or channel current; i_g

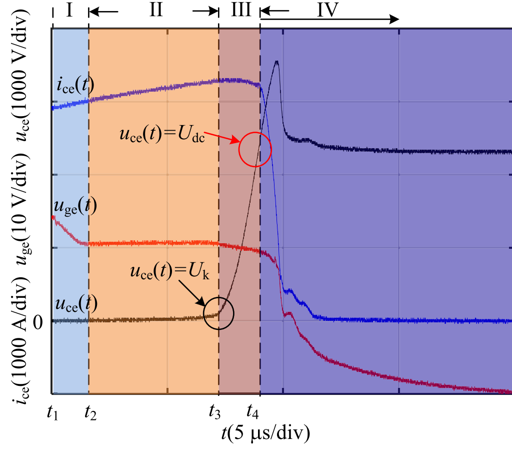

Fig. 2. Typical voltage and current waveforms during turn OFF.

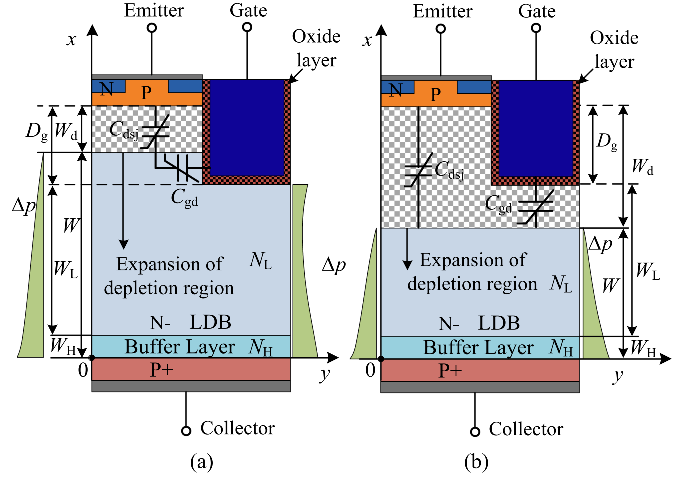

Fig. 3. Chip cross-section structure and expansion of depletion region during turn OFF. (a) $W_d < D_g$. (b) $W_d \geq D_g$.

and i_{gd} are the gate current and current between gate and drain, respectively.

According to Fig. 1, we can divide the circuit into four parts: diode part, MOSFET part, hole current part, and capacitances part. The diode part has a close relationship with the carrier distribution due to the conductivity modulation effect. The influence of excess carrier distribution on the MOSFET part and the hole current part can be described by the boundary condition as [21]

$$\left.\frac{\partial \Delta p}{\partial x}\right|_{x=W} = \frac{1}{2qA}\left(\frac{i_{\text{mos}}}{D_{\text{n}}} - \frac{i_{\text{p}}}{D_{\text{p}}}\right) \tag{2}$$

where $\partial \Delta p/\partial x|_{x=W}$ is the excess carrier concentration gradient at the emitter side; q is the electronic charge; D_{n} and D_{p} are the electron and hole diffusivities, respectively; and A is the device active area.

As for the capacitances part, the C_{dsj} is taken as an example and it can be calculated by as [15]

$$C_{\text{dsj}} = (A - A_{\text{gd}})\sqrt{qN_{\text{c}}\varepsilon_{\text{si}}/(2u_{\text{de}})} \tag{3}$$

where A_{gd} is the gate–drain overlap area; ε_{si} is dielectric constant of silicon; and N_{c} is the space charge region carrier concentration. That is [34]

$$N_{\text{c}} = N_{\text{L}} + i_{\text{p}}/(qA\upsilon_{\text{p}}) - i_{\text{mos}}/(qA\upsilon_{\text{n}}) \tag{4}$$

where N_{L} is the doping density in the base; and υ_{p} and υ_{n} are the electron and hole velocity, respectively.

According to (4) and the relation of i_{mos} and excess carrier distribution shown in (2), the capacitances part also closely relates to the excess carrier distribution.

Therefore, the calculation for excess carrier distribution is the core part for modeling an IGBT turn-OFF process.

Fig. 2 shows the typical turn-OFF transient current and voltage waveforms of a high-power IGBT under double pulse experimental conditions. According to the turn-OFF mechanism, this article divides the turn-OFF process into four stages.

Combining the four parts in Fig. 1 and the turn-OFF stages in Fig. 2, we analyze the excess carrier distribution difference between QS and NQS assumptions and its influence on turn-OFF characteristics.

Stage I (t_1–t_2): In the first stage, the IGBT is working in the saturation state; and with decreasing gate voltage u_{ge}, the device approaches the desaturation state.

Stage II (t_2–t_3): The device starts to work in the desaturation state at t_2. In this stage, the discharge in the gate terminal brings the expansion of the depletion region and an increase in voltage u_{ce} at the same time.

Fig. 3 shows the chip cross-section structure and expansion of the depletion region [34]. In Fig. 3, D_{g} is the distance from the bottom of the trench gate to the P-base; W_{d} is the width of the depletion region; W is the width of the quasi-neutral base region; W_{L} is the width of the low-doped base (LDB) region; W_{H} is the width of the buffer layer or field stop (FS) layer; N_{L} is the doping concentration in the LDB; and N_{H} is the doping concentration in the buffer layer. Fig. 3(a) and (b) shows the depletion region with $W_{\text{d}} < D_{\text{g}}$ and $W_{\text{d}} \geq D_{\text{g}}$, respectively. When W_{d} equals D_{g}, the voltage u_{ce} at t_3 is represented by U_{k} in Fig. 2.

Meanwhile, as Fig. 3(a) shows, the excess carrier concentration has a nonzero value under the gate overlap, and carriers show a 2-D distribution effect around the gate region.

According to Fig. 1, the voltage u_{ce} mainly consists of the diode voltage u_d and the voltage across the capacitance C_{dsj}. The voltage across the capacitance C_{dsj} equals the voltage across the depletion region shown in Fig. 3.

According to the above analysis, the diode voltage u_d, the electron current, hole current, and capacitances all closely relate to the excess carrier distribution. The excess carrier concentration gradient at the emitter side can be approximately expressed as [8]

$$\left.\frac{\partial \Delta p}{\partial x}\right|_{x=W} = -\frac{2}{qAW^2}Q_{\text{T}} + \frac{1}{3qADW}Q_{\text{T}}\frac{\text{d}W}{\text{d}t}. \tag{5}$$

According to (5), the excess carrier distribution is closely related to the change rate of quasi-neutral base region width dW/dt. The larger dW/dt will significantly influence the carrier distribution. Under QS assumption, the dW/dt is assumed as 0. Therefore, the dW/dt will cause a definite difference between the excess carrier distributions under QS and NQS assumptions.

Because of the Miller effect, the gate voltage $u_{\rm ge}$ in Fig. 1 shows small changes. Therefore, the increase in voltage across the depletion region is mainly determined by the capacitances $C_{\rm gd}$ and $C_{\rm dsj}$. The gate-drain nonlinear capacitance $C_{\rm gd}$ is [15]

$$C_{\rm gd} = \begin{cases} C_{\rm gd0} & u_{\rm de} < u_{\rm ge} - U_{\rm Td} \\ C_{\rm oxd}C_{\rm gdj}/\left(C_{\rm oxd} + C_{\rm gdj}\right) & u_{\rm de} \geq u_{\rm ge} - U_{\rm Td} \end{cases} \quad (6)$$

where $U_{\rm Td}$ is the drain–gate overlap depletion threshold voltage; $C_{\rm gdj}$ is the gate–drain nonlinear capacitance; $C_{\rm gd0}$ is the capacitance when $u_{\rm de} < u_{\rm ge}+U_{\rm Td}$, that is, $W_d < D_g$, and this stage corresponds to Fig. 3(a). The $C_{\rm gd0}$ is mainly determined by the gate oxide capacitance $C_{\rm oxd}$.

At stage II, considering that the capacitance $C_{\rm gd}$ is much larger than the capacitance $C_{\rm dsj}$, the change in voltage $u_{\rm ce}$ is mainly determined by the larger one $C_{\rm gd}$. That is, the voltage $u_{\rm ce}$ in this stage is primarily determined by the gate oxide capacitance $C_{\rm oxd}$ which is related to the chip size and has a relatively large value for high-power IGBTs.

Therefore, the capacitance $C_{\rm dsj}$ shown in (3) can be approximately calculated with $N_{\rm c} = N_{\rm L}$ in stages I and II when performing the modeling. This treatment reasonably avoids the influence of hole and electron currents on the calculation for $C_{\rm dsj}$ and can simplify the model.

In addition, the capacitance $C_{\rm gd}$ in this stage is relatively large, and the change rate of the quasi-neutral base region width dW/dt is low. According to (5), this feature contributes to a small carrier distribution difference between QS and NQS assumptions.

Stage III (t_3–t_4): When $W_{\rm d}$ is greater than $D_{\rm g}$, shown in Fig. 3(b), the capacitances $C_{\rm gd}$ and $C_{\rm dsj}$ become relatively small, and the voltage $u_{\rm ce}$ starts to increase rapidly. When the voltage $u_{\rm ce}$ increases to the direct current (dc) voltage $U_{\rm dc}$ at t_4, the current $i_{\rm ce}$ decreases rapidly.

The voltage across the depletion region is much greater than the diode voltage in this stage. Therefore, the change in voltage $u_{\rm ce}$ is mainly affected by the capacitances $C_{\rm gd}$ and $C_{\rm dsj}$.

Referring to (6), the gate–drain nonlinear capacitance $C_{\rm gd}$ is determined by the gate oxide capacitance $C_{\rm oxd}$ and $C_{\rm gdj}$ in this stage. The gate–drain nonlinear capacitance is [32]

$$C_{\rm gdj} = A_{\rm gd}\sqrt{-qN_{\rm c}\varepsilon_{\rm si}/2/u_{\rm gd}}. \quad (7)$$

From (3), (4), and (7), we can see that the influence of carrier distribution on capacitance $C_{\rm gdj}$ and $C_{\rm dsj}$ is described by the term $i_{\rm p}/(qA\upsilon_{\rm p}) - i_{\rm mos}/(qA\upsilon_{\rm n})$, and the larger current ratio $i_{\rm mos}/i_{\rm ce}$ contributes to the less influence on the capacitances.

Due to the large voltage change rate d$u_{\rm ce}$/dt in this stage, the carrier distributions must show a larger difference between QS and NQS assumptions than stages I and II. However, for high-power IGBTs, the deeper and wider trench gate and buffer layer technologies can bring about some special characteristics to the excess carrier distribution as follows:

1) By optimizing the gate structure rather than increasing the excess carrier lifetime [9], the excess carriers accumulate in the gate region with a relatively small excess carrier lifetime. This technology in high-power IGBTs brings about a small ON-state voltage drop and a rapid decrease of excess carriers after $W_{\rm d} > D_{\rm g}$. Compared with stages I and II, due to the lack of carrier accumulation effect offered by the trench gate structure, the excess carrier concentration at the emitter side remains low. This feature contributes to realizing a larger current ratio $i_{\rm mos}/i_{\rm ce}$ and smaller influence of $i_{\rm p}/(qA\upsilon_{\rm p}) - i_{\rm mos}/(qA\upsilon_{\rm n})$ on the concentration $N_{\rm c}$. Therefore, this feature can reduce the influence of the excess carrier difference between NQS and QS assumptions on capacitances $C_{\rm gd}$ and $C_{\rm dsj}$.
2) By introducing a buffer layer, the forward-blocking voltage can be supported by a thinner N-base region [9]. As a result, with the increasing voltage $u_{\rm ce}$ during turn OFF, the excess carriers were quickly swept out to the buffer layer. The excess carriers in the buffer layer can recombine and disappear much more rapidly. In addition, after the depletion region reaches the buffer layer, the change rate of quasi-neutral base region width dW/dt will significantly decrease due to the large doping concentration $N_{\rm H}$ in the buffer layer. Therefore, the buffer layer technology also contributes to a slight difference in excess carrier distributions between QS and NQS assumptions.

Therefore, the two features of high-power IGBTs are likely to slightly influence the excess carrier distribution difference between QS and NQS assumptions in modeling the turn-OFF process.

Stage IV (after t_4): A current oscillation or a tail current will occur in this stage. The characteristics in this stage are determined by the excess carriers in the quasi-neutral base region and have a close relationship with the capacitances and the hole current. If few or no base excess carriers remain when the channel current $i_{\rm mos}$ is close to zero, the current oscillation will occur easily [34]. The current oscillation originates from the coupling of capacitances in the device and the stray inductances in the application circuit. If some excess carriers remain, the slow recombination of the remaining excess carriers will result in a tail current [34], [35]. The tail current in this stage affects the turn-OFF peak voltage and losses. Under the QS assumption, the excess carriers disappear with the shut off of the channel current, and no remaining excess carriers form the tail current. Therefore, the carrier distribution in stage IV must be calculated with NQS assumption.

The conclusions about the excess carrier distributions in different turn-OFF stages are summarized as follows:

1) In stages I and II, because the capacitance $C_{\rm gd}$ is relatively large and then the voltage change rate d$u_{\rm ce}$/dt is small, the excess carrier distributions show a slight difference between QS and NQS assumptions. In stage III, before the depletion region reaches the FS layer, the excess carrier concentration at the emitter side is usually low. After the depletion region reaches the FS layer, the change rate of the quasi-neutral base region width dW/dt will significantly decrease. The two features benefit from the trench gate and FS layer technologies in high-power IGBTs and bring about a slight carrier distribution difference between QS and NQS assumptions. Therefore, before the voltage $u_{\rm ce}$ increases to the dc voltage $U_{\rm dc}$, the turn-OFF process can be modeled with QS assumption.

2) After the voltage u_{ce} increases to the dc voltage, the carrier distributions under QS and NQS assumptions will show a significant difference. Therefore, the modeling for stage IV must be based on NQS condition.

III. Modeling the IGBT Turn-off Process Based on Both Quasi Static and Nonquasi Static Assumptions

A. Comparison Between Quasi Static and Nonquasi Static Assumptions

The carrier distribution in the quasi-neutral base region is governed by the ADE. The 2-D ADE under NQS assumption is [32]

$$D\left(\frac{\partial^2 \Delta p(x,y,t)}{\partial x^2}+\frac{\partial^2 \Delta p(x,y,t)}{\partial y^2}\right) = \frac{\Delta p(x,y,t)}{\tau_{\mathrm{eff}}}+\frac{\partial \Delta p(x,y,t)}{\partial t} \tag{8}$$

where D is the ambipolar diffusivity and τ_{eff} is the effective excess carrier lifetime.

The 2-D ADE under QS assumption is

$$D\left(\frac{\partial^2 \Delta p(x,y)}{\partial x^2}+\frac{\partial^2 \Delta p(x,y)}{\partial y^2}\right)=\frac{\Delta p(x,y)}{\tau_{\mathrm{eff}}}. \tag{9}$$

Based on (8), (9), and the 2-D finite-element method, we calculate the turn-OFF voltage u_{ce}, voltage u_{ge}, current i_{ce}, and the excess carrier distribution. The required device structure parameters for calculation refer to [36]. The working condition is the typical double pulse experiment. The turn-OFF current is 3180 A and the dc voltage is 2800 V. The gate voltage U_g changes from 15 to −9 V. The stray inductance in the current transfer loop is 260 nH. In addition, to reflect the influence of du_{ce}/dt on results, three resistances R_{OFF} are selected in the calculation.

1) Voltage and Current: Fig. 4 compares the voltage and current waveforms between QS and NQS assumptions with the R_{OFF} is 5, 10, and 15 Ω, respectively.

From Fig. 4, we can clearly see that before the voltage u_{ce} increases to dc voltage U_{dc}, the voltage and current waveforms between QS and NQS assumptions are basically identical. In addition, the high consistency of waveforms is still achieved under small driving resistance $R_{\mathrm{OFF}} = 5\ \Omega$ in Fig. 4(a), where the voltage change rate du_{ce}/dt is relatively large. Therefore, it is reasonable to adopt the QS assumption to model stages I, II, and III during turn OFF.

After u_{ce} increases to U_{dc}, the waveforms show a noticeable difference. The results are consistent with the analysis conclusions in Section II. There are tail currents resulting from the recombination of remaining excess carriers when adopting the NQS assumption. By contrast, the current and voltage oscillation occurs under the QS condition. Therefore, the QS assumption cannot describe the tail current. After the voltage u_{ce} increases to the dc voltage, the turn-OFF process must be modeled under NQS condition.

2) Excess Carrier Distribution: To make a more straightforward comparison between QS and NQS assumptions, we further compare carrier distributions. Taking Fig. 4(a) as an example,

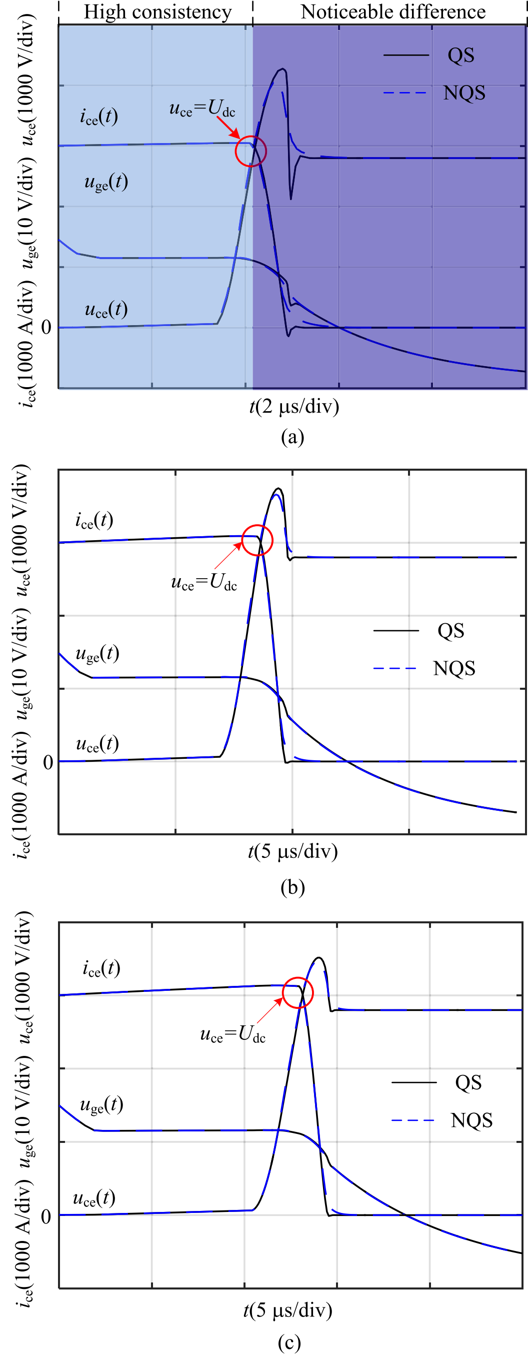

Fig. 4. Comparison of turn-OFF voltages and currents. (a) $R_{\mathrm{OFF}} = 5\ \Omega$. (b) $R_{\mathrm{OFF}} = 10\ \Omega$. (c) $R_{\mathrm{OFF}} = 15\ \Omega$.

Fig. 5 first shows the carrier distributions in different stages. According to Fig. 5(a), the excess carriers near the gate show a significant difference along the y-direction, which is consistent with the results shown in Fig. 3. Therefore, the 2-D effect should be considered when calculating the carrier distributions in stages I and II, which puts high requirements on the device gate structure parameters and increases the difficulty of engineering application.

According to Fig. 5(b), with the increasing voltage u_{ce} in stage III, the excess carriers show a slight difference along

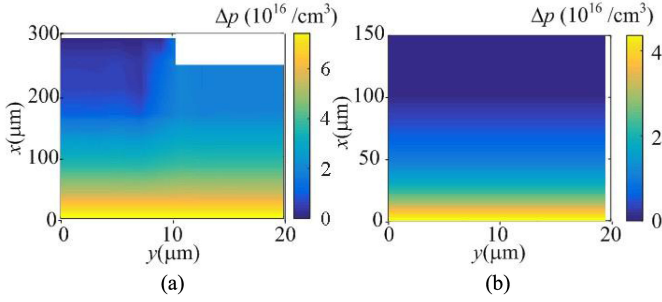

Fig. 5. Excess carrier distributions in base during turn OFF. (a) Stage I or II. (b) Stage III.

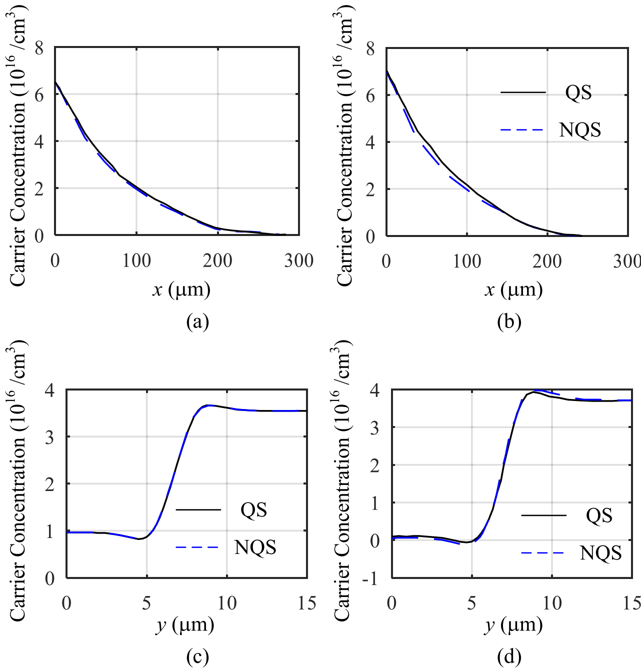

Fig. 6. Comparison of excess carrier distributions in base at $y = 0$ and $x = W_{\rm L} + W_{\rm H}$ (along the bottom of trench gate): (a) $t = 0.5$ μs, $u_{\rm ce} = 9$ V, along with x and $y = 0$, (b) $t = 3.5$ μs, $u_{\rm ce} = 67$ V, along with x and $y = 0$, (c) $t = 0.5$ μs, $u_{\rm ce} = 9$ V, along with y and $x = W_{\rm L} + W_{\rm H}$, and (d) $t = 3.5$ μs, $u_{\rm ce} = 67$ V, along with y and $x = W_{\rm L} + W_{\rm H}$.

the y-direction. They can be seen as 1-D distribution along the x-direction. In this stage, the width of the depletion region $W_{\rm d}$ is greater than the distance $D_{\rm g}$, which is shown in Fig. 3(b), the excess carrier 2-D distribution effect is gradually eliminated. Therefore, the carrier concentration can be calculated based on the 1-D distribution.

Fig. 6 further compares the carrier distributions in stages I and II. The working condition still corresponds to Fig. 4(a). For reflecting the carrier 2-D distribution effect, Fig. 6(c) and (d) compares the carrier distributions along the bottom of the trench gate.

From Fig. 6, we can see that the carrier distributions at $y = 0$ and $x = W_{\rm L} + W_{\rm H}$ all show minor differences between the two assumptions. Referring to the above analysis, the change rate of the width of the quasi-neutral base region dW/dt is the critical factor influencing the difference of carrier distributions between QS and NQS conditions. In stages I and II, the change

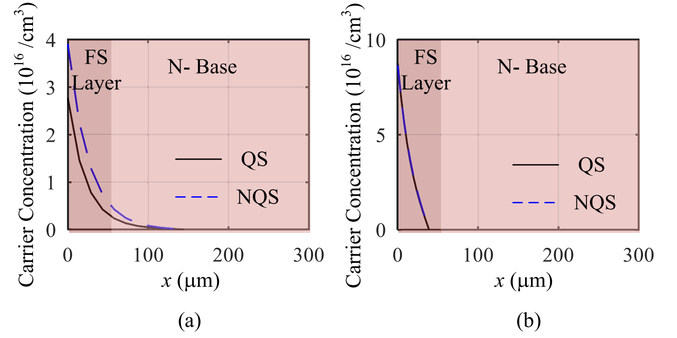

Fig. 7. Comparison of excess carrier distributions in base at $y = 0$: (a) $t = 3.7$ μs, $u_{\rm ce} = 630$ V, and (b) $t = 4.57$ μs, $u_{\rm ce} = 2755$ V.

rate of voltage d$u_{\rm ce}$/dt is relatively small, which brings about a small change rate of the quasi-neutral base region width dW/dt. Therefore, we can understand that the slight difference between the two assumptions results from the small dW/dt. In addition, it is feasible to model stages I and II according to the QS assumption.

With increasing $u_{\rm ce}$ and d$u_{\rm ce}$/dt, the carrier distributions in stage III under QS and NQS assumptions are shown in Fig. 7. Only the carrier distributions at $y = 0$ are displayed because the carriers show a slight difference along the y-direction. Fig. 7(a) shows that the carrier distributions show a relatively more significant difference between QS and NQS assumptions than stages I and II. However, because the excess carrier concentration at the emitter side remains low, the difference in carrier distributions at the emitter side between the two assumptions is still small. When the voltage $u_{\rm ce}$ increases to 2755 V, shown in Fig. 7(b), the depletion region reaches the FS layer, and the carrier distributions between the two assumptions show a very little difference. The main reason is that the change rate of depletion region dW/dt in the FS layer is minimal, caused by the high doping concentration in the FS layer. In addition, the relatively small carrier lifetime in the FS layer also contributes to the slight difference in carrier distributions between the two assumptions.

According to the turn-OFF stage III analysis, the capacitances part in Fig. 1 is the critical factor influencing the turn-OFF voltage $u_{\rm ce}$. From (3), (4), and (7), the capacitances $C_{\rm gd}$ and $C_{\rm dsj}$ also have close relationships with the current ratio $i_{\rm mos}/i_{\rm ce}$. The comparison of nonlinear capacitances $C_{\rm gd}$ and $C_{\rm dsj}$ under different voltages $u_{\rm ce}$ are shown in Fig. 8(b), where slight differences of capacitances $C_{\rm gd}$ and $C_{\rm dsj}$ between QS and NQS conditions are obtained.

From Fig. 8(a), we can see that the current ratio $i_{\rm mos}/i_{\rm ce}$ remains a relatively large level, which can reduce the influence of the $(i_{\rm ce} - i_{\rm mos})/(qA\upsilon_{\rm p}) - i_{\rm mos}/(qA\upsilon_n)$ on capacitances $C_{\rm gd}$ and $C_{\rm dsj}$. Therefore, due to the large level of the current ratio $i_{\rm mos}/i_{\rm ce}$, the slight difference in the current ratio $i_{\rm mos}/i_{\rm ce}$ shown in Fig. 8(a) will not bring about noticeable differences for the nonlinear capacitances $C_{\rm gd}$ and $C_{\rm dsj}$, which is shown in Fig. 8(b).

In conclusion, before the voltage $u_{\rm ce}$ increases to the dc voltage, the turn-OFF process can be modeled under QS condition. After the voltage $u_{\rm ce}$ increases to the dc voltage, the turn-OFF process should be modeled under NQS condition.

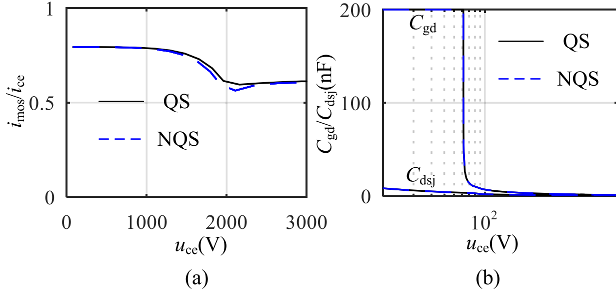

Fig. 8. Comparison of current ratio $i_{\mathrm{mos}}/i_{\mathrm{ce}}$ and nonlinear capacitances $C_{\mathrm{gd}}/C_{\mathrm{dsj}}$ under different voltage u_{ce} during turn OFF ($R_{\mathrm{g}} = 5\ \Omega$). (a) Comparison of current ratio $i_{\mathrm{mos}}/i_{\mathrm{ce}}$. (b) Comparison of nonlinear capacitances C_{gd} and C_{dsj}.

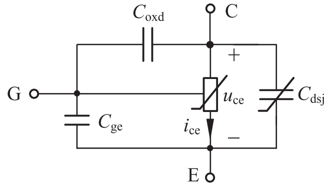

Fig. 9. Equivalent circuit of an IGBT before the voltage u_{ce} increases to the voltage U_k during turn OFF.

Adopting the QS assumption can undoubtedly simplify the model. However, as the above analysis, the carrier 2-D distribution effect should be considered when calculating the carrier distributions in stages I and II, which puts high requirements on the chip gate structure parameters and increases the difficulty of engineering application.

Considering that the voltage and current characteristics of IGBTs under the QS assumption are indeed the static-state output characteristic curve, we can model stages I and II in another way. For the IGBT application engineering, it is enough to obtain the voltage and current characteristics of IGBTs. Therefore, if one method can be brought to describe the static-state output characteristic curve directly, we can avoid the complex calculation for the carrier 2-D distribution.

B. Modeling Stages I, II, and III Based on Quasi Static Assumption

1) Stages I and II: One behavioral model is suitable for the IGBT static-state model because the static-state output characteristics are independent of the stray inductances, stray capacitances, and other parameters in the application circuit. It is basically the characteristics of the device itself.

The IGBT U-I relation in [37] is adopted in this article. Fig. 9 shows the equivalent circuit model where a three-terminal nonlinear resistance represents the U-I relation of IGBT

$$i_{\mathrm{ce}} = \beta(u_{\mathrm{ge}} - U_{\mathrm{T}})^{\gamma} \tanh\left[\theta(u_{\mathrm{ce}} - U_{\mathrm{min}})^{\lambda}\right] \tag{10}$$

where β, λ, θ, and γ are coefficients to be extracted by the steady-state output curve; U_{T} is the channel threshold voltage; and U_{min} is the minimum conduction voltage.

2) Stage III: After stage II, because the carrier distribution is required to determine the capacitances C_{gd} and C_{dsj}, the IGBT must be modeled with the circuit model shown in Fig. 1. The diode part can be ignored for the relatively small diode voltage u_d. The MOSFET part and the boundary conditions in [20], [21] are adopted in this article.

The current equation and charge continuity equations, rather than the ADE, are adopted to calculate the carrier distribution. To make the model suitable for different current levels, from low current to high current, the electron and hole currents at all injection levels are shown as follows [34]:

$$\begin{aligned} i_{\mathrm{n}} &= qAn\mu_{\mathrm{n}}\boldsymbol{E} + qAD_{\mathrm{n}} \times \nabla n \\ i_{\mathrm{p}} &= qAp\mu_{\mathrm{p}}\boldsymbol{E} - qAD_{\mathrm{p}} \times \nabla p \end{aligned} \tag{11}$$

where *p* and *n* are the hole and electron concentrations; and $n = \Delta p + N_{\mathrm{B}}$; $p = \Delta p + n_{\mathrm{si}}^2/N_{\mathrm{B}}$; and μ_n and μ_p are the electron and hole mobilities, respectively.

Combing the relation $i_{\mathrm{ce}} = i_{\mathrm{p}} + i_{\mathrm{n}}$ and $\Delta n = \Delta p$, we can replace the electric intensity with the collector–emitter current i_{ce}. In addition, using the finite differential method, we can obtain the hole current at discretized points shown as

$$i_p\left(i\right) = \frac{p_i\mu_{\mathrm{p}}i_{ce}}{n_i\mu_{\mathrm{n}} + p_i\mu_{\mathrm{p}}} - qA\frac{p_i\mu_{\mathrm{p}}D_{\mathrm{n}} + n_i\mu_{\mathrm{n}}D_{\mathrm{p}}}{n_i\mu_{\mathrm{n}} + p_i\mu_{\mathrm{p}}}\frac{\Delta p_{i+1} - \Delta p_i}{\Delta W_i} \tag{12}$$

where $i = 1$ to *NP*, and *NP* is the number of discrete units. $n_i = \Delta p_i + N_{\mathrm{B}}$; $p_i = \Delta p_i + n_{\mathrm{si}}^2/N_{\mathrm{B}}$; and ΔW_{i} is the width of discrete units.

The charge continuity equation is [34]

$$\begin{aligned} qA \times \partial\Delta n/\partial t &= \partial i_n/\partial x - qA \times n/\tau_{\mathrm{n}} \\ qA \times \partial\Delta p/\partial t &= -\partial i_{\mathrm{p}}/\partial x - qA \times p/\tau_{\mathrm{p}} \end{aligned} \tag{13}$$

where τ_{n} and τ_{p} are the excess electron carrier and hole carrier lifetimes, respectively.

Under QS assumption, the time differential term $\partial\Delta p / \partial t$ or $\partial\Delta n / \partial t$ in (13) is ignored, which can effectively reduce the computational complexity. Combining the relation of $\Delta n = \Delta p$, we make integral calculations to (13) on discrete elements and obtain the variations of hole currents on discrete elements

$$\Delta i_{\mathrm{p}}\left(i\right) = qA\Delta W_i\left(\Delta p_i + \Delta p_{i+1}\right)/2/\tau_{\mathrm{eff}} \tag{14}$$

where τ_{eff} is the equivalent excess carrier lifetime, it is [23]

$$\tau_{\mathrm{eff}} = \left(\Delta p\tau_{\mathrm{H}} + N_{\mathrm{B}}\tau_{\mathrm{L}}\right)/\left(\Delta p + N_{\mathrm{B}}\right) \tag{15}$$

where τ_{L} and τ_{H} are the equivalent electron and hole lifetimes in low injection level and high injection level, respectively.

By (12) and (14), the carrier concentration at discretized points can then be calculated.

C. Modeling Stage IV Based on Nonquasi Static Assumption

Under NQS assumption, the electron current and hole current at discretized points are the same as (13). While the time differential terms $\partial\Delta p / \partial t$ or $\partial\Delta n / \partial t$ in (13) must be considered. After the integral operations, the variations of hole currents on

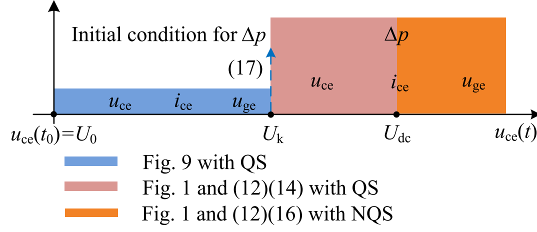

Fig. 10. Calculation diagrams of the proposed method.

discrete elements are

$$\Delta i_{\mathrm{p}}(i) = \frac{qA}{2}\left[\begin{array}{l}\Delta W_i\left(\frac{\partial \Delta p_i}{\partial t} + \frac{\partial \Delta p_{i+1}}{\partial t} + \frac{\Delta p_i + \Delta p_{i+1}}{\tau_{\mathrm{eff}}}\right) \\ + \frac{\partial \Delta W_i}{\partial t}\left(\Delta p_i + \Delta p_{i+1}\right)\end{array}\right]. \tag{16}$$

D. Initial Condition for Calculation of Carrier Distribution

The initial condition for calculating the carrier distribution is determined by (17) which is the 1-D analytical solution of ADE under QS condition [7]. The carrier distribution diagram refers to Fig. 7 in [22] and will not be covered here

$$\begin{aligned}\Delta p(x) &= P_{\mathrm{L0}}\frac{\sin h\left[(W-x)/L_{\mathrm{L}}\right]}{\sin h\left(W/L_{\mathrm{L}}\right)} \\ \Delta p(x^*) &= \frac{P_{\mathrm{H0}}\sin h\left[(W_{\mathrm{H}}-x^*)/L_{\mathrm{H}}\right] + P_{\mathrm{HW}}\sin h\left(x^*/L_{\mathrm{H}}\right)}{\sin h\left(W_{\mathrm{H}}/L_{\mathrm{H}}\right)}\end{aligned} \tag{17}$$

where L_{L} and L_{H} are the ambipolar diffusion lengths in LDB and buffer layer, respectively; P_{L0} is the excess carrier concentration at buffer layer edge of the LDB; P_{H0} is the excess carrier concentration at collector edge of the buffer layer; and P_{HW} is the excess carrier concentration at LDB edge of the buffer layer. P_{L0}, P_{H0}, and P_{HW} in (17) can be calculated by the formulas (18)–(24) in [38].

Modeling the carrier distribution under the QS assumption starts at t_3 in Fig. 1. When the voltage u_{ce} increases to U_{k} and the width of the depletion region W_{d} equals D_{g}, the carrier 2-D distribution effect basically disappears [14]. At the same time, because the critical voltage U_{k} and its change rate $\mathrm{d}u_{\mathrm{ce}}/\mathrm{d}t$ are relatively small, the difference in carrier distributions between QS and NQS assumptions can be negligible. Therefore, it is reasonable to determine the initial condition under QS condition when the voltage u_{ce} increases to the voltage U_{k}.

The critical voltage U_{k} is

$$U_{\mathrm{k}} = u_{\mathrm{ge}} + U_{\mathrm{Td}}. \tag{18}$$

This treatment method takes into account both the carrier distribution characteristics about one and two dimensions and the difference between QS and NQS assumptions, and it can meet the requirements of accuracy and engineering applicability, avoiding considering the 2-D carrier distribution effect near the gate and reducing the dependence on the chip gate structure parameters.

Fig. 10 shows the calculation diagrams of the proposed method. In Fig. 10, the device turns OFF at t_0, and the voltage u_{ce} is U_0. Using the proposed static-state circuit shown in Fig. 9, we calculate the voltage u_{ce}, u_{ge}, and current i_{ce} before the voltage u_{ce} increases to the voltage U_{k}. When the voltage u_{ce} increases to the critical voltage U_{k}, we determine the initial condition by (17) for calculation of carrier distribution and perform the modeling based on the circuit shown in Fig. 1 and QS assumption. Therefore, when $U_{\mathrm{k}} \leq u_{\mathrm{ce}} \leq U_{\mathrm{dc}}$, we calculate the carrier distribution by (12) and (14). The calculation does not consider the time differential term $\partial\Delta p/\partial t$ in (13), which can simplify the calculation process and improve the calculation efficiency.

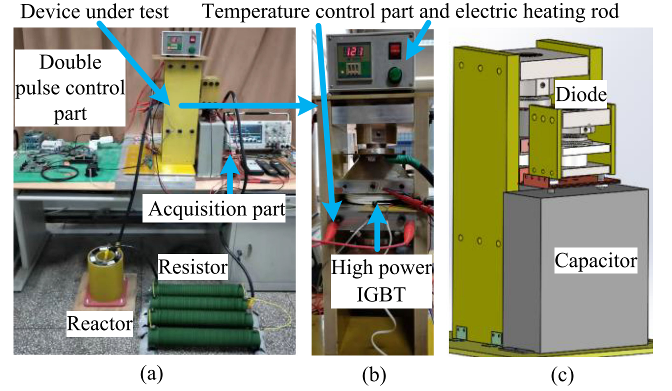

Fig. 11. Experimental platform and an IGBT under test in the laboratory. (a) Experimental platform. (b) Left side of press-pack semiconductor module. (c) Right side of press-pack semiconductor module.

After the voltage u_{ce} increases to the dc voltage U_{dc}, we perform the modeling based on the circuit shown in Fig. 1 and NQS assumption. The carrier concentration Δp is calculated by (12) and (16).

IV. Verification and Comparison

To further verify the proposed model, we establish a high-power double pulse test platform in the laboratory. Fig. 11 displays the experimental platform and the device under test. The selected type of IGBT is TOSHIBA ST2100GXH24A. The Tektronix oscilloscope MDO3034, Tektronix high-voltage probe THDP0100, and the PEM Rogowski current transducer CWT mini HF150B are used to perform the acquisition of transient waveforms.

A. Verification With Experiments

The relevant parameters of the model can be obtained following the methods in [24] and [39], [40], and the extracted parameters used in the model are listed in Table AI, where I_{sne} is the collector electron saturation current.

Meanwhile, the temperature dependences of model parameters are referred to [20], [26], and [41]. This article will not repeat it due to the limitation of space.

To verify the model, this article implements the proposed method into the SABER simulator using the MAST language and calculates the turn-OFF voltages and currents. Fig. 12 compares the turn-OFF voltage and current waveforms. The breaking current is 3000 A, and the dc voltage is 2200 V. The temperatures

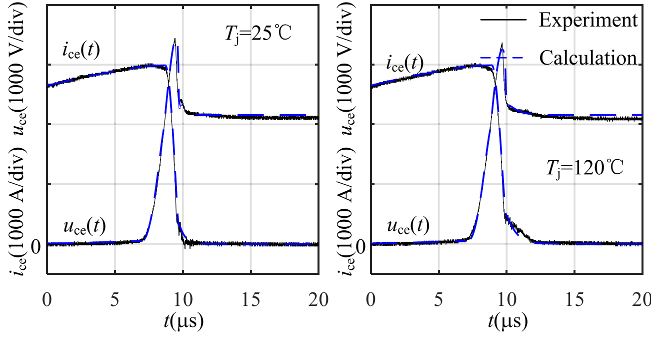

Fig. 12. Comparison of turn-OFF voltages and currents between experiments and calculations: $U_{\rm dc} = 2200$ V/$I_{\rm OFF} = 3000$ A.

TABLE I
COMPARISON OF TURN-off PARAMETERS BETWEEN EXPERIMENTS AND CALCULATIONS ($T_{\rm j} = 25$°C)

Test conditions	Parameters	Measurement	Proposed model	Relative errors (%)
	E_{off} (J)	7.53	7.21	4.3
U_{dc} = 3100 V	U_{peak} (V)	3830	3703	3.2
I_{off} = 1200 A	t_{off} (μs)	9.7	10.2	5.5
	du/dt_{max}(V/μs)	2174	2293	5.0
	E_{off} (J)	9.22	8.93	3.2
U_{dc} = 2200 V	U_{peak} (V)	3440	3310	3.8
I_{off} = 3000 A	t_{off} (μs)	9.5	9.9	4.2
	du/dt_{max}(V/μs)	2151	2255	4.8
	E_{off} (J)	20.2	19.1	5.5
U_{dc} = 2050 V	U_{peak} (V)	3660	3500	4.4
I_{off} = 5800 A	t_{off} (μs)	8.8	9.1	3.4
	du/dt_{max}(V/μs)	2083	2200	5.6

TABLE II
COMPARISON OF TURN-off PARAMETERS BETWEEN EXPERIMENTS AND CALCULATIONS ($T_{\rm j} = 120$°C)

Test conditions	Parameters	Measurement	Proposed model	Relative errors (%)
	E_{off} (J)	8.78	8.68	3.0
U_{dc} = 3100 V	U_{peak} (V)	3650	3590	1.7
I_{off} = 1200 A	t_{off} (μs)	10.62	10.11	4.8
	du/dt_{max}(V/μs)	2131	2235	4.9
	E_{off} (J)	10.8	10.4	3.7
U_{dc} = 2200 V	U_{peak} (V)	3360	3290	2.1
I_{off} = 3000 A	t_{off} (μs)	10.37	9.98	3.8
	du/dt_{max}(V/μs)	2090	2220	6.2
	E_{off} (J)	22	20.8	5.5
U_{dc} = 2050 V	U_{peak} (V)	3590	3458	3.7
I_{off} = 5800 A	t_{off} (μs)	9.32	8.94	4.1
	du/dt_{max}(V/μs)	2041	2197	7.6

under test are 25°C and 120°C. The turn-OFF driving resistance is 8.2 Ω. The gate driving voltage U_g changes from 15 to −9 V. The stray inductance is 315 nH. According to the comparison shown in Fig. 12, a good agreement can be obtained between the calculated and experimental waveforms.

Tables I and II compare turn-OFF losses, the peak values of voltage $u_{\rm ce}$, the turn-OFF time, and the maximum du/dt between experiments and calculations at 25°C and 120°C. The breaking currents are 1200, 3000, and 5800 A. The dc voltages are 3100, 2200, and 2050 V. According to Tables I and II, the maximum relative errors between the measured and calculated values for turn-OFF losses, peak voltages, turn-OFF time, and the maximum du/dt are 5.5%, 4.4%, 5.5%, and 7.6%, respectively. Therefore, the proposed model can accurately describe the turn-OFF process of high-power IGBTs under different working conditions.

TABLE III
RELATIVE ERRORS OF TURN-off PARAMETERS FOR DIFFERENT MODELS

Test conditions	Parameters	Proposed model	Modified Hefner model	Fourier-series Based model	igbt1_2
	E_{off} (J)	4.3 %	14.1 %	13.8 %	4.5 %
U_{dc} = 3100 V	U_{peak} (V)	3.2 %	11.9 %	9.6 %	7.8 %
I_{off} = 1200 A	t_{off} (μs)	5.2 %	17.6 %	8.4 %	9.7 %
	du/dt_{max}(V/μs)	5.0 %	11.8 %	12.7 %	12.6 %
	E_{off} (J)	3.2 %	8.6 %	9.9 %	4.4 %
U_{dc} = 2200 V	U_{peak} (V)	3.8 %	10.3 %	7.9 %	7.9 %
I_{off} = 3000 A	t_{off} (μs)	4.2 %	15.7 %	13.4 %	11.7 %
	du/dt_{max}(V/μs)	4.8 %	14.6 %	12.1 %	7.6 %
	E_{off} (J)	5.5 %	8.1 %	7.5 %	9.6 %
U_{dc} = 2050 V	U_{peak} (V)	4.4 %	7.9 %	7.1 %	13.5 %
I_{off} = 5800 A	t_{off} (μs)	3.4 %	8.5 %	5.9 %	10.7 %
	du/dt_{max}(V/μs)	5.6 %	7.8 %	6.1 %	17.8 %

It should be pointed out especially that benefiting from the advanced chip technologies, for example, FS layer and deeper and wider trench gate structure, the high-power IGBTs have relatively small tail currents. However, it does not rule out the possibility that a small number of devices in the market still have large tail currents, and the carrier distributions between QS and NQS assumptions will show a relatively large difference. Therefore, the method in this article may show low accuracy for this kind of device.

B. Comparison

In this section, we compare the proposed method and the popular high-power IGBT models, that is, the modified Hefner mechanism model [20], the Fourier-series base mechanism model [21], and the behavioral model igbt1_2 embedded in the SABER simulator.

Table III shows the relative errors of turn-OFF parameters for different models at 25°C. From the results, we can see that the Hefner model and Fourier-series-based model show relatively large errors, especially for the working condition where the conduction current and working voltage are 1200 A and 3100 V. The relative errors for the turn-OFF time and the turn-OFF loss are up to 17.6% and 13.8%, respectively. Under this working condition, the carrier concentration is relatively small and the depletion region expands to the FS layer. As a result, the carrier distribution should be calculated under all injection levels. However, only the high injection condition is considered in the modified Hefner model and the Fourier-series-based model. The accuracy of the behavioral model igbt1_2 depends on the specific turn-OFF voltage/current waveform which is used to extract the model parameters and shows large changes with different working conditions.

Fig. 13 compares turn-OFF waveforms between the proposed method and the other popular models with $U_{\rm dc} = 2200$ V and $I_{\rm OFF} = 3000$ A. The results show that the waveforms obtained by the proposed model are highly close to the experiment

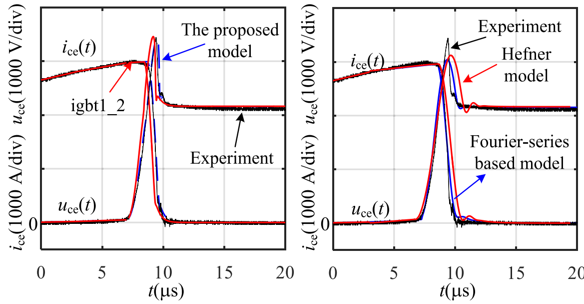

Fig. 13. Comparison of turn-OFF waveforms between the proposed method and the other popular models: $U_{dc} = 2200$ V/$I_{OFF} = 3000$ A.

TABLE IV
EXECUTION TIMES OF THE SIMULATIONS FOR COMPARED MODELS

Calculated conditions	Proposed model	Modified Hefner model	Fourier-series based model	igbt1_2
Turn off total time	1.72 s	1.58 s	1.71 s	1.36 s
$u_{ce} < U_{dc}$ stage	0.61 s	0.62 s	0.64 s	0.51 s
$u_{ce} > U_{dc}$ stage	1.11 s	0.96 s	1.07 s	0.85 s

waveforms. By contrast, the other models show obvious large differences. For the compared models, the voltage or current change rate are not accurately simulated. The voltage and current change rate is closely related to the nonlinear capacitances C_{gd}/C_{dsj} and the hole current in devices which are influenced by the carrier distribution. Therefore, the calculations for the carrier distribution, nonlinear capacitances between device terminals, and the hole current in devices are crucial for modeling high-power IGBTs.

In conclusion, the differences between different models are reflected in two main aspects. First, the calculation for carrier distribution shows large differences. The calculations for carrier distribution are performed under high injection levels in the Hefner and Fourier-series-based models. The influence of doping concentration on the carrier distribution and the ambipolar diffusivity is ignored. The carrier distribution results will directly influence the hole current. Second, the calculations for nonlinear capacitances C_{gd} and C_{dsj} are also different. For example, the influence of carrier concentration on nonlinear capacitances is not considered in the behavioral model igbt 1_2, which causes the unsatisfactory applicability for different injection levels.

Table IV shows the turn-OFF execution times for different models. Simulations were performed using AMD Ryzen 7 5800 3.4 GHz CPU and 16.0 GB RAM under the same simulation conditions. From the results, we can see that the total execution times for different models are comparable. It is noteworthy that the entire time of the proposed model is not increased evidently due to the carrier distribution calculation under all injection levels. By further comparing the calculation times of different stages, we can see that the execution time for stage $u_{ce} < U_{dc}$ of the proposed method is less than these of the two mechanism models: the modified Hefner model and the Fourier-series-based model. In stage $u_{ce} > U_{dc}$, the proposed method needs more execution times than the other three models for adapting all injection levels and improving the simulation accuracy. Overall, the proposed method has a good calculation efficiency comparable to the other popular models. Therefore, it is exactly the adoption of the QS assumption when $u_{ce} < U_{dc}$ in the proposed method that has this good effect.

As for the needed parameters for different models, it is almost identical for the proposed model, the modified Hefner mode, and the Fourier-series-based model. The additional parameters β, λ, θ, γ, and U_{min} in this article can be directly extracted by fitting the steady-state output curve in device datasheet. The parameters extraction for the behavioral model igbt 1_2 is relatively simple. However, the accuracy of igbt1_2 under different working conditions is far from guaranteed.

V. CONCLUSION

Aimed at the high accuracy and the simplification to the computation when modeling the turn-OFF process of high-power IGBTs, this article proposes a novel modeling method which makes full use of the carrier distribution characteristics of high-power IGBTs and adopts QS and NQS assumptions to model different turn-OFF stages.

In the proposed method, the carrier 2-D distribution effect and all injection levels are fully considered. As a result, the accuracy of the proposed method is much better than the existing popular models. Especially, the model can effectively adapt to different conduction levels and has a good accuracy for various working conditions. However, the calculation efficiency of the proposed model is not obviously reduced due to the improved accuracy. It has a good calculation efficiency which is comparable to the existing popular high-power models. That good effect is due to the consideration to the carrier distribution characteristics of high-power IGBTs under QS and NQS assumptions and the adoption of QS assumption before the collector–emitter voltage increases to the dc voltage during turn off. To facilitate the engineering application, the model is also implemented into the SABER circuit simulator with the MAST language.

APPENDIX

The extracted parameters for the ST2100GXH24A model are shown in Table AI.

TABLE AI
PARAMETERS USED IN PROPOSED MODEL OF ST2100GXH24A

Parameters	Values	Parameters	Values
W_H (cm)	0.007	C_{ge}/C_{oxd} (nF)	478/200
N_H (cm^{-3})	2.0×10^{17}	A (cm^2)	30
W_L (cm)	0.0205	I_{sne} (A)	1.88×10^{-13}
N_L (cm^{-3})	4.2×10^{13}	τ_L (μs)	1.9
U_{Td} (V)	50	τ_H (μs)	0.1
U_T (V/25°C)	7.8	U_T (V/125°C)	6.5
U_{min} (V/25°C)	1.57	U_{min} (V/125°C)	0.95
θ (25°C)	0.20	θ (125°C)	0.21
λ (25°C)	0.89	λ (125°C)	0.86
β (25°C)	593.8	β (125°C)	575.7
γ (25°C)	1.46	γ (125°C)	1.41

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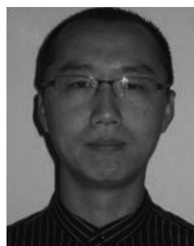

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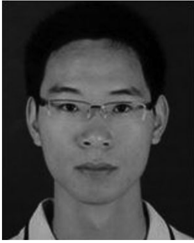

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