Harmonic Weighting and Target Function Design Strategy to Minimize Switch Voltage Stress of Class Φ_2 Inverter

Desheng Zhang, Liangliang Lu, Qiaoling Tong, *Member, IEEE*, Qiao Zhang, *Member, IEEE*, Run Min, *Member, IEEE*, Han Peng, *Senior Member, IEEE*, and Xuecheng Zou, *Senior Member, IEEE*

***Abstract*—For very high frequency (VHF) class Φ_2 inverter, conventional design method requires complex tuning for parameters. Without fully quantitative calculations, the tuning highly depends on experience that cannot achieve optimal design. In this article, a target function design strategy is proposed based on quantitative harmonic weighting, which simplifies the design procedures and minimizes the switch voltage stress. First, the target switch voltage with minimized peak value is derived by optimizing the harmonic weighting. With the result, the power switch is modeled as a voltage source to simplify the calculations, where the branch currents are solved to provided fully quantitative analysis. Based on the analysis, optimal features of switching node impedance are derived to achieve the target switch voltage. In addition, basic constrains of the resonant tank are analyzed to reduce circling currents. Combining the optimal features and basic constrains of the resonant tank, the circuit parameters are calculated directly, which minimizes the switch voltage stress and improves power efficiency. Compared with conventional design, a 27.12 MHz prototype demonstrates 10.2% reduction in average switch voltage stress and 7.2% improvement in average efficiency.**

***Index Terms*—Design method, harmonic weighting, resonant converter, very high frequency (VHF), voltage stress.**

I. Introduction

VERY high frequency (VHF) power inverters are widely explored in recent years [1], [2]. Compared with conventional power conversion techniques, VHF power convertor reduces the switching loss with soft switching techniques, thereby significantly increases the switching frequency to tens of megahertz. Since the energy storage requirement is greatly reduced, VHF techniques provide great potential for higher power density and dynamic performance [3], [4].

For various VHF topologies, class E inverter is widely used due to its simple topology and easy realization of zero-voltage switching (ZVS) [5]–[8]. But, the switch voltage stress in class E inverter reaches 3.6–4.4 times of the input voltage, which limits the input range and power switch selection. During power up and input/load variations, the voltage stress can be considerably higher than that under steady-state operation, which might damage the power switch. Even though a switch is not destroyed immediately in a transient, the long-term repetitive voltage stress will gradually degrade its electrical performance, leading to system instability [9]. Therefore, reducing the switch voltage stress can effectively improve system reliability.

To reduce the switch voltage stress, class F inverter shapes the switch voltage waveform with a high-order resonant tank composed of massive components, which reduces the stress to two times of the input voltage [10]. As a compromise between classes E and F topology, class Φ_2 topology absorbs the second harmonic of the switch voltage by adding a simple series resonant branch to class E inverter [11], which reduces the voltage stress to 2.2–2.6 times of the input voltage. With reduced voltage stress and small component count, class Φ_2 topology has been widely used in dc/dc converters [12]–[16], power amplifiers [17] and wireless power transfer (WPT) systems [18]–[20].

Furthermore, extensive researches are carried out on modeling and design of class Φ_2 converter [21]–[23]. In [21], the circuit parameters are roughly calculated with empirical initial value of resonant capacitor and pole positions of the resonant tank. Then, an iterative tuning procedure based on circuit simulation is carried out to reduce switch voltage stress and realize ZVS. To reduce the iterative tunings, a parameter scanning approach is introduced to obtain values of resonant parameters [23]. Nevertheless, parameter scanning is also a time-consuming strategy for optimal parameter design. From above literatures, empirical design provides solutions to determine the circuit parameters. However, without complete quantitative analysis, the design procedures often require massive computer-aided simulations to optimize the voltage stress and efficiency.

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Desheng Zhang, Qiaoling Tong, Run Min, and Xuecheng Zou are with the School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: dszhang@hust.edu.cn; tongqiaoling@hust.edu.cn; minrun@hust.edu.cn; estxczou@gmail.com).

Liangliang Lu is with the School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China, and also with the Lunar Exploration and Aerospace Engineering Center, State Administration for Science Technology and Industry for National Defence, Beijing 100190, China (e-mail: d202080855@hust.edu.cn).

Qiao Zhang is with the School of Automation, Wuhan University of Technology, Wuhan 430070, China (e-mail: zhangqiao@whut.edu.cn).

Han Peng is with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: pengh@hust.edu.cn).

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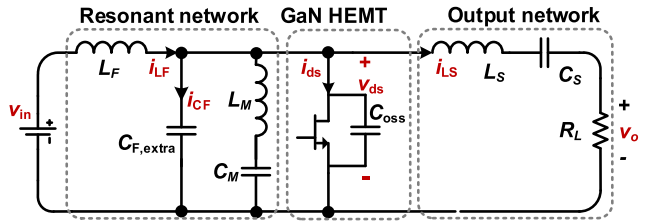

Fig. 1. Topology of class Φ_2 inverter.

In modeling resonant inverters, the well-known fundamental frequency approximation (FHA) method can be used to derive the required parameters [24]–[27]. However, the calculations are very complex, since they include multiple differential equations. To simplify the equations, the order of resonant tank across the power switch is reduced by approximation, where the high order branch is modeled by a capacitor with an equivalent series resistance [27]. However, all the approaches ignore high-order harmonic components that limit the accuracy, especially for class Φ_2 inverter. A normalized full-order analytical model for class Φ_2 inverter is proposed in [28]. Based on the model, the influences of resonant parameters on power output capability are thoroughly analyzed to achieve maximum power. However, all above methods have not quantitatively explored the influence of harmonic weightings on voltage stress and efficiency. For optimal parameter design, fully quantitative calculations are required to determine the harmonic weightings.

To simplify the design procedures and minimize the switch voltage stress, this article proposes a target function design method based on optimal harmonic weighting. First, the typical switching node voltage is sine fitted with the fundamental and third harmonics based on spectrum analysis. By optimizing the harmonic weighting, the target switch voltage ($v_{\mathrm{ds,tag}}$) is derived to minimize the voltage stress. Then, the switching device is modeled as a voltage source with $v_{\mathrm{ds,tag}}$, which simplifies the circuit as a linear network. Based on the simplified circuit, the target switch current ($i_{\mathrm{ds,tag}}$) is solved and fully quantitative analyses are provided. Furthermore, optimal features of switching node impedance (Z_{ds}) are derived to realize $v_{\mathrm{ds,tag}}$. Additionally, combining the optimal features and basic constrains of the resonant tank, the circuit parameters are directly calculated.

This article is organized as follows. Section II reviews conventional design method of class Φ_2 inverter. Section III presents the optimal harmonic weighting and target function design strategy. In Section IV, a design example is presented. In Section V, experimental results are presented to verify the effectiveness of the proposed design method. Finally, Section VI concludes this article.

II. Conventional Design Method of Class Φ_2 Inverter

The topology of class Φ_2 inverter is shown in Fig. 1. Since the switch voltage waveform is shaped by the switching node impedance, the operation of class Φ_2 inverter highly relies on careful selection of resonant components. The conventional design procedures consist four steps: load network design; resonant tank design; resonant capacitor tuning; and resonant inductor tuning, which are summarized as follows.

A. Design of the Load Network

The first step of conventional design method is to determine values of L_S and C_S in the load network. C_S is a dc blocking capacitor, which is relatively large. Furthermore, based on the well-known FHA model and output power, L_{S} is calculated by

$$L_S = \frac{R_L}{\omega_s} \cdot \sqrt{\frac{8v_{\mathrm{in}}^2}{\pi^2 P_o R_L} - 1} \tag{1}$$

where $\omega_s = 2\pi f_s$ represents the switching frequency, v_{in} is input voltage, R_L is load resistance, and P_o is the rated output power.

B. Initial Design of Resonant Tank

An initial value of C_F ($C_F = C_{\mathrm{oss}} + C_{\mathrm{F,\ extra}}$) is selected based on experience and the rated output power. Then, values of L_F, L_M, C_M are determined by (2). This step highly relies on experience. For example, a large value of C_F leads to high circling losses, whereas a small value leads to degraded waveforms

$$L_F = \frac{1}{9\pi^2 {f_s}^2 C_F}, L_M = \frac{1}{15\pi^2 {f_s}^2 C_F}, C_M = \frac{15}{16} C_F. \tag{2}$$

C. Tuning $\mathrm{C_{F,\ Extra}}$ to Reduce the Switch Voltage Stress

Adjusting $\mathrm{C_{F,extra}}$ so that the switching node impedance (Z_{ds}) satisfies

$$4\mathrm{dB} < \frac{Z_{\mathrm{ds},\omega s}}{Z_{\mathrm{ds},3\omega s}} < 8\mathrm{dB} \tag{3}$$

where $Z_{\mathrm{ds,\ \omega s}}$ is the magnitude of Z_{ds} at fundamental frequency and $Z_{\mathrm{ds,\ 3\omega s}}$ is the magnitude of Z_{ds} at the third harmonic. Value of $C_{F,\ \mathrm{extra}}$ directly affects the shape of switch voltage. With a proper value of $C_{F,\ \mathrm{extra}}$, the peak switch voltage is reduced.

D. Tuning L_F to Achieve ZVS

For VHF power inverters, ZVS is essential to reduce the switching loss. To achieve ZVS, L_F is adjusted until the phase of Z_{ds} at fundamental frequency is between 30° and 60°.

With conventional design method, the switch voltage waveforms and spectrums in published class Φ_2 inverters are shown in Fig. 2. With different tunings, the designs induce different $v_{\mathrm{ds}}/v_{\mathrm{in}}$ (normalized switch voltage). As indicated by spectrums of $v_{\mathrm{ds}}/v_{\mathrm{in}}$, the designs induce varying harmonic components, where the fundamental and third harmonics are dominant. To minimize the switch voltage stress, quantitative analysis of the harmonic magnitude is required.

Above conventional design method provides a solution to determine circuit parameters of class Φ_2 inverter. However, the method is not straightforward to optimize the voltage stress and efficiency. Specifically, it must select an initial value of resonant capacitor, which highly relies on experience of designer. An improper resonant capacitor might lead to degraded waveforms or high circling losses. Additionally, a tuning procedure is required after initial calculations, which is a time-consuming procedure.

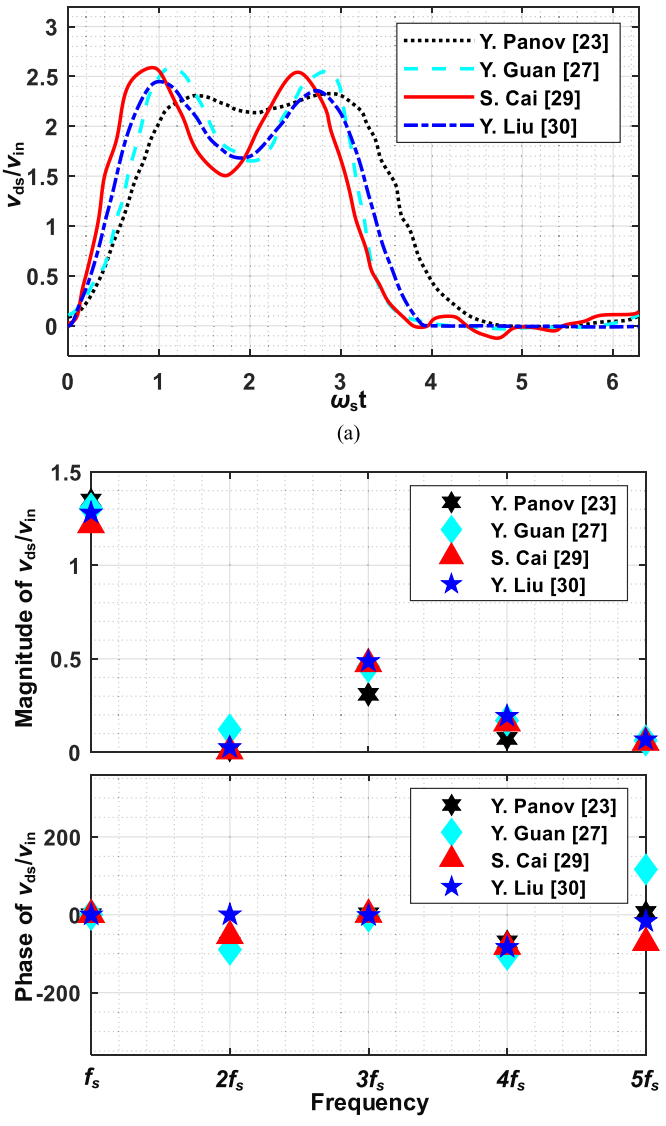

Fig. 2. Switch voltage waveforms and spectrums in published class Φ_2 inverters. (a) Waveforms of normalized $v_{\rm ds}$. (b) Spectrums of normalized $v_{\rm ds}$.

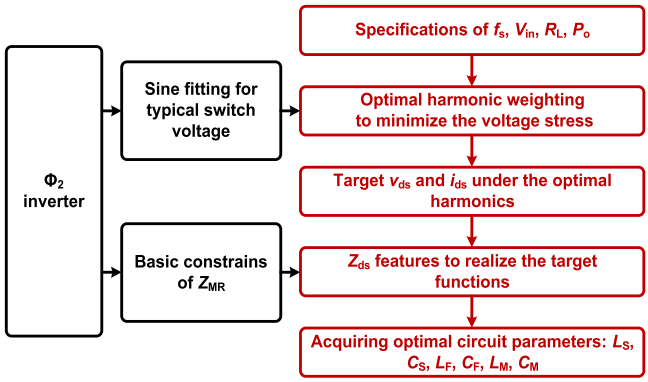

Fig. 3. Target function design for class Φ_2 inverter.

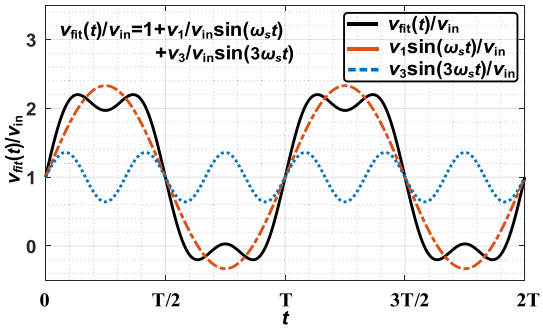

Fig. 4. Fitted switching node voltage and its harmonics.

TABLE I
RELATIVE ERROR OF SINE FITTING

Prototypes	Relative error
Y. Panov [23]	0.8%
Y. Guan [27]	3.8%
S. Cai [29]	3.3%
Y. Liu [30]	1.1%

III. OPTIMAL HARMONIC WEIGHTING AND TARGET FUNCTION DESIGN STRATEGY TO MINIMIZE THE VOLTAGE STRESS

To minimize the voltage stress and simplify the design procedures, a target function design strategy is proposed based on optimal harmonic weighting. The overall design procedure is shown in Fig. 3. First, optimal harmonic weighting to minimize the voltage stress is derived through sine fitting of typical switch voltage. To achieve the weighting, the target switch voltage/current (i.e., $v_{\rm ds,tag}$ and $i_{\rm ds,tag}$) are calculated by modeling the power switch as a voltage source. Furthermore, combining basic constrains of the resonant tank ($Z_{\rm MR}$), features of switching node impedance ($Z_{\rm ds}$) are derived to realize the target functions. Finally, the optimal circuit parameters are straightforwardly calculated.

A. Sine Fitting of the Switch Voltage

According to the spectrum in Fig. 2(b), the switch voltage is mainly composed of the fundamental and third harmonics. With near symmetrical switch voltage, the fundamental and the third harmonics should keep in phase. Therefore, the switch voltage can be sine fitted as shown in Fig. 4, where $\omega_s = 2\pi f_s$ represents the switching frequency and $T = 2\pi/\omega_{\rm s}$.

Furthermore, waveforms in Fig. 2(a) are fitted with different weightings. The relative error is calculated by

$$\text{err} = \frac{\int_0^T \left(v_{\rm ds}(t) - v_{\rm fit}(t)\right)^2 dt}{\int_0^T v_{\rm ds}^2(t) dt} \tag{4}$$

where $v_{\rm ds}(t)$ is the original switch voltage, and $v_{\rm fit}(t)$ is the fitted $v_{\rm ds}$ waveform. As given in Table I, the sine fitting for typical switch voltage induces relatively small error.

Since the sine fitting error for typical switch voltage is small, the switch voltage can be approximated as

$$v_{\rm ds}(t) \approx v_{\rm in} + v_1 \sin(\omega_s t) + v_3 \sin(3\omega_s t) \tag{5}$$

where v_1 and v_3 are the magnitude of the fundamental and third harmonics. The average value of (5) is $v_{\rm in}$, which is consistent with voltage-second balancing of L_F.

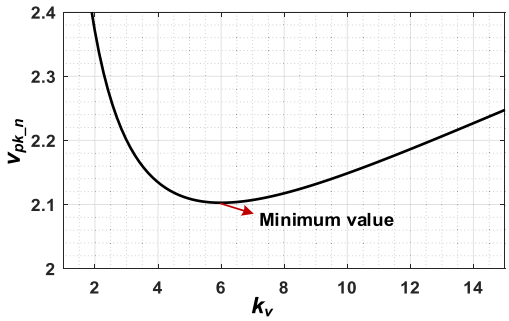

Fig. 5. Typical switch voltage and its harmonics.

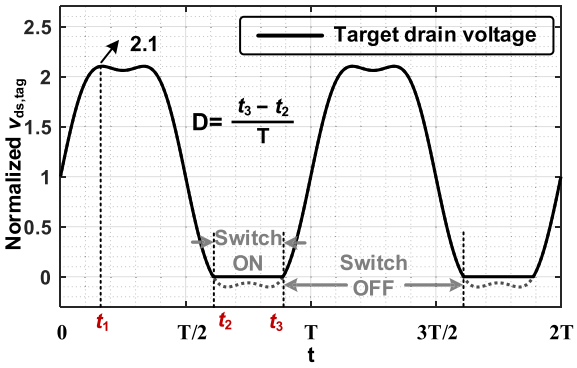

Fig. 6. Target switch voltage to minimize the voltage stress.

B. Optimal Harmonic Weighting to Minimize the Voltage Stress

In order to minimize the voltage stress, optimal values of v_1 and v_3 are derived as follows. By setting derivative of $v_{\rm ds}$ as zero, peak value of $v_{\rm ds}$ ($v_{\rm pk}$) is calculated. The derivative is given by

$$v'_{\rm ds}(t) = v_1\omega_s\cos(\omega_s t) + 3v_3\omega_s\cos(3\omega_s t). \tag{6}$$

By setting (6) as zero, the time when $v_{\rm ds}$ reaches its maximum value is derived as

$$\omega_s t_1 = \arccos\left(\sqrt{\frac{3}{4} - \frac{v_1}{12v_3}}\right). \tag{7}$$

Substituting (7) into (5), the normalized $v_{\rm pk}$ is calculated as

$$v_{\rm pk\_n} = \frac{v_{\rm pk}}{v_{\rm in}} = 1 + \frac{v_1}{v_{\rm in}}\left[\frac{1}{3} + \frac{1}{k_v}\right]\sqrt{1 + \frac{1}{3}k_v} \tag{8}$$

where $k_v = v_1/v_3$. Variation of $v_{\rm pk\_n}$ with k_v is plotted in Fig. 5.

To find the minimal value of $v_{\rm pk\_n}$, derivative of (8) with respect to k_v is calculated as

$$\frac{\partial v_{\rm pk\_n}}{\partial k_v} = \frac{v_1}{6v_{\rm in}k_v^2\sqrt{9+3k_v}}\left(-18 - 3k_v + k_v^2\right). \tag{9}$$

Setting (9) as 0 derives $k_v = 6$, where $v_{\rm pk\_n}$ achieves its minimal value. Furthermore, values of v_1 and v_3 are given by $v_1 = 4v_{\rm in}/\pi$ and $v_3 = v_1/k_v = 2v_{\rm in}/3\pi$, where v_1 is the typical value under fundamental wave approximation. With $k_v = 6$, the target $v_{\rm ds}$ to minimize voltage stress is plotted in Fig. 6. The duty ratio is determined by zero-crossing point of the target drain voltage (t_2 and t_3), as shown in Fig. 6. Values of t_2 and t_3 are calculated by solving (5) with $v_{\rm ds}(t) = 0$, and the results are given by (10). Then, the duty ratio is calculated as $D = (t_3\text{-}t_2)/\mathrm{T}$

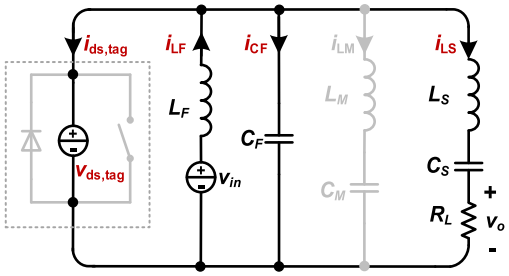

Fig. 7. Equivalent voltage source model for class Φ_2 inverter.

$$\begin{cases} t_2 = \frac{\pi}{\omega_s} \\ +\frac{1}{\omega_s}\mathrm{asin}\left(\sqrt{\frac{[v_1+3v_3]}{3v_3}}\sin\left(\frac{1}{3}\mathrm{asin}\left(\frac{3v_{in}}{[v_1+3v_3]\sqrt{\frac{v_1+3v_3}{3v_3}}}\right)\right)\right) \\ t_3 = \frac{2\pi}{\omega_s} \\ -\frac{1}{\omega_s}\mathrm{asin}\left(\sqrt{\frac{[v_1+3v_3]}{3v_3}}\sin\left(\frac{1}{3}\mathrm{asin}\left(\frac{3v_{in}}{[v_1+3v_3]\sqrt{\frac{v_1+3v_3}{3v_3}}}\right)\right)\right) \end{cases}. \tag{10}$$

C. Target Functions of V_{ds} and I_{ds} Under the Optimal Harmonics

With the derived values of v_1 and v_3, the target switch voltage is given by

$$v_{\rm ds,tag}(t) \approx v_{\rm in}\left(1 + \frac{4}{\pi}\sin(\omega_s t) + \frac{2}{3\pi}\sin(3\omega_s t)\right). \tag{11}$$

When the harmonic magnitudes equal to the derived values, the sine fitting error is small as described in Section III-A. Therefore, the switch is modeled as a voltage source, and the circuit is simplified as a linear network in Fig. 7.

Furthermore, with $v_{\rm ds,tag}$, the branch currents ($i_{\rm LF}$, $i_{\rm CF}$, $i_{\rm LS}$, $i_{\rm LM}$) are derived as

$$\begin{cases} i_{\rm LF}(t) = \frac{1}{L_F}\int v_{\rm in} - v_{\rm ds,tag}(t)dt \\ = \frac{4v_{\rm in}}{\pi\omega_s L_F}\cos(\omega_s t) + \frac{2v_{\rm in}}{9\pi\omega_s L_F}\cos(3\omega_s t) + \overline{i_{\rm ds,tag}} \\ i_{\rm CF}(t) = C_F\frac{dv_{\rm ds}(t)}{dt} = \frac{4v_{\rm in}C_F\omega_s}{\pi}\cos(\omega_s t) \\ +\frac{2v_{\rm in}C_F\omega_s}{\pi}\cos(3\omega_s t) \\ i_{\rm LS}(t) = \frac{4v_{\rm in}}{\pi|Z_L(j\omega_s)|}\sin(\omega_s t - \angle Z_L(j\omega_s)) \\ +\frac{2v_{\rm in}}{3\pi|Z_L(j\omega_s)|}\sin(3\omega_s t - \angle Z_L(j3\omega_s)) \\ i_{\rm LM} = I_2\sin(2\omega_s t) \end{cases} \tag{12}$$

where $\overline{i_{\rm ds,tag}}$ is the average value of $i_{\rm ds,tag}(t)$, I_2 is the magnitude the resonant current in L_M-C_M branch, which equals the peak value of $i_{\rm LF}$(t)-$i_{\rm CF}$(t)-$i_{\rm LS}$(t) during switch OFF. $Z_L(j\omega)$ is the impedance of the load network, which is given by

$$Z_L(j\omega) = \frac{-\omega^2 L_S C_S + j\omega R_L C_S + 1}{j\omega C_S}. \tag{13}$$

With (12), $i_{\rm ds,tag}(t)$ is approximated as

$$\begin{aligned} &i_{\rm ds,tag}(t) = i_{\rm LF}(t) - i_{\rm CF}(t) - i_{\rm LS}(t) \\ &\approx \overline{i_{\rm ds,tag}} + I_1\cos(\omega_s t) - I_3\cos(3\omega_s t) \end{aligned} \tag{14}$$

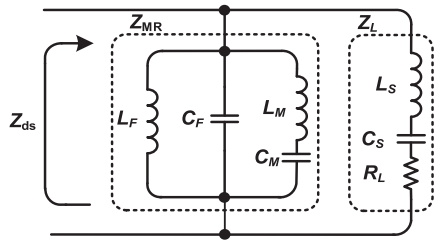

Fig. 8. Impedance network of the switching node.

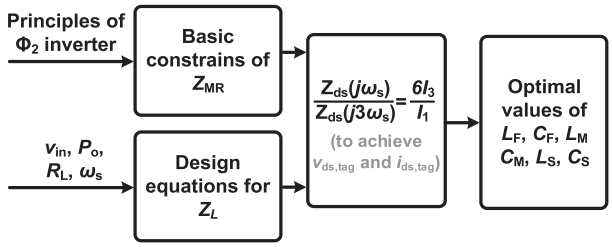

Fig. 9. Design procedures to realize the target functions.

where I_1, I_3 are given by (15). (Detailed derivations are given in Appendix A). The current of L_M -C_M branch (i_{LM}) is neglected in (14) since it only contains the second harmonic, which has little effect on the switch voltage waveform

$$\begin{cases} I_1 = \frac{4v_{\mathrm{in}}}{\pi}\sqrt{\left[\frac{1}{\omega_s L_F} - C_F\omega_s + \frac{1}{|Z_L(j\omega_s)|}\sin(\angle Z_L(j\omega_s))\right]^2 + \left[\frac{\cos(\angle Z_L(j\omega_s))}{|Z_L(j\omega_s)|}\right]^2} \\ I_3 = \frac{2v_{\mathrm{in}}}{3\pi}\sqrt{\left[\frac{1}{3\omega_s L_F} - 3C_F\omega_s + \frac{1}{|Z_L(j3\omega_s)|}\sin(Z_L(j3\omega_s))\right]^2 + \left[\frac{\cos(Z_L(j3\omega_s))}{|Z_L(j3\omega_s)|}\right]^2} \end{cases} \tag{15}$$

With above analytical expressions, root mean square (RMS) currents of L_F, L_M, L_S, and power switch is calculated by (16), and the efficiency is calculated by (17), where R_{LF}, R_{LS}, R_{LM} are the parasitic resistance of L_F, L_S, L_M, and R_{dson} is on resistance of the power switch. By reducing RMS values of branch currents, the total loss can be reduced and overall efficiency can be improved

$$\begin{cases} I_{\mathrm{LF,RMS}} = \sqrt{\left(\overline{i_{\mathrm{ds,tag}}}\right)^2 + \frac{1}{2}\left(\frac{4v_{\mathrm{in}}}{\pi\omega_s L_F}\right)^2 + \frac{1}{2}\left(\frac{2v_{\mathrm{in}}}{9\pi\omega_s L_F}\right)^2} \\ I_{\mathrm{LS,RMS}} = \sqrt{\frac{1}{2}\left(\frac{4v_{\mathrm{in}}}{\pi|Z_L(j\omega_s)|}\right)^2 + \frac{1}{2}\left(\frac{2v_{\mathrm{in}}}{3\pi|Z_L(j\omega_s)|}\right)^2} \\ I_{\mathrm{LM,RMS}} = I_2/\sqrt{2} \\ I_{\mathrm{ds,RMS}} = \sqrt{\left(\overline{i_{\mathrm{ds,tag}}}\right)^2 + \frac{1}{2}{I_1}^2 + \frac{1}{2}{I_3}^2} \end{cases} \tag{16}$$

$$\begin{cases} \eta = \frac{P_O}{P_{\mathrm{IN}}} = \frac{P_O}{P_{\mathrm{Loss}}+P_O} \\ P_{\mathrm{Loss}} = {I^2}_{\mathrm{LF,RMS}}R_{LF} + {I^2}_{\mathrm{LS,RMS}}R_{\mathrm{LS}} \\ +{I^2}_{\mathrm{LM,RMS}}R_{\mathrm{LM}} + {I^2}_{\mathrm{ds,RMS}}R_{dson} \end{cases}. \tag{17}$$

Finally, analytical expressions of switch voltage and current are summarized as

$$\begin{cases} v_{\mathrm{ds,tag}}(t) \approx v_{\mathrm{in}}\left(1 + \frac{4}{\pi}\sin(\omega_s t) + \frac{2}{3\pi}\sin(3\omega_s t)\right) \\ i_{\mathrm{ds,tag}}(t) \approx \overline{i_{\mathrm{ds,tag}}} + I_1\cos(\omega_s t) - I_3\cos(3\omega_s t) \end{cases}. \tag{18}$$

With $v_{\mathrm{ds,\,tag}}$ and $i_{\mathrm{ds,\,tag}}$, design equations for the resonant tank will be derived to minimize the switch voltage stress and provide a straightforward design procedure.

D. Resonant Tank Design to Realize the Target Functions

In this part, design equations to achieve $v_{\mathrm{ds,tag}}$ and $i_{\mathrm{ds,tag}}$ are provided to calculate the circuit parameters. As shown in Fig. 8, the impedance of switching node is $Z_{\mathrm{ds}} = Z_{\mathrm{MR}}\|Z_L$. While Z_L is the output branch that filters the high order harmonics in load, Z_{MR} is the main resonant tank to shape v_{ds}.

The design procedure is shown in Fig. 9. Basic constrains of Z_{MR} are derived according to principles of class Φ_2 inverter,

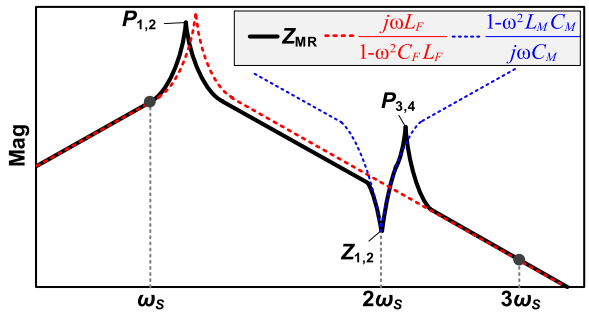

Fig. 10. Typical magnitude frequency response of Z_{MR}.

while Z_{L} is designed with the power specifications (i.e., v_{in}, P_o, R_L, ω_s). Furthermore, design equations to achieve $v_{\mathrm{ds,tag}}$ are provided to calculate the optimal circuit parameters.

1) Basic Constrains of Z_{MR}: The main resonant tank involves two parallel branches, i.e., L_F-C_F and L_M-C_M branches. The impedance is calculated by

$$\begin{aligned} Z_{\mathrm{MR}}(j\omega) &= \frac{j\omega L_F}{1-\omega^2 C_F L_F}\|\frac{1-\omega^2 L_M C_M}{j\omega C_M} \\ &\approx \frac{j\omega L_F(1-\omega^2 L_M C_M)}{[1-\omega^2(L_F C_F + L_F C_M)][1-\omega^2(L_M C_F C_M)/(C_F+C_M)]}. \end{aligned} \tag{19}$$

Furthermore, typical bode plot of Z_{MR} is shown in Fig. 10. Expansion of (19) consists a pair of conjugate zeros ($Z_{1,2}$) and two pairs of conjugate poles (lower poles $P_{1,2}$, higher poles $P_{3,4}$). L_M-C_M branch determines frequency of the conjugate zeros, which is set at $2\omega_{\mathrm{s}}$ to eliminate the second harmonic voltage. Two pairs of conjugate poles locate near ω_{s} and $3\omega_{\mathrm{s}}$, which generate the fundamental and third harmonics.

The impedance magnitude of Z_{MR} should be as high as possible, so that to reduce the circling currents of L_M-C_M, L_F-C_F branches. Therefore, combining with the basic principles of class Φ_2 inverter, Z_{MR} should fulfill the following basic constrains.

1) At $2\omega_s$, $|Z_{\mathrm{MR}}|$ should be 0 so that to absorb the second harmonic.
2) Z_{MR} should be inductive at ω_s and capacitive at $3\omega_s$, so that to keep the harmonics in phase.
3) At ω_s, $|Z_{\mathrm{MR}}|$ should be as high as possible so that to reduce the circling loss and improve power efficiency.

In order to meet constrain (a), $Z_{1,2}$ should be set at the second harmonic frequency, i.e.,

$$Z_{1,2} = 2\omega_s = \frac{1}{2\pi\sqrt{L_M C_M}} \tag{20}$$

so that $|Z_{\mathrm{MR}}|$ at $2\omega_s$ is zero and the second harmonic voltage is absorbed to reduce the voltage stress.

TABLE II
PARAMETER TUNINGS OF CLASS Φ_2 INVERTER

	Proposed method (Calculated values)	Conventional method (Calculated/adjusted values)
L_S	145nH	152nH / 152nH
L_F	135nH	80nH / 62nH
L_M	430nH	55nH / 55nH
C_S	4nF	4nF / 4nH
C_F	200pF	200pF / 290pF
C_M	20pF	156pF / 155pF
R_L	25Ω	25Ω / 25Ω

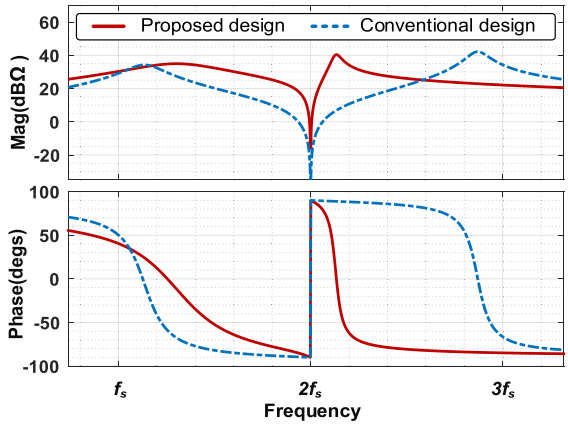

Fig. 11. Characteristics of $Z_{\rm ds}$ with different design methods.

To meet constrain (b), $P_{1,2}$ and $P_{3,4}$ should be located within $(\omega_{\rm s}, 2\omega_{\rm s})$ and $(2\omega_{\rm s}, 3\omega_{\rm s})$, respectively. According to constrain (c), $P_{1,2}$ should locate near $\omega_{\rm s}$ to reduce the circling loss. Considering component tolerances, the poles are set at $1.1\omega_{\rm s}$, i.e.,

$$P_{1,2} = 1.1\omega_s \approx \frac{1}{2\pi\sqrt{L_F(C_F + C_M)}}. \tag{21}$$

Furthermore, the impedance of L_M-C_M branch should be high, so that to reduce the circling loss of L_M-C_M branch. Specifically, the series impedance of L_M-C_M branch beyond $2\omega_{\rm s}$ should be much higher than parallel impedance of L_F-C_F branch. To increase the L_M-C_M impedance and prevent the fundamental and third harmonic currents flowing through L_M-C_M branch, C_M should be much smaller than C_F. In this design, C_M is set as $0.1C_F$ (Detailed considerations for ratio of C_F and C_M are given in Appendix B), i.e.,

$$C_M = 0.1C_F. \tag{22}$$

With above design equations, circling currents of the resonant tank can be reduced, which improves the overall power efficiency.

2) Design Equations of the Output Branch: The output branch is designed according to specifications of the inverter. As a dc blocking capacitor (relatively large), C_S is near shorted at high frequency. Therefore, transfer function from $v_{\rm ds}$ to v_o approximates

$$\left|\frac{v_o(j\omega)}{v_{\rm ds}(j\omega)}\right| \approx \frac{R_L}{|R_L + j\omega L_S|}. \tag{23}$$

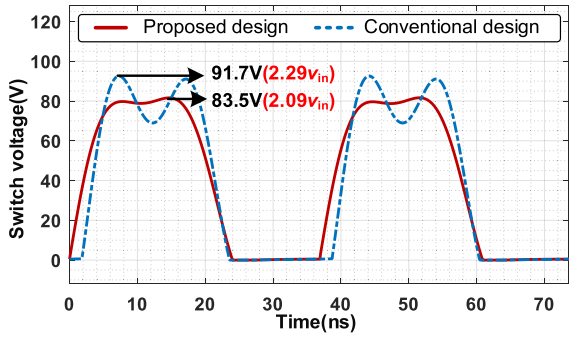

Fig. 12. Simulated $v_{\rm ds}$ waveforms.

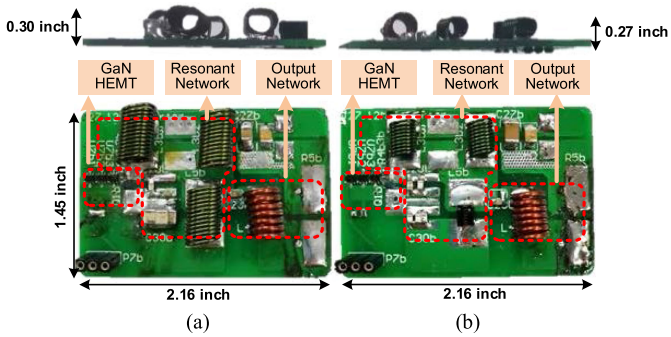

Fig. 13. Class Φ_2 inverter prototypes. (a) Proposed design. (b) Conventional design.

TABLE III
IMPLEMENTATION OF THE CLASS Φ_2 INVERTER

	Proposed method	Conventional method [27, 29]
L_S	150nH (6 turns of 1.3mm diameter copper wire with inner diameter 4.6mm)	150nH (6 turns of 1.3mm diameter copper wire with inner diameter 4.6mm)
L_F	143nH (3 2929SQ-431 in parallel)	60nF (3 2222SQ-181 in parallel)
L_M	430nH (2929SQ-431GEC)	56nH (1812SMS-56NGLC)
C_S	4.7nF	4.7nF
C_F	10pF+ 190pF ($C_{\rm OSS}$)	110pF+190pF ($C_{\rm OSS}$)
C_M	20pF	153pF
$C_{\rm in}$	4.7μF	4.7μF
R_L	2.5~25Ω	2.5~25Ω
Switch	EPC2019	EPC2019
Driver	3 NC7WZ17 in parallel	3 NC7WZ17 in parallel

With $v_{\rm ds,tag}(j\omega_s) = 4v_{\rm in}/\pi$ and $v_{\rm ds,tag}(j3\omega_s) = 2v_{\rm in}/3\pi$, the output power is given as

$$P_o = \frac{1}{2R_L}\left(\frac{4v_{\rm in}}{\pi}\frac{R_L}{|R_L + j\omega_s L_S|}\right)^2 + \frac{1}{2R_L}\left(\frac{2v_{\rm in}}{3\pi}\frac{R_L}{|R_L + j3\omega_s L_S|}\right)^2. \tag{24}$$

Substituting $v_{\rm in}$, P_o, R_L, ω_s into (24) derives value of L_S directly.

3) Design Equation to Achieve Optimal Harmonic Weighting: Furthermore, to realize $v_{\rm ds,tag}$ and $i_{\rm ds,tag}$ in (18), magnitude

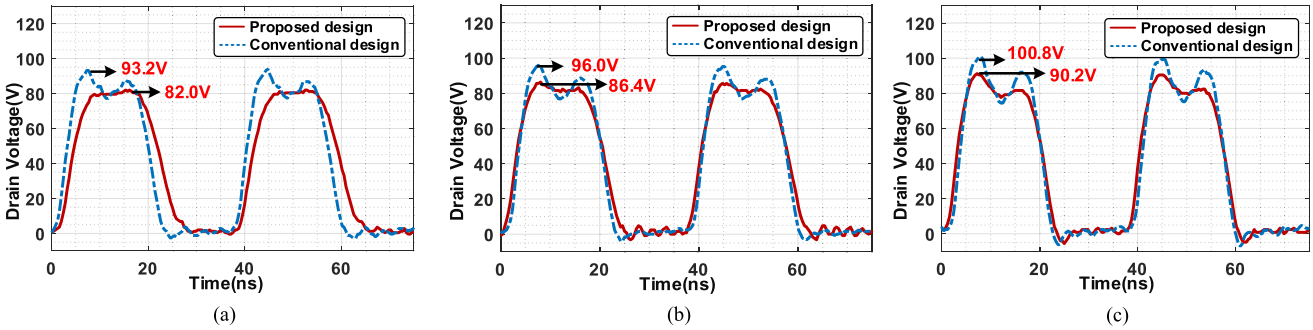

Fig. 14. Switch voltage under different load resistance when $v_{\rm in} = 40$ V. (a) $R_L = 25\ \Omega$. (b) $R_L = 16\ \Omega$. (c) $R_L = 5\ \Omega$.

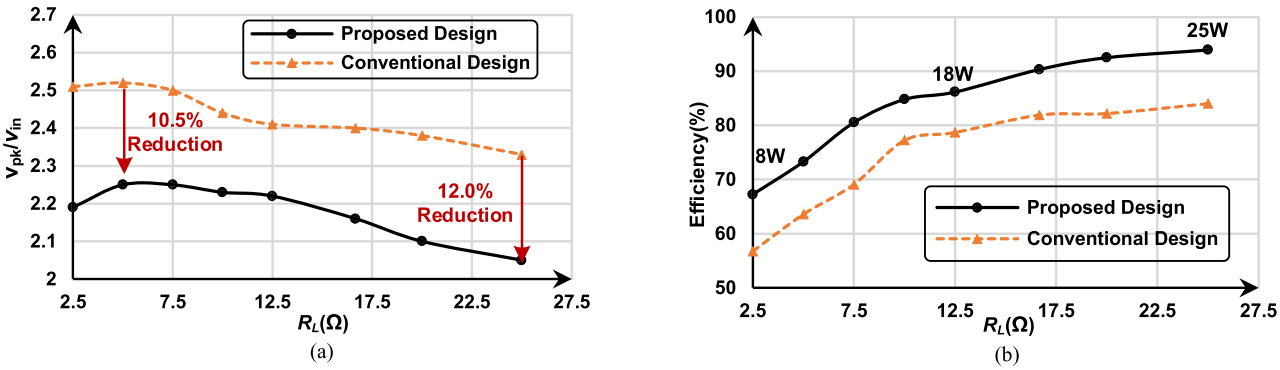

Fig. 15. Comparisons under different loads. (a) Normalized $v_{\rm pk}$ under different load. (b) Efficiency under different loads.

of the switching node impedance is given by

$$\frac{|Z_{\rm ds}(j\omega_s)|}{|Z_{\rm ds}(j3\omega_s)|} = 6\frac{I_3}{I_1} \tag{25}$$

where $Z_{\rm ds}(j\omega_s)$ and $Z_{\rm ds}(j3\omega_s)$ are the impedance at fundamental and third harmonic frequencies, respectively. Finally, combining (20)–(22), (24), and (25), the optimal circuit parameters are directly calculated.

IV. Simulations

Simulations are presented to verify effectiveness of the proposed method. Specifications of the class Φ_2 inverter are the same as experiments (i.e., $f_s = 27.12$ MHz, $v_{\rm in} = 40$V, $R_L = 25\ \Omega$, $P_o = 25$ W). The calculated results with conventional and the proposed methods are given in Table II. Comparatively, the proposed method acquires larger resonant inductor L_M, L_F and smaller capacitor C_M, C_F to obtain higher characteristic impedance.

As shown in Fig. 11, magnitude of $Z_{\rm ds}$ around $2\omega_{\rm s}$ with the proposed method is higher than that with conventional design, which implies smaller circling loss in L_M-C_M branch and higher efficiency. Furthermore, the proposed design achieves the same phase at $\omega_{\rm s}$ with smaller C_F and larger L_F, which implies that the circling current to realize ZVS is reduced with the proposed method.

Circuit simulations are carried out in MATLAB/Simulink. The simulated $v_{\rm ds}$ waveforms of both conventional design and proposed design are shown in Fig. 12. Compared with conventional design, the proposed method reduces the peak switch voltage from 91.7V ($2.29v_{\rm in}$) to 83.5V ($2.09v_{\rm in}$).

V. Experiments

Experiments are carried out on class Φ_2 inverter prototypes with conventional and the proposed methods, which are designed as the inverter stage of a WPT system. The switching frequency is selected as 27.12MHz to meet RF emission limitations of electromagnetic compatibility standards CISPR-11. Main specifications of the inverters are given in Table III, and the prototypes are shown in Fig. 13. The power switch is a GaN HEMT from EPC (EPC2019). The gate driver is realized with three high-speed buffers NC7WZ17, since commercial gate driver IC cannot provide reliable gate drive voltage at VHF. The buffer ICs is placed as closely as possible to the GaN HEMT, so that to reduce parasitic inductance of PCB trace. The resonant inductors are air core inductor from Coilcraft, and the resonant capacitors are realized using multilayer ceramic capacitors with C0G dielectric material.

A. Comparisons Under Different Loads

In order to compare the designs with different loads, the measured $v_{\rm ds}$ are plotted by Fig. 14. When $R_L = 25\Omega$, the peak $v_{\rm ds}$ with conventional design is 93.2 V ($2.33v_{\rm in}$). Comparatively, the proposed design reduces the peak value to 82.0V ($2.05v_{\rm in}$), where a voltage reduction of 12.0% is achieved. When $R_L = 16\ \Omega$, the peak $v_{\rm ds}$ with conventional and proposed designs are 96.0

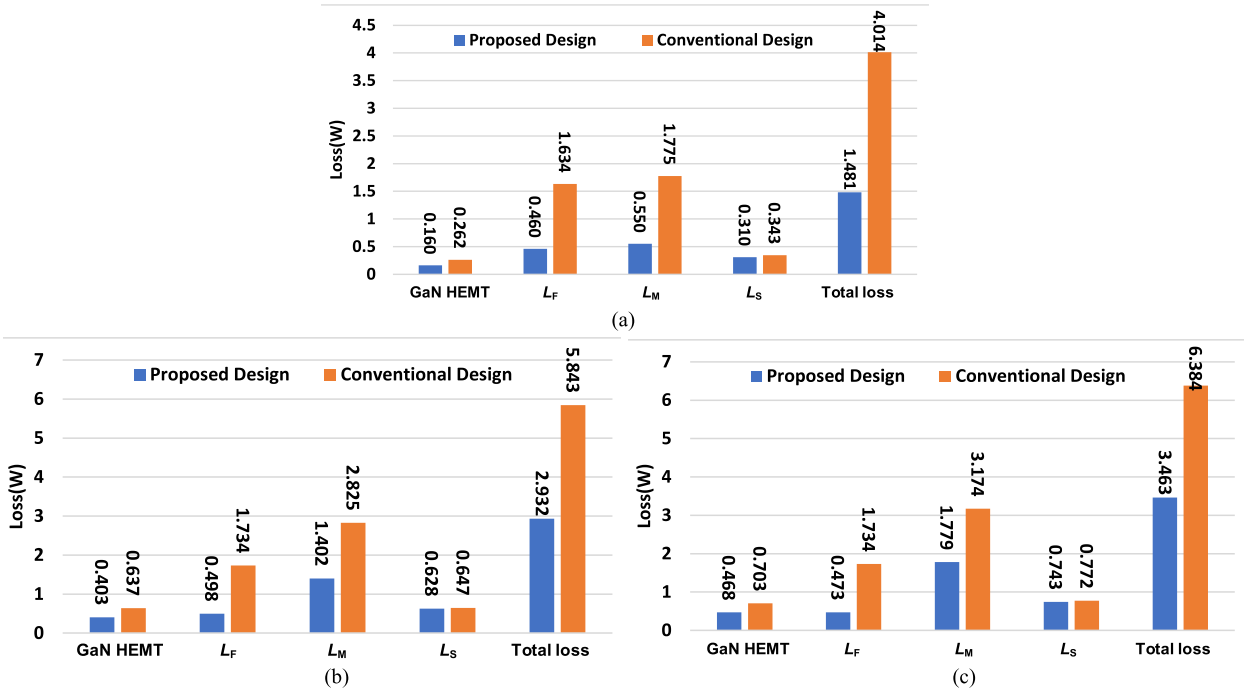

Fig. 16. Loss breakdown for the prototype. (a) 25 W. (b) 18 W. (c) 8 W.

V ($2.4v_{\rm in}$) and 86.4 V ($2.16v_{\rm in}$, reduced by 10%), respectively. When $R_L = 5\ \Omega$, the peak $v_{\rm ds}$ is 100.8 V ($2.52v_{\rm in}$) with conventional design and 90.2 V ($2.26v_{\rm in}$, reduced by 10.5%) with the proposed design.

The normalized peak $v_{\rm ds}$ with respect to load resistance is shown in Fig. 15(a). As R_L increases, the peak $v_{\rm ds}$ decreases with both designs, while the proposed design always reduces the value by more than 10%. Fig. 15(b) shows the drain efficiency change with respect to load resistance, which is defined as $P_o/P_{\rm dc\cdot in}$ [11]. The total efficiency is defined as $P_o/(P_{\rm dc\cdot in}+P_{\rm gate})$. With GaN HEMT, the estimated gate driver loss is less than 0.25 W. Therefore, the measured drain efficiency is very close to total efficiency. With the proposed design, the efficiency is improved by more than 7% in the whole range, and an efficiency of 93.6% is achieved at full load. The power density of proposed and conventional designs is 31.9 and 35.5 W/inch^3, respectively. Since the proposed method acquires larger inductors to reduce the circling current and improve power efficiency, the power density is slightly lower than conventional design.

Based on LTspice simulation, loss breakdown analysis for 8, 18, and 25 W are provided in Fig. 16 to explain how the efficiency is improved. Parasitic resistance of the inductors are measured with *LCR* meter and considered in the simulation. The power switch model used in the simulation is level-3 spice model provided by the manufacturer. With RMS currents of each branch and the parasitic resistance, losses of each component are calculated. Compared with conventional design, the proposed method significantly reduces the losses on L_F and L_M. The reason lies in the resonant network with increased impedance (i.e., larger inductance and smaller capacitance), which reduces the RMS value of circling currents. Under 25 W, the proposed design reduces the total loss from 4.014 to 1.481 W. Losses on L_F and L_M are significantly reduced. Whereas losses on $L_{\rm S}$ are close, since both designs have the same output network. Under 8 and 18 W, losses of L_F and L_M are also reduced, which improves power efficiency.

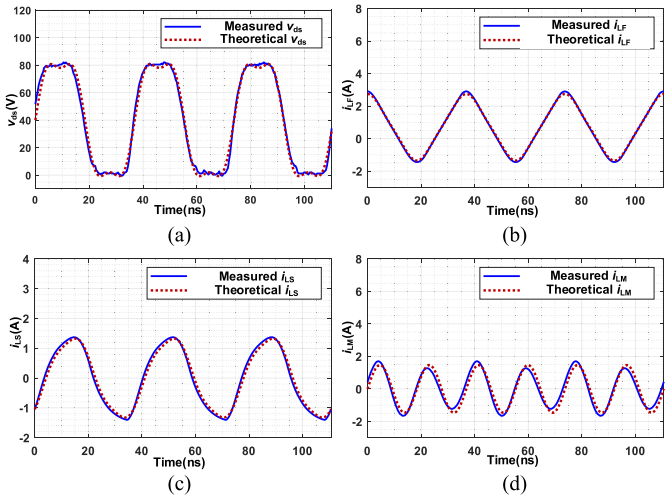

Fig. 17. Comparisons of experimental and theoretical waveforms. (a) Switch voltage. (b) Input current. (c) Output current. (d) Current through L_M-C_M.

Fig. 17 compares the theoretical and experimental waveforms when $v_{\rm in} = 40$ V, $R_L = 25\ \Omega$. The theoretical $v_{\rm ds}$ is based on (5), while the theoretical currents are calculated by substituting the parameters in Table III into (12). The theoretical waveforms match the experimental waveforms well, which demonstrate effectiveness of the proposed modeling method.

B. Comparisons Under Different Inputs

For both designs, the switching node voltages with $v_{\rm in} = 35$ V, $v_{\rm in} = 30$ V and $v_{\rm in} = 25$ V are given in Fig. 18. When

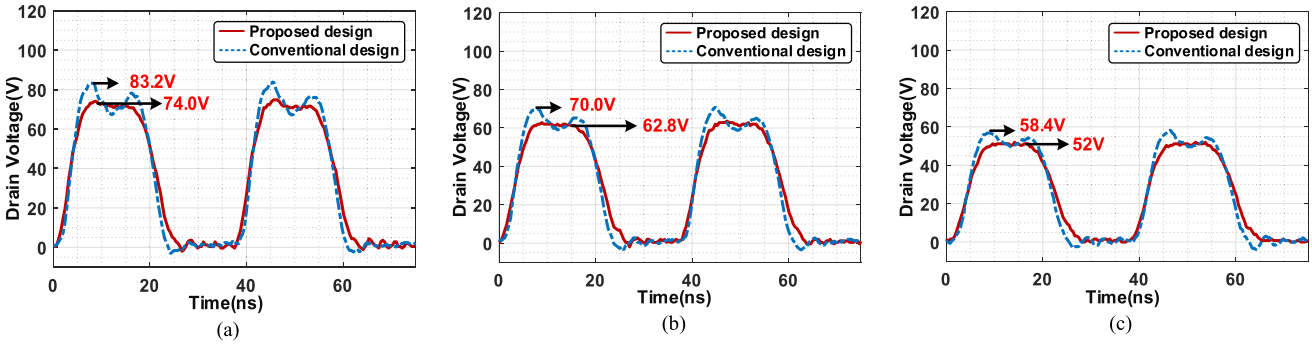

Fig. 18. Switch voltage under different input voltage when $R_L = 16\ \Omega$. (a) $v_{\rm in} = 35$ V. (b) $v_{\rm in} = 30$ V. (c) $v_{\rm in} = 25$V.

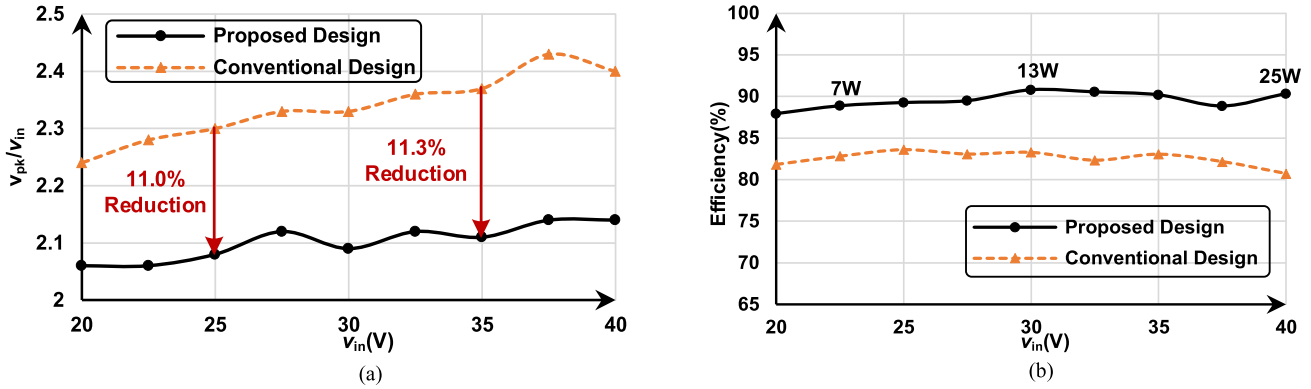

Fig. 19. Comparisons under different inputs. (a) Normalized $v_{\rm pk}$ under different inputs. (b) Efficiency under different inputs.

$v_{\rm in} = 35$ V, the peak $v_{\rm ds}$ with conventional design is 83.2 V ($2.38v_{\rm in}$), whereas the peak $v_{\rm ds}$ with the proposed design is 74.0 V ($2.11v_{\rm in}$, reduced by 11.3%). When $v_{\rm in} = 30$ V, the peak $v_{\rm ds}$ with conventional and the proposed designs are 70.0 V ($2.33v_{\rm in}$) and 62.8 V ($2.09v_{\rm in}$, reduced by 10.3%), respectively. When $v_{\rm in} = 25$V, the peak $v_{\rm ds}$ is 58.4 V ($2.34v_{\rm in}$) with conventional design and 52.0 V ($2.08v_{\rm in}$) with proposed design, and a reduction of 11.0% is achieved.

Fig. 19(a) shows the normalized peak $v_{\rm ds}$ with respect to input voltage. As the input voltage increases, the peak $v_{\rm ds}$ increases with both designs, while the proposed design always reduces the value by more than 9%. Fig. 19(b) shows the efficiency change with respect to input voltage. With the proposed design, the efficiency is improved by more than 6% in the whole range, and a peak efficiency of 90.9% is achieved.

To further verify effectiveness of the proposed target function design method, two additional design examples are presented, conventional designs are also realized for comparisons. Main specifications and results of the design examples are given in Table IV. The experimental results prove that the proposed design method reduces the switch voltage stress and improves the overall efficiency.

Comprehensive comparisions of different design methods are given in Table V. Compared with conventional method, scaning method and multiple harmonics design method, the propsoed target function method is straightforward, which does not require parameter tuning after design. Moreover, with the optimal harmonic weightings, the switch voltage stress is reduced.

TABLE IV
MAIN SPECIFICATIONS OF THE DESIGN EXAMPLES

	Second example of class Φ_2 inverter		Third example of class Φ_2 inverter	
	Proposed design	Conventional design	Proposed design	Conventional design
$v_{\rm in}$	60V	60V	40V	40V
P_o	40W	40W	25W	25W
F_s	27.12MHz	27.12MHz	13.56MHz	13.56MHz
R_L	25Ω	25Ω	25Ω	25Ω
L_S	200nH	200nH	305nH	305nH
L_F	168nH	72nH	252nH	123nH
L_M	527nH	61nH	790nH	92nH
C_S	4nF	4nH	4nF	4nH
C_F	163pF	250pF	430pF	470pF
C_M	16.3pF	141pF	43.4pF	375pF
Efficiency	89.50%	83.17%	85.03%	75.77%
$v_{\rm pk}/v_{\rm in}$	2.07	2.31	2.06	2.29

VI. CONCLUSION

This article proposes a target function design strategy based on harmonic weighting for VHF class Φ_2 inverter, which minimizes the switch voltage stress and reduces the circling losses. Fully quantitative analysis and straightforward design strategy for class Φ_2 inverter are provided. By quantitatively analyzing the influence of harmonic weightings on voltage stress and

TABLE V
COMPARISON WITH OTHER DESIGN METHODS

DESIGN METHOD		Switching frequency	Parameter tuning after design	v_{pk}/v_{in}
Proposed method	/	27.12MHz	No tuning	2.05~2.25
Conventional method	[27]	20MHz	Required	2.57
	[29]	4MHz	Required	2.53
Scanning method	[23]	30MHz	No tuning	2.35
	[30]	10MHz	No tuning	2.44
Multiple Harmonics method	[31]	1MHz	No tuning	2.54

efficiency, the optimal harmonic weightings are derived to minimize switch voltage stress. Then, by optimizing the impedance of the resonant tank, the proposed design method achieves the target harmonic weightings and reduces the circling losses. Experimental results demonstrate considerable improvement in voltage stress and efficiency under various working conditions. The proposed harmonic weighting and target function design method can be used to optimize the voltage stress and efficiency of class Φ_2 inverters or isolated dc–dc converters.

APPENDIX A

This appendix is provided to prove (14). According to (12), the power switch current $i_{\mathrm{ds,tag}}(t)$ is calculated as

$$\begin{aligned} i_{\mathrm{ds,tag}}(t) &= i_{\mathrm{LF}}(t) - i_{\mathrm{CF}}(t) - i_{\mathrm{LS}}(t) \\ &= \frac{4v_{\mathrm{in}}}{\pi\omega_s L_F}\cos(\omega_s t) + \frac{2v_{\mathrm{in}}}{9\pi\omega_s L_F}\cos(3\omega_s t) + \overline{i_{\mathrm{ds,tag}}} \\ &\quad - \frac{4v_{\mathrm{in}}C_F\omega_s}{\pi}\cos(\omega_s t) - \frac{2v_{\mathrm{in}}C_F\omega_s}{\pi}\cos(3\omega_s t) \\ &\quad - \frac{4v_{\mathrm{in}}}{\pi\left|Z_L(j\omega_s)\right|}\sin(\omega_s t - \angle Z_L(j\omega_s)) \\ &\quad - \frac{2v_{\mathrm{in}}}{3\pi\left|Z_L(j\omega_s)\right|}\sin(3\omega_s t - \angle Z_L(j3\omega_s)). \end{aligned} \tag{A1}$$

Then, (A1) is reorganized as

$$i_{\mathrm{ds,tag}}(t) = \overline{i_{\mathrm{ds,tag}}} + I_1\cos(\omega_s t + \theta_1) - I_3\cos(3\omega_s t - \theta_3) \tag{A2}$$

where i_1, i_3, θ_1, θ_3 are calculated as

$$I_1 = \frac{4v_{\mathrm{in}}}{\pi}\sqrt{\left(\frac{1}{\omega_s L_F} - C_F\omega_s + \frac{1}{|Z_L(j\omega_s)|}\sin(\angle Z_L(j\omega_s))\right)^2 + \left(\frac{\cos(\angle Z_L(j\omega_s))}{|Z_L(j\omega_s)|}\right)^2}$$

$$I_3 = \frac{2v_{\mathrm{in}}}{3\pi}\sqrt{\left(\frac{1}{3\omega_s L_F} - 3C_F\omega_s + \frac{1}{|Z_L(j3\omega_s)|}\sin(\angle Z_L(j3\omega_s))\right)^2 + \left(\frac{\cos(\angle Z_L(j3\omega_s))}{|Z_L(j3\omega_s)|}\right)^2}$$

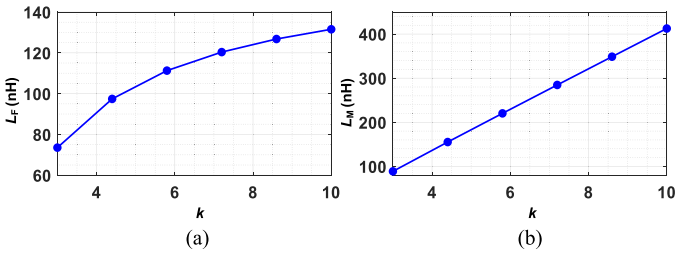

Fig. 20. Calculated values of L_F and L_M under different k. (a) L_F with respect to k. (b) L_M with respect to k.

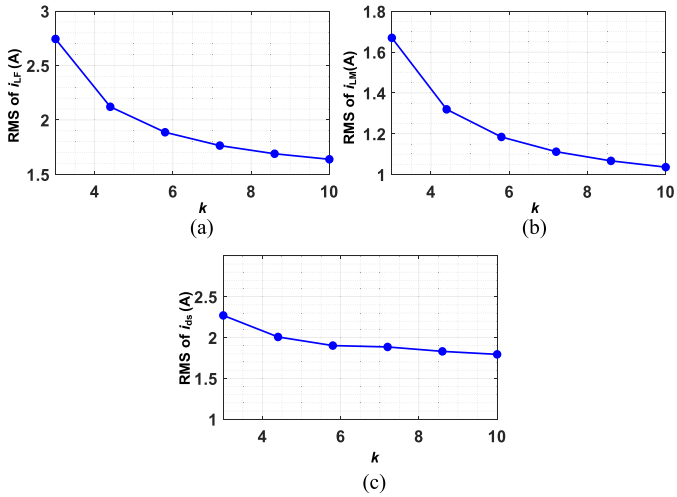

Fig. 21. RMS currents in L_F, L_M, and the power switch under different k (a) RMS current in L_F. (b) RMS current in L_M. (c) RMS current in the power switch.

$$\theta_1 = \mathrm{asin}\left[\cos(\angle Z_L(j\omega_s))\right] = \frac{\pi}{2} - \angle Z_L(j\omega_s)$$
$$\theta_3 = \mathrm{asin}\left[\cos(\angle Z_L(j3\omega_s))\right] = \frac{\pi}{2} - \angle Z_L(j3\omega_s). \tag{A3}$$

For reasonable load range of class Φ_2 inverter, θ_1 and θ_3 are small and neglectable, therefore, the power switch current is approximated as

$$i_{\mathrm{ds,tag}}(t) = \overline{i_{\mathrm{ds,tag}}} + I_1\cos(\omega_s t) - I_3\cos(3\omega_s t). \tag{A4}$$

APPENDIX B

This appendix provides detailed considerations for the ratio of C_F and C_M, which is denoted as k, i.e.,

$$C_M = \frac{1}{k}C_F. \tag{A5}$$

Combining (A5) with the proposed design equations i.e., (20), (21), and (25), the four parameters $<L_F, L_M, C_F, C_M>$ are calculated under different k. Variations of L_F and L_M with k are plotted in Fig. 20 . Obviously, a high k can effectively increase values of L_F and L_M, which reduce unnecessary cycling losses in the resonant tank.

Furthermore, RMS currents in L_F, L_M and the power switch under different k are given by Fig. 21. With higher k, RMS values of i_{LF} and i_{LM} reduce significantly, which indicates lower circling losses and higher power efficiency.

Based on above results, increasing k can effectively reduce the circling losses. Therefore, in the proposed method, the ratio of C_F and C_M is set to 10 to reduce circling losses, i.e.,

$$C_M = \frac{1}{10} C_F = 0.1 C_F. \tag{A6}$$

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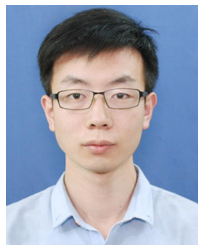


Desheng Zhang received the B.Eng. degree in 2018 from the School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in microelectronics.

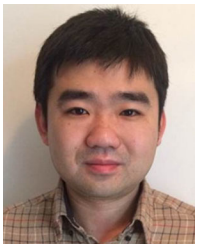
His research interests include the design and control of very high frequency power converters.

Liangliang Lu received the B.Eng. and M.S. degrees from Beijing Institute of Technology, Beijing, China, in 2007 and 2010, respectively. He is currently working toward the Ph.D. degree in microelectronics with the School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, China.

From 2010 to 2015, he was a General Designer with General Design Department, China Academy of Launch Vehicle Technology. Since then, he was a General Designer with the Lunar Exploration and Space Engineering Center, State Administration of Science, Technology and Industry for National Defense, Arlington, VA, USA. His current research interests include modeling and control of power converters.

Qiaoling Tong (Member, IEEE) received the B.Eng. and Ph.D. degrees from the School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, China, in 2003 and 2010, respectively.

From 2008 to 2010, he was a Research Scholar with the Department of Electrical Engineering and Computer Science, University of California, Irvine, CA, USA. He is currently a Professor with the School of Optical and Electronic Information, Huazhong University of Science and Technology. His current research interests include sensorless control of dc–dc converters and VLSI implementation of intelligent algorithms.



Qiao Zhang (Member, IEEE) received the B.Eng., M.Eng., and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 2003, 2006, and 2010, respectively.

From 2008 to 2009, he was a Visiting Scholar with the Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield, U.K. From 2009 to 2016, he was a Research Engineer with IMRA Europe U.K. Research Centre. He is currently an Associate Professor with the School of Automation, Wuhan University of Technology, Wuhan, China. His research interests include the power electronics system design and control, such as dc–dc converter sensorless control strategies, electrical machine parameters estimation by control theory, system nonlinearity compensation for dc–dc converters and voltage source inverters.

Run Min (Member, IEEE) received the B.Eng. degree from the School of Software and Microelectronics, Northwestern Polytechnical University, Xi'an, China, in 2010, and the Ph.D. degree from the School of Optical and Electronic Information, Huazhong University of Science and Technology (HUST), Wuhan, China, in 2016.

He is currently an Associate Professor with HUST. His research interests include modeling, analysis, and control of power electronic systems.

Han Peng (Senior Member, IEEE) received the B.S. degree from Southeast University, Nanjing, China, and the Ph.D. degree from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2006 and 2011, respectively, all in electrical engineering.

From 2011 to 2017, she was a Lead Electrical Engineer with the Global Research Center of General Electric Company, Niskayuna, NY, USA. Since 2018, she has been a Professor with the Huazhong University of Science and Technology, Wuhan, China. She has authored or coauthored more than 20 papers in refereed journals and international conference proceedings. She has four U.S. patent and two Chinese patents. Her research covers various different applications, as energy harvesting, communication power, healthcare electronics, more electrical aircraft systems, and electric vehicles. Her research interests include high frequency, high power density power management IC design, high frequency supply modulators, and applications of wide bandgap power devices.

Dr. Peng has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2017. She was an Associate Technical Program Chair for 2019 IEEE Energy Conversion Congress and Exposition.

Xuecheng Zou (Senior Member, IEEE) received the Ph.D. degree from the Department of Electronic Science and Technology, Huazhong University of Science and Technology, Wuhan, China, in 1993.

He is currently a Professor with the School of Optical and Electronic Information, Huazhong University of Science and Technology. His main research areas include the dc–dc converters design and the Internet of things.