GaN-Based Multichip Half-Bridge Power Module Integrated on High-Voltage AlN Ceramic Substrate

Carsten Kuring, Mihaela Wolf, Xiaomeng Geng, Oliver Hilt, Jan Böcker, Joachim Würfl, *Member, IEEE*, and Sibylle Dieckerhoff, *Member, IEEE*

***Abstract*—Power electronic systems employing wide-bandgap GaN transistors promise high efficiency operation and power density but require minimized parasitic circuit elements and an effective cooling concept. This article presents a half-bridge module integrating two 600 V/170 mΩ gallium nitride (GaN) high-electron mobility transistors with their gate drive stages and a fraction of the dc-link capacitance on a patterned multilayer polycrystalline AlN-substrate. The high-voltage isolation at a layer distance of 10 μm and a dense chip-by-chip integration on the GaN half-bridge module enable a compact lateral commutation loop design combined with improved cooling capability of the power transistors. Consequently, the GaN half-bridge module allows for higher load currents at lower device temperature while most parasitic circuit elements are reduced compared to a conventional printed circuit board (PCB) design. The parasitic circuit elements of the GaN half-bridge module and a reference four-layer PCB half-bridge are evaluated using 3D-FEM field simulation and in-circuit measurements. Selected finite element method (FEM) simulation results are validated by *S*-parameter measurements and further used to parametrize a lumped commutation loop model. The thermal characterization of the GaN half-bridge module validates the improved cooling capability of the GaN half-bridge power module. Transient switching characteristics are studied in hard-switching mode. The device temperature and converter efficiency are evaluated in dc/dc buck-converter operation.**

***Index Terms*—Inductance, integrated circuit design, converters, multichip modules, switched circuits.**

I. Introduction

WIDE bandgap gallium nitride (GaN) high-electron mobility transistors (HEMT) achieve increasingly high switching speeds and loss densities demanding for advanced assembly technology. Due to relatively small chip-sizes of state-of-the-art GaN transistors, loss generation is concentrated and requires an appropriate cooling solution. Furthermore, minimized parasitic inductances of the commutation loop and the gate drive loop are necessary to achieve stable switching transitions and to minimize the transient turn-OFF voltage stress as well as the related dynamic R_{ON}-increase [1], [2]. System optimization concerning parasitic circuit elements [3]–[5] and thermal management of the power semiconductors is a permanent issue in power electronics and typically introduces contradictory demand, so that power electronic designs are commonly a tradeoff solution with respect to the particular mission profile, especially when bottom-side cooled GaN transistors are employed [6]–[10]. During the last decades, AlN ceramics have been identified as a promising candidate for power electronics packaging due to the high thermal conductivity ($>170\,\mathrm{W{\cdot}m^{-1}{\cdot}K^{-1}}$) in combination with good electrical isolation.

This article presents an integrated GaN half-bridge power module (GaN HBM) embedding the gate drive and power circuitry on a multilayer polycrystalline AlN high-voltage assembly platform. The proposed assembly approach combines both, the electrical interface as well as the thermal management of the GaN HEMTs, hence reducing the manufacturing complexity compared to hybrid application of printed circuit board (PCB) and direct bonded copper (DBC) technology [11], [12], PCB embedding combined with AlN ceramic substrate [13]. In order to quantify the results, a comparison with a conventional PCB-based reference half-bridge (PCB HB) shows that the proposed chip-by-chip integration combines the advantages of multilayer PCB design in terms of minimized parasitic elements with the high cooling capability of single-layer [14] and multilayer DBC designs [15]–[18]. Technologically similar GaN multilayer multichip modules integrating a low-voltage RF power amplifier stage on a ceramic substrate is reported in [19]. A simulation-based optimization of a promising high-voltage GaN HEMT multilayer half-bridge design integrated on an organic substrate is presented in [20], while experimental validation is pending. Insulated metal substrates allow a flexible electrical layout while good cooling capabilities can be achieved through careful optimization, but remain limited to a single layer [21], [22] design or a larger layer distance [23].

The article is divided into five sections. After introducing the analyzed GaN HBM in Section II, Section III presents a detailed simulation-based evaluation of the parasitic circuit elements using the *electrostatic solver* (*ES*), *magnetoquasistatic solver*

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Carsten Kuring, Xiaomeng Geng, and Jan Böcker are with the Technische Universität Berlin, 10587 Berlin, Germany (e-mail: carsten.kuring@tu-berlin.de; xiaomeng.geng@tu-berlin.de; jan.boecker@tu-berlin.de).

Mihaela Wolf, Oliver Hilt, and Joachim Würfl are with the Ferdinand-Braun-Institut, 12489 Berlin, Germany (e-mail: mihaela.wolf@fbh-berlin.de; oliver.hilt@fbh-berlin.de; hans-joachim.wuerfl@fbh-berlin.de).

Sibylle Dieckerhoff is with the Technical University of Berlin, 10829 Berlin, Germany (e-mail: sibylle.dieckerhoff@tu-berlin.de).

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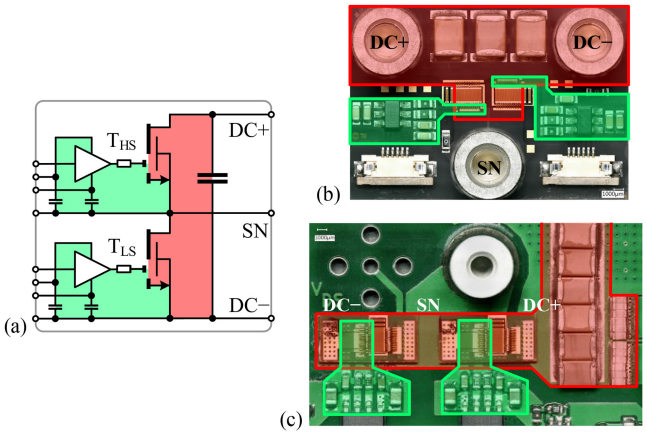


Fig. 1. (a) Commutation loop (red) and gate drive loops (green). (b) GaN HBM built on AlN substrate ($20 \cdot 28$ mm^2) versus (c) the PCB HB.

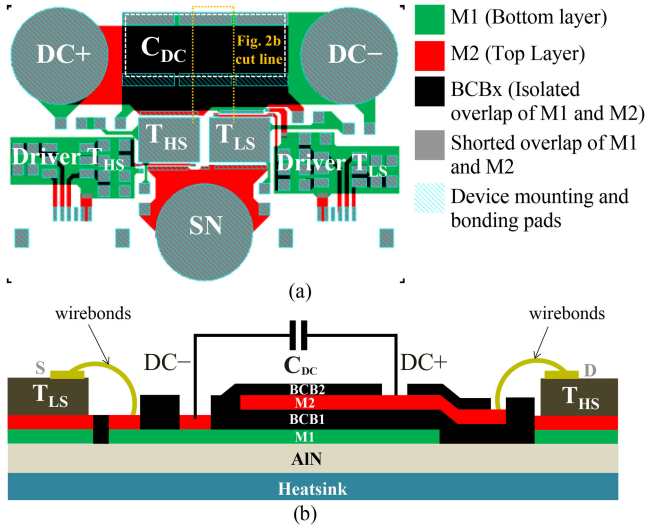


Fig. 2. (a) HBM layout and (b) cross section of the processed levels in the dc-link capacitor mounting area on the AlN substrate.

(*MQS*), and *full wave solver* (*FWS*) of the three-dimensional (3-D) FEM software CST Studio Suite [24]. The simulation methodology is verified by means of single port reflection measurement in Section IV. The functional validation of the GaN HBM is shown in Section V through thermal measurements, double-pulsed switching tests, and dc/dc operation. All analyses, simulations, and measurements of the GaN HBM in Sections II, III and V are compared to a four-layer reference PCB half-bridge. The article summarizes with conclusions and an outlook on future optimization steps.

II. GaN Half-Bridge Modules

The proposed GaN HBM as well as the reference PCB HB employ the same batch of 92 mm gate-width 600 V / 170 mΩ normally off bottom-side cooled GaN HEMTs fabricated by Ferdinand-Braun-Institut using the mature GaN-on-Si technology platform [25]. Both investigated half-bridge setups follow different design regimes concerning the commutation loop design and cooling approach as described in Sections II-A and II-C.

A. GaN HBM Integrated Circuit Components

The GaN HBM integrates two active pGaN HEMT devices with their gate drivers including the gate resistors, gate driver ICs, and bypassing capacitors [see Fig. 1(a) and (b), green area], as well as a fraction of the dc-link capacitance [see Fig. 1(a) and (b), red area]. The gate drive power supply and the pulsewidth modulation control signals are generated externally and connected to the module by flexible flat cables. Additional dc-link capacitors, the dc-link voltage supply, and the switching node are connected to the half-bridge module by high-current board-to-board connectors (DC+, DC−) which also serve to mechanically fix the module within the overall test setup. The GaN HEMT chips are soldered to their metalized mounting area on the polycrystalline AlN substrate, which provides the thermal interface and electrical isolation to the water-cooled heatsink attached underneath.

The GaN HBM is designed with a lateral commutation loop to combine optimum thermal interfacing of the GaN power transistors with minimized layout-related parasitic capacitances of the switching node (SN) [see Fig. 2(a)]. Although lateral commutation loops tend to increase the parasitic commutation stray inductance compared to vertical design based on flux compensation [26], the proposed chip-by-chip integration on AlN substrate can compensate this disadvantage (see Section III).

B. High-Voltage Multilayer AlN Integration Platform

The evaluated GaN HBM is built on a prepatterned high-voltage AlN-ceramic carrier, being fabricated in a two-metal-levels technology. The high-voltage AlN integration platform allows for a high degree of design flexibility similar to a two-layer PCB-design. An accurate and high-density device integration can be achieved utilizing a contact mask lithography at ± 2 μm resolution. Using FBH's front-end processing capabilities, 600 μm thick 4" AlN polycrystalline insulating wafers have been coated with two Au-based metal layers, M1 and M2, and two insulating dielectric layers, BCB1 and BCB2 [see Fig. 2(a)].

Electroplated gold with 5 and 7 μm thickness is used for the first (M1) and second (M2) interconnect metallization, respectively. Benzocyclobutene (BCB) polymer serves as 10 μm dielectric layer (BCB1) in-between M1 and M2, and as 5 μm final passivation layer (BCB2). Because of its high breakdown field strength of 530 V/μm [27], the BCB1 layer forms the high-voltage isolation between M1 and M2 interconnection lines. Plasma-etched vias in the BCB1 layer are used to electrically connect M2 with M1. Tungsten titanium (WTi) is applied as adhesion promoter for the metallization layers on AlN and BCB. Preassembly electrical verifications of the fabricated module layouts are carried out at wafer level in order to confirm the high-voltage isolation between M1 and M2 interconnection traces (see Fig. 3).

Due to the low thermal conductivity of the BCB-layer (0.29 Wm^{-1}K^{-1}), both metallization layers are thermally and electrically shorted in the footprint area of the GaN HEMTs, to enable optimum vertical heat dissipation from the GaN chip

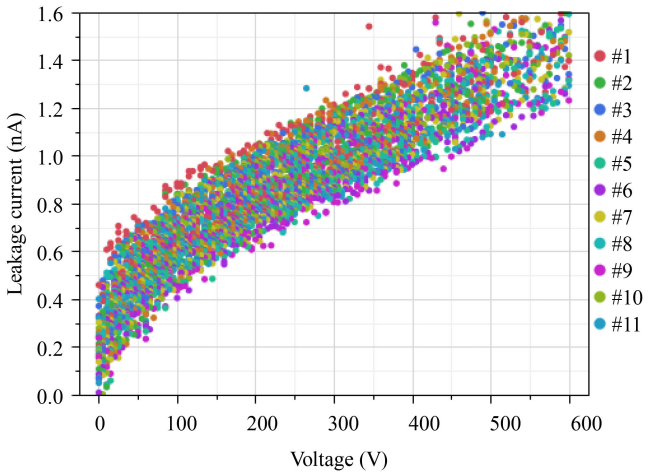


Fig. 3. Breakdown measurements of the BCB1 isolation between M1 and M2 traces up to 600 V obtained from multiple GaN HBM samples (#1–#11).

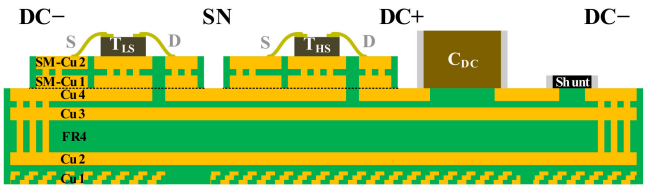


Fig. 4. Cross section of the PCB HB implementing a vertical commutation loop by a four-layer half-bridge PCB (layers Cu1–Cu4) and two-layer PCB submounts (layers SM-Cu1, SM-Cu2) utilized as transistor package.

toward the AlN substrate. In the dc-link area (DC+, DC−), the M1–M2 layer-overlap creates a low inductance parasitic capacitance adding up to the mounted on-board SMD-type dc-link capacitors and supporting fast current commutation (see Fig. 2).

C. Reference PCB Half-Bridge

The PCB HB is realized with a vertical commutation loop design on a four-layer PCB board to achieve a small parasitic commutation loop stray inductance at an increased parasitic switching node capacitance [26] [see Figs. 1(c) and 4]. The GaN HEMT chips are soldered and wire-bonded to separate two-layer PCB submounts which serve as transistor packages and are in turn soldered to the four-layer half-bridge PCB. In our setup this packing approach is favored to direct mounting of the chips for two reasons: the (additional) two-layer PCB submounts are designed to have a similar thickness like lead frames in molded packages used for commercial GaN devices [28], [29], and furthermore, the PCB submounts improve flexibility and interchangeability during device characterization to enable fast feedback to the device technology development. Similar to the GaN HBM, the GaN HEMTs are bottom-side cooled. Thermal vias in the chip area of the PCB submount provide thermal paths to the underlying four-layer main PCB which is exposed to forced airflow for heat dissipation. The low-side transistor is thermally connected to relatively large copper areas in the three upper layers [see Fig. 4, Cu2–Cu4]. The high-side transistor dissipates its losses through the switching node metallization. Accordingly, the design of the switching node layout is a tradeoff between thermal design constraints and minimization of the parasitic switching node capacitance. The vertically oriented commutation loop in the four-layer main PCB uses 35 μm thick Cu layers. The commutation loop incorporates the upper and both inner layers [see Fig. 4, Cu2–Cu4] at distances of 140 μm (Cu3 $\leftrightarrow$ Cu4) and 1200 μm (Cu2 $\leftrightarrow$ Cu3). The PCB submounts serving as transistor package employ two 35 μm Cu layers (SM-Cu1, SM-Cu2) at a distance of 730 μm resulting in an overall stack-up height of 800 μm.

TABLE I
SOLVER SETTINGS APPLIED IN FEM FIELD SIMULATION

Solver setting	Solver		
	ES	MQS	FWS
Stopping criterion	0.1%	1%	1%
Refinement percentage	1%	1%	1%
Desired Accuracy	10 Sep.	10 May	10 May
Min. meshing passes	2	8	10

III. SIMULATION-BASED EVALUATION OF THE PARASITIC CIRCUIT ELEMENTS

Although generally a point of concern in power electronics, the extremely fast switching transients and small device capacitances of GaN HEMTs further increase the need to reduce layout related parasitic circuit elements. Hence, for the GaN HBM and PCB HB comparison, both layouts have been modeled and simulated using a 3D-FEM field simulation tool of *CST Studio Suite 2019* [24]. Combining results obtained with the *ES*, *MQS*, and *FWS*, a third-order lumped commutation loop model suitable for the GaN HBM as well as for the PCB HB is derived and parametrized.

A. Parasitic Capacitances of the Power Loop

Parasitic capacitances either support or deteriorate the intended switching behavior depending on their actual position in the circuit. While the parasitic AlN layout dc-link capacitance effectively adds up to the capacitors mounted on-board, the switched parasitic capacitances between fixed and switched nodes degrade the switching performance. These layout-related capacitances are computed using the electrostatic solver. In the simulation, all models of the dc-link MLCCs, GaN HEMTs ,and gate drive circuitry are neglected. The dielectric constants of the isolation layer are assumed as $\varepsilon_{\mathrm{r,BCB}} = 2.65$ for BCB (GaN HBM) and $\varepsilon_{\mathrm{r,FR4}} = 4.3$ for FR4 (PCB HB). The applied solver settings are given in Table I.

In the dc-link area, the GaN HBM has a large horizontal overlap of the M1 and M2 metallization layers. These are part of the dc-link nodes DC+ and DC− and separated by a 10 μm isolating BCB layer. This geometry forms a parasitic capacitor (see Fig. 2) of $C_{\mathrm{p,\,DC}} =$ [148;160] pF, depending on the termination of the attached heatsink (see Table II). Due to the low-inductive layout, this capacitance leads to a higher resonant frequency than the mounted MLCCs (see Fig. 5) and therefore offers an additional bypass in a frequency range below 1 GHz. For comparison, in the PCB HB the dc-link nodes share significantly less overlapping Cu-area resulting in a much

TABLE II
CONTRIBUTION OF PARASITIC LAYOUT CAPACITANCES TO OVERALL PARASITIC CAPACITANCES

GaN HBM: heatsink shorted to DC+				
Contribution of \ to	$C_{p,DC}$ (pF)	$C_{p,DC+/SN}$ (pF)	$C_{p,SN/DC-}$ (pF)	$C_{p,SN}$ (pF)
Commutation loop layout	160	10.1	0.25	10.4
Gate driver layout	-	5.44	0.02	5.46
Total	160	86.5[1]	71.2[1]	158[2]
GaN HBM: heatsink floating				
Contribution of \ to	$C_{p,DC}$ (pF)	$C_{p,DC+/SN}$ (pF)	$C_{p,SN/DC-}$ (pF)	$C_{p,SN}$ (pF)
Commutation loop layout	148	2.67	4.82	7.48
Gate driver layout	-	0.49	2.80	3.29
Total	148	74.0[1]	78.5[1]	153[2]
GaN HBM: heatsink shorted to DC−				
Contribution of \ to	$C_{p,DC}$ (pF)	$C_{p,DC+/SN}$ (pF)	$C_{p,SN/DC-}$ (pF)	$C_{p,SN}$ (pF)
Commutation loop layout	153	0.21	10.2	10.4
Gate driver layout	-	0.02	5.49	5.50
Total	153	71.1[1]	86.6[1]	158[2]
PCB HB				
Contribution of \ to	$C_{p,DC}$ (pF)	$C_{p,DC+/SN}$ (pF)	$C_{p,SN/DC-}$ (pF)	$C_{p,SN}$ (pF)
Commutation loop layout	18	0.43	32.1	32.5
Gate driver layout	-	0.03	4.82	4.85
Total	18	74.0[1]	108[1]	182[2]

[1]Total capacitance values ($C_{p,DC+/SN}$ and $C_{p,SN/DC-}$) include the voltage-related average output capacitance of the top side or bottom side HEMT C_O (V_{DS} = 0–400 V) = 70.9 pF.
[2]Total capacitance values ($C_{p,SN}$) of the switching node include parasitic capacitance between the top side gate island and low voltage circuit caused by the digital isolator ($C_{p,ISO}$ = 2 pF) and the dc/dc converter ($C_{p,DCDC}$ = 4 pF) employed for gate voltage power supply [30]–[32].

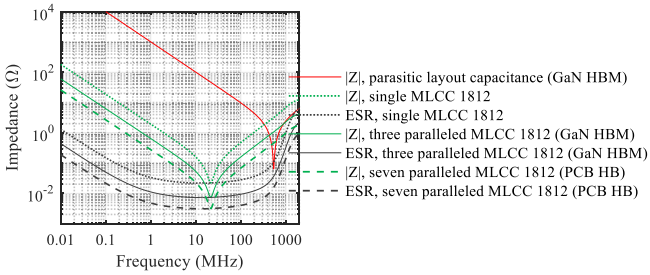


Fig. 5. Impedance of layout-integrated parasitic dc-link capacitor established within the GaN HBM layout obtained from *FWS* simulation (red) vs. impedance of a single, three and seven paralleled 1812 SMD dc-link MLCC [33].

smaller $C_{p,\,DC}$ = 18 pF. Compared with the capacitance of the mounted dc-link MLCCs in the range of several hundreds of nanofarad [see Fig. 1(b) and (c)], the contribution of the layout capacitances is small, but it still may support clean switching in the first few nanoseconds of the switching event. In contrast, the switched parasitic capacitances need to be reduced as much as possible in fast GaN-based power converters, since their charging and discharging reduces switching speed, increases switching losses, gives rise to stronger common-mode EMI perturbation and in consequence affects converter efficiency. All circuit components such as GaN HEMTs, digital isolators, gate voltage supply as well as the layout contribute to the capacitance. GaN HBM and PCB HB layouts are separately simulated (see Fig. 6), considering the commutation loop traces (see Fig. 1, red) as well as the gate island layout (see Fig. 1, green). The gate

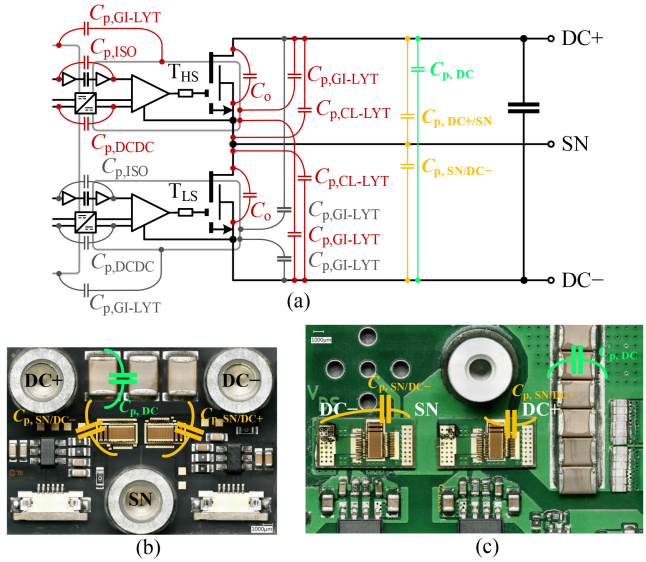


Fig. 6. Schematic (a) and micrographs of GaN HBM (b) and PCB HB (c) including parasitic layout and component capacitances (red) contributing to parasitic capacitance of the switching node (yellow), layout-integrated parasitic dc-link capacitance (green) and irrelevant (grey) parasitic capacitances.

island of the top side power transistor is floating according to the switching state of the transistors. The bottom side gate island is referenced to the bottom side transistor's source node with constant DC− potential. Only the actively switched parasitic capacitances (see Fig. 6, red) are accounted to compute the switching node capacitances $C_{p,SN}$.

The lateral orientation of the HBM commutation loop leads to relatively small capacitances between the dc-link nodes DC+, DC− and the switching node. Shorting the heatsink and backside of the AlN-module to DC−, which is a common method to reduce common-mode electromagnetic interference, affects the electric field distribution within the AlN-substrate and results in minor changes of the capacitances (see Table II). Despite the different power loop designs—the PCB HB has a vertical commutation loop (see Section II-C)—both setups have the gate islands placed side by side to the respective GaN HEMT to avoid vertical overlapping. This gate layout increases the capacitance of the switching node by 3.3 pF in case of a floating heatsink and by 5.5 pF if the heatsink is shorted to DC−. This is in a similar range as in the PCB HB (4.85 pF). In both setups the contribution of the layout to $C_{p,SN}$ results from the commutation loop traces. It can be concluded that for the presented layouts, the switching node capacitance node capacitance is dominated by the output capacitance of the GaN HEMTs (see Table II and Fig. 7).

B. Parasitic Stray Inductance of the Commutation Loop

The parasitic stray inductance of the commutation loop directly affects the transient turn-OFF voltage overshoot, the switching losses, and, specifically for GaN HEMTs, the dynamic ON-state characteristics [2] and the stability of the switching transitions. Since layout and circuit components contribute to the inductance, the impact of each subcomponent is computed based on stepwise extended models of the GaN HBM and the

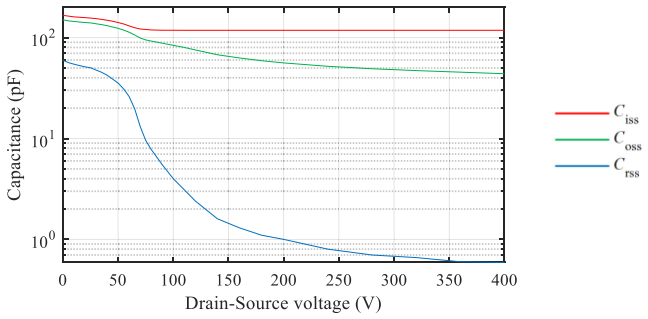


Fig. 7. Small-signal device capacitances of the 600 V normally off 92 mm GaN HEMTs applied in the investigation, $V_{GS} = -2.0$ V.

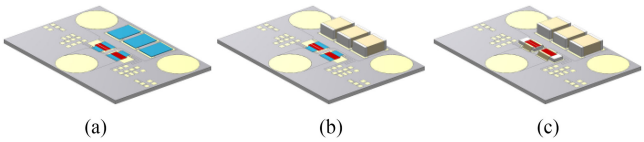


Fig. 8. Stepwise extension of the physical model of the GaN HBM for evaluation of the parasitic stray inductance. (a) DC-link capacitors and transistor shorted. (b) Model of DC-link capacitors included; transistors shorted. (c) Model of DC-link capacitors and transistors included.

PCB HB design to enable the optimization of the switching cell. The initial model of the GaN HBM is limited to the blank AlN-substrate layout and components such as the GaN HEMTs and dc-link MLCCs, are replaced by flat footprint-equivalent short circuit elements [see Fig. 8(a), blue structures]. Subsequent iterations of the simulation model are stepwise extended by the physical representation of the dc-link capacitors [see Fig. 8(b)] and the power transistors [see Fig. 8(c)]. The MLCC are modeled as solid copper blocks to reduce the computation effort. However, this results in deviations concerning current displacement and frequency-dependent characteristics of the equivalent series resistance (ESR) and equivalent series inductance (ESL) compared to a real MLCC [34]. The comparison of the GaN HBM and PCB HB remains feasible as both simulation models and test setups rely on the same MLCC model and device, respectively. The GaN HEMTs ON-state resistance is emulated by commutation loop segments (see Figs. 8 and 14, red structures) which are placed in the location of the active chip-area. Their resistivity is chosen such that the effective absolute resistance matches the rated ON-state resistance of the GaN HEMTs of 200 mΩ. The excitation source which is essentially required in *MQS* and *FWS* simulation in the frequency domain, is inserted in the middle of the active chip area of the high-side transistor (see Fig. 8, left-side red structure). This location is chosen since in conventional hard-switched operation the characteristic turn-OFF voltage oscillation occurs when the high-side transistor is already conducting after turn-OFF of the low-side transistor. Due to this relatively high ON-state resistance, the extend of current displacement due to skin- and proximity effects is assumed to be small resulting in a homogenous current distribution in the real transistor. Similarly, the excitation current source in the simulation enforces a homogeneous current density within its cross section.

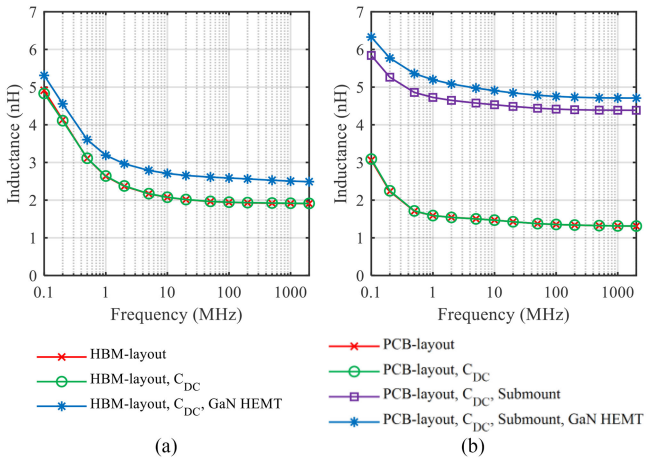


Fig. 9. Parasitic stray inductance of the commutation loop computed by *MQS* 3D-FEM field simulation. (a) GaN HBM. (b) PCB HB.

The stray inductance of each setup is initially evaluated using the *MQS*. The *MQS* neglects capacitive displacement currents occurring e.g., within the isolating layers (BCB-layer of the GaN HBM or FR4-layer PCB HB). Accordingly, layout-inherent resonances are neglected so far. The applied solver settings are given in Table I.

The *MQS* simulation in the frequency domain computes the frequency-dependent commutation loop impedance, which is used to derive the equivalent lumped stray inductance:

$$L_\sigma = \mathrm{Im}(\underline{Z}) \cdot \omega^{-1}. \tag{1}$$

The sinusoidal excitation is swept from 100 kHz up to 2 GHz to cover common values of the switching frequency as well as parasitic oscillations. In all configurations, L_σ strongly decreases up to approx. 1 MHz due to frequency-dependent current density distribution in the commutation loop (see Fig. 9). The horizontal commutation loop of the GaN HBM leads to a larger stray inductance $L_{\sigma,\mathrm{HBM}} = 1.95\ \mathrm{nH}\,|_{f\,=\,100\ \mathrm{MHz}}$ compared to $L_{\sigma,\mathrm{PCB}} = 1.35\ \mathrm{nH}\,|_{f\,=\,100\ \mathrm{MHz}}$ for the vertical commutation loop of the PCB HB (see Fig. 1, red lines). In both half-bridges, the dc-link capacitors cause a negligible increase of L_σ (see Fig. 9, red versus green lines). This effect relates to the simplified dc-link MLCC capacitor model, which neglects the real internal multilayer structure.

In difference to our simulation, high-frequency oscillations in the real setup will cause a strongly inhomogeneous current density in each dc-link capacitor, so that a significantly derated effective capacitance compared to the nominal rating is to be expected. Considering the power transistor chips and their wire bonds causes a further increase of L_σ by 0.4–0.6 nH for both half-bridge designs [see Fig. 9(a), green versus blue line; Fig. 9(b), purple versus blue line). The overall stray inductance of the PCB HB is mainly caused by the PCB-submount serving as transistor package [see Fig. 8(b)]. In summary, based on the simulation results, the GaN HBM achieves a 46 % lower stray inductance of $L_{\sigma,\mathrm{HBM}} = 2.6\ \mathrm{nH}|_{f\,=\,100\ \mathrm{MHz}}$ despite the horizontal commutation loop.

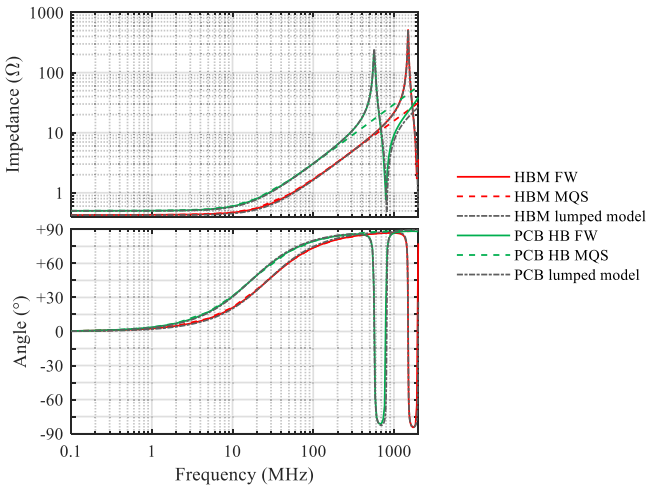


Fig. 10. Commutation loop impedance of GaN HBM and PCB HB obtained from *MQS* and *FWS* simulation vs. fitted lumped model.

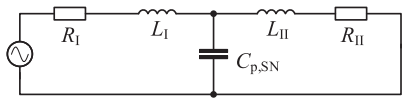


Fig. 11. Third-order lumped model of the PCB HB commutation loop.

TABLE III
LUMPED MODEL CIRCUIT ELEMENTS

Model parameter		HBM	PCB HB
Commutation loop stray inductance[1]	L_σ	2.49 nH	4.71 nH
Stray inductance share	k_L	0.5644	0.4916
Partial stray inductance	$L_{\sigma,\mathrm{I}}$	1.41 nH	2.32 nH
Partial stray inductance	$L_{\sigma,\mathrm{II}}$	1.08 nH	2.39 nH
Commutation loop resistance[2]	R_σ	426 mΩ	501 mΩ
Resistance share	k_R	0.5257	0.4023
Partial resistance	R_{I}	224 mΩ	202 mΩ
Partial resistance	R_{II}	202 mΩ	299 mΩ
Switching node layout capacitance[3]	$C_{\mathrm{p,SN}}$	10.4 pF	32.5 pF

[1]Obtained from *MQS* simulation, $f = 2$ GHz.
[2]Obtained from *MQS* simulation, $f = 100$ kHz.
[3]Obtained from *ES* simulation.

C. Layout Inherent Resonances

Separate simulations of layout related capacitances and inductances allow to identify the contribution of each parasitic element and to apply a stepwise optimization procedure. In order to detect layout resonances, *FWS* simulation is required which further allows to derive a lumped commutation loop model. The circuit model applied in *FWS* simulations includes all components of the commutation loop, as exemplary shown in Fig. 4. Furthermore, the PCB HB model includes a representation of a 50 mΩ SMD-based shunt used for transient drain current measurement in the real-world setup. Parasitic device capacitance introduced by the GaN HEMTs are neglected in the model to allow identification of the layout related resonances.

In the frequency range well below the first resonant frequency, *MQS* and *FWS* simulations deliver similar results in terms of the commutation loop impedance, since capacitive displacement currents covered by *FWS* simulation but neglected by *MQS* simulation are considerable small (see Fig. 10). Comparing both investigated setups, the GaN HBM achieves significantly higher resonant frequencies (1.50 and 1.92 GHz versus 564 and 812 MHz), due to its smaller power loop stray inductance and switching node capacitance. The impedances of the full circuit setups are expected to be more similar as the overall switching node capacitances are dominated by the GaN HEMTs output capacitance.

D. Lumped Commutation Loop Model

Optimization of the power electronic circuit essentially relies on circuit simulation using lumped elements of circuit components and parasitics. Co-simulation linking circuit and field simulation within a single simulation task is a promising tool but introduces significant computation effort. A lumped model of the commutation loop is therefore favorable in conventional circuit simulators like different available Spice derivatives. Based on the *FWS* simulation results, each depicting a third-order transfer function, a simplified lumped equivalent circuit is derived (see Fig. 11). The parasitic components $C_{\mathrm{p,SN}}$, L_σ, and R_σ are taken from the *ES* and *MQS* simulation results, respectively. In order to achieve the observed third-order transfer function, the overall commutation loop stray inductance L_σ and resistance R_σ are split into their corresponding subcomponents

$$L_{\mathrm{I}} = k_L \cdot L_\sigma \qquad R_{\mathrm{I}} = k_R \cdot R_\sigma$$
$$L_{\mathrm{II}} = (1 - k_L) \cdot L_\sigma \qquad R_{\mathrm{II}} = (1 - k_{\mathrm{R}}) \cdot R_\sigma \tag{2}$$

leaving the inductance share k_L and resistive share k_R as free parameters to fit the resulting transfer function of the lumped model to the one obtained from the *FWS* field simulation. Fitting of k_L and k_R by means of least-squares approximation delivers a well matching frequency-dependent commutation loop impedance for both investigated half-bridge configurations (see Fig. 10 and Table III). In this simplified modeling approach, the impact of the skin effect on the resistance occurring in the field simulation and experiment is neglected. Furthermore, the ESR and ESL of the dc-link MLCCs are neglected in both, FEM field simulation and lumped circuit model, but can be covered by adjusting the parameters of the lumped model.

E. Stray Inductance of the Gate Loop

In accordance with the previous analysis, the gate loop inductance is investigated using the *MQS* and applying (1). The simulations rely on a set of 3-D circuit models where each gate loop circuit component is either modeled by its physical representation or replaced by a footprint-equivalent short-circuit plane (see Fig. 12). This simulation approach allows to estimate the contribution ΔL_σ of each component to the overall gate loop inductance (see Table IV). The excitation source is located within the gate driver lead frame model [see Fig. 12(b) and (f)] or the respective short-circuit plane [see Fig. 12(a), (c)–(e)]. The simulations of the reference PCB HB are limited to the low-side gate loop as both, high-side and low-side gate loops have an identical layout. The reference PCB layout achieves a similar low gate loop inductance as the high-side GaN HBM. The gate circuit on the PCB is routed using several layers in the mounting area

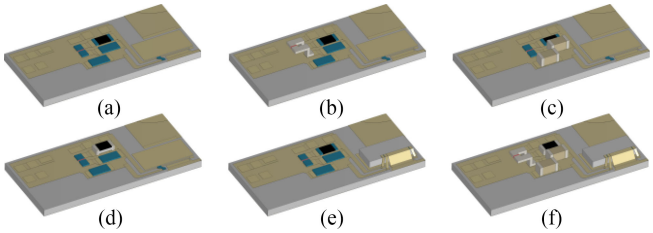


Fig. 12. Stepwise extended model of the low-side GaN HEMT turn-ON gate loop on the GaN HBM. (a) Gate loop layout w/o components. (b) Pin-structure emulating the SOT23-6 driver lead frame. (c) Bypass capacitors of the gate driver voltage supply. (d) Gate resistor. (e) GaN HEMT w/ ribbon bonding. (f) Complete model w/ all components attached; (a)–(e) all other gate-loop components are replaced by footprint-equivalent short circuit planes (blue).

TABLE IV
CONTRIBUTION OF GATE LOOP COMPONENTS TO OVERALL GATE LOOP INDUCTANCE

Component		Setup		
		GaN HBM low-side gate loop	GaN HBM high-side gate loop	PCB HB
Complete gate loop	L_σ	4.7–8.8	3.0–5.6	4.6–7.1
Layout	(nH)	3.2–7.7	1.5–4.4	2.3–4.4
Driver		0.5–0.9	0.6–1.0	1.1–1.5
Bypass capacitor		< 0.1	< 0.1	< 0.1
Gate resistor	ΔL_σ	0.1–0.4	0.1–0.4	0.1–0.2
PCB submount	(nH)	–	–	0.6–0.8
GaN HEMT w/ Bonding		0.5–0.9	0.4–0.9	0.3–0.4

of the gate driver voltage bypass capacitors. The turn-ON gate loop employs both upper Cu-layers "Cu3" and "Cu4" whereas the turn-OFF gate loop is routed using layer "Cu2" and "Cu4." Consequently, layout related flux compensation is more effective for the turn-ON gate loop leading to a smaller inductance [see Fig. 13(e) versus (f)]. Aside from the gate loop layout, the gate driver housed in a relatively large SOT23-6 SMD package [35] and the GaN HEMT including its bonding wires are the most significant contributors to the overall gate-loop inductance in the GaN HBM (see Table IV). The impact of the driver stage is even stronger for the PCB HB using a larger SOIC-8 package [30]. A smaller driver package, flip-chip mounting of the GaN HEMT or even monolithic integration of the driver and the GaN HEMT chip are feasible approaches to optimize the design. Comparing the simulation results of the gate layout without attached components [see Figs. 12(a) and 13, light blue lines] to the gate layouts with attached gate resistors [see Figs. 12(d) and 13, grey lines) shows an increase of the overall gate loop inductance by [0.1;0.4] nH. Therefore, flipped mounting of the gate resistors appears to be a suitable option to minimize the gate loop inductance without any design change.

IV. MODEL VERIFICATION BY MEASUREMENT

Model verification by means of measurement is generally challenging due to small dimensions of the compact GaN based setups. Even small modifications of the test setup which are required for inserting a sourcing signal and extraction of a measurement signal affect the investigated DUT. In the following,

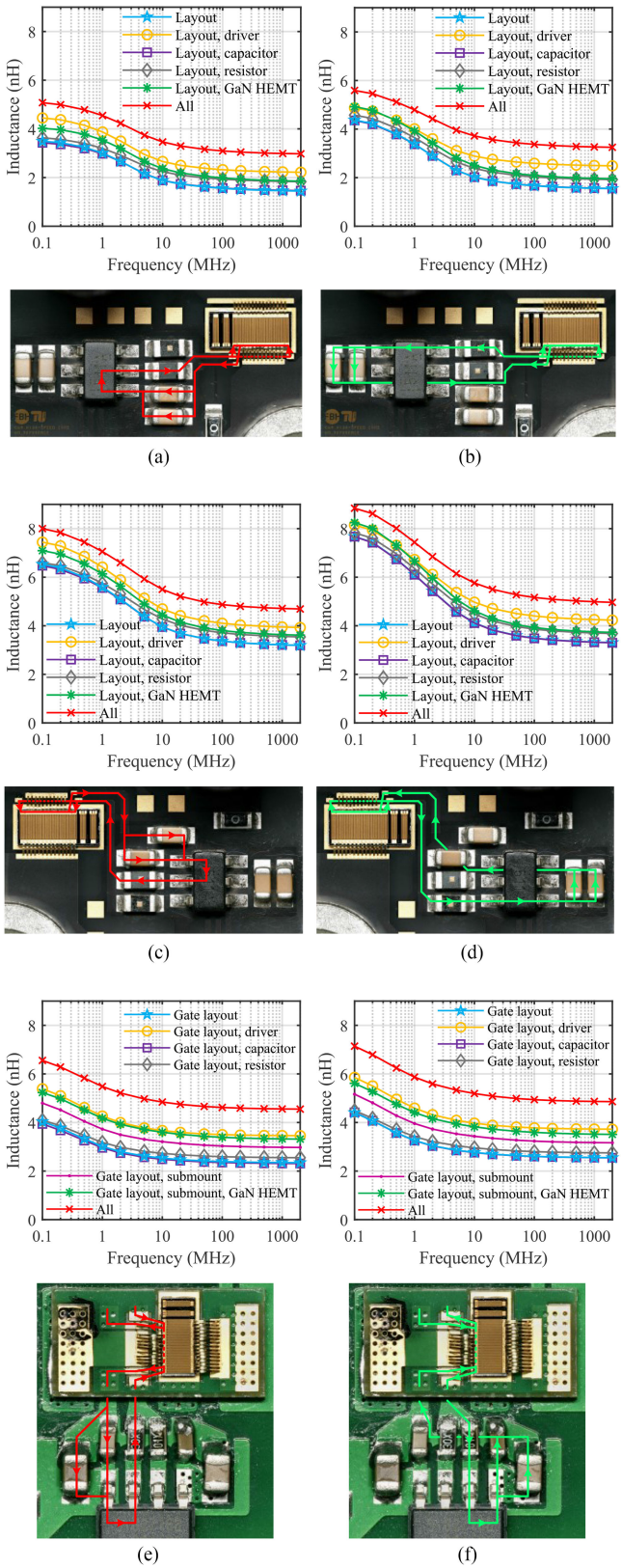


Fig. 13. Parasitic inductances extracted from MQS field simulation and micrographs of the gate loop of the GaN HBM (a)–(d) versus PCB HB (e), (f). (a) High-side turn-on gate loop. (b) High-side turn-off gate loop. (c) Low-side turn-on gate loop. (d) Low-side turn-off gate loop. (e) Low-side turn-on gate loop. (f) Low-side turn-off gate loop.

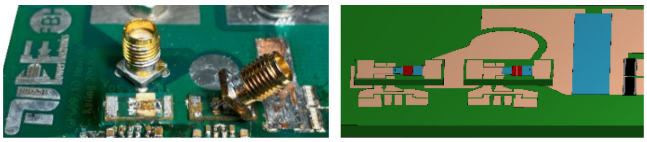


Fig. 14. PCB HB setup modified for VNA measurement (left) and the corresponding 3-D model employed in FEM field simulation (right).

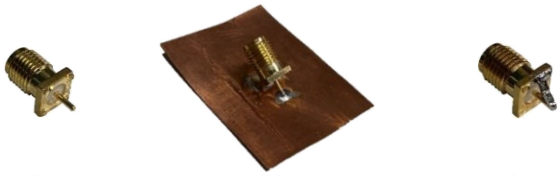


Fig. 15. Custom standards used for VNA calibration to compensate parasitic properties of the applied SMA socket. (a) Open. (b) Short. (c) 50 Ω match.

the model verification is exemplarily done for the PCB HB comparing the results from *MQS* and *FWS* simulation with single port reflection measurements using a HP 8753A Virtual Network Analyzer (VNA). The PCB HB is modified to conduct the VNA measurements as follows

1) the dc-link MLCCs are replaced by copper foil effectively shorting their footprint area (see Fig. 14);
2) the PCB submounts remain on the board, while the transistor chips including their bonding wires are disassembled;
3) the bottom side transistor chip is replaced by a Cu foil shorting drain and source pads of the PCB submount;
4) a subminiature version A (SMA) socket required for S-parameter measurement is attached in the mounting area of the topside transistor chip.

The SMD-shunt based on 12 paralleled flipside-mounted 0603-size 1 Ω resistors and dedicated for transient drain current measurement in the double-pulse test remains unchanged. Reference *MQS*- and *FWS*-simulation are carried out using a model corresponding to the modified PCB HB.

In order to achieve a reasonable measurement accuracy despite of the bulky SMA socket which connects the PCB commutation loop to the VNA, custom standards are used for open, match and short calibration (see Fig. 15). The short plane and matching network are mounted at the same angle as in the PCB HB to compensate the stray inductance resulting from the socket layout and mounting angle. The reflection measurement is executed using the maximum frequency range of the HP8753A of 300 kHz up to 3 GHz in logarithmic sweep mode.

This covers common values of the switching frequency of several hundreds of kilohertz up to high-frequency oscillations in the gigahertz range occurring during switching transients of GaN-based converters.

Measurement results of the scattering parameter

$$\underline{S}_{11} = (\underline{Z}_\sigma - \underline{Z}_0)(\underline{Z}_\sigma + \underline{Z}_0)^{-1} \tag{3}$$

are used to calculate the commutation loop impedance [36]

$$\underline{Z}_\sigma = \underline{Z}_0 \left(\underline{S}_{11} + 1\right)\left(1 - \underline{S}_{11}\right)^{-1} = R_\sigma + \mathrm{j}\omega L_\sigma \tag{4}$$

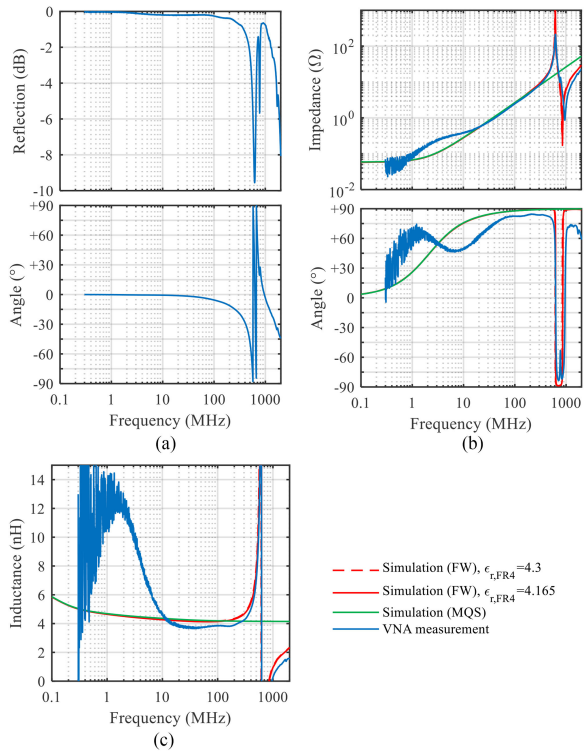


Fig. 16. Commutation loop VNA measurement versus FEM simulation results. (a) Scattering parameter S11. (b) Commutation loop impedance. (c) Commutation loop inductance.

where $\underline{Z}_0 = 50\ \Omega$ is the output impedance of the VNA. The assumption of a basic ohmic-inductive equivalent circuit enables the extraction of the commutation loop inductance (1) in the frequency range below the first resonant frequency for the *MQS* and *FWS* simulation model as well as the VNA measurement (see Fig. 16). Similar to the previous analysis, *MQS* and *FWS* simulation deliver identical values for impedance and inductance up to approx. 300 MHz, when capacitive displacement currents become significant and the *MQS* simulation is no longer accurate. Furthermore, the impedance extracted from the VNA measurement shows similar values starting at approx. 30 MHz. At lower frequencies, the accuracy of the VNA is limited due to high quality factor (Q factor) of the commutation loop and strong reflection, respectively. The VNA measurement shows additional intermediate resonances at 762 and 785 MHz, which become especially notable in the commutation loop phase plot [see Fig. 16(b)]. These resonances result from the lowest Cu-layer "Cu1" of the PCB HB stack-up. This copper layer is employed for external dc-link supply, but is neglected in the field simulation model as it is not part of the inner commutation loop. Finally, a slight tuning of the FR4 dielectric constant from originally $\varepsilon_{\mathrm{r,FR4}} = 4.3$ toward $\varepsilon_{\mathrm{r,FR4}} = 4.165$ results in further improved matching of the FWS simulation model with the VNA measurement.

V. In-Circuit Characterization

The AlN-based integration of the GaN HBM promises benefits in switching performance and cooling capability. These

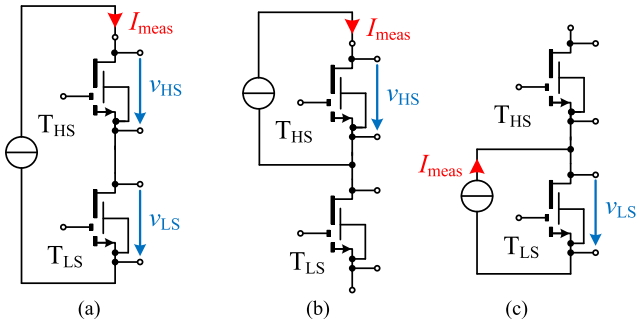


Fig. 17. Test schemes applied for (a) simultaneous and (b), (c) separate thermal characterization of both power transistors of GaN HBM and PCB HB. a) THS: ON, TLS: ON. (b) THS: ON, TLS: OFF. (c) THS: OFF, TLS: ON.

improvements are validated separately using static thermal measurements and double-pulse switching tests.

A. Thermal Characterization

The cooling capability of the GaN HBM and the reference PCB HB are evaluated in a dc-measurement, where a time-constant current I_{meas} causes conduction losses and self-heating of the GaN transistors. The transistor losses are adjusted by the current I_{meas}, and the maximum chip surface temperature is limited to approx. 130 °C. In thermal steady state, the ON-state voltages v_{HS}, v_{LS}, the current I_{meas} and the ambient temperature measured by a PT100 are acquired by digital multimeters (Fluke 8846A) [37] to calculate the dissipated power, ON-resistance and temperature rise of each transistor (see Fig. 17). Despite the open-case packaging of the GaN HEMTs (see Fig. 1), an accurate measurement of the junction temperature is challenging. The chip surface temperature is measured using a thermal camera (FLIR E60) [38] and is expected to be lower than the internal junction temperature, because

1) the channel region is significantly shorter than the spatial resolution of the thermal camera system;
2) the channel region is covered by several epitaxial and passivation layers;
3) the metallic source-connected field plates completely screen the transistor heat source;
4) different visible structures on the GaN-chip have a specific infrared emissivity.

Therefore, the internal junction temperature is calculated from the resistance by the following:

$$\begin{aligned} T\left(R_{\mathrm{on}}\right) &= a \cdot R_{\mathrm{on}}^2 + \mathrm{b} \cdot R_{\mathrm{on}} + \mathrm{c} \\ \mathrm{a} &= -1.27 \cdot 10^3 \mathrm{K}\Omega^{-2}; \mathrm{b} \\ &= 1.38 \cdot 10^3 \mathrm{K}\Omega^{-1}; \mathrm{c} = 1.31 \cdot 10^2 \mathrm{K} \end{aligned} \tag{5}$$

fitted from the characteristic static ON-state resistance curve (see Fig. 18), which was previously acquired in a reference measurement. This indirect acquisition of the junction temperature relies on the assumption that the transistor is being operated in the ohmic region. In case of high drain current values, the transistor approaches the saturation region, and the calculated

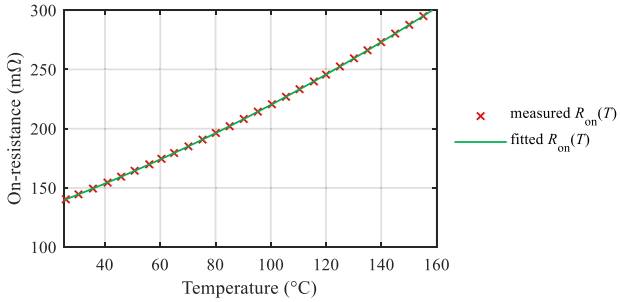


Fig. 18. Static ON-state resistance versus device temperature of the 600 V normally off GaN-on-Si HEMTs used in both GaN half-bridge designs.

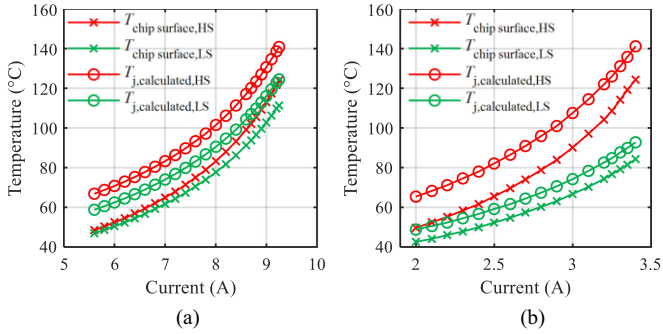


Fig. 19. Chip surface temperature measured with a thermal camera and calculated junction temperature versus dc-current self-heating of both GaN HEMTs simultaneously in the GaN HBM and PCB HB. (a) GaN HBM. (b) PCB HB.

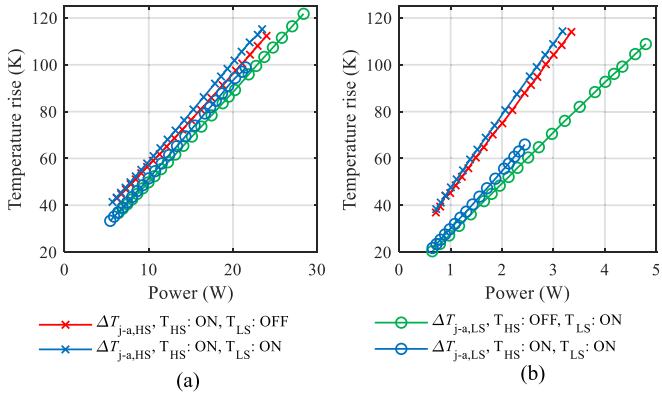


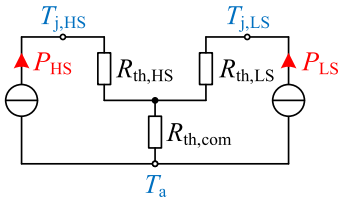
Fig. 20. Temperature rise versus dissipated power per GaN HEMT chip in the GaN HBM and PCB HB. (a) GaN HBM. (b) PCB HB.

temperature (5) becomes larger than the internal junction temperature. It therefore represents an upper estimation boundary of the real junction temperature (see Fig. 19). To obtain a worst-case estimation of the thermal resistance, the following evaluations are based on the calculated junction temperature. Since the same open-case packaged GaN HEMTs are used in both setups (see Fig. 1), the error between real and calculated junction temperature is assumed to be similar. Evaluating each transistor in the GaN HBM individually results in a thermal resistance of 4.68 and 4.29 K/W [see Fig. 20(a), red and green lines, and Table V]. Simultaneous loss dissipation in both transistors leads to almost doubled total losses of the module [see Fig. 20(a), blue lines] but only slightly increased thermal resistance of

TABLE V
THERMAL RESISTANCES[1] IN THE GAN HBM AND PCB HB

GaN HEMT state		GaN HBM		PCB HB	
High-side	Low-side	$R_{\text{th, j-a, HS}}$ (K/W)	$R_{\text{th, j-a, LS}}$ (K/W)	$R_{\text{th, j-a, HS}}$ (K/W)	$R_{\text{th, j-a, LS}}$ (K/W)
ON	OFF	4.68	–	34.1	–
OFF	ON	–	4.29	–	22.7
ON	ON	4.91	4.60	36.0	27.0

[1]Obtained from measurement at maximum dc current.



	GaN HBM	PCB HB
$R_{th,HS}$ (K/W)	4.43	31.53
$R_{th,LS}$ (K/W)	4.04	20.18
$R_{th,com}$ (K/W)	0.248	2.52

Fig. 21. Fitted static thermal half-bridge model and thermal resistance values for both investigated half-bridge setups.

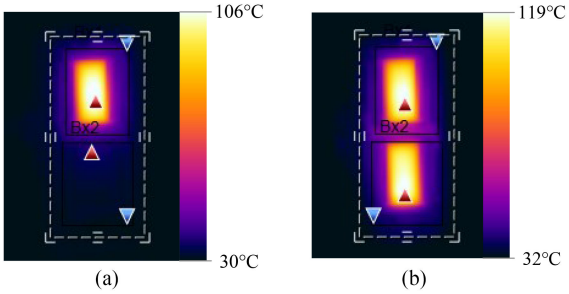


Fig. 22. Thermograph of the GaN HBM during thermal characterization. (a) Single transistor self-heated (TLS: ON, THS: OFF). (b) Both transistors self-heated (TLS: ON, THS: ON).

4.91 and 4.60 K/W of the high-side and low-side transistors, respectively (see Table V). Combining these measurement data, a static thermal model covering separate as well as simultaneous heating of both GaN transistors has been parameterized for both half-bridge setups. Overall, the GaN HBM achieves between 5 and 7 times lower thermal resistances compared to the PCH HB as well as strongly reduced thermal cross-heating (see Fig. 21). Similar thermal resistance values of [4.6, 6.2] K/W are reported for comparable small commercial bottom-side cooled GaN HEMTs mounted on a DBC-substrate [9], [16]. Larger top-cooled devices can easily achieve a lower thermal resistance of [2.07; 2.33] K/W [39]. However, further optimization potential is indicated for the GaN HBM by the thermographs in Fig. 22 showing a strong thermal gradient from the active chip area towards the AlN-substrate underneath. This effect is caused by the high vertical thermal resistance from the GaN channel dissipating the losses through the transistor's strain-adaption epitaxial layers [40] and the 450 μm thick Si-substrate towards the solder joint between GaN-on-Si chip and AlN substrate. The fitted values $R_{\text{th,HS}}$ and $R_{\text{th,LS}}$ (see Fig. 21) offer a rough estimation of the transistor-specific thermal resistance values. Thinning down the GaN HEMT's Si-substrate as it is commonly done for commercial transistors is expected to mitigate this thermal bottleneck in the GaN HBM setup.

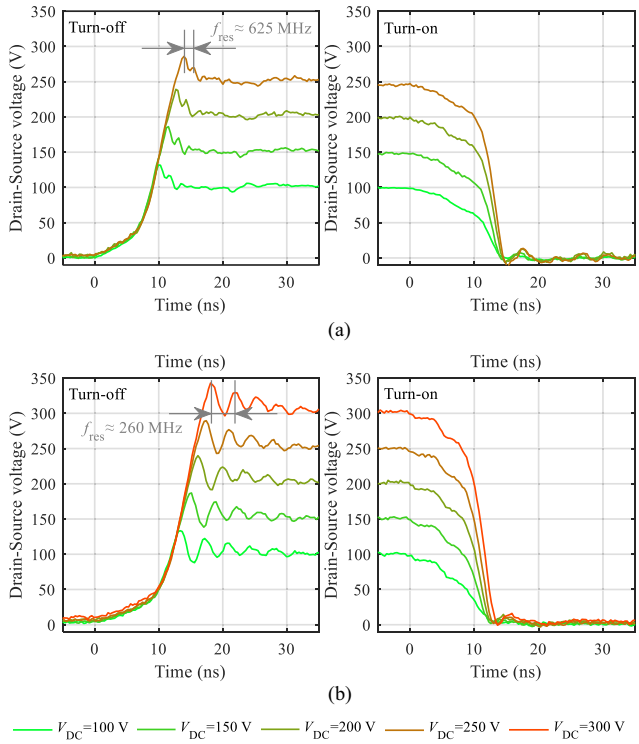


Fig. 23. Transient drain–source voltage during hard-switched turn-OFF (left) and turn-ON (right) under clamped inductive switching conditions, $I_L = 8$ A. (a) GaN HBM. (b) PCB HB.

B. Switching Characteristics

The AlN-based GaN HBM has a significantly increased cooling capability compared to the reference PCB HB. To ensure a reasonable comparison of both setups concerning switching behavior, self-heating of the GaN HEMTs needs to be limited, especially for the PCB HB. Therefore, the dynamic characterization relies on the double-pulse test, where self-heating effects are minimized. As discussed, a minimization of the gate loop impedance is crucial to achieve fast switching of GaN transistors, and the integration of the gate drive stages with the power transistor on the AlN substrate enables a significantly smaller gate loop and lower gate loop inductance. This is achieved for the high-side transistor in the GaN HBM, while the low-side gate loop requires further optimization (see Section III-E). Besides from different gate driver stages (GaN HBM: Texas Instruments UCC27511 versus PCB HB: Silicon Labs Si8271) identical gate drive parameters ($V_{\text{G,on}} = 6.0$ V, $R_{\text{G,on}} = 20\ \Omega$, $V_{\text{G,off}} = -2.0$ V, $R_{\text{G,off}} = 10\ \Omega$) are used in both half-bridge setups (see Fig. 23). Due to the relatively high values of the employed gate resistors, the difference in the maximum gate drive current capability between both driver units is expected to be neglectable.

The drain–source voltage is captured using a Tektronix MSO-5 oscilloscope (2 GHz) in high-resolution sampling mode (12 bits vertical resolution at 3.125 GS/s) connected to the test setup by a TPP0850 high-voltage single-ended probe (850 MHz, 1.8 pF), which has been customized for coaxial interconnection

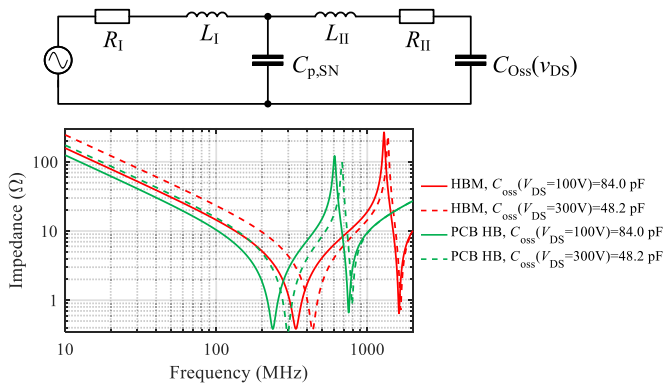


Fig. 24. Schematic and impedance of the extended fourth-order lumped commutation loop model considering the GaN HEMTs parasitic output capacitance.

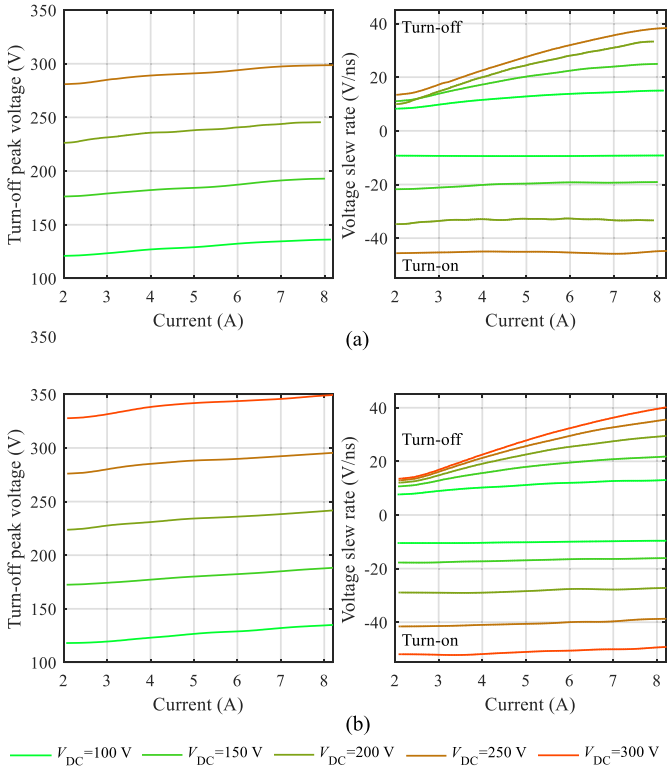


Fig. 25. Drain–source peak voltage during hard-switched turn-off (left) and drain–source voltage slew rate (average 20 %–80%, right; turn-OFF: $\Delta v_{DS}/\Delta t > 0$; turn-ON: $\Delta v_{DS}/\Delta t < 0$) under clamped inductive switching conditions. (a) GaN HBM. (b) PCB HB.

to the GaN HBM and PCB HB test setup. Transient measurements of the GaN HBM are limited to a dc-link voltage up to $V_{DC} = 250$ V as we observed a short-circuit failure in our sample device at $V_{DC} \geq 300$ V related to the GaN HBM layout, while the GaN HEMTs remained intact (see Section V-E).

In the PCB HB design the parasitic turn-OFF drain–source voltage oscillation has a frequency of approx. 265 MHz at $V_{DC} = 250$ V after hard-switched turn-OFF [see Fig. 23(a)]. For reference, the lumped commutation loop model (see Section III-D) is extended by the parasitic output capacitance of the low-side transistor (see Fig. 7) which is in blocking state during the turn-OFF voltage oscillation. Depending on this nonlinear output capacitance, the first pole of the commutation loop impedance shifts within [235; 300] MHz for the PCB HB (see Fig. 24). This is in agreement with the observed turn-OFF oscillation in the double-pulse measurement [see Fig. 23(b), $f_{res} \approx 260$ MHz]. In contrast, for the HBM the captured turn-OFF oscillation is significantly less pronounced due to a higher frequency of approx. 625 MHz at significantly lower amplitude.

The turn-OFF drain–source peak voltage as well as the drain–source voltage slew rate in Fig. 25 are extracted from a series of several hundreds of double-pulse tests similar to Fig. 23. Assuming identical operation parameters, i.e., dc-link voltage $V_{DC} = 250$ V and load current $I_L = 8$ A, the GaN HBM achieves slightly higher voltage slew rates of $+38$ and -45 V/ns during turn-ON and turn-OFF, respectively, compared to $+35$ V/ns and -39 V/ns in the PCB HB. The observed voltage slew rates are expected to be significantly higher for lower gate resistor values as demonstrated in [41] for an earlier device generation based on the same technology platform. The deviation of voltage slew rate between GaN HBM and PCB HB results from the smaller layout-related capacitance of the switching node (see Table II: $C_{p,SN,AlN} = 8$ pF versus $C_{p,SN,PCB} = 32$ pF), leading to faster charging of $C_{p,SN}$ during turn-OFF and discharging during turn-ON. Additionally, a minor impact due to different gate-loop designs of both setups remains possible. The measured turn-OFF peak voltage is similar for both investigated setups. The transistor PCB-submount is the main contributor to the overall stray inductance in the PCB HB [see Fig. 9(b)]. Therefore, the voltage overshoot at the transistor terminals, which is not captured by the measurement, is expected to be notably higher. In contrast, the power transistor chips are directly mounted on the GaN HBM, so that the measured voltage overshoot is in better agreement with the peak overvoltage occurring at the GaN chip.

C. DC/DC Operation

Finally, the general operability is validated in continuous dc/dc hard-switched continuous current mode buck-converter operation where the operation conditions according to Table IV are applied. In- and output voltage as well as currents and converter efficiency are measured using a ZES Zimmer LMG600-series power analyzer. Due to a defect occurring during the double-pulse switching tests of the GaN HBM employing 92 mm GaN transistors (see Section V-C), continuous operation tests are conducted using larger GaN HEMTs ($w_G = 210$ mm), while both the PCB HB and GaN HBM layout remain widely identical. The 92 and 210 mm GaN HEMTs and the associated AlN carriers come from the same fabrication batches and are based on the same technology. The gate resistors according to Table VI are applied to compensate for reduced turn-OFF switching speeds in the 210 mm GaN HBM as elaborated in detail in Section V-E.

In accordance with the thermal characterization results the GaN HBM allows for significantly increased load current from 6 A up to 15 A in switched operation, while the device temperatures are notably lowered by 43 K at the same time [see Fig. 26(a)]. At similar output current the device temperature is further reduced by up to 87 K. At switching frequencies $f_s \geq 100$ kHz the GaN HBM is operated more efficiently compared to

TABLE VI
CONTINUOUS OPERATION PARAMETERS

Parameter		Value
Input voltage	V_{in}	100 V
Duty cycle	D	0.5
Switching frequency	f_s	[50; 200] kHz
Deadtimes	t_D	100 ns
Gate resistors	$R_{G,on}$ / $R_{G,off}$	15 Ω / 3.9 Ω (GaN HBM) 20 Ω / 10 Ω (PCB HB)
Filter inductor	L_{FL}	854 µH
	R_{FL}	42.5 mΩ
	C_{FL}	76 pF
In- and output filter capacitor	C_{FC}	2 mF
	R_{FC}	3.1 mΩ

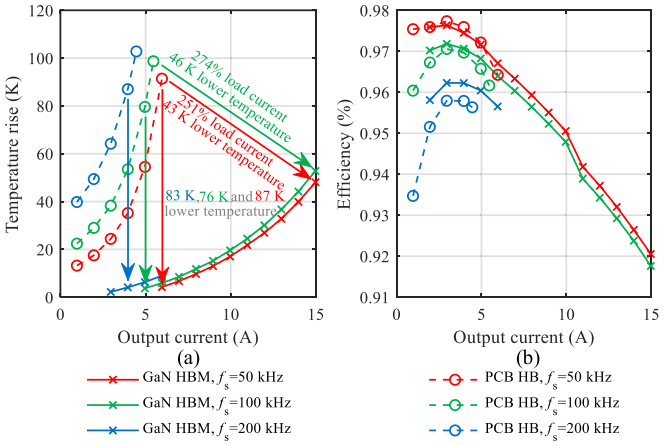


Fig. 26. Comparison of the GaN HBM and PCB HB concerning (a) device temperature rise and (b) efficiency versus average output current in dc/dc operation.

the conventional PCB HB which is mainly related to lower device temperatures and therefore reduced on-state conduction losses [see Fig. 26(b)]. In general, the ESR-related dc-link ripple losses are expected to be higher in the GaN HBM employing only three instead of seven paralleled dc-link MLCC capacitors (see Fig. 5). In most considered operation points, increased dc-link ripple losses occurring in the GaN HBM are (over)compensated by lower conduction losses due to improved cooling capability compared to the PCB HB. Assuming a low switching frequency $f_s = 50$ kHz and load currents $I_{out} = [2; 5]$ A the transistors are operated at moderate device temperature and therefore moderate conduction losses even in the PCB HB. Considering these specific operation conditions combined with increased turn-OFF losses of the GaN HBM (see Section V-E), the efficiency of the GaN HBM is slightly reduced compared to the reference PCB HB.

D. Discussion of Prospective System Design Advantages

The proposed GaN HBM allows for a flexible multilayer layout design integrating the GaN HEMTs on a thermally conductive AlN carrier. The implemented assembly technology achieves similar or even lower values of most parasitic circuit elements compared to the conventional four-layer reference PCB HB. Thermal characterization measurements as well as switched

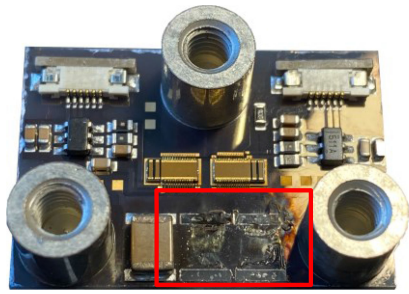


Fig. 27. Damaged GaN HBM using 92 mm GaN HEMTs showing dc-link short circuit and delamination of metallization layers after double-pulse testing at $V_{DC} = 300$ V.

dc/dc operation have proven significantly higher cooling capability of the GaN HBM enabling lower device temperatures at higher load currents and therefore reduced thermal device stress. The measured switching characteristics validate reduced parasitic oscillations, and in consequence, electromagnetic interference is expected to be reduced, resulting in minimized filter effort. These advantages of the proposed GaN HBM technology can be used to improve power electronic systems according to the particular optimization strategy in terms of efficiency, power density, and system reliability.

E. Discussion of Remaining Technological Limitations

The GaN HEMTs and the AlN carrier with integrated layout traces are the critical building blocks of the proposed GaN HBM. High-voltage operation of the power transistors has been previously validated in [41] and [42] as well as characterization measurements of the PCB HB up to $V_{DC} = 450$ V. The AlN-integrated layout assembly has been qualified through static leakage measurements up to $V_{DC} = 600$ V (see Fig. 3). The thermal characterization presented in Section V-A has further proven the improved cooling capability at a time-constant dc-current and thermal stress. In double pulse switching tests and dc/dc operation, the GaN HBM is excited to combined thermal, electrical, and even mechanical stress. The initial prototype GaN HBM sample using 92 mm GaN HEMTs has successfully demonstrated switched operation up to 250 V but failed at a higher dc-link voltage $V_{DC} \geq 300$ V (see Section V-B) which is lower than the originally targeted operation voltage of $V_{DC} = 500$ V, and also lower than the breakdown capability of the AlN assembly and power transistors. The damaged GaN HBM exhibits a dc-link short circuit as well delamination of the metallization layers in the mounting area of the on-board DC-link MLCCs while the GaN HEMTs remained intact (see Fig. 27). The observed fault can be attributed to a breakdown of the BCB isolation layer, possibly due to mechanical strain occurring during the assembly and the soldering process of the on-board components. Accordingly, upcoming investigation are targeting improved system reliability in addition to separate qualification of the individual subcomponents. A second closely related issue was observed during loss measurements in dc/dc operation based on the second GaN HBM sample using 210 mm GaN HEMTs. In agreement with double pulse measurements in

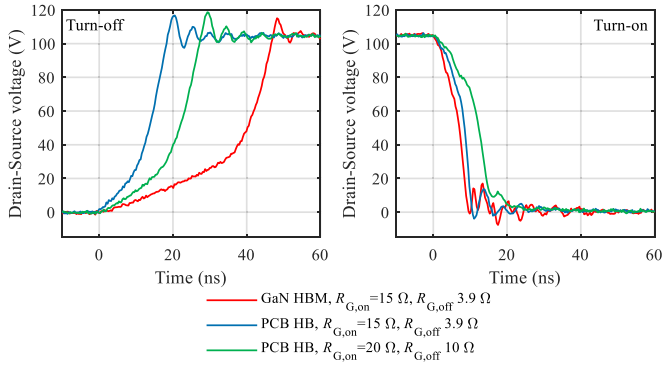


Fig. 28. Comparison of switching transients of the GaN HBM and PCB HB using 210 mm GaN HEMTs and different gate resistor configurations in continuous dc/dc operation and thermal steady state, $I_L = 5$ A.

Section V-B, switching tests show that the GaN HBM achieves a slightly faster turn-ON transition using the same gate resistor configuration as the reference PCB HB (see Fig. 28, right, red versus blue plot lines). In contrast, the turn-OFF transition (see Fig. 28, left) of the GaN HBM is significantly slower compared to the PCB HB, even if the latter uses larger gate resistors. This leads to significantly increased turn-OFF losses of the GaN HBM. Subsequent analyzes of the GaN HBM revealed a damage of the metallization layer at the gate resistor mounting pad resulting in an increased turn-OFF gate resistance. The defective solder pad was attributed to a partial dissolution of the gold metallization during the soldering process. Improvements of the GaN HBM were tackled within the Au fabrication process by including an additional metallization level consisting of a stack of Ti/Pt/Au in order to ensure a proper soldering finish for the required assembly components on the AlN carrier. This resulted in increased reliability and mechanical robustness of the solder pads validated by several soldering test runs. Accordingly, implementing these process optimizations into the upcoming iterations of the GaN HBM promises a significant reduction of turn-off losses and increased efficiency compared to the reference PCB HB.

VI. Conclusion

The proposed half-bridge module integrates a GaN HEMT switching cell, including the gate drive circuitry on a multilayer AlN-substrate. This module achieves four times smaller parasitic capacitance of the switching node, as well as lower commutation loop inductance than the reference PCB design. Furthermore, the proposed HBM module demonstrates significantly enhanced cooling capability along with slightly improved switching behavior.

Future optimization of the GaN half-bridge module will tackle design variations based on a vertical commutation loop to achieve even lower parasitic inductances, compared to the horizontal commutation loop design presented here. A pareto optimum design will further consider thermal and electrical constraints. Furthermore, interaction of on-chip transistor structures such as gate-, drain-, and source-busses and the module's layout need to be considered. Based on the analysis detailed in this article, further developments in terms of layout optimization and technological adjustments are currently considered for higher dc-link voltages. The applied AlN technology is in general suitable for and aims at GaN power modules operating at more than 600 V while successful switched operation has been limited to 250 V so far. Accordingly, the ongoing optimization of the GaN HBM processing technology targets improved system reliability under combined thermal, electrical, and mechanical stress conditions.

Finally, the concept of hybrid integrated power electronics demands for further optimization on module- and system-level: While the integrated module presented here is limited to the fundamental half-bridge converter, more complex converter topologies applying the same hybrid integration approach should be considered. The further integration of a filter stage is a feasible option to de-couple parasitic capacitances of loads connected to the output terminal. On system level, optimized micro cell power electronic components like the proposed integrated half-bridge module can serve as a fundamental building block of larger power electronic systems. Such macro systems, containing several micro cells could be dynamically reconfigured according to changing application demands.

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Carsten Kuring received the B.Eng. degree in electrical engineering and information technology from HTWK Leipzig, Leipzig, Germany, in 2013, and the M.Sc. degree in electrical engineering from Friedrich-Alexander University Erlangen-Nuremberg, Erlangen, Germany, in 2016. He is currently working toward the Ph.D. degree in the Power Electronics Research Group, Technische Universität Berlin, Berlin, Germany, focuses on characterization and application of wide-bandgap GaN and Ga_2O_3 power electronics.

Mihaela Wolf (Alexandru) received the Ph.D. degree in electronic engineering from Polytechnics University of Cataluña, Cataluña, Spain, in 2013.

In 2009, she joined the Group of Power Devices and Systems, IMB-CNM (CSIC), Barcelona, Spain. Her main research activity has been dealing with modeling, design, and characterization of silicon carbide semiconductor devices, development of digital integrated circuits on SiC, and reliability and irradiation effects on SiC devices. As a postdoc, she joined TU Dresden, Germany, dealing with electrothermal modeling and characterization methods for CNTFETs. Since 2016, she has been with Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, Berlin, Germany, dealing with the design and development of GaN power devices and monolithically integrated GaN power systems, characterization and investigation of switching dynamics, and reliability effects of GaN power devices.

Xiaomeng Geng received the B.S. degree from China Agricultural University, Beijing, China, in 2015, and the M.S. degree from Technische Universität Berlin, Berlin, Germany, in 2019, both in electrical engineering. She is currently working toward the Ph.D. degree in power electronics in Technische Universität Berlin, Berlin, Germany.

Her research interests include application of wide bandgap semiconductor device, high-frequency converters, and layout optimization toward high-frequency applications.

Oliver Hilt received the Ph.D. degree in experimental physics from Free University Berlin, Berlin, Germany, in 1995, for his work on the delocalized charge transport in liquefied rare gases, which was performed at the Hahn-Meitner-Institut Berlin, Berlin.

For his postdoctoral work with the Delft University of Technology, Delft, The Netherlands, and Leiden University, Leiden, The Netherlands, he analyzed the charge transport mechanisms in organic conductors and semiconductors for optoelectronic applications. In 1999, he joined the sglux GmbH, Berlin, to develop a titanium-dioxide-based wide-band-gap ultraviolet photodiode. After the successful introduction of the photodiode to the market in 2003, he was promoted to Chief Executive Officer. In 2006, he joined the Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin, for the development of GaN switching transistors for high-voltage power applications and is currently the Head of the GaN Power Electronics Group.

Jan Böcker received the M.Sc. degree in electrical engineering from the Technische Universität Berlin, Berlin, Germany, in 2013, and the Dr.-Ing. degree in electrical engineering, in 2020.

Since then, he has been as a Research Associate with the Power Electronics Group, Technische Universität Berlin, focusing on wide bandgap devices and highly compact converter design. His research interests include control strategies for dc–dc converters and various converter topologies in drive and grid applications, particularly the modular multilevel converter.

Joachim Würfl (Member, IEEE) received the Ph.D. degree in electrical engineering from the Technical University of Darmstadt, Darmstadt, Germany, in 1989, where he focused on the technology and design of high temperature and high-power GaAs-based devices.

As a postdoc, he developed micromechanical sensors based on III/V compound semiconductors with the Technical University of Darmstadt. Since 1992, he has been with the Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin, Germany, where he has been responsible for clean room technology, process development, and processing of III/V optoelectronic and microwave devices. Additionally, he has been in charge of the design and development of power heterojunction bipolar transistors and power GaN devices. In 2007, he has been appointed the Head of the newly implemented business field GaN electronics. In this function, he is managing several projects on GaN-based L- and X-band power devices and monolithic microwave ICs, high-voltage power devices, and high-frequency robust lownoise amplifiers. He is responsible for the design, technological implementation, characterization, and reliability testing of these devices. He has authored more than 100 scientific papers in related fields.

Sibylle Dieckerhoff (Member, IEEE) received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from RWTH Aachen University, Aachen, Germany, in 1997 and 2004, respectively.

From 1997 to 2002, she was a Research Associate with the Institute for Power Electronics and Electrical Drives, RWTH Aachen, and Daimler-Chrysler Research and Technology, Berlin, Germany. In 2003, she joined Siemens AG, Krefeld, Germany, as a Development Engineer, followed by positions as a Senior Researcher with the Technical University of Berlin (TU Berlin), Berlin, and as a Professor with the Beuth University of Applied Sciences Berlin. Since 2010, she has been a Professor of power electronics with TU Berlin. Her research interests include wide bandgap power devices and their application, grid converters and their control in electric grids, and multilevel converters.

Dr. Dieckerhoff was a member of the Administrative Committee of the IEEE Power Electronics Society from 2017 to 2019 and has served as the Vice-Chairperson of the German ETG/VDE Steering Committee from 2013 to 2016. She is also a member of the International Scientific Committee of the European Power Electronics and Drives Association (EPE).