Frequency-Based Active Ripple Compensation Technique to Reduce Bulk Capacitance in Integrated Offline LED Drivers

Ruan M. Ferraz, Lucas H. G. Resende, Henrique A. C. Braga, *Senior Member, IEEE*, Pedro S. Almeida, *Member, IEEE*, J. Marcos Alonso, *Fellow, IEEE*, and Guilherme M. Soares, *Member, IEEE*

***Abstract*—In order to increase the power density and the lifespan of light-emitting diodes (LED) drivers, several studies have proposed active ripple compensation (ARC) techniques for minimizing the converter bulk capacitance. However, a common side effect of the ARC method is the increase in the total harmonic distortion (THD) of the converter input current. In this context, a frequency-based ARC technique is proposed as an alternative to the conventional ARC methodology, in which the duty cycle is modulated. The analyses presented in this article show that the frequency-based ARC approach applied to resonant converters has a better performance than the one used in hard-switching converters, since it allows for a huge capacitance reduction with a small THD increase. Furthermore, this article presents a generalized analysis of ARC techniques applied to integrated offline LED drivers, which reduce the number of components and the overall LED driver cost. The input current harmonic content and the output ripple reduction have been theoretically predicted for several converters. Experimental results gathered from a 96-W laboratory prototype supplied from a 127-V 60-Hz grid attested the superior performance of the frequency-based active ripple compensation, since a capacitance reduction of 66.6% has been obtained with an increase of only 0.9% in the THD.**

***Index Terms*—Active ripple compensation (ARC), capacitance reduction, high power factor (PF), light-emitting diode (LED) drivers, resonant converter.**

Manuscript received February 18, 2022; revised April 20, 2022; accepted May 16, 2022. Date of publication May 23, 2022; date of current version June 24, 2022. This work was supported in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - Brasil (CAPES) - Finance Code 001, in part by the National Council for Scientific and Technological Development under Grant 408114/2018-5, in part by INERGE and FAPEMIG under Grant APQ-01435-18, in part by the Brazilian Institution the Federal University of Juiz de Fora (UFJF), and in part by Spanish Government under Grant PID2019-105568RB-I00. Recommended for publication by Associate Editor M. Ponce-Silva. *(Corresponding author: Ruan M. Ferraz.)*

Ruan M. Ferraz, Lucas H. G. Resende, Henrique A. C. Braga, and Pedro S. Almeida are with the Universidade Federal de Juiz de Fora, Juiz de Fora 36036-900, Brazil (e-mail: ruan.ferraz@engenharia.ufjf.br; lucas.resende@engenharia.ufjf.br; henrique.braga@ufjf.edu.br; pedro.almeida@engenharia.ufjf.br).

J. Marcos Alonso is with the Electrical Engineering Department, University of Oviedo, 33003 Oviedo, Spain (e-mail: marcos.uniovi@gmail.com).

Guilherme M. Soares is with the Energy, Federal University of Juiz de Fora, Juiz de Fora, Minas Gerais 36036-900, Brazil (e-mail: guilherme.marcio@ufjf.edu.br).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3177155.

Digital Object Identifier 10.1109/TPEL.2022.3177155

I. Introduction

LIGHT-EMITTING diodes (LEDs) have becoming the main source of artificial lighting. Features, such as high luminous efficacy, high-color-rendering index, low operating temperature, ability to emit white light, small size, and long life, make them advantageous in lighting, especially because of their potential of reducing energy consumption [1]–[4].

In order to maximize the benefits of the technology, the LED must be properly driven by an electronic circuit. This device must control the average value and ripple level of the LED current, which can significantly affect the photometric performance of the LEDs [5]. Furthermore, the current ripple can cause stroboscopic and flickering effects, which could be noticeable to the human eye in some circumstances [6]. Thus, this undesirable low-frequency (LF) ripple in the LED current is a limiting factor for solid-state lighting systems [7], [8].

The subject of LF ripple is especially important in offline LED power supplies, since the pulsating single-phase power at the input produces a LF voltage ripple at its output at a frequency twice that of line frequency. These instantaneous power oscillations are typically filtered out by electrolytic capacitors, which are known to reduce the circuit lifespan, or alternatively by using a bank of metallized film capacitors, which have a better lifespan, but decrease the power density of the drivers [9], [10].

In order to mitigate these problems and to attenuate the output current ripple, some studies have proposed techniques based on alternative topologies [11], [12], on design procedures [13]–[15], or on control techniques [16]–[25]. Among the aforementioned alternatives, two-stage LED drivers, which are composed of a power control (PC) stage connected at the output of the power factor correction (PFC) stage, have been used to reduce the LF ripple. In order to reduce the component count and the driver cost, some works have proposed the use of integrated topologies, which are based on the integration of the PFC and the PC stages [15], [24].

Regarding the alternatives based on control methods, some studies rely on the reduction of the instantaneous power unbalance between the input and the output of the converter [19]–[21], [23]–[25]. This approach for capacitance minimization, also called active ripple compensation (ARC), is implemented by a large-signal modulation of the control variables of the LED driver. Although this technique usually provides good results in

terms of capacitance reduction, it has the drawback of increasing the input current distortion, mainly when it is employed in pulse width modulation converters. Thus, most of the ARC techniques proposed in the literature allows for reducing the output current ripple at the cost of an increase in the input current total harmonic distortion (THD).

In this context, this article proposes an alternative that allows for output ripple compensation with a lesser negative impact on THD, the switching frequency modulation, which can be applied to resonant PC stages, thus improving the overall LED driver efficiency by employing soft-switching [15]. Furthermore, this article presents a more complete and generalized analysis of the ARC technique based on this large-signal modulation of the control variable in integrated offline converters. In this way, as will be shown, the strategy of the switching frequency modulation has several advantages and can be used to design LED drivers with high efficiency and very low capacitance.

The rest of this article is organized as follows. Section II presents the generalized analysis of the ARC technique based on the large-signal modulation of the control variable. Section III addresses the design example of an integrated offline LED driver associated to the switching frequency-based ARC technique. Section IV presents the experimental results from a laboratory prototype. Finally, Section V concludes this article.

II. Active Ripple Compensation Techniques

This section presents the study of the ARC technique based on the large-signal modulation of the control variable in integrated offline LED drivers, comparing duty cycle versus switching frequency modulation. The analysis carried out in this section considers that the driver is based on integrated topologies whose first stage (PFC) operates in the discontinuous conduction mode (DCM), since it allows the converter to achieve a high power factor (PF) without using a loop for controlling the input current.

The effectiveness of the ARC technique when applied to integrated converters is related with the frequency response characteristic of such converters. As given in [26], the output-to-control transfer function of an integrated converter depends only on the output stage. In addition, the operating principles of each stage are preserved although they share switches. Therefore, both stages can be discussed separately in order to simplify the analysis. First, the PFC stage with duty cycle or frequency modulation will be considered to calculate the THD. Thereafter, the values of the ARC parameters required to reduce the LF ripple in the LED current will be evaluated in the PC stage.

The line voltage can be defined by its root mean square (rms) value V_G and angular frequency ω_L, as described by (1). In offline converters, it is well-known that the main variables (e.g., the output current) oscillate at twice the line frequency. Similarly to what was presented in [25], an extra control parcel at twice the line frequency has been added, thus allowing it to influence the large-signal behavior of the converter. In this way, the duty cycle and the switching frequency functions used in the analysis of this section may well be represented by (2) and (3), respectively.

$$v_g(t) = \sqrt{2}V_G \sin(\omega_L t) \tag{1}$$

$$d(t) = d_0[1 + k_d \sin(2\omega_L t + \varphi_d)] \tag{2}$$

where d_0 is the dc component, k_d the relative amplitude, and φ_d is the modulation phase of duty cycle modulation.

$$f(t) = f_0[1 + k_f \sin(2\omega_L t + \varphi_f)] \tag{3}$$

where f_0 is the dc component, k_f is the relative amplitude, and φ_f is the modulation phase of switching frequency modulation.

A. PFC Stage Analysis

The analysis outlined in this section aims to present the main topologies applied to a single-phase voltage-mode controlled PF preregulators, addressing the ARC characteristics regarding each one. It is important to highlight that although uncommon, the analysis of the ARC technique presented here also considers PFC preregulators with variable frequency, thus allowing a comparison with duty cycle modulation. The PFC preregulators that operate in DCM behave like voltage-followers, which allows them to achieve a high PF at their input. However, depending on the converter, it is not possible to have an ideal sinusoidal current at the converter input, being that nonsinusoidal current condition, the case of buck and boost-type topologies. On the other hand, the buck–boost-type topologies can achieve a unity PF when operating in DCM.

Some considerations are made to simplify the analysis as follows. All input current harmonics are suppressed by the electromagnetic interference (EMI) filter. The modulations of duty cycle and of switching frequency are not introduced simultaneously. The dc-linked capacitor (i.e., output capacitor of the PFC stage) is large enough, so that the bus voltage $v_B(t)$ can be treated as a constant value, and therefore does not interfere in the THD analysis of the converter with the ARC technique.

The harmonic content of the input current can be obtained by using the Fourier series. The amplitude of the hth order harmonic component of the converter input current can be calculated by (4). In this work, the THD of the input current was chosen to evaluate the power quality of the converter, as given in (5).

$$I_h = \frac{2}{T_L}\int_0^{T_L} \sin(h\omega_L t) i_g(t) \mathrm{d}t \tag{4}$$

where T_L is the line period and h is the harmonics order of the line frequency.

$$\mathrm{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1}. \tag{5}$$

Furthermore, the deviation of THD of PFC preregulators, which is calculated according to (6), represents an interesting parameter for the generalized analysis of the ARC technique.

$$\Delta\mathrm{THD} = \mathrm{THD}_m - \mathrm{THD}_o \tag{6}$$

where THD_m is the THD of the preregulator with the ARC technique and THD_o is the THD of the preregulator when the ARC technique is not used.

TABLE I
EQUATIONS OF PFC PREREGULATORS OPERATING IN DCM

Topology	Input current of the PFC stage: i_g	PFC stage inductance design equation
Buck PFC preregulator	$\begin{cases} \frac{d^2(\lvert v_g\rvert - v_B)}{2fL_{bu}}, & \text{if } \lvert v_g\rvert > v_B \text{ and } v_g > 0 \\ -\frac{d^2(\lvert v_g\rvert - v_B)}{2fL_{bu}}, & \text{if } \lvert v_g\rvert > v_B \text{ and } v_g < 0 \\ 0, & \text{if } \lvert v_g\rvert \le v_B \end{cases}$ (8)	$L_{bu} = \frac{\eta}{T_L P_o}\int_{t_1}^{\frac{T_L}{2}-t_1} \frac{v_g(\lvert v_g\rvert - v_B)d^2}{f}\mathrm{d}t,$ (9) where t_1 is the instant of time given by $t_1 = \frac{T_L}{2\pi}\sin^{-1}\left(\frac{V_B}{\sqrt{2}V_G}\right).$ (10)
Boost PFC preregulator	$\frac{d^2}{2fL_{bo}}\left(\frac{v_g v_B}{v_B - \lvert v_g\rvert}\right).$ (11)	$L_{bo} = \frac{\eta}{T_L P_o}\int_0^{T_L} \frac{v_B d^2 v_g^2}{f(v_B - \lvert v_g\rvert)}\mathrm{d}t.$ (12)
Buck–boost PFC preregulator	$\frac{d^2}{2fL_{bb}}v_g.$ (13)	$L_{bb} = \frac{\eta}{T_L P_o}\int_0^{T_L} \frac{d^2 v_g^2}{f}\mathrm{d}t.$ (14)

Table I gives the input current equations for buck, boost, and buck–boost preregulators according to [27]. The input current of a converter using the ARC technique is also affected by LF large-signal modulation of the control variable, so that the power processed by the converter is also modified according to the values of such parameters. Therefore, the PFC stage inductance, whose value can be obtained by using the third column equation of Table I, can be calculated by means of the power balance between the input and the output of the converter, as stated in (7), by considering the control variable modulation.

$$\frac{1}{T_L}\int_0^{T_L} v_g(t) i_g(t)\mathrm{d}t = \frac{P_o}{\eta} \tag{7}$$

where P_o is the output power and η is the global efficiency of the integrated converter.

1) Buck PFC Preregulator: The input current is proportional to the input voltage, but only within the time interval in which the rectified line voltage is higher than the bus voltage. When $|v_g(t)|$ falls below the bus voltage, the input current is zero. The period in which the input current is not zero was named as conduction angle θ. The higher the conduction angle, the closest the input current to a perfect sine waveform, and the lower the harmonic content. According to [28], a minimum conduction angle of 130° is necessary in order to ensure the compliance with the international electrotechnical commission (IEC) 61000-3-2 class C standard.

Fig. 1 shows the deviation of THD, defined in (6), of buck PFC preregulator for two values of θ. For each conduction angle, a set of curves was generated, being each one characterized by a certain value of modulation angle and plotted for several values of relative amplitude modulation (k_d and k_f). In order to ensure the average power balance of the converter, for each point on the graph a new value of the buck inductance must be calculated, so that the power delivered to the load remains constant.

As shown in Fig. 1, the cases that presented the harmonic components of the input current above the limits of the IEC 61000-3-2 standard were highlighted in red. The ARC technique has little influence on the value of the THD when the relative amplitude of the modulation (k_d and k_f) is low, especially for modulation angles of 0° and 180°. On the other hand, the control

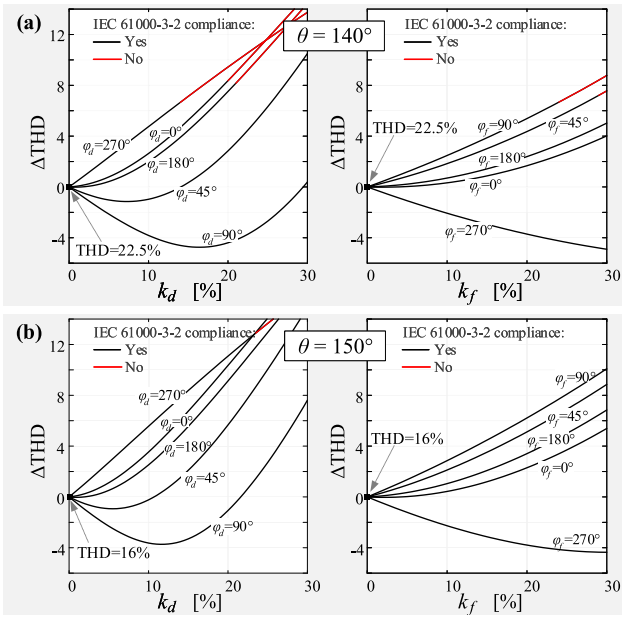


Fig. 1. Deviation of THD for buck PFC preregulator operating in DCM with the ARC technique modulating duty cycle or switching frequency. (a) conduction angle of $\theta = 140°$; (b) conduction angle of $\theta = 150°$.

variable modulation can be used to reduce the input current distortion. The highest THD reduction occurs when $\varphi_d = 90°$ in $d(t)$ modulation and when $\varphi_f = 270°$ in $f(t)$ modulation. In general, the THD of the converter is less sensitive to k_f when compared to k_d, thus allowing a larger $f(t)$ modulation. For example, with $\theta = 150°$ and $\varphi_d = \varphi_f = 0°$, $\Delta\text{THD} = 4\%$ (i.e., $\text{THD} = 20\%$) is obtained when $k_d = 11\%$ or $k_f = 25\%$. As mentioned before, a minimum conduction angle of 130° is necessary for the conventional buck PFC preregulator in order to ensure the compliance with the IEC 61000-3-2 class C standard. However, the value of this angle can be reduced with the ARC technique, i.e., the buck PFC preregulator with ARC can be used in applications that demand higher output voltages.

2) Boost PFC Preregulator: The input current of the PFC boost operating in DCM depends on the value of the bus voltage, and therefore of the dc static gain (V_B/V_G). According to [15], the converter only meets the requirements of the IEC

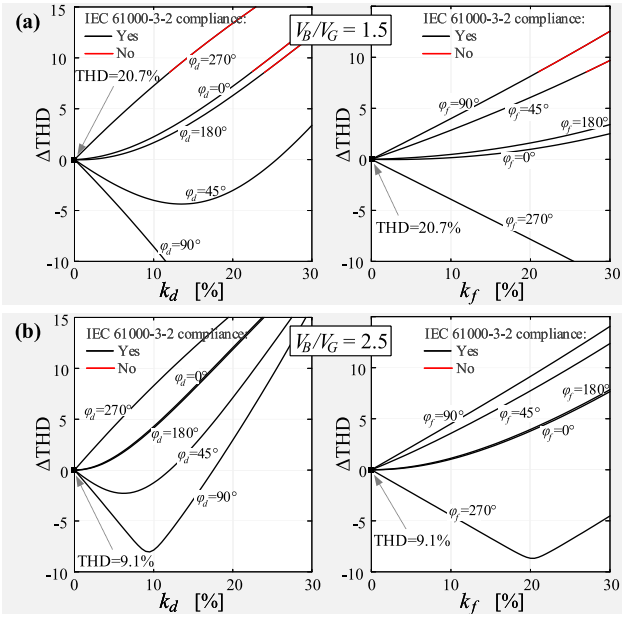


Fig. 2. Deviation of THD for boost PFC preregulator operating in DCM with the ARC technique modulating duty cycle or switching frequency. (a) dc static gain of $V_B/V_G = 1.5$; (b) dc static gain of $V_B/V_G = 2.5$.

61000-3-2 class C standard if the dc static gain is larger than 1.27. Similar to the buck converter analysis, the ΔTHD of boost preregulator with the ARC technique for some values of V_B/V_G was shown in Fig. 2. For each dc static gain, a set of curves was generated, being each one characterized by a certain value of modulation phase and plotted for several values of relative amplitude modulation. For each case in the graph, the boost inductance is recalculated by (12) to keep the output power constant.

As verified in the buck converter, the input current distortion can be reduced by the control variable modulation, especially when $\varphi_d = 90°$ in $d(t)$ modulation and when $\varphi_f = 270°$ in $f(t)$ modulation. The results show that the deviation of the THD of boost preregulator can increase as the relative amplitude of modulation grows. However, this variation is smaller for $f(t)$ modulation when compared to $d(t)$ modulation. It is important to highlight that boost PFC preregulator in association with the ARC technique can also meet the requirements of the IEC 61000-3-2 class C standard with the dc static gain less than 1.27 if the purpose is not capacitance reduction.

3) Buck–Boost PFC Preregulator: Differing from the buck- and boost-type preregulators, the input current shape of the buck–boost PFC operating in DCM does not depend on the bus voltage. Therefore, the input current waveform is ideally sinusoidal, if the duty cycle and the switching frequency are kept within a half line cycle.

Fig. 3 shows the ΔTHD of buck–boost preregulator with the ARC technique for several values of k_d and k_f, keeping the output power constant. Since the input current waveform is assumed sinusoidal, the deviation on THD for buck–boost preregulator always increases, as the relative amplitude of large-signal modulation from ARC grows. The figure shows that the input current distortion does not depend significantly on the modulation angle

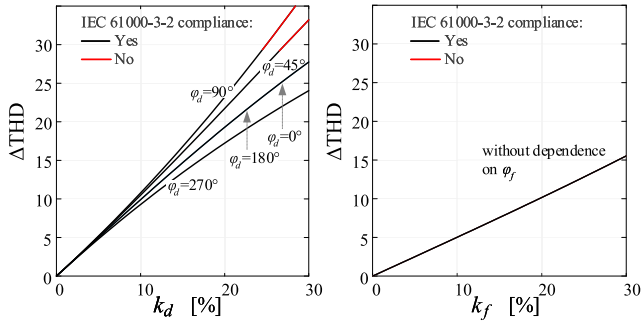


Fig. 3. Deviation of THD for buck–boost PFC preregulator operating in DCM with the ARC technique modulating duty cycle or switching frequency.

when a large-signal modulation of the switching frequency is used. In addition, k_d has a greater influence than k_f on ΔTHD.

This section compared the more conventional and known ARC approach of duty cycle large-signal modulation with a novel ARC technique based on the switching frequency large-signal modulation, both applied to the three basic PFC preregulator topologies operated in DCM. The analyses showed that the $f(t)$ modulation has a lower impact on the power quality when compared with the duty cycle modulation. Furthermore, the large-signal modulation of the switching frequency can be used for the purpose of power quality improvement, which allows for the use of buck and boost topologies in compliance with the IEC 61000-3-2 class C standard over a wide voltage gain range (V_B/V_G), or, as proposed in this article, aiming the capacitance reduction in order to increase the power density and the lifespan of LED drivers. Regarding capacitance reduction, the LF ripple transmission must also be analyzed, thus the ART technique can be evaluated according to the input current distortion and to the LF output current ripple in integrated offline LED drivers.

B. PC Stage Analysis

This section presents how the deliberate modulation of the control variable impact the LF ripple transmission of the converters used as a PC stage. First, a converter sensitivity analysis will be presented in order to show the behavior of the converters with the control variable modulation. Thereafter, the values of the ARC parameters required to reduce the LF ripple will be measured and related to the THD analysis shown in the previous section.

Because in many drivers, the bus voltage is significantly larger than the output voltage, step-down converters are typically employed as the second stage in offline LED drivers. Three topologies are studied in this section: 1) buck and 2) buck–boost operating in DCM; and 3) *LLC* resonant converter with frequency modulation, which is a converter fairly common in offline medium- and high-power LED drivers and has become an industry standard in these offline applications. In order to produce more generalized results, some parameters of the *LLC* converter were normalized as follows.

1) Q is the normalized ac-side load resistance.

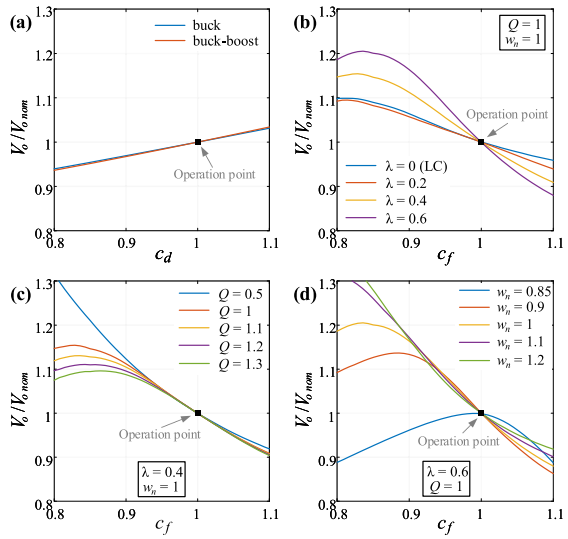


Fig. 4. Normalized output voltage of converters as the PC stage. (a) Buck and buck–boost converters. (b) *LLC* resonant converter for variations of λ. (c) *LLC* resonant converter for variations of Q. (d) *LLC* resonant converter for variations of ω_n.

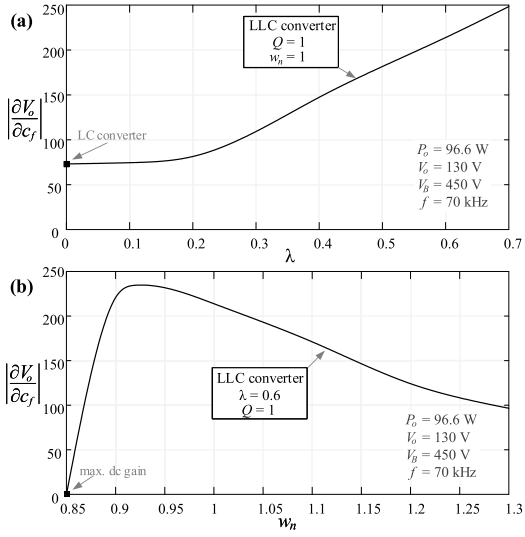


Fig. 5. Sensitivity analysis of the *LLC* converter used as the PC stage for several values of (a) λ; and (b) ω_n.

2) λ is the inductance ratio, which can be found by dividing the series inductance by the magnetizing inductance.
3) ω_n is the normalized design switching frequency.

In order to investigate the behavior of the output voltage of the converters, the normalized output voltage was evaluated for variations of the control variable, as shown in Fig. 4. The ARC technique was disregarded in this analysis ($k_d = k_f = 0$). In addition, the normalized control variables were defined as $c_d = D/D_{\text{nom}}$ and $c_f = f/f_{\text{nom}}$ for variations in the duty cycle and switching frequency, respectively. Fig. 4(a) presents the behavior of the normalized output voltage V_o/V_{nom} of the buck and buck–boost converter designed for the same operating point (nominal duty cycle D_{nom} and nominal output voltage V_{nom}). Both converters present a quasilinear behavior and have very similar curves and sensitivities.

Fig. 4(b) shows the normalized output voltage of the *LLC* converter according to variations in the switching frequency for several values of λ. The results show that at the operating point, the curve slope (i.e., parametric sensitivity) increases as the inductance ratio grows. The lowest output voltage sensitivity occurs when $\lambda = 0$, which is a specific case of the *LLC* converter, known as *LC* series resonant converter. It is important to highlight that the curves were obtained from the design methodology, and the accurate modeling for an *LLC* resonant converter was proposed in [29], which is able to accurately predict the LED current.

Fig. 4(c) shows the normalized output voltage for several values of Q. As can be seen, the impact of the quality factor becomes negligible around the operating point. Fig. 4(d) presents the normalized output voltage according to variations in the switching frequency for several values of normalized design switching frequency. As expected, the *LLC* converter operates very close to the maximum dc gain as ω_n reduces, a case that should be avoided to ensure operation under zero voltage switching (ZVS) conditions (inductive tank characteristic). On the other hand, the *LLC* converter is typically designed to operate at the series resonant frequency ($\omega_n = 1$), thus obtaining greater efficiency and better power quality. This case allows a wide variation of the switching frequency value while preserving the ZVS operation. In this sense, Fig. 4 shows that the inductance ratio has a major influence on the *LLC* converter sensitivity.

In order to quantify the sensitivity related to converters used as the PC stage, a case with $P_o = 96.6$ W, $V_o = 138$, $V_B = 450$ V, and $f(t) = 70$ kHz was investigated, considering the converters evaluated in Fig. 4. The sensitivity can be calculated as the partial derivative of the *LLC* average output voltage with respect to the normalized switching frequency, which is denoted as $\partial V_o/\partial c_f$. Fig. 5(a) shows the sensitivity analysis in absolute values for several values of inductance ratio. As can be seen, the sensitivity of the *LLC* converter increases as λ grows. Fig. 5(b) shows the sensitivity analysis in absolute values for several values of ω_n. When the *LLC* converter is operating close to the maximum dc gain, the sensitivity increases as ω_n grows. However, in the region in which the converter is usually designed to operate, this sensitivity reduces with increasing normalized frequency.

Regarding the hard-switching dc–dc converters, the sensitivity to duty cycle can be obtained by the partial derivative of the output voltage with respect to the normalized duty cycle ($\partial V_o/\partial c_d$). In this way, the sensitivity to duty cycle of the buck and buck–boost converter are constant and equal to 43 and 46 V, respectively. Although uncommon, the $f(t)$ modulation was also evaluated in the hard-switching topologies (i.e., buck and buck–boost). In these examples, $|\partial V_o/\partial c_f|$ of the buck and buck–boost converter are equal to 22.1 and 23.5 V, respectively. Therefore, these hard-switching converters have a sensitivity to $d(t)$ modulation approximately twice that to $f(t)$ modulation. On the other hand, load-resonant converters can be considered more sensitive than hard-switching converters, thus requiring a lower relative amplitude modulation—thus a lower control effort—for achieving the same ripple reduction.

TABLE II
PARAMETERS OF THE ARC TECHNIQUE (k_d OR k_f) FOR OUTPUT RIPPLE REDUCTION

			$\Delta I_{o\%}$			
		PC stages	100%	75%	50%	25%
Relative amplitude of the modulation (%)	k_d See (2)	Buck	0%	7%	13%	20%
		Buck-boost	0%	6.7%	13.5%	20.5%
	k_f See (3)	Buck	0%	14%	27.5%	40%
		Buck–boost	0%	14%	27.5%	39.8%
		LC (λ = 0)	0%	2%	4.2%	6.8%
		LLC (λ = 0.2)	0%	1.5%	2.5%	4%
		LLC (λ=0.4)	0%	0.75%	1.5%	2.2%
		LLC (λ=0.6)	0%	0.5%	1%	1.5%

TABLE III
ΔTHD OF INTEGRATED CONVERTERS WITH THE ARC TECHNIQUE FOR $\Delta I_{o\%} = 50\%$

PC stages	Control variable	ΔTHD–see (6) Buck PFC	boost PFC	Buck–boost PFC
Buck	Duty cycle	5.4%	6.5%	12.8%
Buck–boost		5.7%	6.9%	13.3%
Buck	frequency	5.9%	6.8%	13.9%
Buck–boost		5.9%	6.8%	13.9%
LC (λ = 0)		0.26%	0.22%	2.1%
LLC (λ = 0.2)		0.13%	0.08%	1.25%
LLC (λ = 0.4)		0.06%	0.03%	0.75%
LLC (λ = 0.6)		0.04%	0.02%	0.5%

Finally, the previously studied converters were evaluated with the ARC technique in order to show the effect of large-signal modulation on the output ripple reduction. Table II gives k_d and k_f modulation amplitudes required to reduce the LF ripple in the LED current for several cases of dc–dc converters used as a PC stage. These converters are supplying an LED lamp with dynamic resistance $r_d = 12\ \Omega$ and nominal threshold voltage $V_t = 129.6$ V. The values of the average output current and the output current ripple were 700 mA for this analysis, when k_d and k_f are equal to zero, thus obtaining an LF current ripple of 100%. The value of the bus ripple that ensures the LF ripple criterion was chosen for each converter. In order to obtain the maximum ripple reduction, the modulation phase was chosen, so that $d(t)$ is completely out of phase with the ac portion of the bus voltage of the hard-switching dc–dc converters. In other words, $\varphi_d = 0\%$, since the phase of the ac portion of the bus voltage is equal to 180°. Regarding the switching frequency modulation, the modulation phase was chosen, so that $f(t)$ is in phase with the ac portion of the bus voltage, i.e., $\varphi_f = 180°$.

The results show that the ARC technique has a better performance in terms of ripple reduction in converters with higher sensitivity. For example, the output current ripple of 50% is obtained when $k_d = 13\%$ for the buck converter and $k_f = 1\%$ for the *LLC* resonant converter with $\lambda = 0.6$. For the same output current ripple, load-resonant converters with frequency modulation require a lower relative modulation amplitude when compared to conventional converters.

In order to show the behavior of the THD of integrated converters with PC stages listed in Table II, the parameters of the ARC technique for an output ripple of 50% were evaluated according to Section II-A and the values of ΔTHD are given in Table III for each combination of PFC and PC stages. For example, by considering the PFC buck–boost integrated with the buck, the output current ripple of 50% is obtained with a duty cycle modulation that generates a THD increase of 12.8%. On the other hand, the same output ripple is obtained with ΔTHD of only 0.5%, if the *LLC* resonant converter with $\lambda = 0.6$ is used as the PC stage with frequency-based ARC. Regarding the hard-switching converters, although k_f is higher than k_d, the values of ΔTHD are similar, since the $f(t)$ modulation has a lower impact on the THD when compared with the $d(t)$ modulation. Thus, the ARC technique applied to the switching frequency is also an alternative for the evaluated nonresonant converters, although the design of such topologies with a large-frequency modulation can be somewhat difficult and can actually increase the volume of some passive elements. On the other hand, when a load-resonant PC stage is used, the frequency-based ARC is an excellent alternative, since it allows for a large capacitance reduction with a very small impact on the THD. This occurs owing to the high modulation sensitivity of those topologies. Furthermore, these converters have higher efficiency when compared to hard-switching converters.

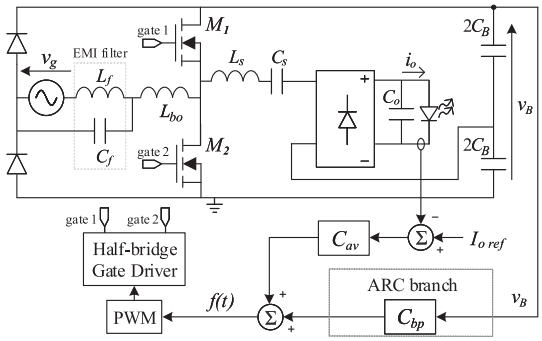


Fig. 6. Integrated offline LED driver based on the *LC* resonant converter with the ARC technique in the switching frequency.

In low-power applications, when the designer pursues simpler topologies composed of only one stage, the duty cycle modulation can be more interesting. On the other hand, the proposed frequency-based ARC yields better results when two-stage converters are needed, since it allows for a huge capacitance reduction while maintaining a low input current distortion and a high overall efficiency.

III. CASE STUDY OF AN OFFLINE LED DRIVER WITH THE ARC TECHNIQUE IN THE SWITCHING FREQUENCY

This section presents a design example of an integrated offline LED driver with frequency-based ARC. The topology chosen in this work was obtained by integrating a totem-pole bridgeless boost PFC and a half-bridge *LC* series resonant converter, as shown in Fig. 6, which is referred by BBLC in this article. It is worth noting that the topology chosen for the PC stage is the one with the lowest sensitivity among the *LLC* converters evaluated in the previous section, being considered the worst case of load-resonant converters, which have high efficiency.

TABLE IV
DESIGN PARAMETERS BASED ON AN *LLC* TOPOLOGY [29]

Symbol	Description	Value
V_G	line voltage	127 V
ω_L	Angular line frequency	$2\pi 60$ rad/s
V_B	Average bus voltage	450 V
Q	Normalized ac-side load resistance	1
λ	Inductance ratio	0
ω_n	Normalized switching frequency	1.2
f_d	Design switching frequency	50 kHz
V_t	Nominal threshold voltage of the LED lamp	129.6 V
r_d	Dynamic resistance of the LED lamp	12 Ω
I_o	Average output current	700 mA
V_o	Average output voltage	138 V
P_o	Output power	96.6 W
ΔI_o	Maximum LF LEDs current ripple	70 mA (10%)
η	Estimated efficiency	92 %

In other words, this topology needs a higher modulation amplitude for capacitance reduction, thus resulting in higher input current distortion. Therefore, this converter was chosen in order to show the higher influence of the frequency modulation on the input current of the integrated offline LED drivers based on load-resonant converters.

The PFC stage was devised to operate in DCM, since in this condition the circuit achieves a high PF at the driver ac input. The duty cycle of this converter is 0.5 in order to obtain a symmetrical switching in the second stage. Moreover, the average bus voltage must be chosen in compliance with the condition given by (15) to ensure the DCM operation in the PFC stage.

$$v_B(t) > \frac{\sqrt{2}V_G}{1-D}. \tag{15}$$

The PC stage operates above the series resonant frequency, thus resulting in ZVS and high efficiency. As can be seen in Fig. 6, the ARC approach requires an additional compensator branch C_{bp} and one voltage sensor for its proper operation as compared to a typical control technique. The compensator C_{av} is used to synthesize the value of f_0, while the block C_{bp} generates the oscillating portion of $f(t)$ in phase with the ac portion of the bus voltage.

The design of the BBLC converter using the ARC technique must be performed in the following three steps.

1) First, the passive elements of the PC stage (L_s and C_s) and the parameters of the switching frequency function (f_0 and k_f) must be obtained.
2) Thereafter, the PFC stage design must be carried out.
3) Finally, the control loop is designed, so that $f(t)$ assumes the desired profile.

A. Design of the PC Stage and the Frequency Modulation

Table IV gives the design parameters of the example converter. The design of the PC stage's elements is done by following the procedure outlined in [29] and by considering a design switching frequency f_d. Since the *LC* series converter is a specific case of the *LLC* converter, the mathematical model presented in [29] can be used considering the turns ratio equal to 1 and the inductance ratio equal to 0. Therefore, by using the design parameters of the converter listed in Table IV, the values of $C_s = 23.9$ nF, $L_s = 610.3$ μH, $f_0 = 70$ kHz, and bus voltage ripple $\Delta V_B = 20$ V can be found.

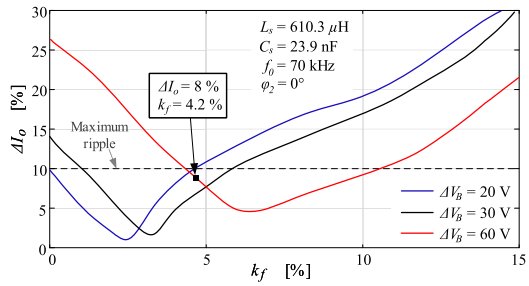


Fig. 7. Behavior of the peak-to-peak output current ripple according to k_f for several values of ΔV_B.

Since the capacitance reduction is associated with an increase in the bus voltage ripple, the relative amplitude of the modulation can be designed by adopting a graphical evaluation of the output current behaviors according to variations of ΔV_B and k_f. Fig. 7 shows the behavior of the relative output current ripple generated and plotted as a function of k_f for several values of ΔV_B. The graphs were obtained by solving the accurate modeling proposed in [29] using the values of C_s, L_s, and ΔV_B, as well as the parameters of the frequency modulation. As shown in Fig. 7, if the ARC technique was not used ($k_f = 0$), bus ripples higher than 20 V would be insufficient for meeting the design requirement of maximum ripple. In other words, lower capacitances can be employed only by using the $f(t)$ modulation. Thus, by choosing $k_f = 4.2\%$, the desired ripple criterion is achieved for a bus ripple of $\Delta V_B = 60$ V, which yields an output current ripple of 8% (56-mA peak-to-peak).

B. Design of the PFC Stage

As long as the switching frequency function has been defined, the PFC stage can now be designed. According to [15], the PFC stage can be treated as a conventional boost DCM PFC for each line half-cycle, which simplifies the analysis and design of the converter. Therefore, the input current of the offline converter is given by (11), in which $d(t)$ is equal to the duty cycle constant value, also denoted by D. In order to ensure the average power balance of the converter, L_{bo} can be calculated by (12), which yields a boost inductance of 413 μH.

The bus capacitance C_B can be calculated as outlined in [15]. According to this work, the bus capacitance can be written as

$$C_B = \frac{\Delta Q_{CB}}{\Delta V_B} \tag{16}$$

where ΔQ_{CB} is the amount of charge injected in (or extracted from) the bus capacitance during each quarter of line cycle.

By considering that the input is a 127-VAC/60-Hz mains and by using the design parameters of the converter listed in Table IV, the bus capacitance can be calculated as 11 μF. It is important to highlight that, if the ARCT was not used (i.e., $k_f = 0$), a capacitance of *ca.* 33 μF should be used for achieving

a similar ripple at the output. Therefore, the modulation of the switching frequency allowed for a capacitance reduction of 66.6% when compared to the conventional approach without modulation. In addition, for the chosen operating point, the THD of 9.15% was increased by only 0.25%, yielding a theoretical THD of 9.4% in accordance with Fig. 2(b). The reliability of the driver was greatly improved by reducing capacitance [30]. The designed capacitance value is commercially available in both technologies: 1) metallized-film; or 2) electrolytic. If the designer pursues a longer lifespan, the metallized-film is the best choice; however, if a cheaper and compact LED driver is desired, the electrolytic technology is more suitable. Therefore, the capacitor technology selection depends on the application.

C. Design of the Control Loop

Since the passive elements and the switching frequency function have been defined, the control circuit can be designed. The transfer function of C_{av} is shown in (17). As it can be noted that this compensator is an integrator, which ensures that the system will have null steady-state error under constant current reference. Furthermore, the crossover frequency (f_{co}) of this transfer function must be tuned so that the output of the C_{av} block does not present any ac component in steady-state, i.e., C_{av} must attenuate all the oscillating components of the error signal. The low crossover frequency allows for appropriate performance of the LED driver even when the *LLC* converter with higher sensitivity, such as $\lambda = 0.6$, is used. In addition, the negative signal is used here, since, in the case of resonant converters, the circuit gain reduces as long as the amplitude of the control variable, which is the switching frequency, increases.

$$C_{av}(s) = -\frac{K_a}{s}. \tag{17}$$

In order to ensure a good attenuation at 120 Hz, a $K_a = 8.17$ Hz was chosen, resulting in a crossover frequency of *ca.* 1.3 Hz, which is two decades below $2\omega_L$.

The expression for C_{bp} was obtained based on a narrow-band second-order band-pass filter, as described in [25]. This element was tuned with a center angular frequency of $2\omega_L$, which ensures that the oscillating component of $f(t)$ is tracked at the desired frequency. In addition, the desired phase of the modulation signal is also ensured, since the filter phase at the tuned angular frequency is null. Therefore, the transfer function of C_{bp} is given by (18), where K_{bp} is the gain at center frequency and B is the filter bandwidth. The gain K_{bp} must be calculated by considering the amplitude of the bus voltage at the frequency of interest ($2\omega_L$). Thus, the desired oscillating portion of $f(t)$ can be obtained by (19), which was derived from the analysis of the control diagram of Fig. 6.

$$C_{bp}(s) = K_{bp}\frac{Bs}{s^2 + Bs + 4\omega_L^2} \tag{18}$$

$$K_{bp} = \frac{2f_0 k_f}{\Delta V_B}. \tag{19}$$

Therefore, by replacing the design results obtained in (19), the calculated value of K_{bp} is equal to 101.5 Hz/V. Finally, the filter bandwidth was chosen as 20 rad/s in order to obtain a proper attenuation of the undesired frequencies.

It is important to highlight that owing to the simplicity of the control structure used in the ARC approach (see Fig. 6), its implementation could be performed by using a simple microcontroller or even by means of analog filters and control circuitry. In order to enable an easier tuning of parameters for the lab prototype, the control system of this work was implemented digitally.

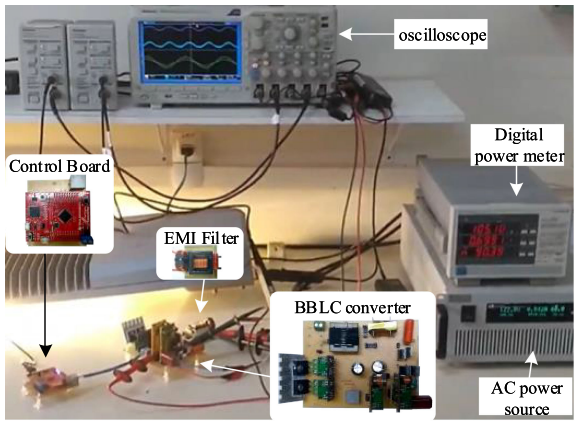


Fig. 8. Photograph of the experimental setup, showing each part of the prototype, and the corresponding boards and components.

TABLE V
MAIN PARAMETERS OF PROTOTYPES

Item	Value
Half-bridge switches	2 × IRFP460 (500V/0.25Ω)
Boost diodes	2 × MUR360S/(600V/3A)
Boost inductor L_b	413 μH/NEE 30-15-14/53T gap = 0.48 mm/4×AWG 28
Bus capacitors	22 μF/400 V electrolytic capacitor equivalent C_B = 11 μF
Resonant inductor L_s	610.2 μH/NEE 30-15-7/53T gap = 0.16 mm/3xAWG 28
Resonant capacitor C_s	22 nF/250V ceramic capacitor
Diode bridge	4 × IDT02S60C (600 V/2A)
Output capacitor C_o	4.4 μF/250 V ceramic capacitor
EMI filter	CM:5 mH/DM: 470μH/220nF
Microcontroller	TI TM4C123G

IV. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a laboratory prototype was built, which is shown in Fig. 8. Table V presents the main elements used in the prototype.

Fig. 9 shows some experimental waveforms from the offline LED driver based on the *LC* resonant converter employing the frequency-based ARC technique with $C_B = 11$ μF/480 V [see Fig. 9(a)] compared with the same circuit without the large-signal modulation of the switching frequency [see Fig. 9(b)], and also with the conventional approach (no active compensation) with a bus capacitance of 33 μF/460 V [see Fig. 9(c)]. The LF output current ripple obtained from this experiment was 58 mA, which is quite close to the 54 mA from theoretical prediction. In

TABLE VI
MEASURED LOSS DISTRIBUTION

Components	Values
EMI filter	0.32 W
MOSFETs switching loss	0.94 W
MOSFETs conduction loss	0.76 W
Input diodes	2 W
L_{bo}	1.3 W
C_B	0.46 W
C_s	0.8 W
L_s	1.6 W
Output diode bridge	1.8 W
C_o	0.2 W
Total	10.18 W

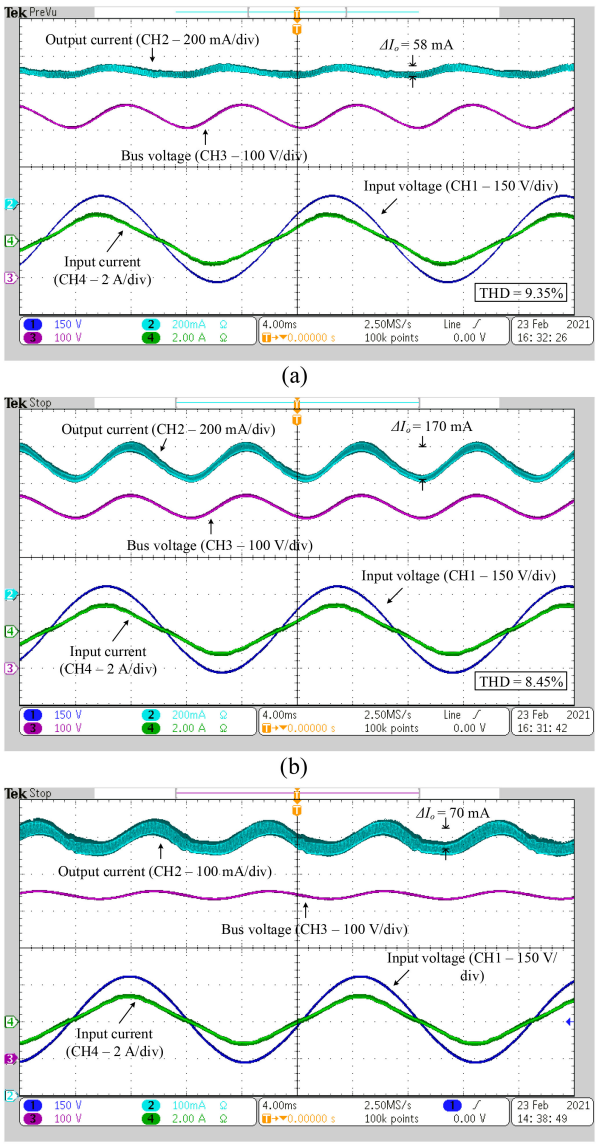


Fig. 9. Experimental waveforms obtained (a) with ARC and $C_B = 11$ μF; (b) without ARC and $C_B = 11$ μF; and (c) without ARC and $C_B = 33$ μF.

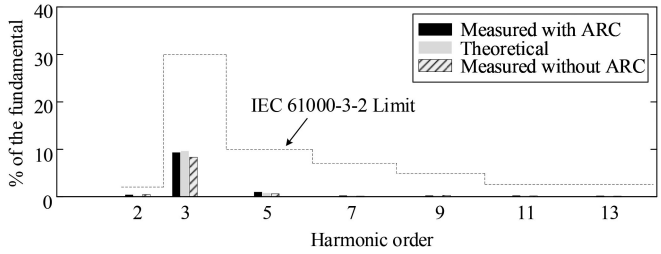


Fig. 10. Harmonic content of the input current compared with IEC limits.

addition, Fig. 9(b) shows a larger ripple when the ARC technique is not used with the same bus capacitance of 11 μF, being necessary an additional value of 22 μF [see Fig. 9(c)] to decrease the output current ripple to a similar level to the one obtained when the ARC technique is employed. The experimental results of the LED driver without ARC were obtained by using only the pure integrator shown in (17), which ensures that the system will have null steady-state error under constant current reference.

It is important to highlight that, as shown in Fig. 9, the output current ripple of the circuit with LF large-signal modulation of the switching frequency is lower than that of the conventional approach (i.e., without ARC) imposing little increase of the input current distortion. As it can be seen, experimental results showed that the ARC technique increased only 0.9% the THD of the input current, when compared with the conventional approach. In addition, this distortion was predicted during the design procedure, so that the harmonic content of the input current remains in compliance with the IEC-61000-3-2 standard, as shown in Fig. 10. The other harmonics are not shown in Fig. 10 because their values were negligible. As can be noted that the experimental results of the input current are also close to the values obtained in the theoretical analysis. The measured THD was 9.35%, which is very close to the 9.4% predicted by the analysis. The measured PF of the BBLC with the ARC technique was 0.986.

Fig. 11 shows experimental waveforms of the current and voltage of the MOSFET M_1 and the output rectifier diode at the positive [see Fig. 11(a)] and negative [see Fig. 11(b)] peak of line voltage. These waveforms show that the converter operates above series resonant frequency and with ZVS. Table VI gives the measured loss distribution in the prototype, which was obtained at nominal input voltage and rated load. Furthermore, those measurements did not take into account the consumption of the control board.

Fig. 12 shows the output current ripple, THD, and efficiency of the converter according to variations in the input voltage. The results show that the output ripple [see Fig. 12(a)] of the driver with the frequency-based ARC technique was much smaller over the entire range, with a small increment of THD [see Fig. 12(b)]. It is important to highlight that the influence of the frequency modulation upon the efficiency [see Fig. 12(c)] is negligible for variations in the input voltage.

The behavior of the output current ripple, THD, and efficiency owing to variations in the output power is shown in Fig. 13. The results showed that the converter with frequency modulation

TABLE VII
COMPARISON AMONG CONTROL TECHNIQUES TO REDUCE BULK CAPACITANCE IN OFFLINE LED DRIVERS

	Proposed frequency-based ARC	Duty-cycle-based ARC [23]	Proportional integral resonant controller [31]	Third harmonic injection [22]	Distorted sinusoidal reference [20]
Topology	BBLC	Double buck–boost	Double buck–boost	PFC boost	PFC boost
ΔTHD	0.9%	17.2%	10.2%	>40%	>25%
Capacitance reduction	66.6%	85%	80.5%	33%	23%
			Performance parameters of the topology		
Efficiency	90.3%	84%	–	91%	–
Output power	96.6 W	75 W	71.5 W	20 W	500 W
Output current ripple	58 mA (8.3%)	50 mA (10%)	56 mA (8%)	14 mA (29.7%)	– –
PFC stage output capacitance	11 μF	22 μF	20 μF	8.8 μF	500 μF
PFC stage output voltage	450 V	160 V	200 V	420 V	400 V
FP	0.986	0.982	0.987	0.91	0.967
THD	9.35%	18.2%	19%	–	–

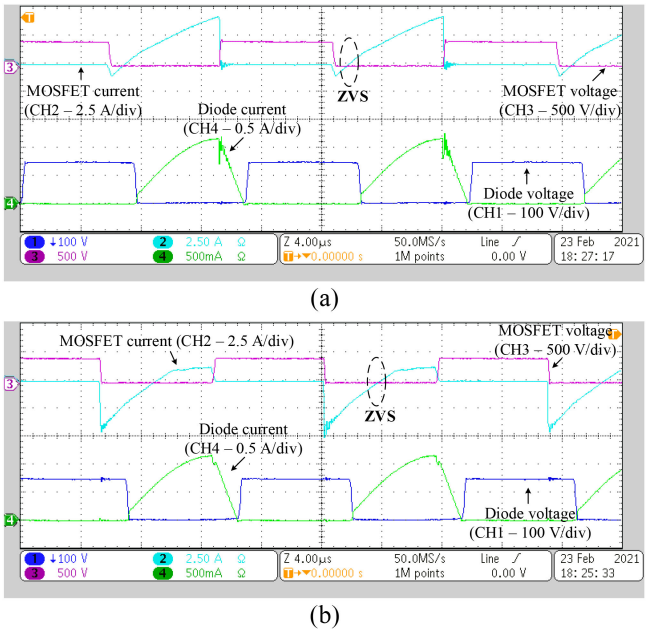


Fig. 11. Waveforms measured at the (a) positive; and (b) negative peak of line voltage. Diode voltage (CH1– 100 V/div), MOSFET M1 current (CH2– 2.5 A/div), MOSFET voltage (CH3– 500 V/div), and diode current (CH4– 500 mA/div). Horiz. scale: 4 μs/div.

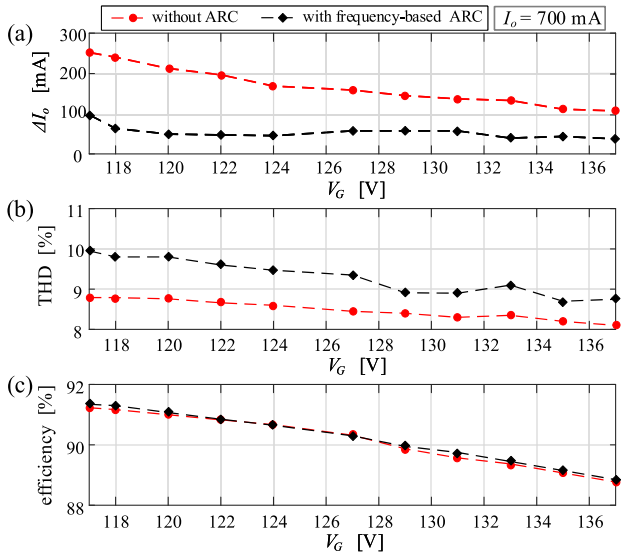


Fig. 12. Output ripple, THD, and efficiency of the converter according to variations in the input voltage.

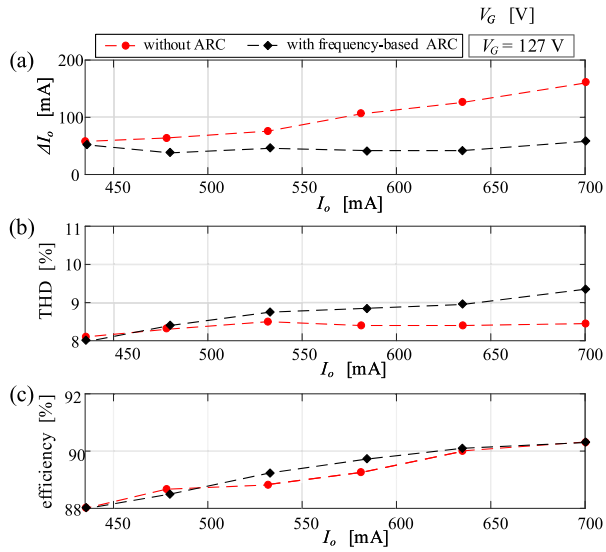


Fig. 13. Output ripple, THD, and efficiency of the converter according to variations in the output power.

ensured a small current ripple for all the analyzed levels. In addition, the influence of the frequency-based ARC upon the THD and efficiency can be considered negligible for variations in the output power.

Table VII gives a brief comparison among the proposed frequency-based ARC and other control techniques devised to reduce bulk capacitance in offline LED drivers, highlighting deviation of THD, and capacitance reduction. Overall efficiency, power, THD, and other performance parameters were also analyzed for each topology whose techniques were applied. Unlike other techniques presented in the literature, the proposed frequency-based ARC can be applied to converters with resonant stages, which allows for the design of high-efficiency low-capacitance LED drivers. A good performance in terms of efficiency was also achieved in [22], since the converter

presented in this article is composed of only one stage. However, the approaches in [20] and [22] yielded a moderate capacitance reduction with a high increase in the input current distortion. In the integrated offline LED driver based on hard-switching topologies proposed in [23] and [24], the obtained capacitance reduction was improved, mainly in [23], but still resulting in a high input current distortion. Moreover, the overall efficiency of these converters is low. It is important to highlight that the proposed frequency-based ARC allows for a large capacitance reduction without affecting the THD significantly. Therefore, the proposed approach is a great alternative concerning reduction of bulk capacitance, improving the driver lifetime, while still maintaining a low output ripple and preventing flickering.

One of the drawbacks of the evaluated topology is that the PFC stage operates with a duty cycle of 0.5, andtherefore, the bus voltage has to be at least twice the peak value of the input voltage. Hence, it poses some difficult to operate in universal-input voltage condition with the 650/700 V voltage rating power devices. However, this disadvantage can be solved by using one of the buck–boost-type topologies instead of boost-based topologies. Regarding the PC stage, the series resonant converter adds no galvanic isolation and has a relatively low efficiency. These drawbacks can be mitigated by employing the *LLC* converter and performing the design procedure proposed in this article.

V. Conclusion

This article presented the generalized analysis of the ARC approach at the control variable of integrated offline LED drivers. The theoretical analysis described the operation of several topologies under the modulation of switching frequency and duty cycle. The duty cycle modulation, which has been explored in some works, was analyzed for several topologies showing that it has a good capacitance reduction potential. However, all of them presenting a relevant drawback, i.e., the significant increase in the THD. The low sensitivity of the LF ripple to duty cycle modulation implies that to achieve a good ripple reduction, a significant modulation in the control variable must be employed, causing a large distortion in the input current. On the contrary, this article proposed an alternative approach based on the modulation of the switching frequency, which allows for a large capacitance reduction without affecting the THD significantly when applied to converters with a load-resonant PC stage. This alternative also increases the overall LED driver efficiency when compared to integrated converters, in which both stages operate under hard-switching condition. Experimental results verified the theoretical analysis, showing that the ARC technique in the switching frequency allowed for a capacitance reduction of 66.6%, while increasing only in 0.9% the input current THD.

References

[1] C.-C. Sun *et al.*, "Packaging efficiency in phosphor-converted white LEDs and its impact to the limit of luminous efficacy," *J. Solid State Lighting*, vol. 1, no. 1, 2014, Art. no. 19.

[2] S. Li, S.-C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. Hui, and C. K. Tse, "A survey, classification, and critical review of light-emitting diode drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1503–1516, Feb. 2016.

[3] A. Laubsch, M. Sabathil, J. Baur, M. Peter, and B. Hahn, "High-power and high-efficiency InGaN-based light emitters," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 79–87, Jan. 2010.

[4] E. S. Lee, B. H. Choi, J. P. Cheon, G. C. Lim, B. C. Kim, and C. T. Rim, "Temperature-robust LC^3 passive LED drivers with low THD, high efficiency and PF, and long life," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 829–840, Sep. 2015.

[5] P. S. Almeida, V. C. Bender, H. A. C. Braga, M. A. D. Costa, T. B. Marchesan, and J. M. Alonso, "Static and dynamic photoelectrothermal modeling of LED lamps including low-frequency current ripple effects," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3841–3851, Jul. 2015.

[6] B. Lehman and A. J. Wilkins, "Designing to mitigate effects of flicker in LED lighting: Reducing risks to health and safety," *IEEE Power Electron. Mag.*, vol. 1, no. 3, pp. 18–26, Sep. 2014.

[7] P. S. Almeida, M. A. D. Costa, J. M. Alonso, and H. A. C. Braga, "Application of series resonant converters to reduce ripple transmission to LED arrays in offline drivers," *Electron. Lett.*, vol. 49, no. 6, pp. 414–415, Mar. 2013.

[8] "IEEE Recommended Practices for Modulating Current in High-Brightness LEDs for Mitigating Health Risks to Viewers," *IEEE Std 1789-2015*, pp. 1–80, Jun. 2015, doi: 10.1109/IEEESTD.2015.7118618.

[9] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.

[10] H. Wang, H. Wang, G. Zhu, and F. Blaabjerg, "An overview of capacitive DC-links-topology derivation and scalability analysis," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1805–1829, Feb. 2020.

[11] D. Camponogara, D. R. Vargas, M. A. D. Costa, J. M. Alonso, J. Garcia, and T. Marchesan, "Capacitance reduction with an optimized converter connection applied to LED drivers," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 184–192, Jan. 2015.

[12] W. Chen and S. Y. R. Hui, "Elimination of an electrolytic capacitor in AC/DC light-emitting diode (LED) driver with high input power factor and constant output current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1598–1607, Mar. 2012.

[13] J. M. Alonso *et al.*, "Reducing storage capacitance in off-line LED power supplies by using integrated converters," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2012, pp. 1–8.

[14] D. Gacio, J. M. Alonso, A. J. Calleja, J. García, and M. Rico-Secades, "A universal-input single-stag2e high-power-factor power supply for HB-LEDs based on integrated buck–flyback converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 589–599, Feb. 2011.

[15] P. S. Almeida, H. A. C. Braga, M. A. D. Costa, and J. M. Alonso, "Offline soft-switched LED driver based on an integrated bridgeless boost–asymmetrical half-bridge converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 761–769, Jan./Feb. 2015.

[16] M. Arias, M. F. Diaz, J. E. R. Cadierno, D. G. Lamar, and J. Sebastián, "Digital implementation of the feedforward loop of the asymmetrical half-bridge converter for LED lighting applications," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 642–653, Sep. 2015.

[17] M. Arias, I. Castro, D. G. Lamar, A. Vázquez, and J. Sebastián, "Optimized design of a high input-voltage-ripple-rejection converter for LED lighting," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5192–5205, Jun. 2018.

[18] L. Gu, X. Ruan, M. Xu, and K. Yao, "Means of eliminating electrolytic capacitor in AC/DC power supplies for LED lightings," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1399–1408, May 2009.

[19] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less AC–DC drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592–601, Mar. 2010.

[20] D. G. Lamar, J. Sebastian, M. Arias, and A. Fernandez, "On the limit of the output capacitor reduction in power-factor correctors by distorting the line input current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1168–1176, Mar. 2012.

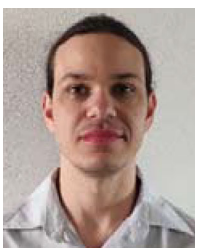
[21] X. Ruan, B. Wang, K. Yao, and S. Wang, "Optimum injected current harmonics to minimize peak-to-average ratio of LED current for electrolytic capacitor-less AC–DC drivers," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1820–1825, Jul. 2011.

[22] C. S. Wong, K. H. Loo, Y. M. Lai, M. H. L. Chow, and C. K. Tse, "An alternative approach to LED driver design based on high-voltage driving," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2465–2475, Mar. 2016.

[23] G. M. Soares, P. S. Almeida, L. W. de Oliveira, J. M. Alonso, and H. A. C. Braga, "Optimized design of a wide-bandwidth controller for low-frequency ripple compensation in offline LED drivers," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1166–1178, Sep. 2018.
[24] G. M. Soares, P. S. Almeida, J. M. Alonso, and H. A. C. Braga, "Capacitance minimization in offline LED drivers using an active-ripple-compensation technique," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3022–3033, Apr. 2017.
[25] G. M. Soares, J. M. Alonso, and H. A. C. Braga, "Investigation of the active ripple compensation technique to reduce bulk capacitance in offline flyback-based LED drivers," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5206–5214, Jun. 2018.
[26] T.-F. Wu and Y.-K. Chen, "Modeling of single-stage converters with high power factor and fast regulation," *IEEE Trans. Ind. Electron.*, vol. 46, no. 3, pp. 585–593, Jun. 1999.
[27] H. Wei and I. Batarseh, "Comparison of basic converter topologies for power factor correction," in *Proc. IEEE Southeastcon Eng. New Era*', 1998, pp. 348–353.
[28] M. A. D. Costa, J. M. Alonso, J. C. Miranda, J. Garcia, and D. G. Lamar, "A single-stage high-power-factor electronic ballast based on integrated buck flyback converter to supply metal halide lamps," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1112–1122, Mar. 2008.
[29] R. M. Ferraz, L. H. G. Resende, H. A. C. Braga, P. S. Almeida, J. M. Alonso, and G. M. Soares, "A novel design approach for LLC resonant converters in off-line LED driving applications," *J. Control, Automat. Elect. Syst.*, vol. 32, pp. 1758–1770, 2021.
[30] P. S. Almeida, D. Camponogara, M. D. Costa, H. Braga, and J. M. Alonso, "Matching LED and driver life spans: A review of different techniques," *IEEE Ind. Electron. Mag.*, vol. 9, no. 2, pp. 36–47, Jun. 2015.
[31] P. Luz, J. Cassol, M. Righi, G. Vargas, R. Prado, and A. Kirsten, "Resonant control applied to bus capacitance reduction in integrated double buck-boost to LED driver," *Eletrônica de Potência*, vol. 23, no. 1, pp. 98–107, 2018.

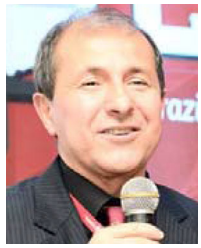
Ruan M. Ferraz received the B.S. degree in electrical engineering and the master's degree from the Federal University of Juiz de Fora, Juiz de Fora, Brazil, in 2017 and 2019, respectively. He is currently working toward the Ph.D. degree with Federal University of Juiz de Fora (UFJF).

Since 2014, he has been a Researcher with Modern Lighting Research Group, Engineering School. His research interests include high-reliability LED drivers, high-power factor rectifiers, active power factor correction, resonant converters, and modeling and control of converters.



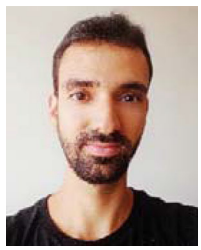
Lucas H. G. Resende received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Juiz de Fora (UFJF), Juiz de Fora, Brazil, in 2017 and 2019, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Federal University of Juiz de Fora (UFJF).

Since 2014, he has been a full-time Researcher with Modern Lighting Research Group, UFJF. His research interests include solid-state lighting, power electronic converters, active power factor correction, and visible light communication.



Henrique A. C. Braga (Senior Member, IEEE) received the B.S. degree in electrical engineering from the Universidade Federal de Juiz de Fora (UFJF), Juiz de Fora, Brazil, in 1982, and the Dr. Eng. degree from the Universidade Federal de Santa Catarina, Florianopolis, Brazil, in 1996.

Since 1985, he has been teaching Basic Electronics and Power Electronics with UFJF, in undergraduate and graduate levels. From 2005 to 2006, he was enrolled in a Postdoctoral cooperation with Universidad de Oviedo, Gijon, Asturias, Spain. He has authored or coauthored about 200 scientific papers in peer-reviewed technical conferences and journals, and also coauthored six book chapters. His research focuses on power electronics field, especially in electronic lighting systems and renewable energy sources applications.



Pedro S. Almeida (Member, IEEE) received the B.S., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Juiz de Fora (UFJF), Juiz de Fora, Brazil, in 2010, 2012, and 2014, respectively.

Since 2015, he has been a Professor of Electrical Engineering (undergraduate and postgraduate courses) with UFJF, where he has also been a Researcher with Modern Lighting Research Group, Engineering School, since 2008. His research interests include electronic power conversion, high-power factor rectifiers and active power factor correction, solid-state lighting and light-emitting diode driving, discharge lamps and electronic ballasts, dimming, spectrophotometry, microcontrollers applied to power electronics, and the modeling and control of electronic power converters.

Dr. Almeida has been a Member of the IEEE Industrial Electronics Society since 2009.

J. Marcos Alonso (Fellow, IEEE) received the M.Sc. and Ph.D. degrees (Hons.) in electrical engineering from the University of Oviedo, Oviedo, Spain, in 1990 and 1994 respectively.

Since 2007, he has been a full Professor with Electrical Engineering Department, University of Oviedo. He has coauthored more than 450 journal and conference publications, including more than 120 publications in highly referenced journals, three books, and two book chapters. He holds eight national and international patents. His research interests include lighting applications, dc–dc converters, power factor correction, resonant inverters, wireless power transfer, and single-phase power electronics in general.

Prof. Alonso was the recipient of 11 IEEE awards. He is a Co-Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS. He was the Chair of the IEEE IAS Industrial Lighting and Displays Committee.

Guilherme M. Soares (Member, IEEE) received the B.S., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Juiz de Fora (UFJF), Juiz de Fora, Brazil, in 2012, 2014, and 2017, respectively.

Since 2010, he has been a full-time Researcher with Modern Lighting Research Group, Engineering School, UFJF, where he has also been a Professor with Electrical Engineering Department, since 2015. His research interests include electronic energy conversion, power factor correction, high reliability LED drivers, solid-state lighting, microcontrollers, optimization applied to power electronics, visible light communication, and Internet of Things.

Dr. Soares is a Reviewer of international journals and conferences in the field of power electronics and electrical engineering.