Electrothermal Coupling Model With Distributed Heat Sources for Junction Temperature Calculation During Surges

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***Abstract*—High junction temperature is usually the main factor leading to device failures in high-power working conditions, such as surges or avalanches. It is of great significance to obtain the junction temperature quickly and accurately. Direct measurement of junction temperature is inconvenient, and usually indirect electrical measurement combined with model calculation is used. An electrothermal coupling junction temperature calculation model with distributed heat sources is proposed in this article. This model can accurately and quickly predict the device behavior during the surge process, as well as the voltage drop and temperature changes of each part of the device, without actually performing surge tests. This article describes the theoretical basis and calculation principles of the model. By taking a commercial SiC merged PiN Schottky diode as an example, this article also explains the details of the establishment of the electrical and thermal characteristic models of the device, as well as the calculation steps of the junction temperature by the thermal coupling model. The calculated device voltage drop curve of the device is in good agreement with the measured ones, and the calculated junction temperature curve is more consistent with the device failure mechanism than the one by the traditional RC thermal circuit model.**

***Index Terms*—Electrothermal coupling, junction temperature, surge, thermal circuit.**

NOMENCLATURE

C_i	Thermal capacitance of layer i.
I	Current flowing into the device.
P_i	Heating power of layer i.
$R_{\text{uni,epi}}$	Unipolar on-resistance of the epitaxy layer of the MPS diode.
$R_{\text{bi,epi}}$	Bipolar on-resistance of the epitaxy layer of the MPS diode.
R_i	Thermal resistance of layer i.
T_i	Temperature of node i.
$T_{k\leftarrow p}$	Temperature response at node k excited by a heating power source at node p.
T_k	Temperature response at node k excited by all heating power sources.
V_{on}	Turn-ON voltage of the MPS diode.
$V_{\text{PN,eff,dev}}$	Effective PN junction trigger voltage of the whole device.
$V_{\text{PN,eff,epi}}$	Effective PN junction trigger voltage of the epitaxial layer.
$V_{\text{PN,eff}}$	Effective PN junction trigger voltage of the MPS diode.
V_{PN}	PN junction trigger voltage of the MPS diode.
V_i	Voltage drop of layer i.
$\Phi_{p\to k}(s;\{R_1,\ldots,R_N\},\{C_1,\ldots,C_N\})$	S-domain transfer function from node p to node k in the thermal branch of the electrothermal-coupling model.
$H_1\to i(s;\{R_1\ldots R_N\},\{C_1\ldots C_N\})$	S-domain transfer function from node 1 to node i in a conventional RC thermal circuit.
$Z_i(s;\{R_1,\ldots R_N\},\{C_1,\ldots C_N\})$	Complex impedance at the right side of node i in a conventional RC thermal circuit.

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I. INTRODUCTION

POWER electronics technology has been widely used in high-power/harsh environments, such as automobiles, aerospace, and military industries, especially with the continuous improvement of SiC and other widebandgap power devices. In these applications, power devices are confronted with high-power extreme conditions, such as surges, avalanches, and short circuits. Under these extreme conditions, the device's self-heating power will substantially increase the junction temperature, and may lead to the damage of the device [1], [2]. In order to improve the design and reliability of power devices, it is necessary to have a good knowledge of the junction temperature changes under extreme operating conditions. Theoretically, the junction temperature can be measured directly, e.g., by estimating the infrared radiation intensity [3], [4] or the liquid crystal luminous intensity [5] on the device surface. However,

these methods require the introduction of additional substances and cannot be applied to packaged devices. Therefore, indirect measurement methods are more practical to obtain the junction temperature.

The idea of the temperature-sensitive parameters (TSPs) of the device can be used to obtain the junction temperature by electrical measurement. TSPs refer to some of the electrical parameters of the device that one-to-one correspond to its junction temperature. Palanisamy *et al.* [2], [6] established a junction temperature test bench based on this idea when studying the aging phenomenon of SiC merged PiN Schottky (MPS) diodes under repetitive surge current pulses, the junction temperature is deduced from the voltage drop of the device measured by a small test current pulse applied immediately after the turn OFF of the surge current. Although this test scheme has high accuracy, the hardware cost is relatively high.

A more convenient method is to use the RC thermal circuit model. Szekely and Bien [7] proposed the concept of the structure function in 1988 [8], [9], which can be obtained by thermal impedance measurement and then be used to establish the RC thermal circuit model. The junction temperature during the surge process is the convolution of the electrical power and the transfer function of the RC thermal circuit model. However, this method is not able to provide the voltage drop and temperature change inside the device. Moreover, the heating power is assumed to be concentrated at the chip surface, and the thermal parameters of each layer are treated as constants, which is not consistent with the physical reality. Compared with the methods abovementioned, dynamic device numerical simulation provides the most abundant information with the lowest cost and the highest applicability [10]. However, considering the complexity of the electrothermal coupling processes, the dynamic numerical simulation usually consumes a great amount of computer time.

In order to deeply understand the behavior of the device under extreme working conditions and to keep a balance between model accuracy and calculation efficiency, this article proposes a distributed heat source electrothermal coupling junction temperature calculation model based on the conventional RC thermal circuit model (hereinafter referred to as "the electrothermal coupling model"). The rest of this article is organized as follows. Section II introduces the basic overview of the electrothermal coupling model and the corresponding theoretical basis. Section III explains the details of the model and its calculation steps. Section IV establishes the thermal and electrical characteristic models of a commercial device and uses the electrothermal coupling model to calculate its junction temperature change during the surge process. Calculation results are also compared with the actual measurement results. Finally, Section V concludes this article.

II. Theoretical Basis of the Electrothermal Coupling Model

Fig. 1 shows the overview of the electrothermal coupling model, which contains both an electrical branch and a thermal branch. A packaged device (including the chip, the solder, and the copper plate) is divided into multiple layers from the junction to the case, and each interface between every two layers is called a "node." Each layer is represented by a thermal resistance and a thermal capacitance in the thermal branch, and by an electrical component in the electrical branch. It should be particularly pointed out that the power source is not shown in Fig. 1, and the topological relationship between the thermal resistance and capacitance shown is only for illustration. In fact, this topological relationship will change according to the position of the heat source. This content will be discussed in Section III.

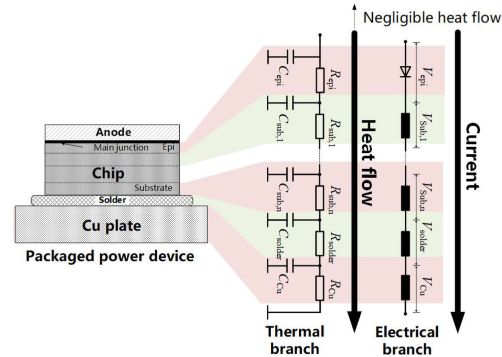


Fig. 1. Overview of the electrothermal coupling model.

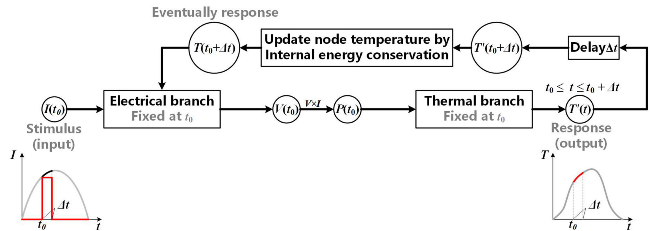


Fig. 2. Basic idea of temperature calculation by the electrothermal coupling model.

Fig. 2 demonstrates the basic idea of temperature calculation by the electrothermal coupling model. The current flowing into the electrical branch is donated as I. All the electrical component voltages are donated as a voltage vector $\boldsymbol{V} = \{V_1, V_2, \ldots, V_N\}$, and all the node temperatures as a temperature vector $\boldsymbol{T} = \{T_1, T_2, \ldots, T_N\}$, in which N is the node number. Suppose that at time instant t_0, there is an initial temperature vector $\boldsymbol{T}(t_0)$, and all the parameters of the electrical and thermal branches are fixed at the values under $\boldsymbol{T}(t_0)$. The current $I(t_0)$ flowing into the electrical branch generates a corresponding voltage vector $\boldsymbol{V}(t_0)$ and the corresponding heating power vector $\boldsymbol{P}(t_0) = \{V_1(t_0)I(t_0), V_2(t_0)I(t_0), \ldots, V_N(t_0)I(t_0)\}$. $\boldsymbol{P}(t_0)$ generates a temperature response vector $\boldsymbol{T}'(t)$ in the thermal branch. In the next short period of time $t_0 \sim t_0 + \Delta t$, assuming that the parameters of the whole model do not change, this response $\boldsymbol{T}'(t)$ is always applicable. At time instant $t_0 + \Delta t$, the current temperature vector $\boldsymbol{T}'(t_0 + \Delta t)$ is taken out and the eventual temperature vector $\boldsymbol{T}(t_0 + \Delta t)$ is calculated according to the internal energy conservation principle (explained in details in Section III-C). The temperature of each node is updated using the eventual temperature vector and the parameters of the electrical and the thermal branches are also updated accordingly. Then, $t_0 + \Delta t$ replaces the position of t_0, and the abovementioned calculation process is repeated until all the time instants are

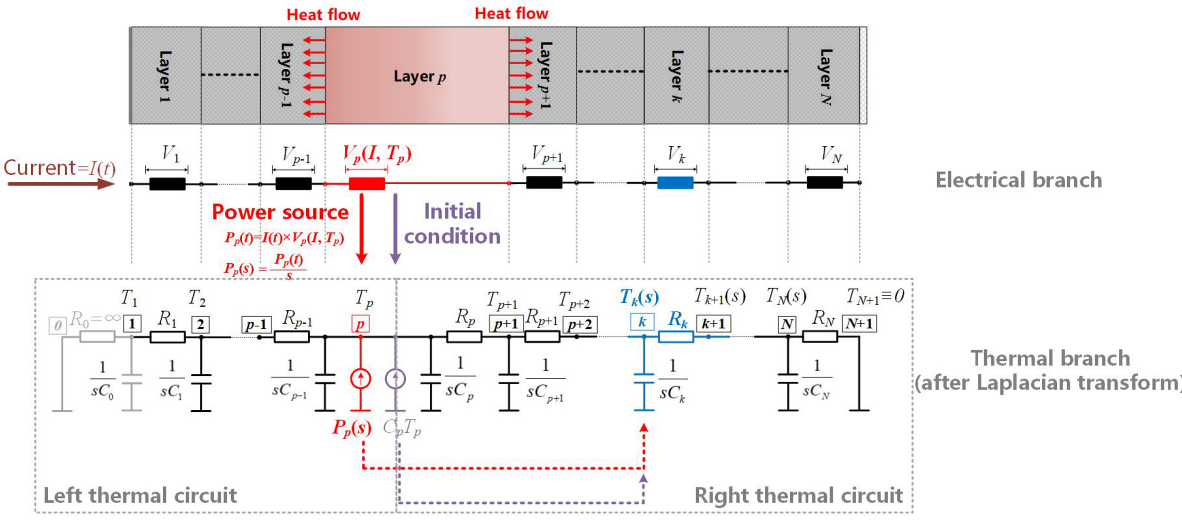


Fig. 3. Structure details of the electrothermal coupling model with the heat source and the initial temperature of only one layer.

processed. The abovementioned algorithm decouples the electrical and thermal processes and linearizes the model by updating the parameters of the electrical branch and the thermal branch successively, which arms the electrothermal coupling model with irrelevance of history and superposition and enables the analysis method of linear system theory [11].

III. Calculation Details of the Electrothermal Coupling Model

According to the discussion in Section II, since the topological relationship between the thermal resistance and the thermal capacitance changes with the position of the heat source, we can only plot the system structure diagram when only one heat source exists. Fortunately, according to the superposition principle, the temperature response of each heat source or initial temperature can be calculated separately and superimposed to obtain the total response. As shown in Fig. 3, the device is divided into N layers from the junction to the case, of which only layer p contains the heat source and the initial temperature T_p. An additional layer 0 with infinite thermal resistance and zero thermal capacitance is added to the left of layer 1 to simulate the adiabatic boundary condition on the left-hand side. The right-hand side of the layer N is directly "grounded" (temperature fixed at the ambient temperature) to simulate the constant temperature boundary condition on the right-hand side. Node numbers are represented by numbers in boxes, and the temperature of node i is represented by T_i. The heat source and the initial temperature in layer p are abstracted as two heat sources at node p. The heat source from the initial temperature only appears explicitly in the thermal branch after the Laplace transform, and its intensity is the total internal energy C_pT_p stored on the thermal capacitance C_p.

As discussed in Section II, the topological relationship between the thermal resistance and capacitance in the thermal branch changes according to the position of the heat source. It comes from the physical fact that one end of an object always needs to be heated up to a higher temperature before the heat flow can spread to the other end of this object. Therefore, the thermal capacitance is always closer to the heat source than the thermal resistance.

A. RC Thermal Circuit Transfer Function

In order to calculate the temperature response at node k under the stimulus of the heat source at node p, we first need to calculate the transfer function from node p to node k. The two heat sources in Fig. 3 are connected in parallel and can be combined into one heat source. The thermal circuits on the left- and right-hand sides of this heat source are connected in parallel and can be divided into two parts. The two split thermal circuits both have the same topology as the conventional RC thermal circuit. Therefore, the total impedance of the left and right subthermal circuits in Fig. 3 can be expressed as

$$\begin{cases} Z_L(s) = Z_1\left(s; \{R_{p-1}, \ldots, R_1\}, \{C_{p-1}, \ldots, C_1\}\right) \\ Z_R(s) = Z_1\left(s; \{R_p, \ldots, R_N\}, \{C_p, \ldots, C_N\}\right) \end{cases} \tag{1}$$

in which

$$\begin{aligned} Z_i(s) &= Z_i\left(s; \{R_1, \ldots R_N\}, \{C_1, \ldots C_N\}\right) \\ &= \frac{1}{sC_i+}\frac{1}{R_i+}\frac{1}{sC_{i+1}+}\frac{1}{R_{i+1}+}\cdots\frac{1}{sC_N+}\frac{1}{R_N}. \end{aligned} \tag{2}$$

Thus, the transfer function from node p (the heat source location) to node k (the temperature response location) is

$$\begin{aligned} &\Phi_{p\to k}\left(s; \{R_1, \ldots, R_N\}, \{C_1, \ldots, C_N\}\right) \\ &= \begin{cases} 1 \le k \le p: \\ \frac{Z_R(s)}{Z_L(s)+Z_R(s)} H_{1\to p-k+1}\left(s; \{R_{p-1}, \ldots, R_1\}, \{C_{p-1}, \ldots, C_1\}\right) \\ p \le k \le N: \\ \frac{Z_L(s)}{Z_L(s)+Z_R(s)} H_{1\to k-p+1}\left(s; \{R_p, \ldots, R_N\}, \{C_p, \ldots, C_N\}\right) \end{cases} \end{aligned} \tag{3}$$

in which

$$H_{1\to i}\left(s;\left\{R_1,\ldots R_N\right\},\left\{C_1,\ldots C_N\right\}\right)=\frac{\prod_{k=1}^{i} Z_k(s)}{\prod_{k=1}^{i-1}\left[R_k+Z_{k+1}(s)\right]}. \tag{4}$$

B. Junction Temperature Calculation Steps

After the foregoing discussion, we can eventually express the junction temperature calculation steps explicitly. We have a knowledge of the following information: the electrical characteristics of each electrical component $V_i(I,T_i)$, the thermal characteristics of each thermal components $R_i(I,T_i)$ and $C_i(I,T_i)$, and the transfer function $\Phi_{p\to k}(s)$ from any node k to any node p. Assuming that we know the temperature of each node at time instant t_{n-1} as $T_1(t_{n-1})$, $T_2(t_{n-1})$,..., $T_N(t_{n-1})$. Then, the thermal resistance and thermal capacitance of each thermal component are

Thermal resistance: $R_1(T_1(t_{n-1}))$, $R_2(T_2(t_{n-1}))$,..., $R_N(T_N(t_{n-1}))$,

Thermal capacitance: $C_1(T_1(t_{n-1}))$, $C_2(T_2(t_{n-1}))$,..., $C_N(T_N(t_{n-1}))$.

Supposing the input current is $I(t_{n-1})$ at this time and assuming that there is only one heat source at node p, the heat source intensity by self heating is $P_p(t_{n-1}) = I(t_{n-1})V_p(I(t_{n-1}),T_p(t_{n-1}))$, and the heat source intensity by the initial temperature is $C_p(T_p(t_{n-1}))T_p(t_{n-1})$. At this time, the temperature response at any node k is

$$\begin{aligned} &T'_{k\leftarrow p}(\tau)\\ &= L^{-1}\left\{\left[\begin{array}{c}\frac{I(t_{n-1})V_p(I(t_{n-1}),T_p(t_{n-1}))}{s}\\ +C_p\left(T_p\left(t_{n-1}\right)\right)T_p\left(t_{n-1}\right)\end{array}\right]\Phi_{p\to k}(s)\right\}\\ &t_n\le\tau\le t_{n-1}.\end{aligned} \tag{5}$$

Varying p from 1 to N, and setting $\tau = t_n$, the temperature response at node k at time instant t_n when all heat sources are present is

$$T'_k\left(t_n\right)=T'_{k\leftarrow 1}\left(t_n\right)+T'_{k\leftarrow 2}\left(t_n\right)+\cdots+T'_{k\leftarrow N}\left(t_n\right). \tag{6}$$

Solving the equation $C_p(T_p(t_{n-1}))T'_k(t_n) = C_p(T_k(t_n))T_k(t_n)$ according to the internal energy conservation principle, the real node temperature $T_k(t_{n-1})$ can be obtained eventually. Varying k from 1 to N, all the node temperatures $(T_1(t_{n-1}), T_2(t_{n-1}), \ldots, T_N(t_{n-1}))$ can be obtained. We can update the electrical and thermal parameters of the system by these new temperature values, and then use these new temperatures as new initial conditions to calculate the temperature at time t_{n+1}. Such a calculation process should be repeated until the node temperatures at all time instants are calculated.

IV. Calculation Example

In this section, a commercial SiC MPS diode from CREE Inc., is taken as an example (serial no. C4D05120A, hereinafter referred to as "the CREE device"), and the electrothermal coupling model is used to calculate the voltage and junction temperature changes during the surge process. The structural parameters of the CREE device are listed in Table I. We first need to establish the thermal and electrical characteristic models of the device and then substitute the surge current data into the electrothermal coupling model to calculate the voltage and junction temperature. Finally, we will compare the difference between the calculated results and the measured ones.

TABLE I
Parameters of the CREE Diode

Variable	Symbol	Value	Unit	Data source
Chip area	A_{chip}	0.0299	cm^2	Microscope
Active area	A_{act}	0.0207	cm^2	Microscope
Chip thickness	t_{chip}	370	μm	Microscope
Epitaxial doping conc.	N_{epi}	6.7×10^{15}	cm^{-3}	By C-V [12]
Epitaxial thickness	t_{epi}	11.8	μm	By C-V [12]
Sub doping conc.	N_{sub}	1.5×10^{18}	cm^{-3}	by on-resistance
Sub thickness	t_{sub}	358.2	μm	Microscope

TABLE II
Thermal Resistance and Capacitance of Each Layer of the CREE Diode

Layer name	Thermal resistance (K/W)	Thermal capacitance (J/K)
Chip	0.31	8.4×10^{-4}
Solder	0.69	0.0032
Copper plate	0.42	0.045

A. Thermal Characteristic Models

The thermal characteristic models of each layer of the device are the dependence of the thermal resistance/capacitance on temperature. Since the geometrical shape of each layer generally keeps the same, only the relationships between the thermal conductivity/specific heat capacity and temperature should be considered. Such relationships for the chip material 4H-SiC are expressed as [13], [14]

$$\begin{cases}\kappa_{\text{SiC}}(T)=4517\times T^{-1.29}[\text{W}/(\text{cm}\cdot\text{K})]\\ c_{V,\text{SiC}}(T)=5.13-\frac{1001}{T}+\frac{3.23\times10^4}{T^2}[\text{J}/(\text{cm}^3\cdot\text{K})].\end{cases} \tag{7}$$

The thermal conductivity/specific heat capacity of the solder and the copper plate can be treated as constants [15]–[18].

According to the definition formulae of thermal resistance ($R_{\text{th}} = \frac{L}{\kappa A}$) and thermal capacitance ($C_{\text{th}} = c_V AL$), for each layer we have

$$\begin{cases}R_{\text{th}}(T)=R_{\text{th}}\left(300\text{K}\right)\frac{\kappa(300\text{K})}{\kappa(T)}\\ C_{\text{th}}(T)=\frac{c_V\left(T\right)}{c_V\left(300\text{K}\right)}C_{\text{th}}\left(300\text{K}\right).\end{cases} \tag{8}$$

The abovementioned formulae relate the thermal resistance and thermal capacitance at any temperature with the ones at room temperature which can be obtained from the thermal impedance test results. The thermal impedance test is conducted on a mentor graphics power tester 1500 A according to the test standard JESD51-14 [19], and the results are given in Table II [20].

B. Electrical Characteristic Models

The electrical characteristic model of each layer of the device is the dependence of the voltage drop on temperature and current. Electrical characteristic models for four different types of electrical components should be established: the epitaxial layer,

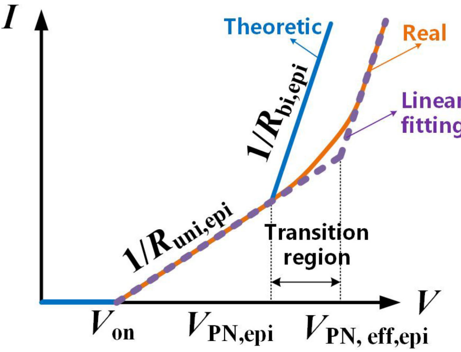


Fig. 4. Theoretical and actual forward *I*–*V* curves of the epitaxial layer of the MPS diode.

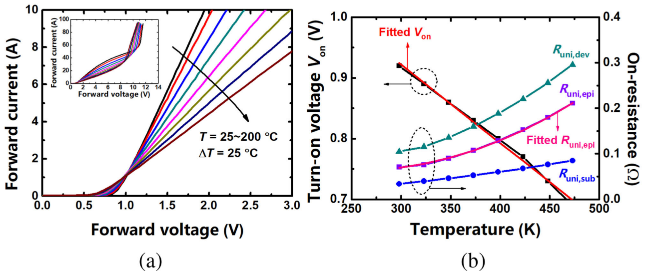


Fig. 5. (a) Measured forward *I*–*V* curves of the CREE device. The inset is the *I*–*V* curves at high current regimes. (b) Dependence of the turn-ON voltage of the device ($V_{\rm on}$), unipolar on-resistance of the epitaxial layer ($R_{\rm uni,epi}$), unipolar on-resistance of the substrate ($R_{\rm uni,sub}$), and unipolar total on-resistance of the device ($R_{\rm uni,dev}$) on temperature, extracted from (a).

substrate layers, solder layer, and copper layer. The substrate is a highly doped N-type semiconductor with a low minority carrier concentration, so it can be considered that it always works in unipolar conduction mode. The electron mobility is [21]

$$\mu_n = \frac{947 \times (T/300)^{-2}}{1 + \left(N_D/1.94 \times 10^{17}\right)^{0.61}} [\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})]. \quad (9)$$

Assuming that the thickness of the ith substrate layer is $t_{\rm sub,\it i}$, its voltage drop is

$$\begin{aligned} V_{\mathrm{sub},i}(I,T) &= \tfrac{1}{q\mu_n N_{\mathrm{sub}}}\tfrac{t_{\mathrm{sub},i}}{A_{\mathrm{chip}}} I \\ &= \tfrac{1+\left(N_{\mathrm{sub}}/1.94\times 10^{17}\mathrm{cm}^{-3}\right)^{0.61}}{1.5\times 10^{-16}\mathrm{cm}^2/\Omega}\tfrac{t_{\mathrm{sub},i}}{N_{\mathrm{sub}}A_{\mathrm{chip}}}\left(\tfrac{T}{300\mathrm{K}}\right)^2 I. \end{aligned} \quad (10)$$

For the solder layer or the copper plate, according to the relationships between the resistivity of the solder/copper and temperature [22], [23], their voltage drops can be ignored in the temperature and current range we consider. Thus, the *V*–*I* characteristic function of the solder layer or the copper plate can be directly set as zero, i.e.,

$$V_{\mathrm{solder/Cu}}(I,T) \equiv 0. \quad (11)$$

Now we discuss about the modeling of the electrical characteristics of the epitaxial layer. According to the shape of the forward *I*–*V* curves of MPS diodes [24], the blue line in Fig. 4 can be used to approximate the *I*–*V* curve of the epitaxial layer of the MPS diode. There are four parameters that completely determine the shape of the *I*–*V* curve: the turn-ON voltage $V_{\rm on}$, the on-resistance in unipolar mode $R_{\rm uni,epi}$, the on-resistance in bipolar mode $R_{\rm bi,epi}$, and the PN junction trigger voltage $V_{\rm PN,epi}$. With the knowledge of these four control parameters, we can use the following equation to calculate the voltage drop of the epitaxial layer from the current and temperature:

$$V_{\mathrm{epi}}(I,T) = \begin{cases} R_{\mathrm{uni,epi}} I + V_{\mathrm{on}}, 0 \le I < \frac{V_{\mathrm{PN,epi}} - V_{\mathrm{on}}}{R_{\mathrm{uni,epi}}} \\ R_{\mathrm{bi,epi}} I + \left(1 - \frac{R_{\mathrm{bi,epi}}}{R_{\mathrm{uni,epi}}}\right) V_{\mathrm{PN,epi}} \\ + \frac{R_{\mathrm{bi,epi}}}{R_{\mathrm{uni,epi}}} V_{\mathrm{on}}, I > \frac{V_{\mathrm{PN,epi}} - V_{\mathrm{on}}}{R_{\mathrm{uni,epi}}}. \end{cases} \quad (12)$$

Since $V_{\rm on}$ and $R_{\rm uni,epi}$ only involve the unipolar operating mode of the device, these two parameters can be directly extracted from the measured *I*–*V* characteristic curves to complete the modeling. Fig. 5(a) shows the measured forward *I*–*V* curves of the CREE device at different temperatures. The inset figure shows the forward *I*–*V* curves at the high current regimes. The relationship between $V_{\rm on}$ or $R_{\rm uni,dev}$ and the temperature T can be extracted from the *I*–*V* curves, as shown in Fig. 5(b). It is obvious that $V_{\rm on}$ decreases linearly as the temperature increases, so a linear function can be used to fit the relationship between $V_{\rm on}$ and T (the red line) while limiting the minimum value of $V_{\rm on}$ to zero. Therefore, the relationship between $V_{\rm on}$ and T is

$$V_{\mathrm{on}}(T) = \max\left\{-0.00129\mathrm{V/K} \times T + 1.31\mathrm{V}, 0\mathrm{V}\right\}. \quad (13)$$

As for the unipolar on-resistance of the epitaxial layer ($R_{\rm uni,epi}$), it can be extracted by subtracting the on-resistance of the substrate layer ($R_{\rm uni,sub}$) from the total unipolar on-resistance of the device ($R_{\rm uni,dev}$) with the parameters in Table I. Since the structure and doping concentration of the device are fixed, the unipolar on-resistance of each part only depends on the electron mobility. According to (9), the on-resistance of the device is always proportional to the square of the temperature. Therefore, a quadratic function can be used to fit the relationship between $R_{\rm uni,epi}$ and T

$$\begin{aligned} R_{\mathrm{uni}}(T) = {}& 3.08 \times 10^{-6}\Omega/\mathrm{K}^2 \times T^2 \\ & -1.56 \times 10^{-3}\Omega/\mathrm{K} \times T + 0.26\Omega. \end{aligned} \quad (14)$$

For real SiC MPS diodes there is a transition region on the *I*–*V* curve, shown as the orange curve in Fig. 4. It is mainly caused by the complicated structure of the P+ regions in the real SiC MPS diode [25], [26]. An MPS diode usually contains multiple P+ regions with different locations and sizes: small and large P+ cells in the active region, and a larger extension of P+ region near the junction termination. A P+ region is triggered ON when the voltage drop below it exceeds the PN junction voltage in SiC. This voltage drop is determined by the current density and the sheet resistance below this P+ region. The wider the P+ region, the lower its trigger-ON voltage. As the forward voltage bias of the device increases, the large P+ region near the junction termination triggers ON first, followed by the large P+ cells, and finally, the small P+ cells in the active region are triggered ON. Therefore, the P+ region trigger-ON process of the MPS diode is extended and blurred, which results in a transition region on the *I*–*V* curve. In order to eliminate the influence of this transition

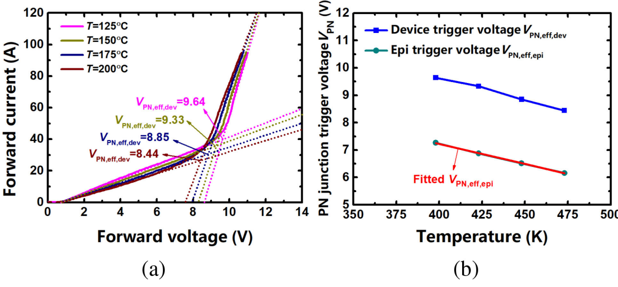


Fig. 6. (a) Equivalent PN junction trigger voltage $V_{\mathrm{PN,eff,dev}}$ can be extracted from the forward *I–V* curves of four temperatures with unobvious self-heating effect. (b) Extracted $V_{\mathrm{PN,eff,dev}}$ and $V_{\mathrm{PN,eff,epi}}$ of the epitaxial layer obtained by subtracting the voltage drop of the substrate part from $V_{\mathrm{PN,eff,dev}}$.

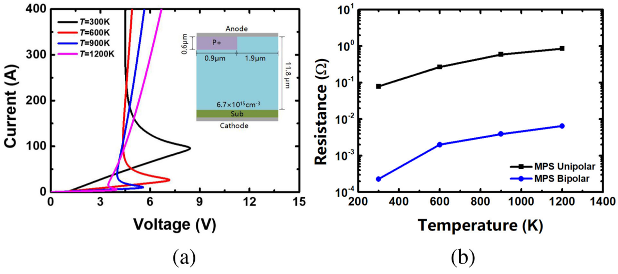


Fig. 7. (a) Simulated *I–V* curves of the epitaxial layer of the CREE diode at different temperatures. The inset shows the simulation structure. (b) Unipolar and bipolar on-resistances of the epitaxial layer extracted from (a).

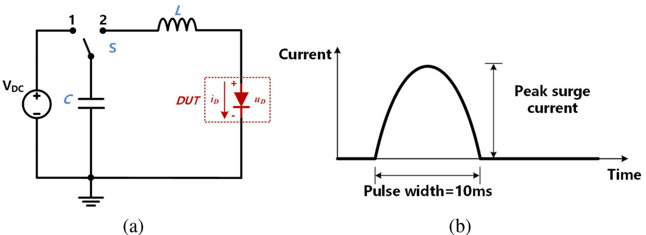


Fig. 8. (a) Surge test circuit diagram. (b) Half-sinusoidal forward current pulse used in surge test, with a pulse width of 10 ms.

region, we extend the unipolar part and the bipolar part of the measured *I–V* curve, and call the voltage value corresponding to the intersection the "equivalent PN junction trigger voltage of the epitaxial layer" $V_{\mathrm{PN,eff,epi}}$, as the purple curve shown in Fig. 4. The abovementioned method is applied to the measured *I–V* curves of the CREE diode, as shown in Fig. 6(a). Due to the inevitable self-heating effect during the measurement of the *I–V* characteristics, which results in distortion of the *I–V* curves, we only select the measurement results at four temperatures (125 °C, 150 °C, 175 °C, and 200 °C) where the self-heating effect is unobvious. The extraction result is shown as the blue curve in Fig. 6(b). By subtracting the voltage drop of the substrate part from the equivalent PN junction trigger voltage of the device $V_{\mathrm{PN,eff,dev}}$, the equivalent PN junction trigger voltage of the epitaxial layer $V_{\mathrm{PN,eff,epi}}$ can be obtained. We can use a linear function to fit the relationship between $V_{\mathrm{PN,eff,epi}}$ and T while limiting its minimum value to zero. The final relationship between $V_{\mathrm{PN,eff,epi}}$ and T is

$$V_{\mathrm{PN,eff,epi}}(T) = \max\{-0.0147\mathrm{V/K} \times T + 13.1\mathrm{V}, 0\mathrm{V}\}. \tag{15}$$

As for the modeling of the bipolar on-resistance $R_{\mathrm{bi,epi}}$, considering that the epitaxial layer in bipolar conduction mode actually operates in a large injection situation, $R_{\mathrm{bi,epi}}$ is very small compared with $R_{\mathrm{uni,epi}}$. It will lead to a large error if $R_{\mathrm{bi,epi}}$ is obtained by subtracting the substrate resistance from the total on-resistance of the device. TACD simulation is used here to help handle such a problem. A simulation structure of the epitaxial layer of the CREE diode is established, as the inset in Fig. 7(a) shows. It has a very thin substrate layer at the cathode to meet the metal contact boundary condition. The simulated *I–V* curves are shown in Fig. 7(a), and the extracted unipolar and bipolar on-resistances are shown in Fig. 7(b). The negative differential resistance branches on the simulated *I–V* curves will not appear on the measured ones because of the blurred and extended trigger-ON process of the multiple P+ regions [10]. It is obvious that at any temperature from 300 to 1200 K, $R_{\mathrm{bi,epi}}$ keeps approximately 1/100 of $R_{\mathrm{uni,epi}}$. Thus, $R_{\mathrm{bi,epi}}$ has less effect on the device characteristics. For simplicity, we can set

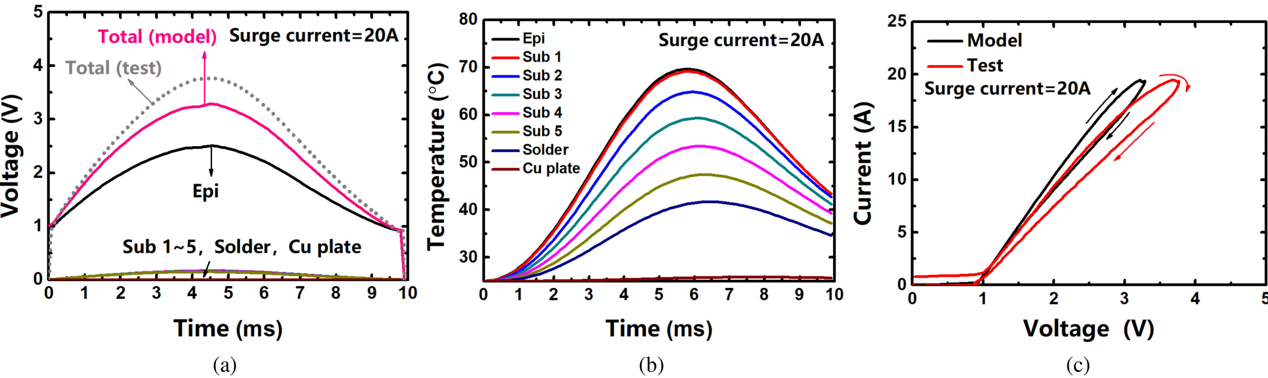
$$R_{\mathrm{bi,epi}}(T) = \frac{1}{100} R_{\mathrm{uni,epi}}(T). \tag{16}$$

At this point, we have completed the electrical and thermal modeling of the entire device.

C. Junction Temperature Calculation During Surge Process

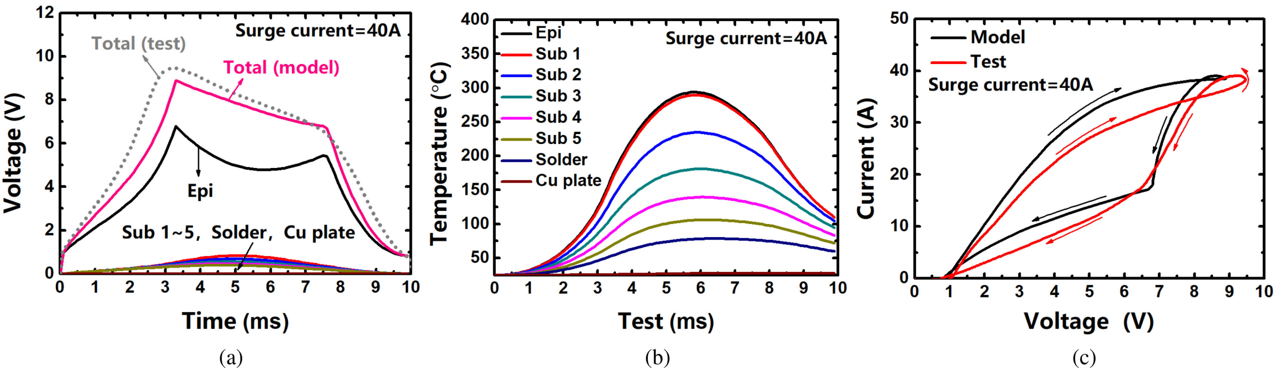
After completing the modeling of the electrical and thermal characteristics of the device, we can use the electrothermal coupling model to calculate the voltage and junction temperature during the surge process, and compare the calculation results with the measured ones. The surge current test circuit used is shown in Fig. 8(a), which consists of a dc voltage source V_{dc}, a capacitor C, an inductor L, a switch S, and the device under test DUT. A half-sinusoidal forward current pulse with a pulse width of 10 ms is used, as shown in Fig. 8(b). As the test starts, the switch S connects to point 1 and the capacitor C is charged by V_{dc}; as the charging process is finished, S connects to point 2 and the surge current pulse is generated by the resonance of the capacitor C and the inductor L. The current peak amplitude of the current pulse can be adjusted by V_{dc}. During each test, such a current pulse is applied on the device while the device voltage and current waveforms are recorded. After each test, the device is cooled down to ensure that its temperature drops down to room temperature. The current peak amplitude of each test is increased until the failure of the device.

As for the calculation, the epitaxial layer is regarded as one layer, and the substrate is divided into five layers. The solder or the copper plate is regarded as one layer, respectively. Figs. 9–12 show the calculation results at different surge currents. Each group of figures is divided into three subfigures, which represent the voltage drop of each layer, the temperature change of each layer, and the *I–V* trajectory, respectively. Each figure (a) also shows the measured total voltage drop of the device (the dashed line) and each figure (c) also shows the



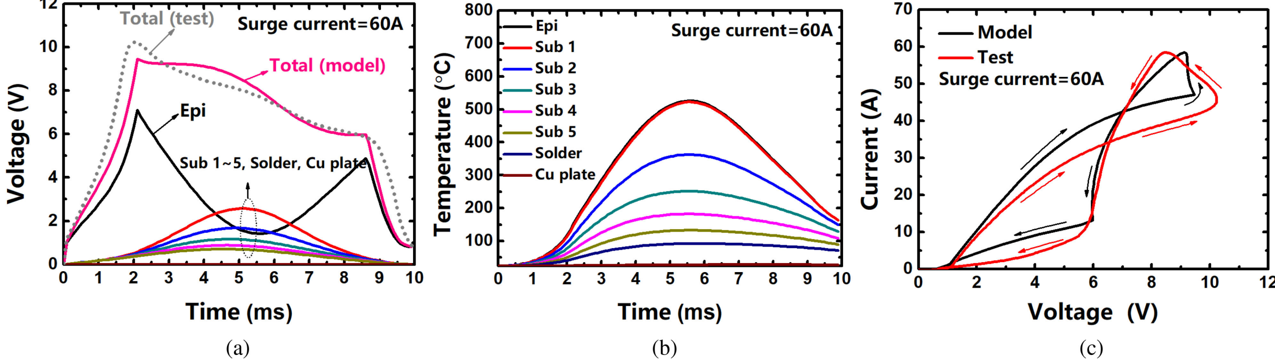
(a) (b) (c)

Fig. 9. Calculated (a) voltage drop and (b) temperature change of each layer of the CREE diode, as well as (c) the I–V trajectory when the surge current is 20 A.



(a) (b) (c)

Fig. 10. Calculated (a) voltage drop and (b) temperature change of each layer of the CREE diode, as well as (c) the I–V trajectory when the surge current is 40 A.



(a) (b) (c)

Fig. 11. Calculated (a) voltage drop and (b) temperature change of each layer of the CREE diode, as well as (c) the I–V trajectory when the surge current is 60 A.

measured I–V trajectory (the solid line). It can be seen that in each figure (a), the calculated total voltage drop curves are all close to the measured results. Detailed analyses are arranged as follows.

As shown in Fig. 9, when the surge current is 20 A, the voltage drop curves of the epitaxial layer and the total device show the shape of a single-peak curve, and the I–V trajectory shows one circle. The device works in unipolar mode during the entire surge process. The junction temperature reaches a peak value of 69 °C at 5.8 ms. Due to the low temperature at this time, the voltage drop of any substrate layer is negligible, and the voltage drop of the epitaxial layer accounts for most of the total voltage drop of the device.

As shown in Fig. 10, when the surge current increases to 40 A, there are two obvious turning points (the first at 3.3 ms and the second at 7.5 ms) on the calculated voltage drop curves of the epitaxial layer and the total device. Between the two turning points, the device works in bipolar mode, in which the trigger voltage of the PN junction decreases as the temperature increases. Thus, the voltage drops of the epitaxial layer and the total device decrease with time. There is an obvious concave part on the epitaxial layer voltage drop curve, resulting in two circles

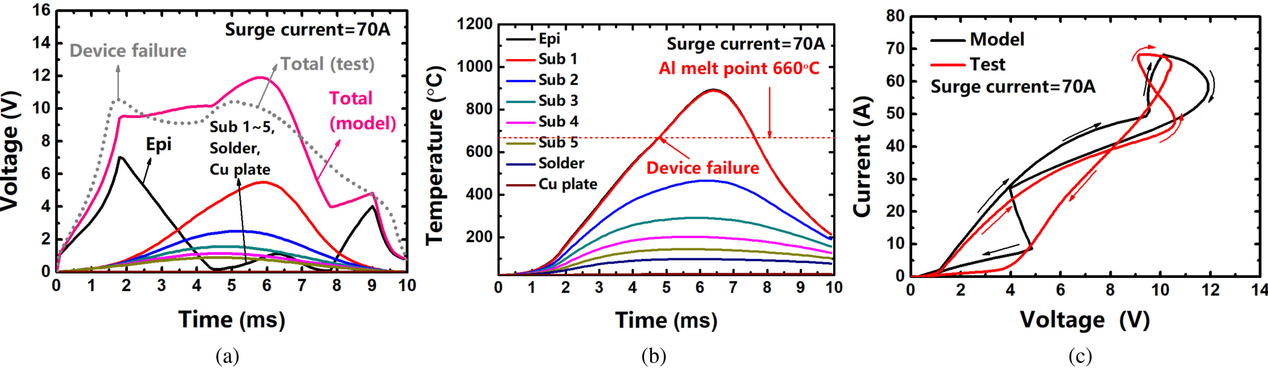


Fig. 12. Calculated (a) voltage drop and (b) temperature change of each layer of the CREE diode, as well as (c) the *I*–*V* trajectory when the surge current is 70 A.

on the *I*–*V* trajectory. This is the "dynamic negative resistance" phenomenon. The on-resistance of the substrate is still at a negligible level, so most of the voltage drop still comes from the epitaxial layer. The main junction temperature reaches a peak of 295 °C at 5.7 ms.

When the surge current increases to 60 A, the basic operating mode of the device is similar to that of 40 A, as shown in Fig. 11. Since the temperature of the device is higher at this time, the PN junction trigger voltage decreases more obviously with the temperature. The second circle representing the bipolar mode on the *I*–*V* trajectory also gradually becomes larger. The main junction temperature reaches a peak value of 528 °C at 5.6 ms.

When the surge current increases to 70 A, the working state of the device changes again, as shown in Fig. 12. There are four obvious turning points on the calculated voltage drop curves (the first at 1.8 ms, the second at 4.5 ms, the third at 7.4 ms, and the fourth at 8.9 ms). During 4.5–7.4 ms, the voltage drop of the epitaxial layer increases from a small value and then decreases again. During this period, the device operates at a large injection situation, and the bipolar on-resistance of the epitaxial layer increases since the carrier mobilities decrease due to high temperature. A high current density combined with an increasing on-resistance leads to an increasing voltage drop of the epitaxial layer. At the same time, the voltage drop of the substrate occupies the main part of the total voltage drop, and it increases with the increase of temperature, so the total voltage drop shows an increasing trend. The four turning points on the total voltage drop curve result in three circles on the *I*–*V* trajectory of the device, which is consistent with the measured results. The calculated main junction temperature reaches a peak value of 890 °C at 6.4 ms. However, the main junction temperature has already reached the melting point of the aluminum electrode (660 °C) at 4.8 ms, so the device fails at this time. This is consistent with the decapsulation results of the device.

Fig. 13(a) summarizes the main junction temperature curves of the CREE device calculated by the conventional RC thermal circuit model and the electrothermal coupling model during the surge process. Fig. 13(b) shows the peak temperature of the main junction extracted from Fig. 13(a). It can be seen that when the surge current is low, the results calculated by the two models are almost the same. When the surge current gradually increases, the

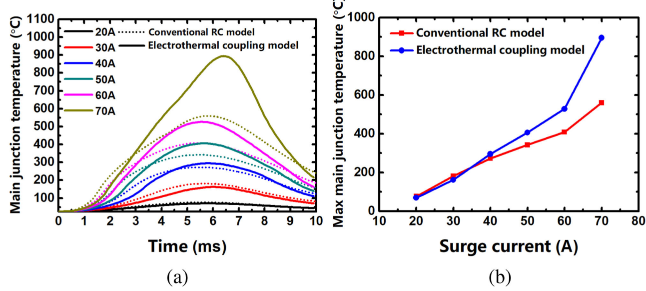


Fig. 13. (a) Main junction temperature change during the surge process and (b) peak junction temperature at each surge current calculated by the conventional RC thermal circuit model and the electrothermal coupling model.

temperature of each layer of the device also gradually increases, resulting in an increasing difference between the calculation results of the two models, and the conventional RC model will increasingly underestimate the device temperature. Thus, it is necessary to use the electrothermal coupling model to calculate the junction temperature change.

V. Conclusion

This article proposes an electrothermal coupling model suitable for calculation of the junction temperature during the surge process. The model uses an electrical branch and a thermal branch to simulate the electrical and thermal behavior of the actual device. Each component in the electrical branch takes the current flowing through itself and the temperature as input, and outputs the corresponding voltage drop. The thermal branch takes its self-heating power as input and outputs the temperature change of each node. The temperature change at each node further changes the electrical and thermal characteristics of each component at the corresponding location. This electrothermal coupling model gives out the voltage drop and temperature change of each layer of the device from the static electrical characteristics and thermal resistance/capacitance parameters of the device without the implementation of actual surge tests. Compared with the conventional RC thermal circuit model, this new model is closer to the actual situation; compared with device dynamic numerical simulation, this new model has the higher

computational efficiency. The use of this new model will greatly deepen our understanding of the behavioral characteristics of the device during the surge process and improve the efficiency of device reliability analysis and optimization.

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