An Asymmetrical DAB Converter Modulation and Control Systems to Extend the ZVS Range and Improve Efficiency

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***Abstract*—This article presents a new optimized hybrid modulation and control systems based on symmetrical and asymmetrical operations of a dual-active-bridge converter to minimize the transformer root-mean-square (RMS) current and extend the zero-voltage-switching (ZVS) range. Various modulation modes are analyzed, and their corresponding power, RMS current equations, and soft-switching conditions are derived. The RMS equations are minimized using the multivariable optimization method, and the corresponding parametric equations are obtained. A hybrid control system has been proposed to regulate the battery current, to ensure smooth inductor current transients, and eliminate the need for a blocking capacitor on the low-voltage side. Using asymmetrical-extended-phase-shift and conventional symmetrical modes, a wider ZVS range is achieved compared to advanced modulations, such as triple phase shift. Moreover, in the low-power region, an optimized RMS current is achieved by applying an optimum dc voltage on the blocking capacitor at the HV side. Hybrid modulation that extended ZVS range and improved RMS current makes the proposed approach a suitable modulation for high-frequency applications and also high-voltage or high-current applications with high C_{oss} losses. The efficiency, ZVS operation, and control system performance are validated by a 5 kW converter.**

***Index Terms*—Asymmetric modulation, dual-active-bridge (DAB) converter, extending zero-voltage-switching (ZVS) range, hybrid modulation, minimizing root-mean-square (RMS) current.**

NOMENCLATURE

V_{bat}	Battery voltage.
V_i	dc-link voltage.
i	Inductor current.
i_{bat}	Battery current.
V_b	Blocking capacitor voltage.
V_c	Output capacitor voltage.
i_s	LV-side bridge rectified current.
V_{ab}	HV-side bridge output voltage.
V_{cd}	LV-side bridge output voltage.
C	Blocking capacitance.
L	DAB converter inductance.
N	Transformer turns ratio.
M	Voltage gain.
C_{bat}	Battery filter capacitance.
L_f	Battery filter inductance.
R_f	Battery filter inductor resistance.
R_p	DAB converter primary resistance.
R_s	DAB converter secondary resistance.
f_s	Switching frequency.
T_s	Switching period.
ω	Switching frequency in radian.
V_{iM}	Input rated voltage.
$V_{\text{bat}M}$	Battery rated voltage.
P_{base}	Base power equal to DAB converter rated power.
L_{base}	Base inductance.
d_1	V_{ab} positive output duty cycle.
d_2	V_{ab} negative output duty cycle.
$d_3 = d_4$	LV bridge duty cycle.
θ	Phase angle between V_{ab} and V_{cd}.
SPS	Single phase shift.
EPS	Extended phase shift.
AEPS	Asymmetric EPS.
LV	Low voltage.
HV	High voltage.

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I. INTRODUCTION

TO CREATE a more flexible and reliable power grid system, especially with the increasing number of intermittent energy sources, such as wind, solar, and hydro, the use of energy storage units have become indispensable. Among various available options for storage units, batteries have found wider applications due to cost-effectiveness, modular nature, and ease of installations [1], [2] and are commonly utilized in residential

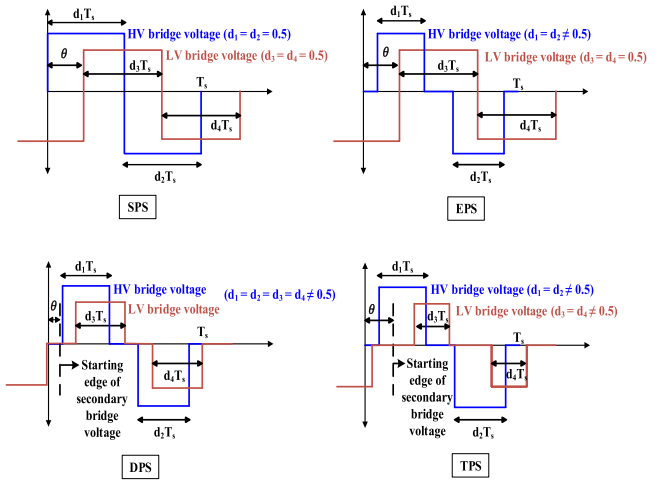

Fig. 1. Operating waveforms of the DAB under common modulation methods.

applications. To interface these batteries to the grid, bidirectional dc–dc converters are used as basic building blocks in ac–dc conversions [3]. Owing to the wide-range variation of the load and sources in residential loads, it is crucial to ensure a high bidirectional converter efficiency over a wide operational range.

The isolated bidirectional dual active bridge (DAB) is a suitable converter for battery interface as it provides high power density, natural bidirectional power transfer capability, galvanic isolation, and extended soft switching range [4]–[8]. As shown in Fig. 1, there are several existing modulation methods for DAB converters focusing on extended zero-voltage-switching (ZVS) range, minimizing root-mean-square (RMS) current and reactive power loss, where the principle of power transfer in all these methods is governed by the phase-shift control method [7]. The most commonly used modulation is the SPS, also termed conventional phase shift [9]–[12]. SPS provides simple control and implementation; however, the converter suffers from high transformer RMS current and limited ZVS range while moving away from the nominal operating point [13], [14]. The EPS provides better adaptivity to changing operating conditions by introducing an inner phase-shift control through HV duty cycle control [14]–[18]. Equally controlling the inner modulation of both the HV and LV bridges results in the dual-phase-shift (DPS) modulation [19]–[22]. In the triple-phase-shift (TPS) modulation, the LV and HV inner modulations are controlled independently, and thus, the highest control flexibility among all the symmetrical modulations is achieved [23]–[28]. Although TPS has more complex modulation and control to achieve a unified solution for the phase shifts compared to EPS or DPS, it can optimize the RMS current, as shown in [23] and [24]. In the low-power region, however, TPS can only guarantee zero current switching (ZCS) for six switches and ZVS for only two switches. Although using the approach in [29], the low-power ZVS range is extended compared to [23] at the expense of higher RMS current, there are still ZCS switching for six of the switches in the medium-power range. In the applications where C_{oss} losses are significant, ZCS may lead to excessive losses and ZVS is more desirable. To extend the ZVS operating range and reduce RMS current, recent papers have proposed asymmetrical modulations that use unequal duties on the bridges or hybrid modulations. The majority of these publications have only considered asymmetrical duty cycles for very special cases among all the possible asymmetrical modulations. For example, the study in [30] proposes an asymmetrical pulsewidth modulation (APWM) operation based on a single asymmetrical mode of operation. Although this assumption simplifies the solution, it generates a high RMS current as the converter is only operating in a narrow voltage gain (M) region and its full capability is not utilized. Moreover, the proposed APWM can only guarantee turn-ON ZCS for six switches and turn-ON ZVS for the other two switches. To further optimize the operation, a hybrid modulation is presented in [31], which proposes a combination of SPS and APWM with a simple optimization objective of setting M equal to 1 with the aid of a dc-blocking capacitor. Even though this setting leads to lower optimization complexity, its efficiency significantly drops in the middle M range due to higher RMS current and narrower ZVS operating range. Alternatively, the study in [32] employs a half-bridge DAB using blocking capacitors in both the LV and HV sides, which limits the application of the approach to low-power levels and a very narrow range of M as once M deviates from the desired value, the efficiency drops due to high RMS current. Asymmetric modulation is also reported for three-phase DAB converters [33], [34], showing improvement compared to the symmetric three-phase DAB in terms of RMS and ZVS range especially at light loads. However, they still operate the three-phase DAB converter under ZCS or even hard switching at light loads and have more complex hardware compared to a single-phase DAB.

This article proposes a hybrid modulation to optimize the efficiency throughout the operation region. For high-power or high-M operation, known modulations, such as TPS, are shown to be the best option and, thus, generated by the proposed hybrid approach. However, for low M and low power, which is the region that the efficiency is impaired by most of the conventional methods, such as SPS or EPS, this article introduces novel asymmetrical modulation modes, which are capable of maintaining ZVS while minimizing the RMS current. In these modes, unequal duties are used on the HV-side bridge, creating an asymmetric waveform, as shown in Fig. 3(b). The duty ratios on the LV bridge are kept at 50% value; thus, this modulation is called AEPS. The proposed solution only uses a capacitor on the HV side, which carries a significantly lower current and, thus, has a small size and negligible losses. With the aid of blocking capacitor, hybrid modulation provides a wider low-power ZVS range and reduced effective ac voltage on the DAB inductor resulting in a lower inductor current ripple and, thus, optimized RMS current. In fact, the AEPS DAB converter can be used in a number of applications given the advantages of AEPS, such as extended ZVS range. Unlike other existing approaches that only provide ZCS, AEPS guarantees ZVS for a wide operating range, and thus, it will be very suitable for high-frequency applications where C_{oss} losses become significant. It is also suitable for HV or high-current applications, where the output capacitance of available semiconductors is relatively high and ZCS and C_{oss} losses cannot be tolerated. Moreover, AEPS provided an

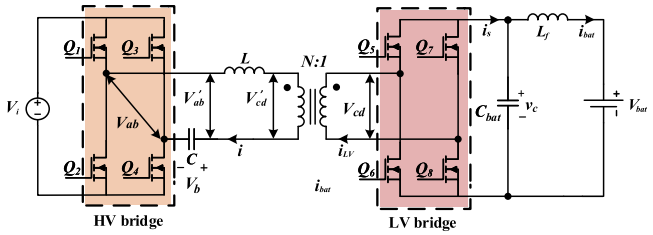

Fig. 2. DAB converter.

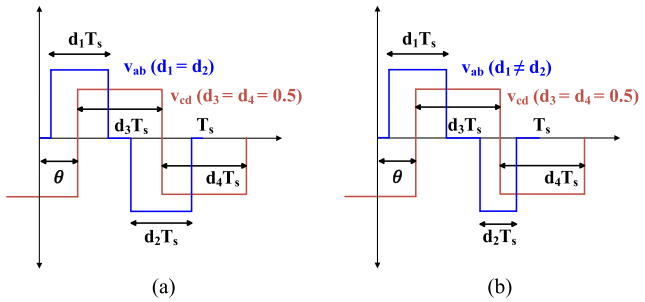

Fig. 3. Basic principle of AEPS modulation. (a) Conventional EPS. (b) Asymmetric EPS or AEPS.

extended ZVS and optimized RMS current that becomes important in applications where the converter may operate at a low-power level for an extended time duration. For example, a battery storage power supply for residential applications rarely operates at its full capacity because normally not all electric appliances and electric loads are turned ON and the system normally ends up operating below 40% rated capacity for the majority of operation time; thus, low-power-range efficiency becomes very important.

To control the power and implement the optimized hybrid modulation, a novel control system with practical considerations is designed and implemented. This control system regulates the battery current, makes the inductor current transient smoother, and eliminates the need for a blocking capacitor in the LV side. The advantages of hybrid modulation and the optimization algorithm proposed in theory and the operational performance of the controllers are validated by a 5 kW GaN-based experimental setup.

II. Proposed Hybrid Modulation

A. General Description of a DAB Converter

Fig. 2 shows the topology of a bidirectional DAB dc–dc converter. Switches Q_1–Q_4 form the HV-side full bridge and Q_5–Q_8 form the LV-side full bridge. In this article, the LV side of the DAB is connected to a battery source V_{bat}, while the HV side is connected to a dc link, which may be feeding a grid-connected inverter. As the dc-link voltage is controlled by the succeeding inverter stage whose analysis is out of the scope of this article, the dc-link voltage is modeled as a constant voltage source V_i. The leakage inductor L is the main energy transferring element, N is the turns ratio, C is the dc-blocking capacitor, L_f is the output filter inductor, and i is the tank current.

The voltage gain ratio is defined as $M = \frac{NV_{\text{bat}}}{V_i}$. The operating power is given by $P = V_{\text{bat}} i_{\text{bat}}$, where i_{bat} is the battery current. The DAB converter in this article is either in the charging mode ($M < 1$ and $P > 0$) or the discharging mode ($M < 1$ and $P < 0$), and according to [35], these two states have similar modulations with similar equations, with the exception of opposite sign in the power, which subsequently results in an opposite sign of θ. For this reason, this study only focused on the charging ($M < 1$ and $P > 0$) case. In the case of design with $M > 1$, the dc-blocking capacitor must be located on the LV side, which is not covered in this article to avoid placing the capacitor on the high-current side.

TABLE I
Maximum Power of Different AEPS Modes

Mode A	$P_{\max_A} = \frac{P_{\text{base}}}{\alpha_L}(\frac{V_i}{V_{iM}})(\frac{V_{\text{bat}}}{V_{\text{bat}\,M}})$
Mode B	$P_{\max_B} = \frac{2P_{\text{base}}}{3\alpha_L}(\frac{V_i}{V_{iM}})(\frac{V_{\text{bat}}}{V_{\text{bat}\,M}})$
Mode C	$P_{\max_C} = \frac{2P_{\text{base}}}{3\alpha_L}(\frac{V_i}{V_{iM}})(\frac{V_{\text{bat}}}{V_{\text{bat}\,M}})$
Mode D	$P_{\max_D} = \frac{P_{\text{base}}}{2\alpha_L}(\frac{V_i}{V_{iM}})(\frac{V_{\text{bat}}}{V_{\text{bat}\,M}})$

B. Principle of Hybrid Modulation

Unlike conventional modulations such as EPS shown in Fig. 3(a) in the AEPS modulation, as shown in Fig. 3(b), the duty cycles d_1 and d_2 on the two half periods of the HV bridge voltage v_{ab} are controlled asymmetrically and independently. This modulation results in an asymmetric V_{ab} voltage with a dc average equal to $V_i(d_1 - d_2)$. This dc component is removed by the capacitor C, thus creating $v'_{ab} = v_{ab} - V_i(d_1 - d_2)$. It can be seen that the control of d_2 is independent of d_1 in AEPS modulation and provides the extra degree of freedom that shapes the tank current waveform with the desired peak values and polarity at the switching instants. This results in a reduction of the transformer RMS current and switching losses.

The modes of operation are defined according to the HV-side (V_{ab}) and the LV-side (V_{cd}) voltage edge sequences. For example, in Mode A, according to Fig. 4 with $d_1{}' = 0.5 - d_1$ and $d'_2 = 0.5 - d_2$: $\theta \geq d'_1\pi$ that results in $d_1 \geq 0.5 - \theta/\pi$, and $(1 + d'_2)\pi \leq \pi + \theta$ that results in $d_2 \geq 0.5 - \theta/\pi$, and in the mode D: $d'_1\pi \geq \theta$ that leads to $d_1 \leq 0.5 - \theta/\pi$ and $(1 + d'_2)\pi \geq \pi + \theta$ that results in $d_2 \leq 0.5 - \theta/\pi$. Thus, according to the above equations, the limits of d_1 and d_2 are different in various modes, and accordingly, the maximum transferable power level is different, as illustrated in Table I. The definition of EPS modes D and A coincides with that of the AEPS in modes D and A when $d_1 = d_2$, respectively. In other words, when the HV-side bridge duties are equal, the modulation is called EPS, and when they are unequal, it is called AEPS.

C. Power Equation and Normalization

Using the voltage and current waveforms from Fig. 4, the average power equation can be derived. The general and maximum power equations for all the AEPS modes can be obtained as listed in Table I. For instance, the average power equation for

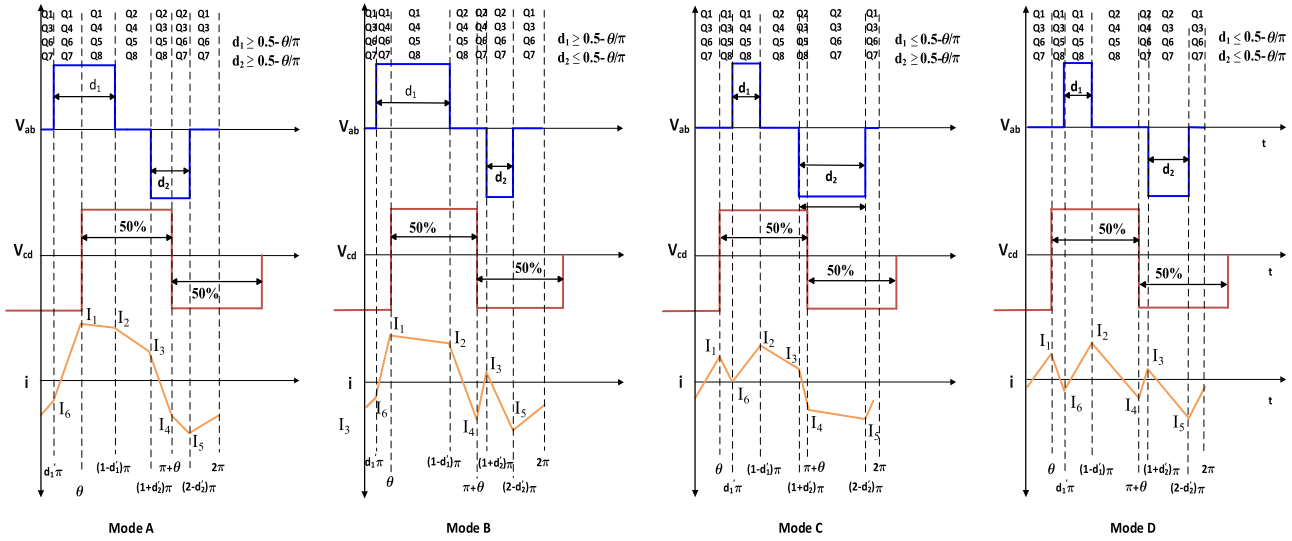

Fig. 4. Typical operating waveforms of a DAB converter under different AEPS modulation modes.

Mode D is derived as

$$P_D = \int_0^{2\pi} \frac{v'_{cd}(wt)i(wt)}{2\pi} d(wt) = \frac{V_i(MV_i)(d_1+d_2)\theta}{wL} \quad (1)$$

where v'_{cd} and $i = \int_0^{2\pi} \frac{v'_{ab}-v'_{cd}}{L} d\theta$, which can be obtained using Fig. 4. Setting the duty cycles to the boundary values at $d_1 = 0.5 - \frac{\theta}{\pi}$ and $d_2 = 0.5 - \frac{\theta}{\pi}$ provides the maximum power in Mode D as follows:

$$P_{\max_D} = \frac{V_i(MV_i)}{16fL}. \quad (2)$$

In order to obtain generalized results, per-unit values are used for parameters such as power and inductance L. Since Mode A generates the highest power capacity, $P_{\max_A}$ is used as a base to express all parameters in per unit. Thus, two per-unit quantities are defined: power percentage $\alpha_P = \frac{P}{P_{\text{base}}}$ and inductance percentage $\alpha_L = \frac{L}{L_{\text{base}}}$, where P_{base} is the converter rated power, which is 5 kW in this research. L_{base} can be calculated as

$$L_{\text{base}} = \frac{V_{iM}(NV_{\text{bat}M})}{8f_s P_{\text{base}}} \quad (3)$$

where V_{iM} is the rated inverter dc-bus voltage and $V_{\text{bat}M}$ is the rated battery voltage. For example, using the base quantities, the maximum power deliverable in Mode D will be

$$P_{\max_D} = \frac{P_{\text{base}}}{2\alpha_L}\left(\frac{V_i}{V_{iM}}\right)\left(\frac{V_{\text{bat}}}{V_{\text{bat}M}}\right). \quad (4)$$

Table I summarizes the maximum power equations of all the AEPS modes. Fig. 5 shows the transferred power curves of different AEPS modes with respect to θ for two values of M. The pattern of these curves provides an insight on the best AEPS modes for a given operating condition. Mode A provides the highest power capacity at $d_1 = d_2 = 0.5$, which is basically the conventional SPS, while AEPS Mode D provides the lowest transferable power. Modes B and C show identical power flow curves with interchanged values of d_1 and d_2; that is why, in this article, Mode B has been selected for the detailed

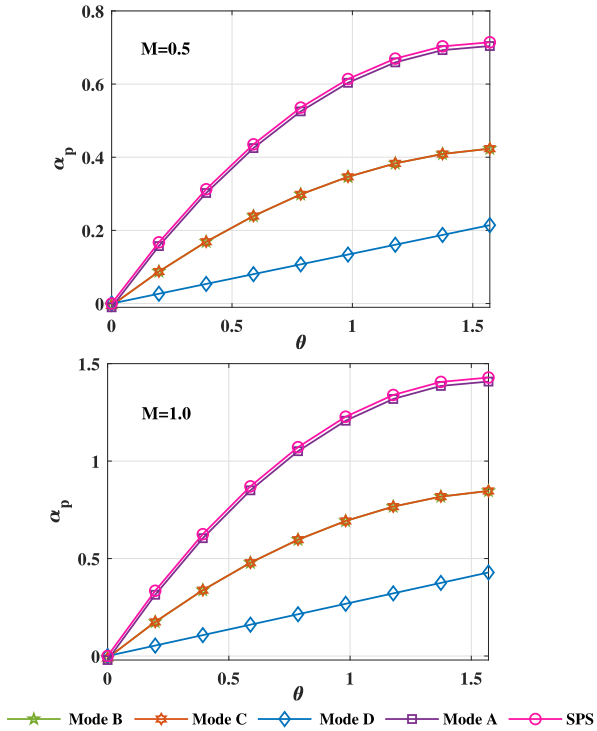

Fig. 5. Normalized power versus θ curves at two values of M for different modes.

analysis. In addition, symmetrical parameters similar to EPS are used for Mode A, because this mode always achieves its minimum i_{rms} values under symmetrical EPS modulation for all the operating conditions. Fig. 6 shows that the i_{rms} values under AEPS modulation are always either equal to or higher than its EPS counterparts. Thus, AEPS operation for mode A will not be used. Therefore, the hybrid modulation incorporates three modes of operation in this article: Mode A with EPS, Mode B with AEPS, and mode D with either EPS or AEPS modulations.

TABLE II
SWITCHING INSTANT CURRENT AND PHASE-SHIFT EQUATIONS FOR DIFFERENT MODES

Mode	Modulation	Switching Currents	Phase Shift
Mode A	EPS	$I_1 = k(\theta + 0.5\pi(M-1)); I_2 = k(M\theta + \pi d_1(1-M));$ $I_3 = k(M\theta - \pi M + \pi d_1(1+M)); I_4 = -I_1; I_5 = -I_2; I_6 = -I_3.$	$\theta = \pi(0.5 - \sqrt{d_1 - d_1^2 - k_2})$
Mode B	AEPS	$I_1 = k(\theta(d_2 - d_1 + 1) - 0.5\pi(d_2 - d_1 + 1 - M));$ $I_2 = k(M\theta + \pi d_1(1 + d_2 - d_1 - M)); I_3 = k(-M\theta + \pi d_2(1 + d_1 - d_2 - M));$ $I_4 = k(\theta(d_2 - d_1) + 0.5\pi(d_2 + d_1 - M)); I_5 = k(-M\theta + \pi d_2(d_2 + M - d_1 - 1));$ $I_6 = k(-M\theta + \pi M + \pi d_1(d_1 - d_2 - 1 - M)).$	$\theta = \pi(0.5 + d_2 - \sqrt{d_2^2 - d_1^2 + d_2 + d_1 - 2k_2})$
Mode D	AEPS	$I_1 = k(\theta(d_2 - d_1) - 0.5\pi(d_1 + d_2 - M)); I_2 = k(M\theta + \pi d_1(1 + d_2 - d_1 - M));$ $I_3 = k(-M\theta + \pi d_2(1 - d_2 + d_1 - M)); I_4 = k(\theta(d_2 - d_1) + 0.5\pi(d_2 + d_1 - M));$ $I_5 = k(-M\theta + \pi d_2(-1 - d_1 + d_2 + M)); I_6 = k(M\theta - \pi d_1(d_2 - d_1 - M + 1)).$	$\theta = (\pi k_2)/(d_1 + d_2)$

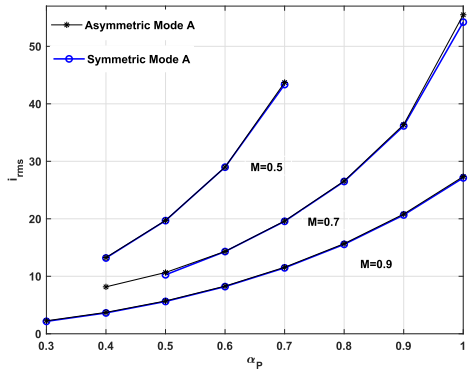

Fig. 6. Comparison of i_{rms} of EPS and AEPS Mode A.

D. ZVS Condition

As shown in [15], to operate DAB under soft switching, the current polarity at the instants of the bridge voltage polarity transitions, as shown in Fig. 4, needs to satisfy the following conditions:

$$\begin{cases} I_6 = i(d_1'\pi) < 0, & \text{HV bridge} \\ I_3 = i((1+d_2')\pi) > 0, & \text{HV bridge} \\ I_1 = i(\theta) > 0, & \text{LV bridge} \\ I_4 = i(\theta + \pi) < 0, & \text{LV bridge} \end{cases}. \tag{5}$$

Evaluating (5) and the switching instant current equations expressed in Table II for each mode, the range of output power for which the DAB converter can operate under ZVS can be calculated.

E. RMS Current Equation

Using Table II and referring to Fig. 4, for any given V_i, V_{bat}, P, d_1, and d_2 values, the inductor current shape and its RMS current in each mode of operation can be calculated. As an example, the inductor RMS current equation for AEPS Mode D is

$$\begin{aligned} i_{\text{rms}}^2 = k^2 \Bigg[& \frac{\pi^2}{3}d_1^4 + \left(\frac{\pi^2 M}{3} - \frac{\pi^2 d_2}{3} - \frac{2\pi^2}{3}\right) d_1^3 + \frac{\pi^2}{3}d_1^2 \\ & + \left(M\theta^2 - \frac{\pi^2 M}{4} - \frac{\pi^2 d_2^3}{3} + \frac{\pi^2 d_2}{3}\right) d_1 + \frac{\pi^2}{3}d_2^4 \\ & + \left(\frac{\pi^2 M}{3} - \frac{2\pi^2}{3}\right) d_2^3 \\ & + \frac{\pi^2}{3}d_2^2 + \left(M\theta^2 - \frac{\pi^2 M}{4}\right) d_2 + \frac{\pi^2 M^2}{12}\Bigg] \end{aligned} \tag{6}$$

where

$$\begin{cases} k_2 = \frac{2PfL}{V_i(MV_i)} = \frac{\alpha_L \alpha_P}{4}\left(\frac{V_{iM}}{V_i}\right)\left(\frac{V_{\text{bat}M}}{V_{\text{bat}}}\right) \\ k = \frac{V_i}{2\pi f L} \end{cases} \tag{7}$$

and the phase shift (θ) is provided in Table II.

F. Minimizing RMS Current

To minimize the RMS current equation, such as (6), the corresponding equations of d_1 and d_2 need to be derived using the multivariable optimization method. It is to be noted that θ is a function of d_1 and d_2. The multivariable optimization of (6) with respect to d_1 and d_2 results in the following:

$$\begin{aligned} & Md_1^2 - \frac{M}{4} + \frac{4}{3}d_1^3 - d_1^2 d_2 - 2d_1^2 \\ & \quad + \frac{2}{3}d_1 - \frac{d_2^3}{3} + \frac{d_2}{3} - \frac{Mk_2^2}{(d_1+d_2)^2} = 0 \end{aligned} \tag{8}$$

$$\begin{aligned} & Md_2^2 - \frac{M}{4} - \frac{d_1^3}{3} - d_2^2 d_1 - 2d_2^2 + \frac{d_1}{3} \\ & \quad + \frac{4}{3}d_2^3 + \frac{2}{3}d_2 - \frac{Mk_2^2}{(d_1+d_2)^2} = 0. \end{aligned} \tag{9}$$

Subtracting (9) from (8) results in

$$\begin{aligned} & (d_1 - d_2)[(M-2)(d_1+d_2) \\ & \quad + \frac{5}{3}(d_1^2 + d_1 d_2 + d_2^2 + \frac{1}{3} - d_1 d_2)] = 0. \end{aligned} \tag{10}$$

The solution of (10) is either $d_2 = d_1$, which results in the EPS mode, or $(M-2)(d_1+d_2) + \frac{5}{3}(d_1^2 + d_1 d_2 + d_2^2 + \frac{1}{3} - d_1 d_2) = 0$, which corresponds to the AEPS mode. Depending on the operating conditions, either EPS or AEPS provides the absolute minimums, which will be determined using the proposed hybrid modulation algorithm later. Focusing on the AEPS case, the corresponding equation can be rearranged and solved to derive the equation of d_2 in the form of $a \pm b$ as follows:

$$\begin{aligned} d_2 = \frac{1}{10}[& -2d_1 - 3(M-2) \\ & \pm \sqrt{9(M-2)^2 - 48(M-2)d_1 - 96d_1^2 - 20}] \end{aligned} \tag{11}$$

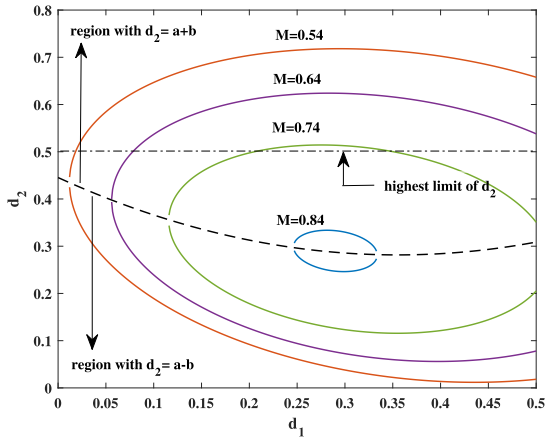

Fig. 7. i_{rms} minimization solutions for d_2 for various M.

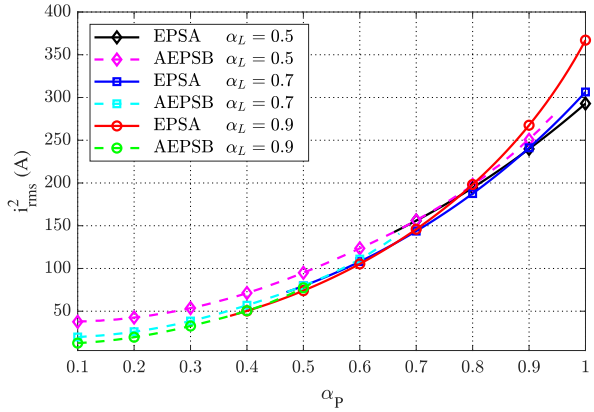

Fig. 8. Minimum EPS mode A and AEPS mode B tank RMS current square in valid ZVS operation range for different values of α_L ($V_{\text{bat}} = 48$ V and $V_i = 400$ V).

where $a = \frac{-2d_1 - 3(M-2)}{10}$ and $b = \frac{\sqrt{9(M-2)^2 - 48(M-2)d_1 - 96d_1^2 - 20}}{10}$. By analyzing the term b, it can be seen that, in order to obtain real values of d_2, the following condition must be satisfied:

$$(M - 3.1547)(M - 0.8453) \geq 0.$$

This suggests either $M \geq 3.1547$ or $M \leq 0.8453$ in order to have a real solution for b. However, since $(M < 1)$ for both charging or discharging cases, $M \geq 3.1547$ solution is invalid, and the condition for voltage gain becomes

$$M \leq 0.8453. \tag{12}$$

This sets the limit of M for AEPS operation as $M_{\text{lim}} = 0.84$. Furthermore, between the two possible solutions of d_2 from (11), the one with $d_2 = a + b$ provides values outside the valid range of 0–0.5, as shown in Fig. 7. Thus, the final solution for d_2 is obtained by selecting $d_2 = a - b$. Now, replacing this solution of d_2 in either (8) or (9) gives an irregular high-order polynomial equation for d_1 that is difficult to solve through conventional techniques. Hence, the method of nonlinear polynomial regression is used in Section II-H to estimate d_1.

G. Converter Parameter Design

The main power components of a DAB converter are transformer turns ratio (N), tank inductance (L), and blocking capacitor C. Using input parameters, such as P, V_i, and V_{bat}, the converter is designed as follows.

1) Transformer Turns Ratio: The transformer turns ratio N should match the voltage conversion ratio of the DAB to decrease circulating current and increase efficiency. In this article, the rated HV dc-link voltage is 400 V that can change between 380 and 420 V. The LV side connected to the battery has the rated voltage of 48 V changing in the range of 40–56 V in a full charge/discharge cycle. The turns ratio must be chosen in a way that for all the possible HV- and LV-side voltages, the voltage gain M is always less than 1:

$$M_{\text{max}} = \frac{NV_{\text{bat}}(\text{max})}{V_{in}(\text{min})} = \frac{N * 56}{380} < 1 => N < 6.78. \tag{13}$$

This requirement is implemented by an integer number of turns $N_{\text{bat}} = 3$ and $N_i = 20$, resulting in $N = 6.67$.

2) Inductance Value Selection: The voltages of $V_i = 400$ V and $V_{\text{bat}} = 48$ V are considered as rated voltages for inductance value selection. In the selection of α_L, there is a tradeoff between the light-load and full-load RMS currents. In fact, increasing α_L improves the light-load RMS current, while it deteriorates the full-load RMS current. Similarly, reducing α_L slightly improves the full-load RMS current, while it deteriorates the light-load RMS current. This trend is shown in Fig. 8, where the current square value is only depicted in the region that satisfies ZVS conditions, and the graphs are drawn for the nominal voltages of $V_i = 400$ V and $V_{\text{bat}} = 48$ V. Similar RMS current trends also exist for different voltage combinations. As such, it can be seen that $\alpha_L = 0.7$ provides a balanced RMS current and, thus, flat efficiency curve throughout the entire operating range. Choosing an inductance value of $L = 44.5$ μH results in the actual percentage inductance of $\alpha_L = 0.7023$. As the total transformer leakage inductance is equal to 15 μH, a 29.5-μH external inductor is added to the HV side.

3) Series Capacitor Selection: The series capacitor required for the AEPS in Fig. 2 should be designed based on the converter operating points at extreme conditions. The capacitance is selected based on the maximum voltage ripple in the cap, V_b. The highest ripple occurs when the inductor current is at the maximum value. According to Fig. 23, the maximum inductor RMS current occurs at the maximum power, and the modulation in that region is EPS mode A. Accordingly, the equation of voltage ripple for EPS mode A is calculated as follows:

$$\begin{aligned}\Delta V_{C_{\text{max}}} = \frac{1}{C} * \Bigg[& \frac{I_1}{2} * \frac{I_1}{I_1 + I_3} * \frac{(\theta - d_1'\pi)T_s}{2\pi} \\ & + \frac{I_1 + I_2}{2} * \frac{((1 - d_1')\pi - \theta)T_s}{2\pi} \\ & + \frac{I_2 + I_3}{2} * \frac{(d_1' + d_2')T_s}{2} \\ & + \frac{I_3}{2} * \frac{I_3}{I_1 + I_3} * \frac{(\theta - d_2'\pi)T_s}{2\pi} \Bigg]\end{aligned} \tag{14}$$

TABLE III
DUTY CYCLE EQUATIONS FOR MINIMUM RMS CURRENT OPERATION WITHIN ZVS RANGE

Mode	Modulation	Estimated Duty Cycles
Mode A	EPS	$d_1 = d_2 = 1.35\alpha_p^4 + 1.45\alpha_p^3 M - 4.1\alpha_p^3 + 10.55\alpha_p^2 M^2 - 21.86\alpha_p^2 M + 13.43\alpha_p^2 - 18\alpha_p M^3 + 33.65\alpha_p M^2 - 15.5\alpha_p M - 0.96\alpha_p + 15.93M^4 - 41.03M^3 + 39.34M^2 - 17.08M + 3.53$
Mode B	AEPS	$d_1 = -35.2\alpha_P^4 + 95.47\alpha_P^3 M - 36.08\alpha_P^3 - 140.56\alpha_P^2 M^2 + 117.67\alpha_P^2 M - 22.61\alpha_P^2 - 2.01\alpha_P M^3 + 4767.1\alpha_P M^2 - 3732.7\alpha_P M + 968.08\alpha_P + 1907.2M^4 - 5487.6M^3 + 5864.5M^2 - 2756.8M + 480.83$
		$d_2 = 74.34\alpha_P^4 + 48.53\alpha_P^3 M - 101.36\alpha_P^3 + 558.76\alpha_P^2 M^2 - 859.45\alpha_P^2 M + 353.15\alpha_P^2 + 1998.5\alpha_P M^3 - 4886.3\alpha_P M^2 + 3963.5\alpha_P M - 1070.7\alpha_P + 5057.6M^4 - 15860M^3 + 18687M^2 - 9800.7M + 1930.3$
Mode D	EPS	$d_1 = d_2 = 1.6115\alpha_p^3 + 7.43\alpha_p^2 M - 6.43\alpha_p^2 + 14.03\alpha_p M^2 - 25.46\alpha_p M + 11.56\alpha_p + 7.58M^3 - 20.27M^2 + 18.86M - 5.67$
	AEPS	$d_1 = 23.48\alpha_P^4 - 38.63\alpha_P^3 M + 12.35\alpha_P^3 + 135.74\alpha_P^2 M^2 - 179.41\alpha_P^2 M + 62.62\alpha_P^2 + 1314.4\alpha_P M^3 - 3146.8\alpha_P M^2 + 2503.7\alpha_P M - 663\alpha_P - 9091.3M^4 + 28106M^3 - 32567M^2 + 16765M - 3234.3$
		$d_2 = -1.99\alpha_P^4 + 4.39\alpha_P^3 M - 2.49\alpha_P^3 + 152.05\alpha_P^2 M^2 - 239.06\alpha_P^2 M + 94.06\alpha_P^2 + 392.2\alpha_P M^3 - 982.8\alpha_P M^2 + 816.7\alpha_P M - 224.78\alpha_P - 4886M^4 + 15159M^3 - 17627M^2 + 9105.7M - 1763.1$

where I_1, I_2, and I_3 are the switching instant currents, as shown in Fig. 4, with the equations provided in Table II. To keep the capacitor voltage ripple below $0.1V_i$, using the above equation, the maximum voltage ripple of 41.9 V is achieved using a 4.5-μF capacitor at the worst-case scenario that is $V_{\text{bat}} = 40\,\text{V}$, $V_i = 420\,\text{V}$, and $P = 5\,\text{kW}$. The current rating of the capacitor is selected according to the maximum inductor RMS current. The maximum current is 21.3 A at $V_{\text{bat}} = 40\,\text{V}$, $V_i = 420\,\text{V}$, and $P = 5\,\text{kW}$.

The voltage rating of the capacitor should tolerate the maximum dc voltage during the extreme asymmetric modulation, where $d_1 - d_2 = 0.5 - 0.085 = 0.415$ at $V_{\text{bat}} = 40\,\text{V}$, $V_i = 420\,\text{V}$, and $P = 500\,\text{W}$, which results in the maximum dc voltage of 174 V across the blocking capacitor. Based on the above criteria, considering an extra safety margin for the transient operation, three parallel capacitors (R75IN41504040J) are used to achieve the maximum current of 24 A and a voltage rating of 250 V.

H. Estimating d_1 in AEPS Modes

The polynomial regression for d_1 is done over a wide variation range of M and k_2, as defined in (7), for superior accuracy. Here, k_2 is a linear function of α_P and α_L, among which the former is an operational parameter and the latter is a design parameter selected at the very beginning without a varying effect on the converter operations in the later stages. Thus, the optimum values of d_1 and d_2 that provide minimum RMS current satisfying ZVS conditions for a wide range of α_P and M are found from simulation, which are then used as references to obtain the estimated duty cycle equations using polynomial regression. This method can be carried out for both the EPS and AEPS modes. Using nonlinear polynomial regression, equations of d_1 and d_2 as functions of α_P and M for all the operating modes are summarized in Table III. The highest limit of M that AEPS is proposed to be used is 0.84 because according to (12), $0.8453 < M < 1$ is the suggested range for EPS. For this reason, in Fig. 9(b), it is shown that for the entire power range and for $M = 0.85$, EPS is the optimal solution. For $M < 0.84$, the hybrid modulation is a combination of AEPS and EPS modulations, as shown in Fig. 9(a). Fig. 9 validates the accuracy of estimated equations for d_1 and d_2 presented in Table III compared to the optimum values from simulation. The results are in close match with maximum error $< 1\%$.

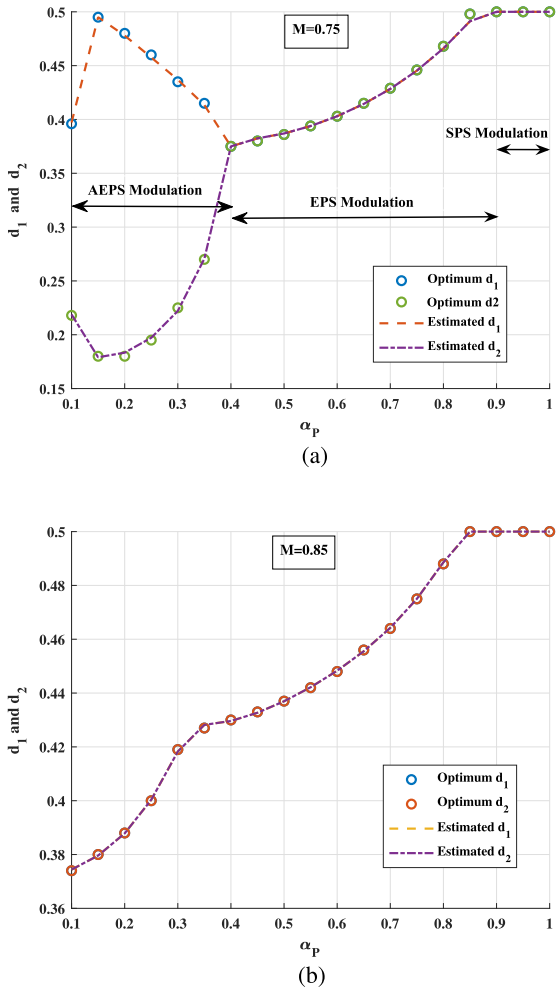

Fig. 9. Accuracy of estimated equations of d_1 and d_2 based on Table III and the actual optimum values from simulations at (a) $M = 0.75$ (b) $M = 0.85$. (a) Optimum is achieved through the hybrid modulation of AEPS and EPS modes. (b) Optimum is achieved through EPS and SPS modulation modes.

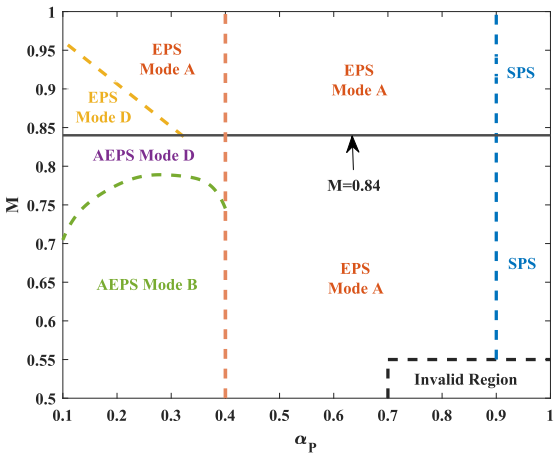

Fig. 10. Optimum operating modes at different values of α_P and M satisfying ZVS conditions.

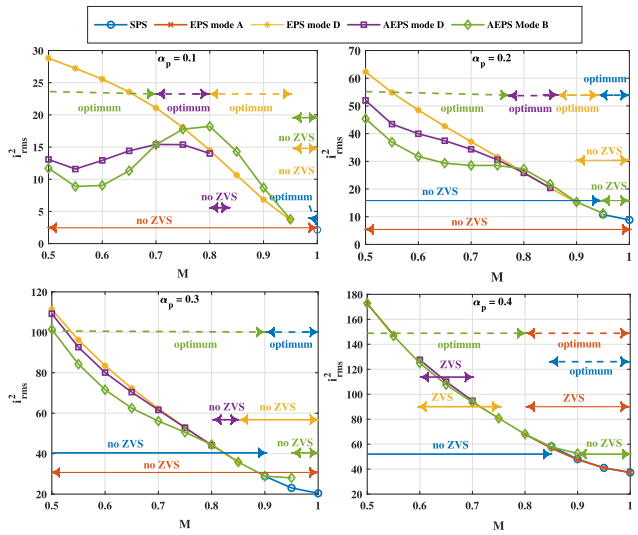

Fig. 11. i^2_{rms} comparison of different modes at different operating conditions.

I. Hybrid Modulation Algorithm

From Fig. 10, it can be observed that for $\alpha_p \leq 0.4$ and $M \leq 0.84$, the AEPS modulations offer the optimum operation with the region being shared by both AEPS Modes B and D. At $\alpha_p \geq 0.9$, the SPS modulation offers the best performance, while the region between α_p of 0.4 and 0.9 is dominated by EPS Mode A in performance. Since AEPS modulation appears to provide higher benefits for $\alpha_P \leq 0.4$, the RMS values of i are observed for the different EPS and AEPS modes in this region, as depicted in Fig. 11. It is seen that the AEPS modulation generates much lower rms values for $M < M_{\text{lim}}$. However, this benefit gradually reduces as power increases. At $\alpha_P = 0.4$, the EPS modes are very close in performance with the AEPS ones, and eventually after this point, EPS will overtake AEPS modulation.

According to these results, the various operating modes can be combined into a hybrid modulation scheme for superior performance and efficiency for all operating conditions. $\alpha_p = 0.4$ can be set as the upper limit of the low-power region, α_{p_L}. In this region, AEPS modulation modes provide superior performance as long as $M \leq M_{\text{lim}}$, or else EPS Modes A and D take over when $M > M_{\text{lim}}$. The lower limit of the high-power region, α_{p_H}, can be given as $\alpha_p = 0.9$, where the conventional SPS modulation provides the best performance. Between α_{p_L} and α_{p_H}, EPS Mode A trumps the other modes. The details of the control system and how this optimized modulation scheme is implemented are provided in Section III.

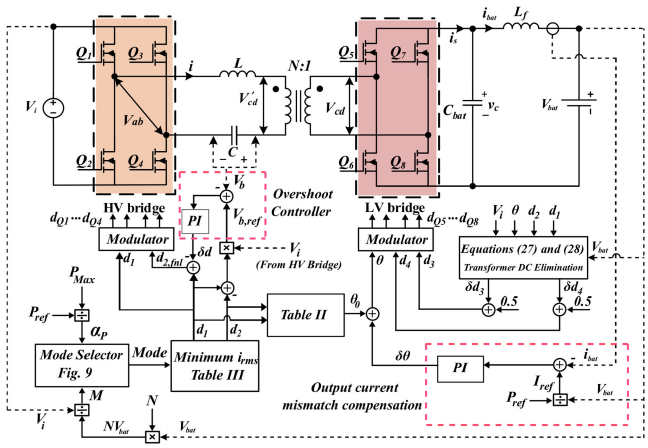

Fig. 12. General block diagram of the closed-loop DAB converter with hybrid modulation.

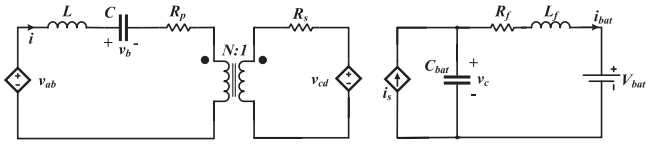

Fig. 13. Equivalent circuit model of the DAB system.

III. Modeling and Control System Description

Fig. 12 shows the block diagram of the proposed hybrid modulation with a closed-loop control system. In this system, P_{ref} is provided externally, which is used to calculate α_P and i_{ref}. The parameters α_P and M are used to determine the optimum mode using Fig. 10. Based on the selected mode, the duty cycles are calculated using the equations from Table III, and the feedforward θ_0 is calculated using Table II. In order to regulate the battery current at i_{ref} and improve the transient and steady-state performance of the system, control schemes are proposed, designed, and shown in Fig. 12, which will be discussed in the subsequent sections.

A. Large-Signal Model Derivation

The equivalent circuit model of the DAB converter in Fig. 12 is illustrated in Fig. 13, where R_p, R_s, and R_f are stray resistances. Thus, the differential equations of the large-signal model can be

derived as

$$\begin{cases} C_{\text{bat}}\frac{dv_c}{dt} & = i_s - i_{\text{bat}} \\ L_f\frac{di_{\text{bat}}}{dt} & = v_c - i_{\text{bat}}R_f - V_{\text{bat}} \\ L\frac{di}{dt} & = v_{ab} - v_b - v'_{cd} - R_t i \\ C\frac{dv_b}{dt} & = i \end{cases} \tag{15}$$

where $R_t = R_p + N^2 R_s$. The state-space equations of the system are derived based on the method used in [36], where the signals are approximated by dc fundamental sine and cosine terms. Using this method, each variable, shown by $x(t)$, and its time derivative can be written as

$$x(t) = \overline{x} + x^{\text{sin}}\text{sin}(\omega t) + x^{\text{cos}}\text{cos}(\omega t) \tag{16}$$

$$\begin{aligned} \frac{dx}{dt} &= \frac{d\overline{x}}{dt} + \left(\frac{dx^{\text{sin}}}{dt} - \omega x^{\text{cos}}\right)\text{sin}(\omega t) \\ &\quad + \left(\frac{dx^{\text{cos}}}{dt} + \omega x^{\text{sin}}\right)\text{cos}(\omega t) \end{aligned} \tag{17}$$

where ω is the switching frequency in rad/s, and $\overline{x}$, x^{sin}, and x^{cos} are the slow varying dc and fundamental amplitudes, which are considered as the new state variables [36].

To derive state-space equations in terms of new state variables and duty cycles, the Fourier series approximation of the tank input and output voltages can be derived using Fig. 3(b) as

$$v_{ab} = V_i(d_1 - d_2) + \frac{2V_i}{\pi}(\text{sin}\pi d_1 + \text{sin}\pi d_2)\text{sin}(\omega t) \tag{18}$$

$$v_{cd} = \frac{4\overline{v}_c}{\pi}\text{cos}\theta\text{sin}(\omega t) + \frac{4\overline{v}_c}{\pi}\text{sin}\theta\text{cos}(\omega t). \tag{19}$$

Since the LV-side capacitor voltage v_c and inductor current i_{bat} are primarily dc variables, their ac components can be neglected. Thus, the time derivatives of the rest of the variables can be achieved by applying (16) and (17) to all variables and the substitution of (18) and (19) into (15). Then, the steady-state solutions can be found by setting the time derivatives to zero, which are not included here for the sake of brevity.

B. Small-Signal Model Derivation

In order to find the linearized state-space model, the state variable vector x is defined as

$$x = \begin{bmatrix} i^{\text{sin}} & i^{\text{cos}} & v_b^{\text{sin}} & v_b^{\text{cos}} & \overline{i} & \overline{v}_b & \overline{v}_c & \overline{i}_{\text{bat}} \end{bmatrix}^T. \tag{20}$$

Assuming $\widetilde{x} = x - \overline{X}_s$ as a small-signal variable, where $\overline{X}_s$ is the equilibrium or the steady-state solution, and applying the small-signal approximation method described in [36], the small-signal state-space matrices are derived as

$$\begin{cases} \frac{d\widetilde{x}}{dt} & = A\widetilde{x} + B_1\tilde{\theta} + B_2\tilde{d}_1 + B_3\tilde{d}_2 \\ \widetilde{y} & = C\widetilde{x} \end{cases} \tag{21}$$

where

$$A = \begin{bmatrix} -\frac{R_t}{L} & \omega & -\frac{1}{L} & 0 & 0 & 0 & \frac{4N\text{cos}\theta_s}{\pi L} & 0 \\ -\omega & -\frac{R_t}{L} & 0 & -\frac{1}{L} & 0 & 0 & \frac{4N\text{sin}\theta_s}{\pi L} & 0 \\ \frac{1}{C} & 0 & 0 & \omega & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C} & -\omega & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_t}{L} & -\frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C} & 0 & 0 & 0 \\ a_{71} & a_{72} & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{\text{bat}}} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_f} & -\frac{R_f}{L_f} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} b_{11} & b_{12} & 0 & 0 & 0 & 0 & b_{17} & 0 \end{bmatrix}^T$$

$$B_2 = \begin{bmatrix} -\frac{2V_i\text{cos}(\pi D_1)}{L} & 0 & 0 & 0 & -\frac{V_i}{L} & 0 & 0 & 0 \end{bmatrix}^T$$

$$B_3 = \begin{bmatrix} \frac{-2V_i\text{cos}(\pi D_2)}{L} & 0 & 0 & 0 & \frac{V_i}{L} & 0 & 0 & 0 \end{bmatrix}^T$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$a_{71} = -\frac{2N\text{cos}\theta_s}{\pi C_{\text{bat}}}, a_{72} = -\frac{2N\text{sin}\theta_s}{\pi C_{\text{bat}}}, b_{11} = -\frac{4N\overline{V_c}\text{sin}\theta_s}{\pi L} \tag{22}$$

$$b_{12} = \frac{4N\overline{V_c}\text{cos}\theta_s}{\pi L}, b_{17} = \frac{2\,N}{\pi C_{\text{bat}}}(I_s^{\text{sin}}\text{sin}\theta_s - I_s^{\text{cos}}\text{cos}\theta_s). \tag{23}$$

In these equations, $\tilde{\theta}$ and $\tilde{i}_{\text{bat}}$ are the input and output of the system, respectively. In order to design $\tilde{i}_{\text{bat}}$ controller, $\tilde{d}_1$ and $\tilde{d}_2$ are considered as disturbances around the operating point. The next section demonstrates the control design method and bode diagrams of the system.

C. Battery Current Control Design

To regulate the output dc current at i_{ref}, a proportional–integral (PI) controller is used to generate a small perturbation that is added to the feedforward θ_0, as shown in Fig. 12. The state-space presentation of the PI controller is

$$\begin{cases} \dot{\widetilde{x}}_c & = e = i_{\text{ref}} - \tilde{i}_{\text{bat}} \\ \tilde{\theta} & = k_i\widetilde{x}_c + k_p e. \end{cases} \tag{24}$$

As a result, the closed-loop augmented state equations can be written as

$$\begin{bmatrix} \dot{\widetilde{x}}_c \\ \dot{\widetilde{x}} \end{bmatrix} = \begin{bmatrix} 0 & -C \\ k_i B_1 & A - k_p B_1 C \end{bmatrix}\begin{bmatrix} \widetilde{x}_c \\ \widetilde{x} \end{bmatrix} + \begin{bmatrix} 1 \\ k_p B_1 \end{bmatrix} i_{\text{ref}}$$

where $\tilde{i}_{\text{bat}}$ is the system output. In order to obtain a range of acceptable gain values (k_p and k_i), the Routh's stability criterion is used for a range of operating conditions α_P and α_M, using the system parameters shown in Table IV. Fig. 14 shows the stability region for two cases: a) α_M is constant and α_P is variable and b) α_P is constant and α_M is variable. For both the cases, the area under the curves is the stable region for the corresponding

TABLE IV
EXPERIMENTAL SETUP PARAMETERS

Parameter	Value
DC-link voltage range V_i	380–420V
DC-link rated voltage V_{iM}	400V
Battery voltage range V_{bat}	40–56V
Battery rated voltage $V_{\text{bat }M}$	48V
Voltage gain (M) range	0.628–0.972
Tank inductance L	44.5μH
Block capacitor C	4.5μF
LV-side filter capacitor C_{bat}	70μF
Switching frequency f	50kHz
Turns ratio N	6.6
Base (nominal) converter power P_{base}	5kW
Transformer core	EE65/32/27 3c94
Blocking Capacitor	3×R75IN41504040J
MCU	TMS320F28335
HV bridge switches	2×GS66508T $C_{\text{oss}} = 65$ pF $R_{\text{ds}}\,(\text{on}) = 50$ mΩ
LV bridge switches	4×GS1008T $C_{\text{oss}} = 250$ pF $R_{\text{ds}}\,(\text{on}) = 7$ mΩ

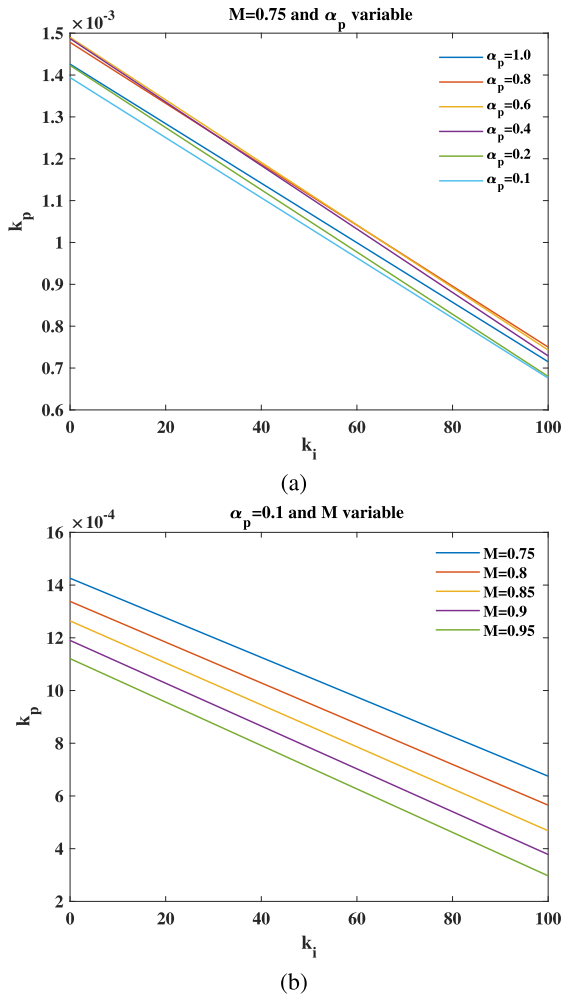

Fig. 14. (a) and (b) Stability plots for the closed-loop system for i_{bat} at different values of k_p and k_i.

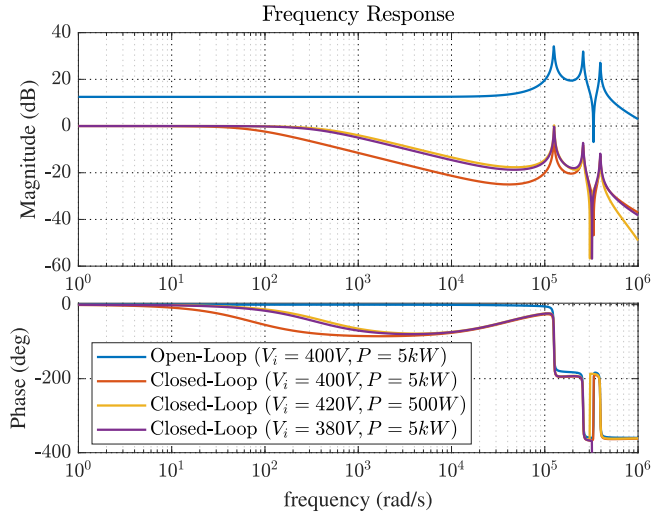

Fig. 15. Frequency response of the i_{bat} control system in different operating modes.

operating point. According to Fig. 14, the worst-case scenario occurs at the minimum power ($\alpha_P = 0.1$) and the maximum voltage gain ($M = 0.95$) as they provide the narrowest range of acceptable gain values. Therefore, the PI gains are designed considering this operating point and the required gain margin and settling time of the system response. The bode diagrams of the system in the nominal and worst-case operating points are illustrated in Fig. 15, where a minimum gain margin of 8 dB is shown for the closed-loop system. The dynamic response of the closed-loop system is demonstrated in Section IV.

D. Tank Current Overshoot Control During Mode Transitions

During AEPS operation, the entire dc component of the HV bridge voltage, v_{ab}, appears across dc-blocking capacitor C, as explained in Section II, which is usually zero or nearly zero during EPS operation. In a system with V_i of 400 V, the value of this dc component can range from 5 to 200 V. As a result, during the transition from EPS to AEPS, where d_1 and d_2 become unequal, or *vice versa*, C might need to be charged from 0 V to about 200 V or discharged by the same amount instantaneously to prevent transformer saturation. This can create high current overshoot, which will result in excessive losses or even damage to components.

To make this transient smooth, a PI controller can be used that controls the rate at which $\delta d = d_1 - d_2$ changes, as shown in Fig. 12 as the overshoot controller. The controller takes the difference between the reference and actual block capacitor voltage V_b as the input, where reference V_b is calculated using d_1 and d_2 obtained from Table III. Next, δd is generated as the output, which is then subtracted from d_1 to produce the final d_2 or $d_{2,\text{fnl}}$, which is ultimately provided to the DAB converter.

Referring to Section III-B, the state-space equations corresponding to this system are rewritten as

$$\begin{cases} \frac{d\bar{i}}{dt} & = \frac{-V_i(\delta d) - \bar{v}_b - R_t\bar{i}}{L} \\ \frac{d\bar{v}_b}{dt} & = \frac{\bar{i}}{C}. \end{cases} \tag{25}$$

TABLE V
PROPOSED HYBRID MODULATION COMPARED WITH OTHER EXISTING APPROACHES

	Modulation	Objective of optimization	ZVS range	RMS Current	Number of variables	M range	Power	Input voltage	Output voltage	f_s	Efficiency	Additional hardware
[31]	APWM + SPS	Voltage match	Narrow	Medium	2	0.5–1	500	300V	100–200V	50kHz	91–97.9%	One capacitor
[30]	APWM	RMS Current	Narrow	High	2	0.56–0.74	500W	380V	42–56V	50kHz	86–95.5%	None
[32]	APWM	RMS current	Narrow	High	3	0.5	625W	200	50V	50kHz	76–95%	Four capacitors
[29]	TPS	RMS current + ZVS	Medium	Medium	3	0.5–1	1000W	200V	200–400V	50kHz	76–95%	None
[23]	TPS	RMS current	Narrow	Low	3	0.8–1.15	1000W	200V	230–160V	20kHz	95.8–98.2%	None
This work	AEPS + TPS	RMS current + ZVS	Wide	Low	3	0.5–1	5000W	380-420V	40–56V	50kHz	93.7–97.7%	One capacitor

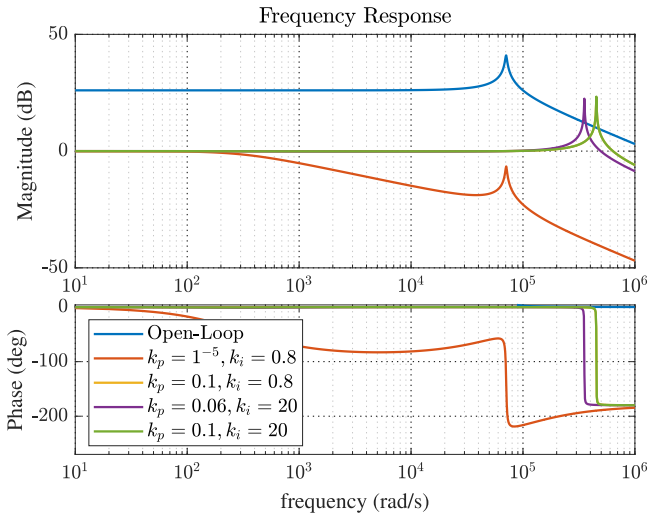

Fig. 16. Frequency response of the overshoot control system with $R_t = 100\ \text{m}\Omega$, and different PI parameters.

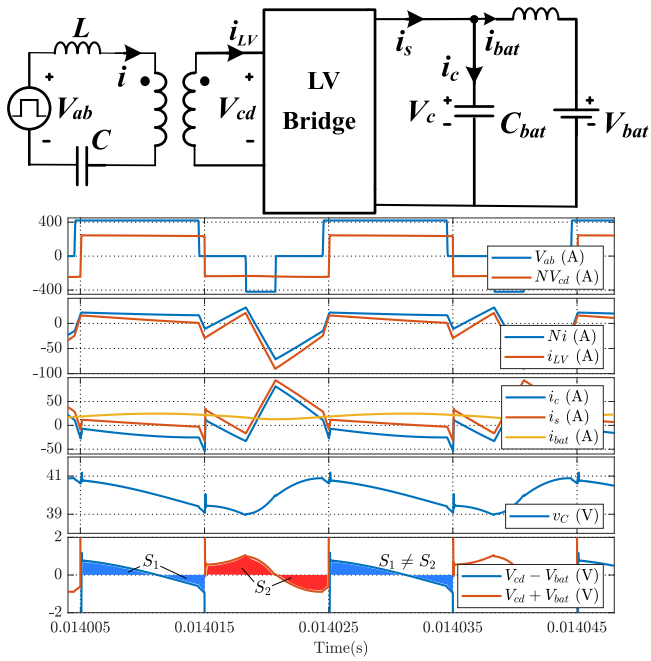

Fig. 17. General diagram of the circuit signals involving with the dc voltage generation in LV tank due to AEPS operation.

Similar to that in Section III-C, the system and PI controller state equations are augmented to obtain the closed-loop matrices and stability criteria. Since the state variables in (25) are decoupled from the other variables of the DAB system, the operating point does not affect the stability of the overshoot controller. Nevertheless, it can be shown that R_t and L have a significant influence on the stability of this system, and the worst case corresponds to the lowest value of R_t and the highest value of L. Thus, the PI controller parameters are chosen regarding the worst-case scenario. The bode diagrams of the system using different PI parameters within the stability range are shown in Fig. 16. It can be observed that except for low values of k_p, all the other scenarios demonstrate nearly zero phase margins and high gain margins. Thus, only small values of k_p can be selected. The exact k_p and k_i values are chosen considering the system step response. The effectiveness of the proposed controller during mode transitions is demonstrated in the experimental results in Section IV.

E. Elimination of the Reflected DC Current on the LV Side

In DAB converters, similar to other isolated topologies, non-ideal phenomena, such as unequal turn ON/OFF times or switch mismatches, can produce finite dc voltage across the transformer. The AEPS modulation itself may also contribute to a small dc bias across the transformer in the LV-side tank. The general diagram explaining this phenomenon is illustrated in Fig. 17, including the simulation waveforms for AEPS mode B modulation with $P = 750\,\text{W}$, $V_{\text{bat}} = 40\,\text{V}$, and $V_i = 420\,\text{V}$. It

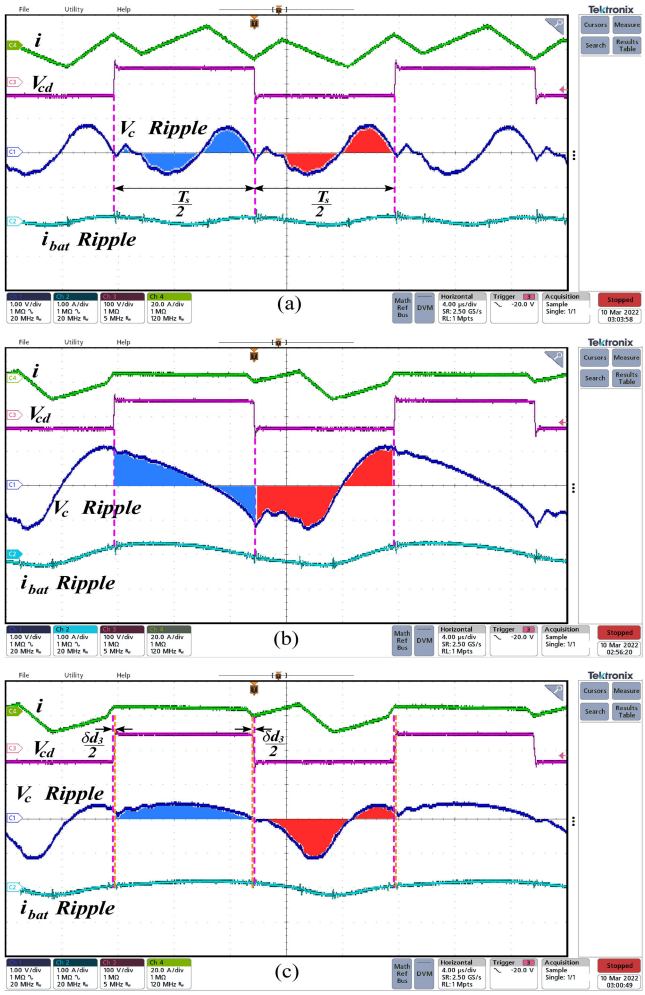

Fig. 18. C_{bat} voltage and battery current at $P = 750\,\text{W}$, $V_{\text{bat}} = 40\,\text{V}$, and $V_i = 420\,\text{V}$ for (a) EPS mode D, (b) AEPS mode B without dc voltage compensation, and (c) AEPS mode B with dc voltage compensation.

can be seen that v_{ab} is asymmetrical, while v_{cd} is symmetrical at 50% duty cycles. The difference of these voltages forms the current, i, in the HV side, which does not have any dc. However, Ni and i_{LV} may not be identical due to a small dc current on the LV side. This dc current is generated as v_{cd} average is not zero because the ripple of v_{cd} during the half period and second half period are not exactly identical. This is shown in the last graph of Fig. 17 or experimental results in Fig. 18, labeled and colored in red and blue by unequal areas S_1 and S_2. The root cause of the unequal areas is the asymmetrical ripple of v_c that is due to the asymmetrical current ripple, i_c, going through C_{bat}, which was because of the asymmetrical current waveform Ni. On the contrary, in EPS modulation, as shown in Fig. 18(a), C_{bat} has a voltage ripple with double switching frequency, which generates an equal amount of dc voltage in the positive and negative half-cycles of v_{cd}.

The generated dc bias creates a dc current limited by the stray resistance of the transformer windings and switching components. The dc current and ripples can increase to an unacceptable level causing extra losses and heating up of the transformer windings [5]. The ripple of v_c in an APES operation in the experiment is shown in Fig. 18(b), with the switching frequency, which can reflect unequal voltage levels on positive and negative half-cycles of v_{cd}. This figure also shows the increased ripple of i_{bat} due to dc current flowing in the transformer.

Although placing a capacitor on the LV side is the most straightforward solution, high current on the LV side makes the design inefficient and bulky. In this article, a feedforward approach is proposed to eliminate the unwanted dc voltage, as shown in Fig. 12 as the Transformer DC Elimination block. This method applies a small modification in the waveform of v_{cd} to create an opposing dc voltage across the transformer. Referring to Fig. 3, the half-cycle duty values of v'_{cd} or v_{cd} are $d_3 = d_4 = 0.5$. A small variation to one of these duty cycle values can generate an additional dc voltage to reverse the effects of the parasitic dc voltage.

The necessary duty cycle adjustment can be calculated through the mathematical analysis of the transformer and input capacitor current and voltage waveforms. Here, the equations of transformer current i are used to obtain equations of i_s on the dc side of the LV bridge using

$$i_s = \begin{cases} -Ni, & 0 \le wt < \theta \\ Ni, & \theta \le wt < \pi + \theta \\ -Ni, & \pi + \theta \le wt \le 2\pi \end{cases}. \tag{26}$$

The current i_c through C_{bat} is $i_s - I_{\text{bat}}$ and the voltage v_c is calculated from i_c, as shown in Fig. 17. This v_c then creates the square voltage v'_{cd}. Now, if the area under the two half cycles in a time period is calculated, the difference in their magnitudes will give the actual value of the generated dc voltage δV. Therefore, δV for AEPS Modes B and D can derived as (27)–(28) shown at bottom of the next page.

It can be shown that the polarity of δV is positive in the entire operating region. Therefore, the duty cycles of v_{cd} should be adjusted appropriately to negate δV. Thus, the compensation equation can be written as follows:

$$V_{\text{bat}}(d_3 - d_4) = -\delta V.$$

Keeping the value of d_4 at 0.5, the final equation of d_3 becomes

$$d_3 = 0.5 - \frac{\delta V}{V_{\text{bat}}} \tag{29}$$

which results in $\delta d_3 = \frac{\delta V}{V_{\text{bat}}}$ and $\delta d_4 = 0$.

The proposed feedforward compensation will have errors in practice depending on the system parameter values. However, the major part of this dc component is eliminated with the open-loop compensation, and the important point is that component uncertainties do not change this dc component significantly and the remaining dc due to the errors will be limited because of the parasitic resistors in the circuit, and it does not move the transformer toward saturation. As demonstrated in the experimental results of Fig. 18(c), the duty cycle adjustment of v_{cd} eliminates the unwanted dc component of the LV current significantly and lowers i_{bat} ripples in comparison with Fig. 18(b).

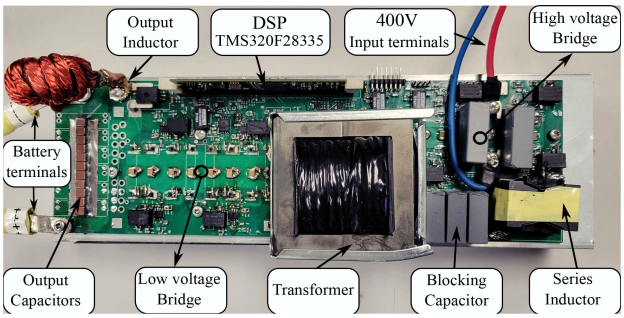

Fig. 19. 5-kW experimental setup.

IV. Experimental Results

To validate the effectiveness of the proposed asymmetric modulation and hybrid control, the DAB circuit is experimentally tested in a setup shown in Fig. 19. In this setup, the parameters are chosen as shown in Table IV. For the HV full bridge, two parallel GS66508T switches are utilized to increase current capability. Likewise, for the LV side, four parallel GS1008T switches are employed to achieve higher current rating and distribute the conduction loss. The transformer uses EE65/32/27 3c94 core material. The litz wire used for the inductor and transformer HV-side winding includes 825 strands of AWG40 for operating at 50 kHz. Each turn of the LV-side winding is designed to have three parallel litz wires with 825 strands of AWG40 to fulfill enough current capability. The proposed modulation and control method is implemented using TMS320F28335 digital signal controller in two nested interrupt service routines (ISRs). The high-priority ISR takes care of signal sampling, protection, and the PI controllers. Calculations of d_1, d_2, θ_0, δV_B, and δV_D, as shown in Fig. 12, only require basic math operations and are executed in the low-priority ISR. The performance analysis of the converter is presented in the following sections.

A. Converter Efficiency and ZVS Realization

In order to assure ZVS, in practice, a minimal inductive current is required to discharge the GaN output capacitance. This minimal current is considered in the practical results and the Appendix. Efficiency is obtained using Tektronix "PA 4000" power analyzer, and the LV-side current measurement is done using LEM "IT 200-S" high-accurate current transducer According to the parameters in Table IV, the low-power region can be defined as lower than 2 kW, where the performance improvement by the AEPS modulation is more significant, as discussed in Section II-I. Fig. 20 shows operating waveforms of five modulation candidates. In this figure, the input voltage is $V_i = 420\,\text{V}$ and the battery voltage is $V_{\text{bat}} = 40$ resulting in $M = 0.628$, and the

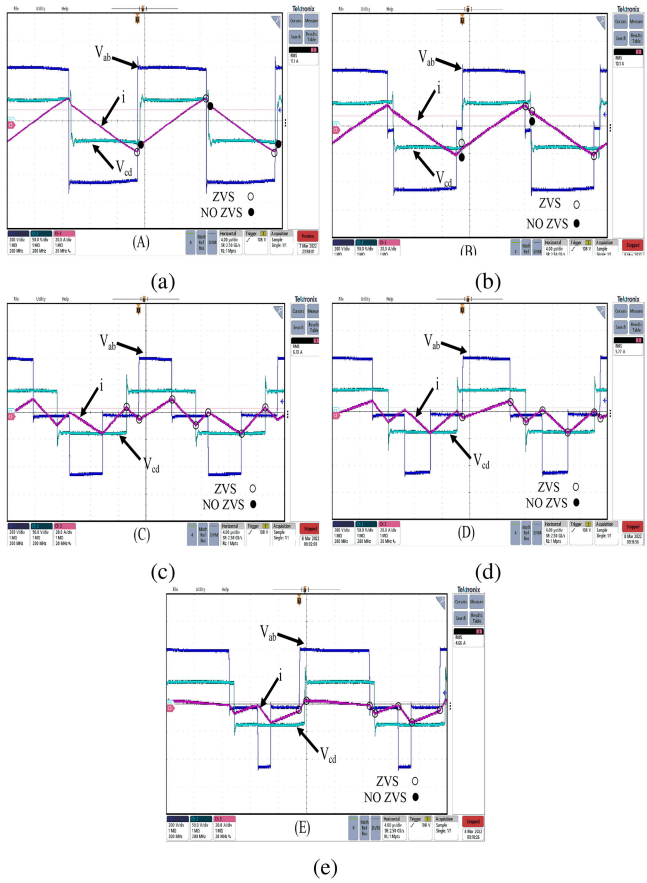

Fig. 20. Experimental waveforms for $M = 0.628$ and $\alpha_P = 0.2$. (a) SPS. (b) EPS Mode A. (c) EPS Mode D. (d) Asymmetric Mode D. (e) Asymmetric Mode B.

power is set at 1 kW that is $\alpha_p = 0.2$. It can be observed that for EPS modulations, the lowest $i_{\text{rms}} = 6.1\,\text{A}$ is achieved in Mode D, while AEPS Mode B achieves $i_{\text{rms}} = 4.65\,\text{A}$, which is 41.5% improvement. According to Fig. 20, for EPS A and SPS, V_{cd} side has hard switching and V_{ab} side has ZVS, but for EPSD, AEPS mode D, and AEPS mode B, all the instances are ZVS. Fig. 21 is presented to show efficiency curves in the low-power $\alpha_p <= 0.4$ region for $M = 0.628$. The asymmetric efficiency curve is 1.5–2.5% higher than the closest symmetric mode D efficiency for $0.1 < \alpha_p < 0.3$. In Fig. 22, efficiency curves for hybrid and SPS modulations are illustrated.

The proposed hybrid modulation generates the optimum modulation depending on the operating point, and the SPS modulation becomes the optimum modulation option for M close to 1 due to the low RMS current. In addition, SPS is the optimum choice for the power range close to the full power due to the highest power transfer capability with the lowest RMS currents,

$$\delta V_B = \frac{-NV_i(-12\theta^2 d_1 + 12\theta^2 d_2 + 12\pi\theta d_1 + 12\pi\theta d_2 - 4\pi^2 d_1^3 + 4\pi^2 d_2^3 + \pi^2 d_1 - \pi^2 d_2) + 12\pi L\omega I_{\text{bat}}}{24LC_{\text{bat}}\omega^2} \tag{27}$$

$$\delta V_D = \frac{-NV_i(-12\theta^2 d_1 + 12\theta^2 d_2 + 12\pi\theta d_1 + 12\pi\theta d_2 - 4\pi^2 d_1^3 + 4\pi^2 d_2^3 + \pi^2 d_1 - \pi^2 d_2) + 12\pi L\omega I_{\text{bat}}}{24LC_{\text{bat}}\omega^2} \tag{28}$$

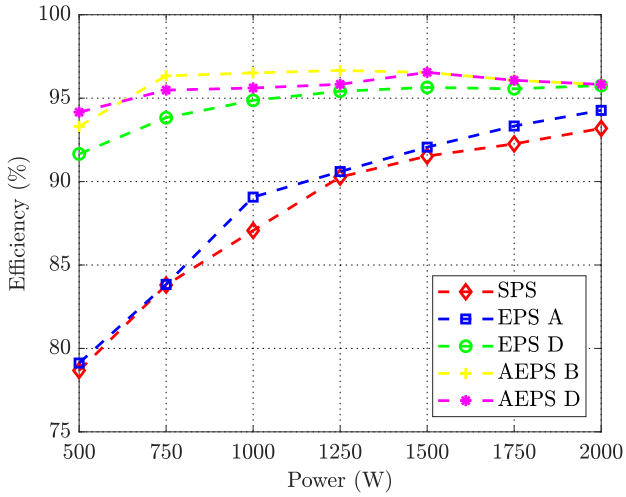

Fig. 21. Efficiency curves at $\alpha_P \leqslant 0.4$ of different modes.

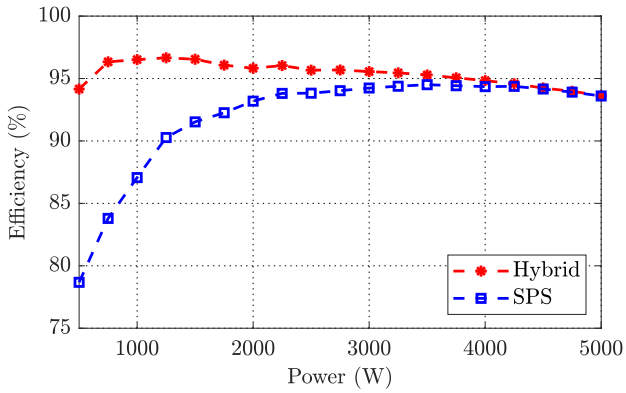

Fig. 22. Overall efficiency of hybrid modulation versus SPS modulation for the entire power range.

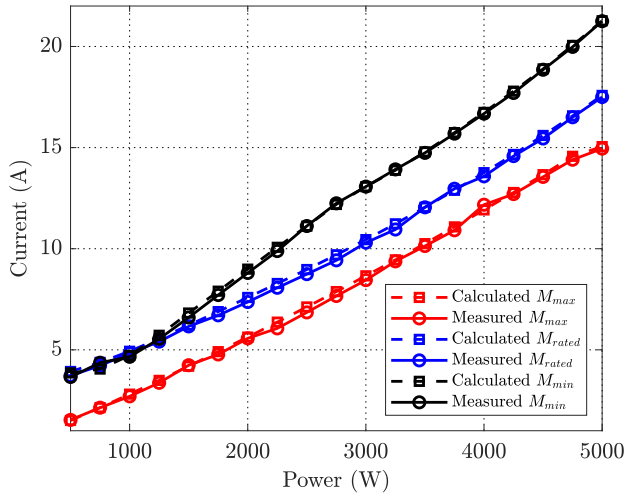

Fig. 23. Calculated and measured tank RMS current at $M_{\text{max}} = 0.972$, $M_{\text{rated}} = 0.792$, and $M_{\text{min}} = 0.628$.

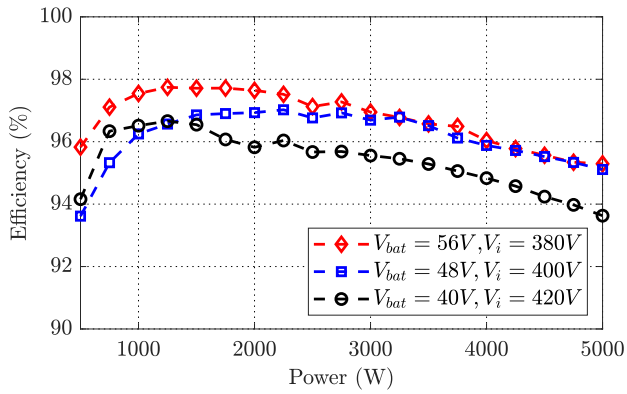

Fig. 24. Hybrid approach measured efficiency at $M_{\text{max}} = 0.972$ ($V_i = 380$ V and $V_{\text{bat}} = 56$ V), $M_{\text{rated}} = 0.792$ ($V_i = 400$ V and $V_{\text{bat}} = 48$ V), and $M_{\text{min}} = 0.628$ ($V_i = 420$ V and $V_{\text{bat}} = 40$ V).

as shown in Fig. 22. It is worth mentioning that voltage gain M and inductance percentage (α_L) determine the power level (α_p), where SPS starts to outperform other modulations, as shown in Fig. 21.

The calculated and measured RMS currents are illustrated in Fig. 23 demonstrating a close match of theory and experimental results. To validate the efficiency curve flatness, Fig. 24 is presented for two extreme and rated voltages set throughout the power range. For $M = 0.792$, efficiency starts from 93.61% at minimum power, reaches to its maximum of 97.02% at 2250 W, and drops to 95.1% at full load, which has 1.49% efficiency gap between light-load and full-load cases. This gap for $M = 0.628$ is 0.53% and for $M = 0.972$ is 0.17%. This narrow efficiency gap between light and full load in practice validates the theory outlined in Section II-G. At full load in Fig. 24, despite having different RMS current, the efficiency in two $M = 0.972$ and $M = 0.792$ cases is almost the same. The reason for this is the higher ZVS switching losses of the LV side according to [27] at $M = 0.972$, where the ZVS switching occurs in extremely higher currents.

The drain–source voltage and the gate–source voltage at three different operating modes have been included to further clarify the ZVS obtained using the hybrid modulation. For example, Fig. 25(a), measured at $V_i = 420$ V, $V_{\text{bat}} = 40$ V, and $P = 500$ W, demonstrates the ZVS operation of LV- and HV-side switches.

B. Dynamic Response of the Converter

To demonstrate transient responses, EPS-to-EPS, EPS-to-AEPS, and AEPS-to-EPS transitions are included in Fig. 26(a)–(c), respectively. For the EPS-to-EPS transition in Fig. 26(a), a power jump from 3.5 to 1 kW is demonstrated, which shows the battery current smoothly following and reaching i_{ref} in about 6 ms, and V_b remains at zero. Fig. 26(b) and (c) shows the EPS-to-AEPS mode transition with a power jump from 2500 to 750 W and reverse condition, respectively. In both the transitions, the battery current follows i_{ref} within 10 ms and the overshoot controller updates the duty values gradually to charge or discharge the blocking capacitor in about 3 ms. The performance of the overshoot controller is highlighted in Fig. 26(d), which shows the initial switching cycles of the transient operation. In this figure, V_{ab} gradually changes from

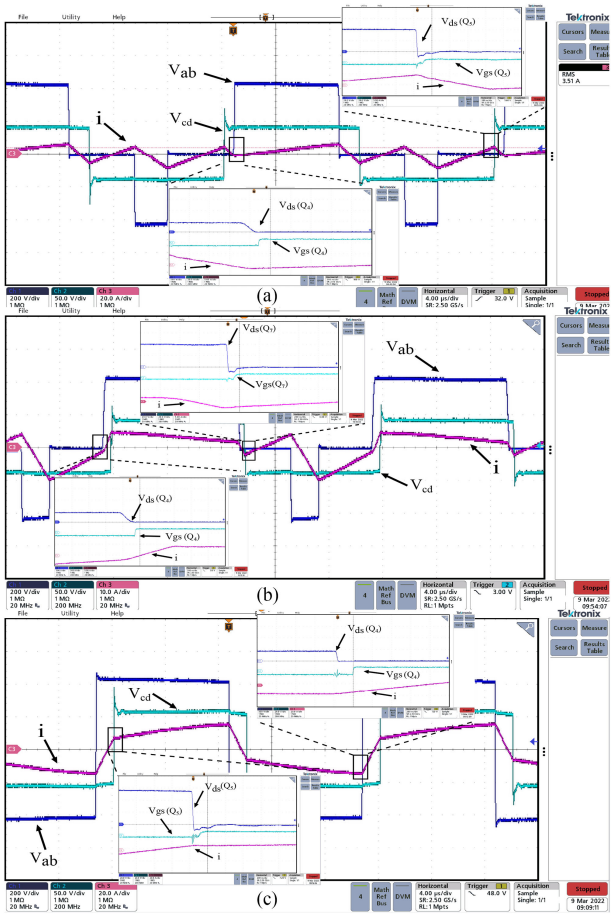

Fig. 25. ZVS operation of the DAB. (a) AEPS mode D: $V_i = 420\,\text{V}$, $V_{\text{bat}} = 40\,\text{V}$, and $P = 500\,\text{W}$. (b) AEPS mode B: $V_i = 420\,\text{V}$, $V_{\text{bat}} = 40\,\text{V}$, and $P = 750\,\text{W}$. (c) SPS: $V_i = 380\,\text{V}$, $V_{\text{bat}} = 56\,\text{V}$, and $P = 4000\,\text{W}$.

an asymmetric to a symmetric waveform, while the tank current changes without any overshoots or oscillations. The dc voltage due to the asymmetrical duty cycles is only applied to the HV side that has a dc-blocking capacitor. The proposed approach controls transient phenomena in the HV tank using a simple PI controller with a low computational complexity. This controller changes the duty cycles gradually so that the capacitor voltage rises or falls gradually to avoid large overshoots in its current. In the LV side, where no capacitor is located, the duty cycles are equal, and there is no concern regarding dc transient. This simple effective implementation eliminates the need for fast control methods as they require high bandwidth, which would add to the complexity and computational burden of the implemented firmware.

An extreme voltage step-change response to the input voltage (V_i) from 420 to 380 V is included in Fig. 27. The step change occurs at t_1 during an AEPS mode B operation at 1500-W output power. This change imposes a small disturbance on the battery current, which is rejected by the i_{bat} controller. Subsequently, for the same i_{ref} value, the hybrid modulation algorithm turns to EPS modulation at t_2. As shown in the figure, V_b is discharged gradually by the overshoot controller during the transition to the EPS operation.

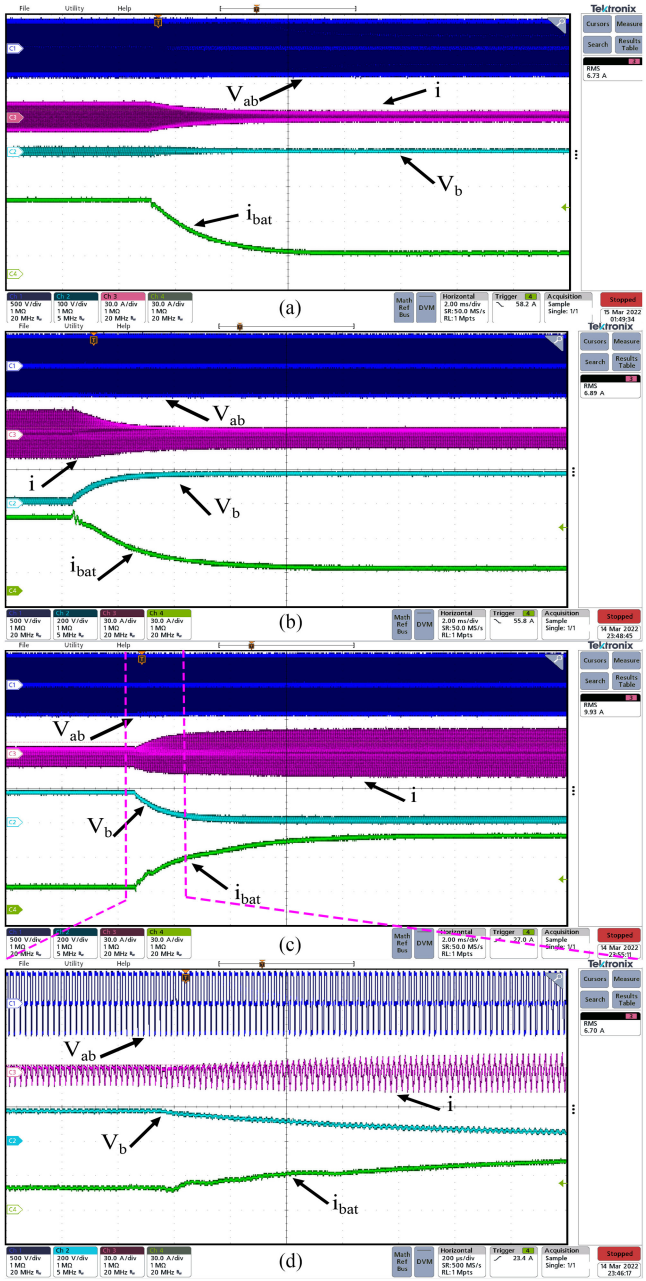

Fig. 26. Controller performance obtained in the transition. (a) EPS-to-EPS transition at $V_i = 380\,\text{V}$ and $V_{\text{bat}} = 56\,\text{V}$. (B) EPS-to-AEPS transition at $V_i = 420\,\text{V}$ and $V_{\text{bat}} = 40\,\text{V}$. (c) AEPS-to-EPS transition at $V_i = 420\,\text{V}$ and $V_{\text{bat}} = 40\,\text{V}$. (d) Zoomed waveform of AEPS-to-EPS transition.

C. Comparison With TPS Modulations

According to Fig. 28(a), efficiency is deteriorated in conventional SPS modulation due to the higher RMS current and LV-side hard-switching losses in low power. The advanced symmetric TPS method and the proposed hybrid modulation in this article are presented to boost the efficiency. In this section, the comparisons of the proposed hybrid modulation with TPS modulations and other asymmetrical modulations are provided. RMS current, efficiency, and ZVS range of operation are the key factors considered in the comparison.

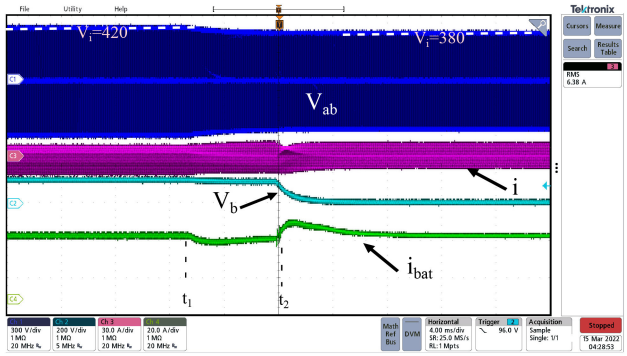

Fig. 27. Input voltage step change from 420 to 380 V ($V_{bat} = 48$ V).

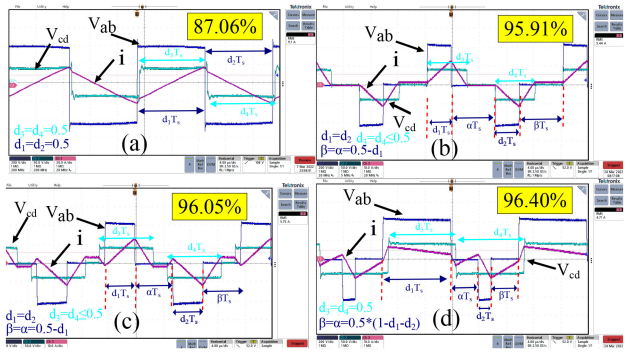

Fig. 28. Operating waveform at (a) SPS, (b) TCM, (c) dual PWM, and (d) AEPS mode B. $V_{bat} = 40$ V, $V_i = 420$ V, and $P = 1000$ W.

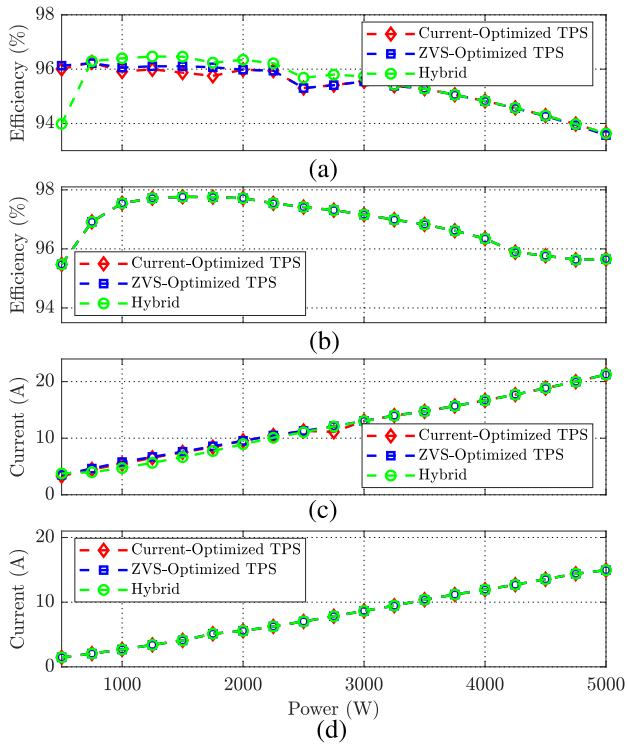

Fig. 29. Practical efficiency at (a) efficiency $M = 0.628$, (b) efficiency $M = 0.972$, (c) RMS current $M = 0.628$, and (d) RMS current $M = 0.972$.

First, the "current-optimized TPS" approaches presented in [23] and [24] and "ZVS-optimized TPS" methods presented in [37] are compared with the proposed hybrid modulation in this article. In the "current-optimized TPS" methods, the objective is to minimize RMS current using a triangle current modulation (TCM) at the low-power region, as shown in Fig. 28(b). The objective of the "ZVS-optimized TPS" method is to maintain ZVS at the expense of a higher RMS current than TCM. As such, for the low-power region, the ZVS-optimized TPS method utilizes dual pulsewidth modulation (PWM), as shown in Fig. 28(c). The hybrid modulation method in this article employs AEPS modulation in the low-power region, as shown in Fig. 28(d), that minimizes RMS current while guaranteeing ZVS; therefore, the efficiency of the proposed hybrid is superior than that of the other two approaches, as shown in Fig. 29. It is worth mentioning that at the high-power region, TPS and hybrid modulation both propose the same modulation, that is, EPS mode A, leading to a similar efficiency, as shown in Fig. 29.

For the power range of 750–3000 W, the proposed hybrid approach achieves higher efficiency due to the following reasons: 1) lower RMS current and 2) lower switching losses due to ZVS as for $P = 2250$ W up to $P = 3000$ W; both the TPS methods [23], [24], [37] can only provide ZCS. For power higher than 3250 W, all the approaches have identical results. For $M = 0.62$ at $P = 500$ W, the AEPS approach has slightly lower efficiency because of the slightly higher core losses that is the result of 50% duty cycle assumption on the LV-side bridge. This problem, however, can be resolved by lowering LV-side duty cycles in a symmetrical fashion, which is beyond the scope of this article.

For the TCM mode in the "current-optimized TPS" method, there are three ZCS switching legs, one at the HV side and two at the LV side. For the dual PWM in the "ZVS-optimized TPS" method, although ZVS is achieved for a larger operating range compared to the current-optimized TPS, for the middle-power range, the method loses ZVS and can only obtain partial ZVS (PZVS), which is the case that inductor current discharges switch output capacitors but is not sufficient for a full discharge, as shown in Fig. 30(b). Utilizing the proposed modulation mode (AEPS mode B), the hybrid method presents wider ZVS range compared to ZVS-optimized TPS, as shown in Fig. 30(c). It should be noted that the PZVS range operation in hybrid modulation is determined by the required minimum inductor current at switching instance. For example, Fig. 30 is for 1.5 and 2.5 A absolute minimum required inductor current at HV and LV legs, respectively. If the absolute required minimum current at the LV side reduces to 1.5 A, which is the case in this article GAN-based converter with low C_{oss} capacitors, the PZVS range is very narrower, and the hybrid modulation obtains ZVS almost in the entire region. Not only hybrid modulation achieves ZVS in the low-M region but also has a lower RMS current, as shown in Fig. 29(c). In Fig. 28(b), the TPS has steep slopes in the inductor current due to the high gap between V_i and NV_{bat}. However, due to a dc-biased voltage on the capacitor, this gap is smaller in the AEPS mode, leading to smoother slopes in the inductor current, as shown in Fig. 28(d). Therefore, the RMS current is lower for the low-M region for hybrid modulation. As the M

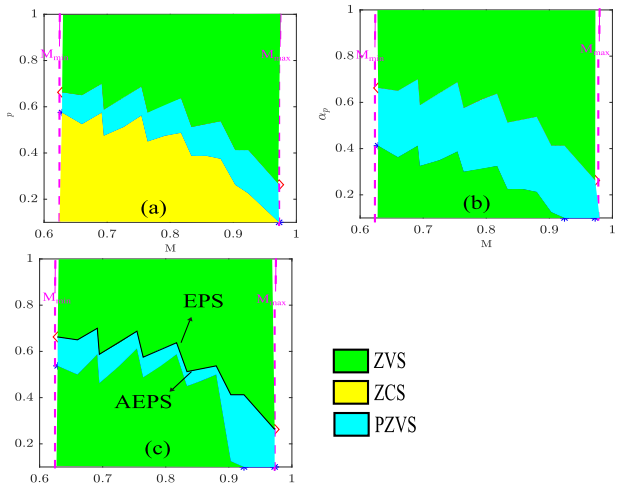

Fig. 30. ZVS region for (a) current-optimized TPS, (b) ZVS-optimized TPS, and (c) hybrid.

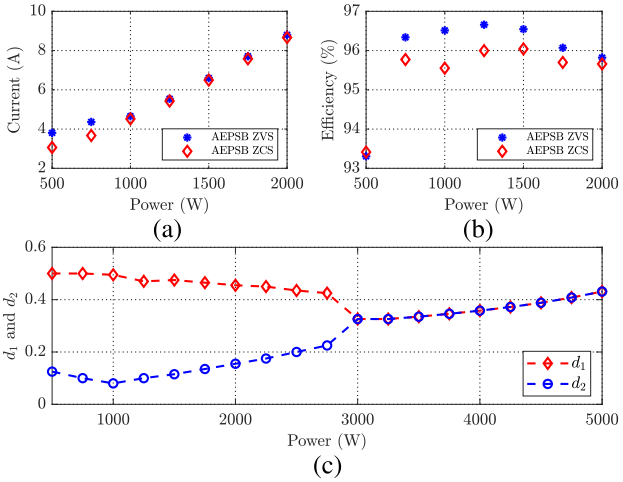

Fig. 31. (a) Tank RMS current. (b) Efficiency for asymmetric mode B with ZCS and ZVS switching at the HV side. (c) Estimated d_1 and d_2. $V_{\text{bat}} = 40$ V and $V_i = 420$ V.

value increases, the slopes of TPS become smaller, and for the middle-M range, TPS presents slightly lower RMS current than hybrid. For high M values, the RMS currents are identical as they both use the same modulations.

It is important to note that the tradeoff between conduction losses and switching losses depend highly on the selected switches. The proposed method can optimize the total losses by choosing the right modulation in various operating points and can target ZVS, ZCS, or RMS minimization all together. The experimental setup in this article employs GaNs in both the HV and LV sides. Because of the low C_{ds} capacitance in GaNs, the C_{oss} losses will be minimal. Therefore, for regions that a modulation method, such as TPS, does not achieve ZVS and can only offer ZCS, the resultant C_{oss} losses will not play a significant role in the efficiency, and therefore, the problems associated with ZCS will not be highlighted in the efficiency comparisons. For different implementations that use Si switches with a higher C_{oss} or for applications operating at higher switching frequencies, the advantages of guaranteeing ZVS by the proposed hybrid approach and, thus, the efficiency improvements will be more significant compared to a TPS that can only offer ZCS.

It is worth mentioning that the proposed hybrid modulation in this article employs duty cycle variables at the HV side for the optimization parameters and has no optimization variable for the LV side as it operates at 50%. However, the TPS approach uses one duty cycle variable for the HV side ($d_1 = d_2 = d_p$) and one variable for the LV side ($d_3 = d_4 = d_s$). Therefore, it is not expected that AEPS is capable of demonstrating higher efficiency in the extremely low-power range, where core losses are dominant and determined by the LV-side bridge duties.

D. Comparison With Other Asymmetrical Modulations

Existing asymmetrical modulations for the DAB converter have considered special modes of asymmetrical waveforms and demonstrated that the asymmetrical modulation can actually outperform other existing approaches such as TPS. For instance, the study in [30] proposes an APWM operation using a single mode of operation. Although this assumption makes the optimization simpler and less complex, it suffers from high RMS current as the converter only operates in a narrow M region and its full capability is not utilized. Moreover, using this method, six switches operate under ZCS condition at turn ON and only two switches turn ON under ZVS condition. The study in [31] presents a hybrid modulation, which is a combination of SPS and APWM with a simple optimization objective of setting the voltage gain equal to 1 with the aid of blocking capacitor. Even though this setting leads to lower optimization complexity, its efficiency significantly drops in the middle-M range due to higher RMS current and narrower ZVS operating range.

The proposed solution in this article only uses a blocking capacitor on the HV side that carries a significantly lower current and, thus, has a small size and a negligible loss. Other asymmetrical approaches either use blocking cap on both the sides [32] or use a limited asymmetrical modulation with a lower number of optimization variables to avoid the use of blocking capacitors [30]. For example, the study in [32] uses the half-bridge topology with a limited low-power application suitable for $M = 0.5$.

The study in [29], which provides the widest ZVS range among all TPS modulations, is also compared with other asymmetrical and proposed hybrid approaches. Despite the wide ZVS range, the method has a period of ZCS switching in the medium-power range. Moreover, it has higher RMS current as it only uses EPS modulation in low-power levels. In the proposed hybrid method in this article, the middle power range also has ZVS because of the asymmetric mode B and the RMS current is also lower than EPS because the effective ac voltage is reduced using the blocking capacitor.

Table V summarizes the highlights of comparisons provided in this section. It should be mentioned that asymmetric modulation used for three-phase DAB converters [33], [34] is not included in the comparison as they may operate the DAB under ZCS or even hard switching at light loads and have more complex hardware.

V. Conclusion

This article proposed a new hybrid modulation that employs various modes of novel AEPS modulation and conventional symmetrical modes. The proposed hybrid approach minimized RMS current while guaranteeing the ZVS operation, which resulted in a high efficiency over a wide operating range. All the AEPS modes were investigated and analyzed to achieve the optimum region for each mode. To implement the optimized modulation, a control system was proposed, which provides the desired performance while addressing unique practical consideration for AEPS modulation and eliminating the need for a blocking capacitor in the LV side. The proposed solution achieved a wider ZVS range by employing a novel AEPS mode B modulation, which would not be feasible to achieve by other symmetrical modulations such as TPS. Moreover, AEPS modulation showed lower RMS current compared to other conventional modulations in the low-gain region. The 5-kW experimental setup validated the efficiency improvement by 10–15% and 1.5–2.5% compared to the SPS and the EPS, respectively, and verified controller performances during transients.

Appendix

A minimal current is required to ensure soft switching transition during dead time to discharge the GaN drain–source capacitor. In Section II-D, the ZVS switching condition is for zero current, and using the presented current optimization procedure in Section II, the ZCS can occur in two instances for the HV side: $d_1'\pi$ and $(1+d_2')\pi$. In the HV side, the loss associated with C_{oss} contributes to considerable efficiency drop, and it is a promising practice to improve efficiency by ensuring ZVS in the HV side. The ZVS conditions for the HV side can be modified as

$$\begin{cases} i(d_1'\pi) < -I_{\text{min}} \\ i((1+d_2')\pi) > I_{\text{min}} \end{cases} \tag{30}$$

where I_{min} is the minimum current that the HV tank requires to ensure ZVS. Because of GaN small C_{oss} capacitor, this current is as small as 1.5 A. The penalty of ensuring ZVS is a slight increase in i_{rms}. However, the benefit is the elimination of switching C_{oss} losses in the HV side. Fig. 31(a) presents i_{rms} for asymmetric Mode B with ZVS or ZCS switching. As observed in Fig. 31(b), despite a marginal increase in RMS current, switching with ZVS has superior efficiency compared to ZCS. The optimum d_1 and d_2 in hybrid modulation, with ZVS switching, are presented in Fig. 31(c). The estimation of duty cycle equations for the case providing ZVS can be performed according to Section II-H.

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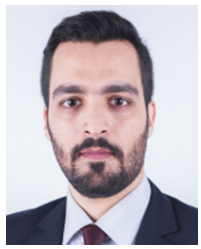

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