A Second-Harmonic Suppression Method Based on Differentiated-Capacitance Design for Input-Parallel Output-Series DAB Fed Single-Phase VSI

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***Abstract*—In the single-phase voltage source inverter (VSI), the instantaneous output power pulsates at twice the line frequency, generating second-harmonic voltage in dc bus. Bulky electrolytic capacitors or additional auxiliary circuits are used in traditional methods, which inevitably limit the system lifetime, efficiency, and power density. In this article, the input-parallel output-series (IPOS) dual active bridge (DAB) with differentiated-capacitance design is adopted as the front-end dc–dc stage. The pulsating power is compensated by the energy gap that the differentiated output capacitors release. The small-signal model of the IPOS DAB fed VSI is built, and based on which, the voltage-complementary algorithm is proposed. Then, the preferred zone and optimization scheme of the main circuit parameters are designed according to the quantitative analysis of the suppressing effect. Furthermore, a 625-W IPOS DAB fed VSI design example is presented and tested. The experimental result shows that at least seven times the capacitance requirements can be reduced without any additional components, and the power quality of both the input current and the output voltage is well guaranteed.**

***Index Terms*—Dual active bridge (DAB), parameter optimization design, second-harmonic suppression, single-phase inverter.**

I. Introduction

As THE interface between ac and dc, the power electronics transformer (PET), consisting of the dual-active-bridge (DAB) converter and the H-bridge dc/ac converter, is considered as the contender for line-frequency transformer [1]. The isolated single-phase inverter or rectifier is the elementary unit of PET, which can be classified into single-stage [2]–[6] and two-stage [7]–[9] structures. In comparison, the two-stage structure is more suitable for applications where the input voltage has a wide variation range or has a large difference in magnitude with the output voltage, such as aircraft power systems [10], fuel cells [11], and photovoltaic cells [12], [13].

In single-phase systems, the instantaneous output power pulsates at twice the line frequency, generating the second-harmonic current (SHC) at the input of VSI. For the dc bus, the SHC would cause second-harmonic voltage (SHV) and distort the output waveform of the dc–ac stage, making it hard to meet the requirements of power quality [14], [15]. For the front-end dc–dc converter, the SHC causes an increment in current stress of semiconductors, inductors, and transformers, decreasing the conversion efficiency [7], [16]. For the dc source, the SHC causes the fuel cells to overheat [17] and the output power of solar cells to vibrate near the maximum power point [18].

In traditional design, the very large, electrolytic capacitors are usually connected in parallel with the dc bus. The lifetime of an electrolytic capacitor is only 3–6 years (<10 000 h) and declines by half with every temperature increase of 10 °C [19], which limits the operational reliability and service life span of the two-stage inverter. In contrast, the metalized film capacitor has a life span of 12–15 years, but its price, volume, and weight are about 10 times the electrolytic capacitor with the same parameters. Hence, it is urgent and significant to eliminate the second harmonic in dc bus, front-end converter, and dc source with smaller main circuit capacitors [20].

In the literature, the methods of reducing the SHC and SHV in the single-phase system have been reported, among which can be classified into topology type and control type [21]. The topology-type methods insert auxiliary circuits to absorb the second harmonic, including the passive decoupling circuit and the active decoupling circuit. The passive decoupling circuit utilizes the *L*–*C* filter with a resonant frequency of $2f_0$ to bypass the SHC [22]. Nevertheless, the magnetic material suffers from the disadvantage of low power density and additional power loss, such as magnetic loss and core loss. The active decoupling circuit inserts nonisolated or isolated power semiconductor circuit to absorb the second harmonic, which includes the boost type [23]–[25], buck type [26], [27], H-bridge type [28], [29], flyback type

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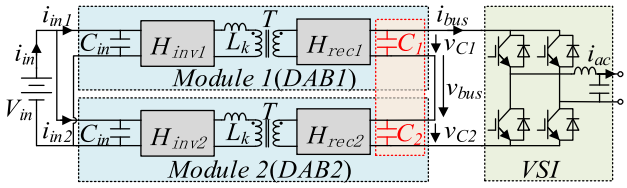

Fig. 1. Main circuit of IPOS DAB fed VSI.

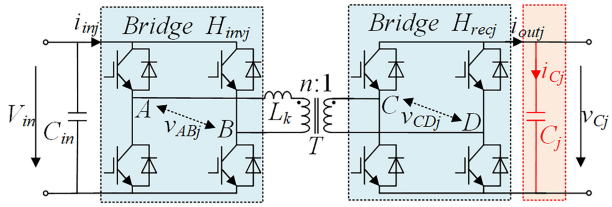

Fig. 2. Main circuit of submodule DABj (j = 1,2).

[30], [31], VSC type [32], [33], etc. However, these additional circuits inevitably increase the volume, cost, and power loss of the system.

The control type only modifies the control strategy, keeping the original topology [21]. To prevent the SHC penetrating into the front-end stage, an alternative approach is increasing the output impedance of dc–dc converters through inserting active damping by virtual-impedance-based control strategy [34]–[36]. Yet, the existing control schemes can only apply for the buck-derived or boost-derived front-end dc–dc converters [37]. Moreover, these approaches still need bulky capacitors to absorb the second harmonic and stabilize the dc bus voltage. The repetitive controller (RC) is adopted in [38], but this method has poor robustness to the frequency fluctuation of the power grid. A current ripple damping control based on a quasi-z source inverter has been proposed in [39]. However, the bulky capacitors are still needed.

To solve the downsides of existing power decoupling technology, this article proposes an original second-harmonic suppression method based on differentiated-capacitance design and resolves the conflict between small harmonics and small capacitance. The input-parallel output-series (IPOS) DAB is adopted as the front-end stage as shown in Fig. 1. This structure reduces the current stress of semiconductors on the primary side and the voltage stress on the secondary side, which is suitable for fuel cells and solar cell systems [40].

As can be seen in Fig. 1, the DAB modules' output capacitors serve as the dc bus capacitor together. In the traditional design, these output capacitors have the same value ($C_1 = C_2$), indicating that module 1 (DAB1) and module 2 (DAB2) are working in the same state. In this article, the differentiated design is employed in C_1 and C_2. The pulsating power is compensated by the energy difference that these capacitors release as the ripple voltages are complementary. Combined with the proposed ripple-complementary algorithm, the SHV in dc bus can be reduced to less than 15% of the traditional design under the same C_1+C_2, and the current ripple of the input source can be reduced up to 50%.

Section II analyzes the working principle of IPOS DAB fed VSI and builds the small-signal model. Based on this, Section III gives a detailed description of the differentiated-capacitance design, including the physical mechanism and working process. It also designs the control algorithm, which can realize the complementarity of capacitors' voltage ripple. Furthermore, it points out and analyzes the uncontrollable interval of this algorithm. This interval makes the algorithm unable to work throughout the 2ω period and influences the suppression effect. Then, Section IV quantitatively analyzes the impact of this interval and conducts the relationship expressions between the harmonic suppression effect and the main circuit parameters. After that, this article gives the preferred zone and optimization scheme of the main circuit parameters. A 625-W prototype has been built and tested in Section V. The experimental results are provided to verify the design method and analysis model of the differentiated-capacitance design.

II. Mathematical Models of Second Harmonic in IPOS DAB Fed Single-Phase VSI

A. Operation Principle of DAB Modules

In traditional designs, v_{C1} and v_{C2} change synchronously and evenly distribute the dc bus voltage ($v_{C1} = v_{C2} = v_{\rm bus}/2$). The submodule topology DABj is shown in Fig. 2 (j = 1,2).

The phase-shift modulation is utilized in DAB to satisfy the power delivery by adjusting the phase-shift angle. In this article, the single-phase-shift modulation is employed. The midpoint voltages v_{ABj} and v_{CDj} are bipolar high-frequency square waves, and the phase-shift ratio between them is marked as d_j. When v_{ABj} is ahead of v_{CDj}, the phase-shift ratio is positive (d_j>0), and the power flows from the primary side to the secondary side; when v_{ABj} lags behind v_{CDj}, the reverse applies. According to the working principle of single-phase-shift modulation, the output power of DABj can be expressed as follows:

$$P_{{\rm out}j} = \frac{nV_{\rm in}v_{Cj}|d_j|(1-|d_j|)}{2f_sL_k} \tag{1}$$

where v_{Cj} is the switching-cycle average of the capacitor's voltage, and f_s is the switching frequency.

Considering v_{Cj} as a constant during one switching period, the output current of DABj can be derived from (1) as follows:

$$i_{{\rm out}j} = \frac{nV_{\rm in}|d_j|(1-|d_j|)}{2f_sL_k}. \tag{2}$$

From (2), $i_{{\rm out}j}$ is only regulated by d_j and independent of v_{Cj}. Meanwhile, $i_{{\rm out}j}$ has a peak value $i_{\rm out\_max}$ under $|d_j| = 0.5$.

Assuming the conversion efficiency is 100%, the input power and output power of DABj are equal. The input current of the front-end stage is the sum of $i_{\rm in1}$ and $i_{\rm in2}$

$$i_{\rm in} = \sum_{j=1}^{2} i_{{\rm in}j} = \sum_{j=1}^{2} \frac{nv_{Cj}|d_j|(1-|d_j|)}{2f_sL_k}. \tag{3}$$

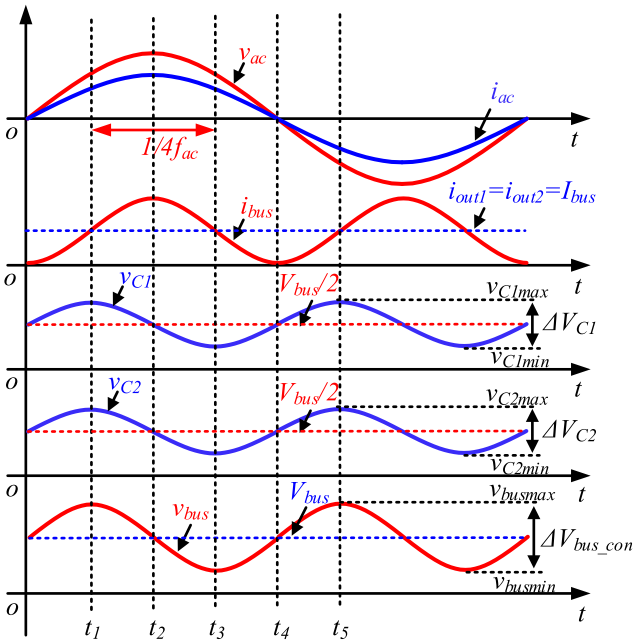

Fig. 3. Key waveforms of IPOS DAB fed VSI under the traditional design.

B. Power Model of Second Harmonic

For the sake of analysis, supposing that the output voltage and current of VSI are pure sinusoidal waveforms, and they can be expressed as follows:

$$\begin{cases} v_{\rm ac} = V_m \sin(\omega t) \\ i_{\rm ac} = I_m \sin(\omega t - \theta) \end{cases} \tag{4}$$

where θ is the load impedance angle. $\theta = 0$ as VSI is connected to the grid.

The dc bus current can be derived as follows:

$$i_{\rm bus} = \frac{MI_m}{2}\cos\theta - \frac{MI_m}{2}\cos(2\omega t - \theta) = I_{\rm bus} + i_{\rm bus\_2\omega} \tag{5}$$

where M is the modulation ratio of VSI.

As seen, $i_{\rm bus}$ is composed of two items, namely, the dc current $I_{\rm bus}$ and the SHC $i_{\rm bus\_2\omega}$. In the traditional design, the dc bus capacitors need to be large enough to compensate most of SHC, and the front-end dc–dc stage only supplies the constant rated power. On combining the above-mentioned analysis with (2), the steady state of d_1 and d_2 satisfy

$$d_1(1-d_1) = d_2(1-d_2) = \frac{2I_{\rm bus} f_s L_k}{nV_{\rm in}}. \tag{6}$$

Fig. 3 shows the waveforms of $v_{\rm ac}$, $i_{\rm ac}$, $v_{\rm bus}$, $i_{\rm bus}$, $i_{\rm out1}$, $i_{\rm out2}$, v_{C1}, and v_{C2} in the traditional design. As seen, v_{C1} and v_{C2} reduce synchronously to compensate the power gap between input and output as $i_{\rm bus} > I_{\rm bus}$ and increase to absorb the power surplus as $i_{\rm bus} < I_{\rm bus}$. The slewing rate of v_{C1} and v_{C2} can be expressed as follows:

$$\begin{cases} \frac{dv_{C1}}{dt} = \frac{I_{\rm out1} - i_{\rm bus}}{C_1} \\ \frac{dv_{C2}}{dt} = \frac{I_{\rm out2} - i_{\rm bus}}{C_2} \end{cases} \tag{7}$$

where $I_{\rm out1}$ and $I_{\rm out2}$ are equal to $I_{\rm bus}$ in the traditional design.

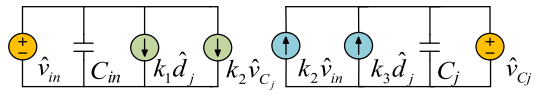

Fig. 4. First-order small-signal circuit of DABj.

After making the integration of (7), we have

$$\begin{cases} v_{C1} = \frac{V_{\rm bus}}{2} + \frac{MI_m}{2\omega(C_1+C_2)}\sin(2\omega t - \theta) \\ v_{C2} = \frac{V_{\rm bus}}{2} + \frac{MI_m}{2\omega(C_1+C_2)}\sin(2\omega t - \theta) \end{cases}. \tag{8}$$

The peak-to-peak value of SHV in dc bus is equal to the sum of ΔV_{C1} and ΔV_{C2}

$$\Delta V_{\rm bus\_con} = \Delta V_{C1} + \Delta V_{C2} = \frac{2MI_m}{\omega(C_1+C_2)}. \tag{9}$$

Substituting (6) and (8) into (3), the input current of the system can be obtained as follows:

$$i_{\rm in} = \frac{V_{\rm bus} I_{\rm bus}}{V_{\rm in}} + \frac{I^2{}_{\rm bus}}{V_{\rm in}\omega\cos\theta}\frac{2}{C_1+C_2}\sin(2\omega t - \theta). \tag{10}$$

As can be seen, the input current also contains SHC due to the fluctuations of v_{C1} and v_{C2}. From (9) and (10), the only way to reduce SHV and SHC in the traditional design is to increase the dc bus capacitances C_1 and C_2, which brings more cost and reduces the system reliability.

C. Small-Signal Model of IPOS DAB Fed VSI

In the above-mentioned analysis, the power model of the second harmonic is built and the relationship between SHV, SHC, and the main circuit parameters under the traditional design is obtained. However, the control ability of d_1 and d_2 to the second harmonic is still not clear. Therefore, the small-signal model is built below, and the idea of differentiated-capacitance design can be derived from it.

After perturbing (2) and (3) about the quiescent operating point, the first-order linearized expressions of $\hat{i}_{{\rm in}j}$ and $\hat{i}_{{\rm out}j}$ are obtained

$$\begin{cases} \hat{i}_{{\rm in}j} = \frac{n}{2f_s L_k}\left[\hat{d}_j(1-2d_j)V_{Cj} + d_j(1-d_j)\hat{v}_{Cj}\right] \\ \hat{i}_{{\rm out}j} = \frac{n}{2f_s L_k}\left[\hat{d}_j(1-2d_j)V_{\rm in} + d_j(1-d_j)\hat{v}_{\rm in}\right] \end{cases}. \tag{11}$$

Set the constants k_1, k_2, and k_3 as follows

$$\begin{cases} k_1 = \frac{nV_{\rm bus}}{4f_s L_k}(1-2d) \\ k_2 = \frac{n}{2f_s L_k}(1-d)d \\ k_3 = \frac{nV_{\rm in}}{2f_s L_k}(1-2d) \end{cases} \tag{12}$$

where d is the steady-state value of d_1 and d_2.

From (11) and (12), the first-order small-signal circuit of DABj is shown in Fig. 4. According to (5), VSI can be equivalent to the parallel of dc load R and ac current sources $i_{\rm bus\_2\omega}$. Combining Fig. 4 with VSI's equivalent circuit, the small-signal model of the IPOS DAB fed VSI can be obtained, which is shown in Fig. 5.

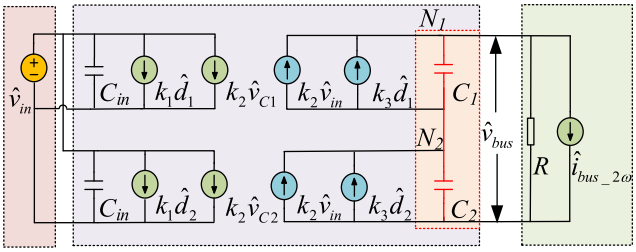

Fig. 5. Small-signal model of the IPOS DAB fed VSI.

Applying KCL in nodes N_1 and N_2

$$C_j\frac{d\hat{v}_{Cj}}{dt}=k_2\hat{v}_{\text{in}}+k_3\hat{d}_j-\frac{\sum_{j=1}^{2}\hat{v}_{Cj}}{R}-\hat{i}_{\text{bus\_2}\omega}. \tag{13}$$

Considering V_{in} is constant, the result of (13) can be rewritten in the S-domain

$$\begin{cases}\hat{v}_{C_1}=\frac{-sRC_2\hat{i}_{\text{bus\_2}\omega}+k_3\left[(sRC_2+1)\hat{d}_1-\hat{d}_2\right]}{s^2RC_1C_2+s(C_1+C_2)}\\ \hat{v}_{C_2}=\frac{-sRC_1\hat{i}_{\text{bus\_2}\omega}+k_3\left[(sRC_1+1)\hat{d}_2-\hat{d}_1\right]}{s^2RC_1C_2+s(C_1+C_2)}\end{cases}. \tag{14}$$

The small-signal expression of dc bus voltage is the sum of $\hat{v}_{C1}$ and $\hat{v}_{C2}$

$$\hat{v}_{\text{bus}}=\hat{v}_{C1}+\hat{v}_{C2}=R\frac{k_3(C_2\hat{d}_1+C_1\hat{d}_2)-(C_1+C_2)\hat{i}_{\text{bus\_2}\omega}}{sRC_1C_2+(C_1+C_2)}. \tag{15}$$

Similarly, the small-signal expression of the system's input current can also be derived as follows:

$$\begin{aligned}\hat{i}_{\text{in}}&=\hat{i}_{\text{in1}}+\hat{i}_{\text{in2}}\\&=k_1(\hat{d}_1+\hat{d}_2)+k_2R\frac{k_3(C_2\hat{d}_1+C_1\hat{d}_2)-(C_1+C_2)\hat{i}_{\text{bus\_2}\omega}}{sRC_1C_2+(C_1+C_2)}.\end{aligned} \tag{16}$$

From (15) and (16), it is easy to find $\hat{v}_{\text{bus}}=0$ and $\hat{i}_{\text{in}}=0$ after d_1 and d_2 meet the constraints of (17), which indicates that the dc bus voltage and input current have no low-frequency ripple under the perturbation of $\hat{i}_{\text{bus\_2}\omega}$, and the complete suppression of the second harmonic can be realized

$$\begin{cases}k_3(C_2\hat{d}_1+C_1\hat{d}_2)-(C_1+C_2)\hat{i}_{\text{bus\_2}\omega}=0\\ \hat{d}_1+\hat{d}_2=0\end{cases}. \tag{17}$$

The solution of (17) is only available under the condition of $C_1\neq C_2$. Thus, the traditional design cannot eliminate the second harmonic by increasing the dc bus capacitance. And this is the root reason for the differentiated-capacitance design proposed in this article. Under this condition, the solution can be obtained as (18), which is the small-signal expression of the ripple-complementary control algorithm to be analyzed below

$$\begin{cases}\hat{d}_1=\frac{(C_1+C_2)\hat{i}_{\text{bus\_2}\omega}}{k_3(C_2-C_1)}\\ \hat{d}_2=\frac{(C_1+C_2)\hat{i}_{\text{bus\_2}\omega}}{k_3(C_1-C_2)}\end{cases}. \tag{18}$$

III. Capacitor Voltage Ripple-Complementary Control

According to the analysis presented in Section II, there is no second harmonic in dc bus voltage and input current as long as $\hat{d}_1$ and $\hat{d}_2$ can track $\hat{i}_{\text{bus\_2}\omega}$ as (18) under differentiated-capacitance design. Substituting (18) into (14), $\hat{v}_{C1}$ and $\hat{v}_{C2}$ turn into

$$\begin{cases}\hat{v}_{C_1}=-\frac{2sC_1C_2R+2(C_1+C_2)}{s^2RC_1C_2+s(C_1+C_2)}\cdot\frac{\hat{i}_{\text{bus\_2}\omega}}{C_1-C_2}\\ \hat{v}_{C_2}=\frac{2sC_1C_2R+2(C_1+C_2)}{s^2RC_1C_2+s(C_1+C_2)}\cdot\frac{\hat{i}_{\text{bus\_2}\omega}}{C_1-C_2}\end{cases}. \tag{19}$$

As can be seen, $\hat{v}_{C1}$ and $\hat{v}_{C2}$ fluctuate with $\hat{i}_{\text{bus\_2}\omega}$ but always satisfy $\hat{v}_{C1}=-\hat{v}_{C2}$. Thus, the control strategy shown in (18) makes the ripple of v_{C1} and v_{C2} to the complementary state and then maintains v_{bus} constant. To achieve this in practice, the charge–discharge of C_1 and C_2 need to be accurately controlled. Since C_1 and C_2 are connected in series, their discharge current and time are determined by the dc bus. Only by designing different d_1 and d_2 to adjust the charge current, can the ripple complementarity be achieved. The control algorithm of IPOS DAB, named ripple-complementary control, would be derived in this section.

A. Design of Ripple-Complementary Control Algorithm

The ripple-complementary control algorithm needs to meet two constraints: the ripple of v_{C1} and v_{C2} is complementary, and the SHC is fully absorbed.

1) Mutual Complementation of v_{C1}'s and v_{C2}'s Ripple: The discharge current of C_1 and C_2 is i_{bus}, so the discharged charge in one switching period T_s is

$$Q_{C_1\_\text{out}}=Q_{C_2\_\text{out}}=i_{\text{bus}}T_s. \tag{20}$$

In the same way, the charged charge of C_1 and C_2 in T_s can be calculated as follows:

$$\begin{cases}Q_{C_1\_\text{in}}=i_{\text{out1}}T_s\\ Q_{C_2\_\text{in}}=i_{\text{out2}}T_s\end{cases}. \tag{21}$$

The variation of v_{C1} and v_{C2} in T_s is

$$\begin{cases}\Delta v_{C_1}=\frac{Q_{C_1\_\text{in}}-Q_{C_1\_\text{out}}}{C_1}\\ \Delta v_{C_2}=\frac{Q_{C_2\_\text{in}}-Q_{C_2\_\text{out}}}{C_2}\end{cases}. \tag{22}$$

In ripple-complementary control, the sum of Δv_{C1} and Δv_{C2} needs to be 0 at all times:

$$\Delta v_{C1}+\Delta v_{C2}=0. \tag{23}$$

Substituting (20)–(22) into (23), the constraint equation of d_1 and d_2 is

$$\frac{d_1(1-d_1)}{C_1}+\frac{d_2(1-d_2)}{C_2}=\frac{2f_sL_k}{nV_{\text{in}}}(I_{\text{bus}}+i_{\text{bus\_2}\omega})\left(\frac{1}{C_1}+\frac{1}{C_2}\right). \tag{24}$$

2) Full Buffering of SHC: To get the similar properties of the bulky capacitor, the algorithm also needs to meet the constraint that all SHC can be compensated by dc bus capacitors. In other words, the front-end dc–dc converter only outputs the required dc power to VSI

$$p_{\text{out1}}+p_{\text{out2}}=P_{\text{ac}}. \tag{25}$$

From the expression of DAB's output power, p_{out1} and p_{out2} are directly related to v_{C1} and v_{C2} that are variable with time.

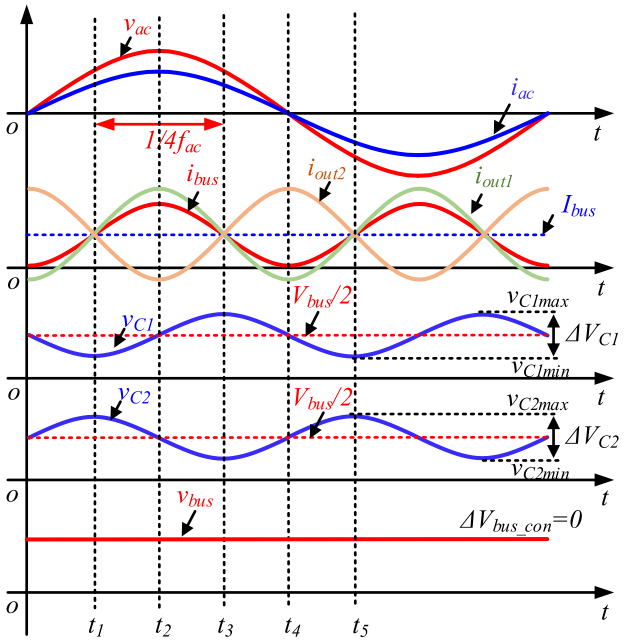

Fig. 6. Key waveforms of IPOS DAB fed VSI under differentiated-capacitance design ($C_1 < C_2$).

This time-varying character would make the control algorithm very complex. Considering ΔV_{C1} and ΔV_{C2} are small, this time-varying character can be neglected in (25). The impact of this simplification will be analyzed in the next section. Substituting (1) into (25), the other constraint equation is

$$d_1(1-d_1)+d_2(1-d_2)=\frac{2f_sL_kV_mI_m\cos\theta}{nV_{\text{in}}V_{\text{bus}}}. \quad (26)$$

Combining (24) and (26), the ripple-complementary control algorithm can be derived as follows:

$$\begin{cases} d_1(1-d_1)=\frac{2f_sL_k}{nV_{\text{in}}}\left(I_{\text{bus}}-i_{\text{bus\_2}\omega}\frac{C_1+C_2}{C_1-C_2}\right) \\ d_2(1-d_2)=\frac{2f_sL_k}{nV_{\text{in}}}\left(I_{\text{bus}}+i_{\text{bus\_2}\omega}\frac{C_2+C_1}{C_1-C_2}\right) \end{cases}. \quad (27)$$

After perturbing and linearizing (27) about the quiescent operating point, the result fits with the small-signal expression in (18). In contrast with the traditional algorithm, the ripple-complementary algorithm injects ripple component, which is in-phase or out-of-phase with the SHC in dc bus.

Substituting (27) into (2) yields the following:

$$\begin{cases} i_{\text{out1}}=I_{\text{bus}}-i_{\text{bus\_2}\omega}\frac{C_1+C_2}{C_1-C_2} \\ i_{\text{out2}}=I_{\text{bus}}+i_{\text{bus\_2}\omega}\frac{C_1+C_2}{C_1-C_2} \end{cases}. \quad (28)$$

The output currents of DAB1 and DAB2 are no longer constant as shown in Fig. 3. And this added ripple current is inversely proportional to the difference between C_1 and C_2. Therefore, using this algorithm in the traditional design would lead to the infinite output current of front-end DAB converters, indicating that the traditional equal-capacitance design does not have the active power decoupling capability.

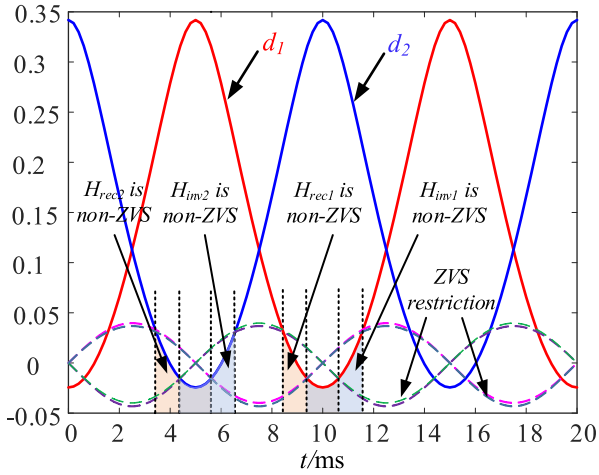

Fig. 7. Non-ZVS interval of DAB1 and DAB2 under differentiated-capacitance design ($C_1 < C_2$).

Fig. 6 shows the typical operating waveforms of the differentiated-capacitance design using ripple-complementary control. The working process is analyzed below.

t_1–t_3($i_{\text{bus}}>I_{\text{bus}}$): The dc bus current is larger than DAB2's output current i_{out2} and smaller than DAB1's output current i_{out1}. v_{C2} drops, and v_{C1} rises. Adjusting the phase-shift ratio to make $|\Delta v_{C1}|$ equals $|\Delta v_{C2}|$ ($\Delta v_{C1}+\Delta v_{C2}=0$), v_{bus} remains constant during this interval. Meantime, the energy stored in C_1 and C_2 decreases to make up for the second-harmonic power as

$$\Delta E_C=\Delta E_{C1}+\Delta E_{C2}=(C_1-C_2)V_{\text{bus}}\Delta v_{C1}<0. \quad (29)$$

t_3–t_5($i_{\text{bus}}<I_{\text{bus}}$): Different from the last period, v_{C2} rises and v_{C1} drops during this interval, and the energy stored in C_1 and C_2 increases to absorb the excess energy of input power. $\Delta v_{C1}+\Delta v_{C2}=0$ still holds.

From the view of power flow, the second-harmonic power in the differentiated-capacitance design is redistributed between C_1 and C_2. The larger capacitor C_2 absorbs a little more second-harmonic power than the VSI generates, but the dc bus voltage stays constant owing to the active voltage complementation of C_1. Overall, the harmonic power is compensated by the energy difference that C_1 and C_2 release as the ripple voltages remain complementary. The working principle of the differentiated-capacitance design is similar to the SHV compensator (SHVC) [32], [33], both of which adopt waveform control on the dc bus capacitance. However, it should be noted that the proposed design method transmits the dc power as the waveform control works and can be implemented into the original circuit without adding any other auxiliary unit.

According to the current-based zero-voltage switch (ZVS) analytical procedure [5], [41], the non-ZVS interval of the proposed method is shown in Fig. 7. As seen, the ZVS is lost near the minimum point of the phase-shift ratio, which is caused by the too-small output current and takes about 10% of the whole second-harmonic period. These non-ZVS intervals would certainly reduce the system's efficiency, but the effect can be neglected because the current stress and switching loss are the smallest during these intervals.

B. Analysis of Uncontrollable Interval

From (2), the allowable variation range of $i_{\text{out}1}$ and $i_{\text{out}2}$ is

$$-i_{\text{out\_max}} \le i_{\text{out}1}, i_{\text{out}2} \le i_{\text{out\_max}} \tag{30}$$

where

$$i_{\text{out\_max}} = \frac{nV_{\text{in}}}{8f_s L_k}.$$

Considering this limitation, the output current of DABj probably cannot follow the ripple-complementary control algorithm in the whole ripple cycle. Substituting (28) into (30), the controllable intervals of DABj are derived as (31), during which $i_{\text{out}j}$ is within limitations. In the remaining uncontrollable interval, $i_{\text{out}j}$ keeps $i_{\text{out\_max}}$ or $-i_{\text{out\_max}}$, and v_{C1} and v_{C2} are not able to achieve the ripple complementarity. Hence, the input current and dc bus voltage are left with low-frequency ripple in practice

$$\begin{aligned} &\textit{DAB1's controllable interval:} -B \le \cos(2\omega t - \theta) \le A \\ &\textit{DAB2's controllable interval:} -A \le \cos(2\omega t - \theta) \le B \end{aligned} \tag{31}$$

where

$$\begin{cases} A = -\left(\frac{i_{\text{out\_max}}}{I_{\text{bus}}} + 1\right)\frac{C_1/C_2 - 1}{C_1/C_2 + 1}\cos\theta \\ B = -\left(\frac{i_{\text{out\_max}}}{I_{\text{bus}}} - 1\right)\frac{C_1/C_2 - 1}{C_1/C_2 + 1}\cos\theta \end{cases}.$$

From the aforementioned equation, the span of the controllable interval is related to parameters A and B. After the rated dc bus current I_{bus} and impedance angle θ are determined, A and B are only related to $i_{\text{out\_max}}$ and C_1/C_2. Considering $i_{\text{out\_max}}/I_{\text{bus}}>1$ in most situations, A is larger than 1, and the limitation of A can be automatically met. The limitation of B will be discussed in the following two cases.

1) $B \ge 1$: Controllable Over the Whole Ripple Cycle: In this case, the complementary-control algorithm remains effective throughout the whole ripple cycle. The working waveforms are ideal as shown in Fig. 6. Theoretically, there would be no second harmonic in dc bus voltage and input current. However, $i_{\text{out\_max}}$ must be large enough as shown in (32), causing an increase in the semiconductors' current stress

$$\frac{i_{\text{out\_max}}}{I_{\text{bus}}} \ge 1 - \frac{1}{\cos\theta}\frac{C_1/C_2 + 1}{C_1/C_2 - 1}. \tag{32}$$

2) $B < 1$: One Uncontrollable Interval: $i_{\text{out\_max}}$ decreases with the increment in L_k. Parameter B is smaller than 1 after $i_{\text{out\_max}}$ reduces to the boundary-value shown in (32). An uncontrolled interval would appear in DAB1's and DAB2's control algorithm. This interval can be calculated as follows:

$$\begin{aligned} &\textit{DAB1's uncontrollable interval:}\ 2\omega t \in \{\alpha, 2\pi - \alpha\} \\ &\textit{DAB2's uncontrollable interval:}\ 2\omega t \in \{\alpha - \pi, \pi - \alpha\} \end{aligned} \tag{33}$$

where $\alpha = \arccos(-B)$.

From the definition of B, α can be also controlled by the ratio C_1/C_2 except for $i_{\text{out\_max}}$. Fig. 8 shows the relationship curve between the span of an uncontrollable interval and C_1/C_2. The smaller the C_1/C_2 is, the shorter the uncontrollable interval is. Therefore, the effect of the uncontrollable interval can be decreased by adjusting C_1/C_2. But C_1/C_2 should be kept in a reasonable range to limit the switching-frequency harmonics.

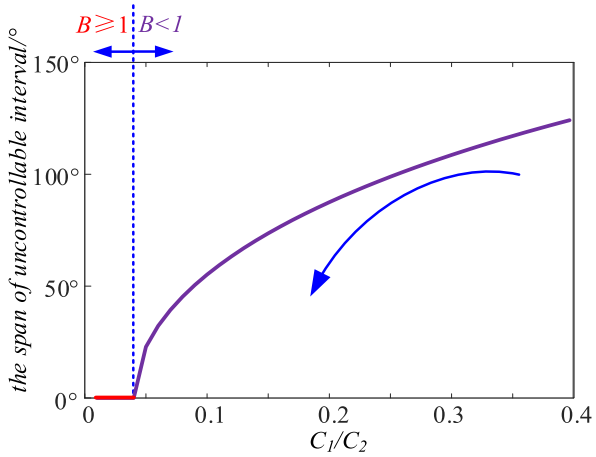

Fig. 8. Relationship curve between the span of uncontrollable interval and C_1/C_2.

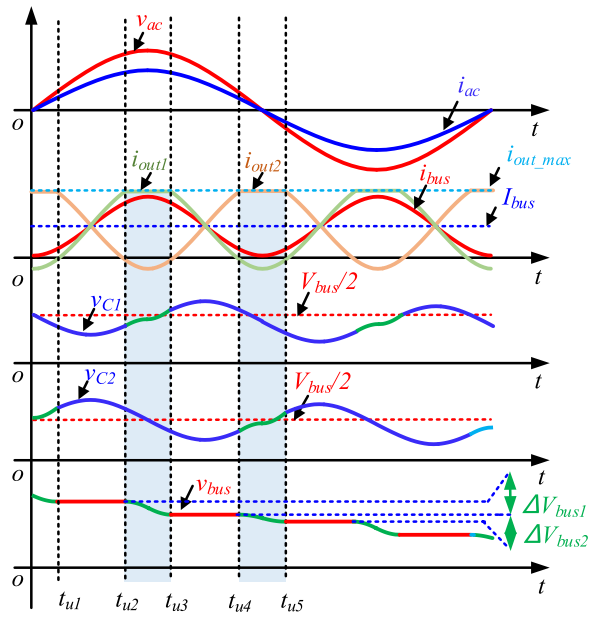

Fig. 9. Key waveforms of IPOS DAB fed VSI under open-loop differentiated-capacitance design ($C_1<C_2$) considering the uncontrollable interval.

Fig. 9 plots the open-loop working waveforms of IPOS DAB fed VSI after considering the uncontrollable interval. As can be seen, $i_{\text{out}1}$ reaches the limitation $I_{\text{out\_max}}$ around the peak of i_{bus}. v_{C1}'s rising rate reduces and cannot follow the falling rate of v_{C2}. After the uncontrollable interval ends in t_{u3}, the dc bus voltage reduces by $\Delta V_{\text{bus}1}$. Around the bottom of i_{bus}, $i_{\text{out}2}$ is also limited, causing a decrease in v_{bus} by $\Delta V_{\text{bus}2}$. Compared with the SHV in the traditional design, $\Delta V_{\text{bus}1}$ and $\Delta V_{\text{bus}2}$ are quite small if the uncontrollable interval is rationally designed, which would be quantitatively analyzed in the next section.

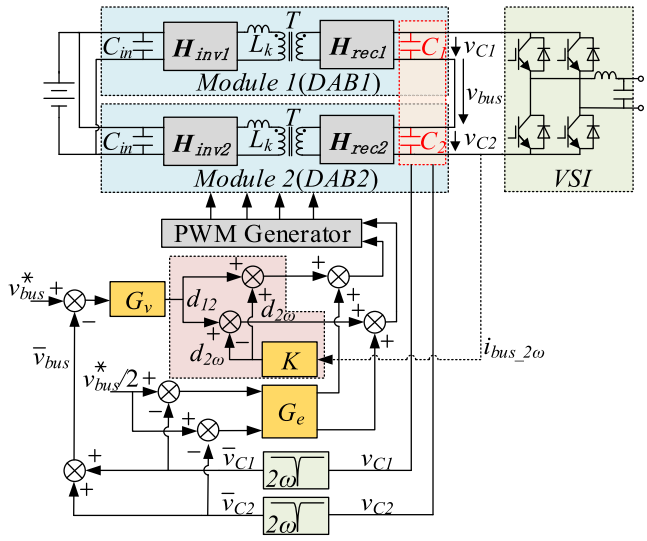

Fig. 10. Diagram of the ripple-complementary controller.

C. Design of Ripple-Complementary Controller

From the above-mentioned analysis, the voltage loop is needed in IPOS DAB to compensate for the decrease $\Delta v_{\rm bus1}$ and $\Delta v_{\rm bus2}$ and stabilize the working point. The control block diagram is shown in Fig. 10. The conventional dual-loop control scheme is used: the outer voltage loop stabilizes the dc component of $v_{\rm bus}$ and the inner voltage balance loop makes the working point of C_1 and C_2 equal. The ripple-complementary algorithm is introduced as a feed-forward item. In order to only regulate the steady-state value without affecting the voltage ripple complementarity, the two-order digital notch filter is implemented after sampling. Hence, $\bar{v}_{C1}$ and $\bar{v}_{C2}$ is free of the second-harmonic component. The proportional-integral (PI) controller G_v corrects the error signal between $v^*_{\rm bus}$ and $\bar{v}_{\rm bus}$ and generates the common dc value d_{12}. The ripple-complementary algorithm injects complementary item $d_{2\omega}$ according to (27). Finally, the voltage-balance loop G_e adds small adjustment Δd_1 and Δd_2 to the controlled quality by compensating the voltage difference between C_1 and C_2. Theoretically, the dc bus voltage ripple can be eliminated in one switching period using the ripple-complementary controller. According to control theory, the feed-forward link does not affect the conventional control loop structure too much [15], so the design step of G_v and G_e is almost identical to the traditional design.

IV. Optimization Scheme of the Main Circuit Parameters

In some high-precision power supplies, the SHV in dc bus can be fully suppressed by designing the IPOS DAB to work in $B \geq 1$. However, the current stress is given priority in general applications whose bus voltage ripple coefficient ($\Delta V_{\rm bus}/V_{\rm bus}$) needs to be within 2%–5%. From the above-mentioned analysis, $\Delta V_{\rm bus}$ is caused by the uncontrollable interval and is related to the main circuit parameters, such as C_1/C_2 and L_k. Due to the approximation of v_{C1} and v_{C2} in (25), the SHC penetrates into the system's input current. The quantitative model of these unexcepted ripples would be established in this section, and an optimal design scheme considering the second-harmonic suppression effect and current stress is proposed.

TABLE I
Slew Rate of v_{C1} and v_{C2} During the Controllable and Uncontrollable Interval

	Controllable interval	*Uncontrollable interval*
$\frac{dv_{C1}}{dt}$	$\frac{2I_{bus}}{(C_1-C_2)cos\theta}cos(2\omega t-\theta)$	$\frac{\left\{\frac{nV_{in}}{8f_sL_k}-I_{bus}\frac{[1-cos(2\omega t-\theta)]}{cos\theta}\right\}}{C_1}$
$\frac{dv_{C2}}{dt}$	$\frac{-2I_{bus}}{(C_1-C_2)cos\theta}cos(2\omega t-\theta)$	$\frac{\left\{\frac{nV_{in}}{8f_sL_k}-I_{bus}\frac{[1-cos(2\omega t-\theta)]}{cos\theta}\right\}}{C_2}$

A. Quantitative Model of the SHV Suppression Effect

Assuming the operating points can be maintained through the ripple-complementary controller, the dc bus voltage ripple is determined by the voltage drop $\Delta V_{\rm bus1}$ and $\Delta V_{\rm bus2}$. From (7), the slew rates of v_{C1} and v_{C2} during the controllable and uncontrollable intervals are summarized in Table I.

1) Calculation of $\Delta V_{\rm bus1}$ During DAB1's Uncontrollable Interval [t_{u2}–t_{u3}]: The slew rate of $v_{\rm bus}$ is equal to the sum of dv_{C1}/dt and dv_{C2}/dt

$$\frac{dv_{\rm bus}}{dt}=\frac{dv_{C1}}{dt}+\frac{dv_{C2}}{dt}=\frac{1}{C_1}\left\{\frac{nV_{\rm in}}{8f_sL_k}-\frac{I_{\rm bus}}{\cos\theta}\left[1+\frac{C_1+C_2}{C_1-C_2}\cos(2\omega t-\theta)\right]\right\}. \tag{34}$$

During the uncontrollable interval, the parameter B meets

$$B=-\left(\frac{i_{\rm out\_max}}{I_{\rm bus}}-1\right)\frac{C_1-C_2}{C_1+C_2}\cos\theta\geq\cos(2\omega t-\theta). \tag{35}$$

Substituting (35) into (34), $dv_{\rm bus}/dt$ is always negative during this interval, which corresponds to the analysis shown in Fig. 9. The reduction of dc bus voltage is the integral of $dv_{\rm bus}/dt$:

$$\Delta V_{\rm bus1}=\int_{t_{u2}}^{t_{u3}}\frac{dv_{\rm bus}}{dt}dt=\frac{1}{\omega C_1}\left[(\pi-\alpha)\left(\frac{nV_{\rm in}}{8f_sL_k}-I_{\rm bus}\right)+I_{\rm bus}\frac{C_1+C_2}{C_1-C_2}\frac{\sin\alpha}{\cos\theta}\right]. \tag{36}$$

2) Calculation of $\Delta V_{\rm bus2}$ During DAB2's Uncontrollable Interval [t_{u4}–t_{u5}]: Following the same steps, the reduction of

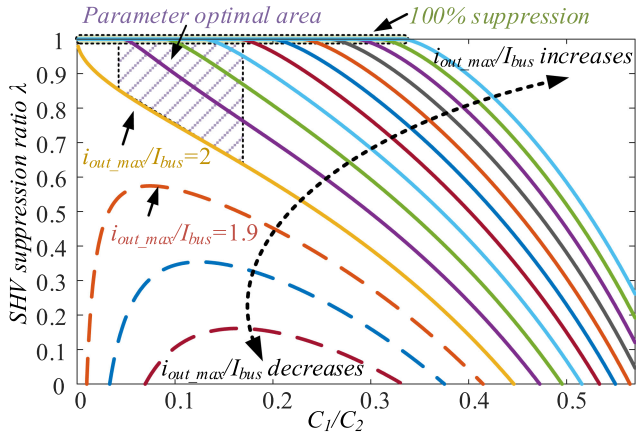

Fig. 11. Relationship curve between SHV suppression ratio λ and $i_{\text{out\_max}}/I_{\text{bus}}$, C_1/C_2.

dc bus voltage during $[t_{u4}$–$t_{u5}]$ can be obtained as follows:

$$\Delta V_{\text{bus2}} = \int_{t_{u4}}^{t_{u5}} \frac{dv_{\text{bus}}}{dt} dt = \frac{1}{\omega C_2}\left[(\pi-\alpha)\left(\frac{nV_{\text{in}}}{8f_sL_k} - I_{\text{bus}}\right) + I_{\text{bus}}\frac{C_1+C_2}{C_1-C_2}\frac{\sin\alpha}{\cos\theta}\right]. \tag{37}$$

The contrast of (36) and (37) shows $\Delta V_{\text{bus2}} = C_1/C_2 \Delta V_{\text{bus1}}$. Therefore, ΔV_{bus2} is smaller than ΔV_{bus1} under $C_2 > C_1$, and the dc bus voltage ripple caused by uncontrollable interval equals ΔV_{bus1}:

$$\Delta V_{\text{bus\_dif}} = \Delta V_{\text{bus1}}. \tag{38}$$

To measure the suppression effect of the proposed method on SHV, the voltage ripple suppression ratio is defined as follows:

$$\lambda = 1 - \frac{|\Delta V_{\text{bus\_dif}}|}{|\Delta V_{\text{bus\_con}}|} \tag{39}$$

where $\Delta V_{\text{bus\_con}}$ is the voltage ripple of traditional design.

Substituting (9) and (38) into (39), λ can be derived as follows:

$$\lambda = 1 - \frac{1+C_1/C_2}{4C_1/C_2}\left[\frac{\pi-\alpha}{\cos\theta}\left(\frac{i_{\text{out\_max}}}{i_{\text{bus}}} - 1\right) - \frac{1+C_1/C_2}{1-C_1/C_2}\sin\alpha\right] \tag{40}$$

where α can be rewritten as follows:

$$\alpha = \arccos\left[\left(\frac{i_{\text{out\_max}}}{I_{\text{bus}}} - 1\right)\cos\theta\frac{C_1/C_2 - 1}{C_1/C_2 + 1}\right].$$

Fig. 11 shows the relationship curves between C_1/C_2, $i_{\text{out\_max}}/I_{\text{bus}}$ and λ. As can be seen, the differentiated-capacitance design with appropriate circuit parameters can suppress SHV greatly. In the design of $i_{\text{out\_max}}/I_{\text{bus}} < 2$, the suppression ratio is up to 60%, but λ is not proportional to C_1/C_2. In the design of $i_{\text{out\_max}}/I_{\text{bus}} \geq 2$, the suppression ratio can be arbitrarily small by reducing C_1/C_2. And complete suppression can be achieved in this case.

B. Quantitative Model of the SHC Suppression Effect

The neglected SHV in (25) multiplies the ripple items in the ripple-complementary algorithm, generating the fourth-harmonic current in dc source. The expression of v_{C1} and v_{C2} can be obtained as (41) in the situation of a small uncontrollable interval

$$\begin{cases} v_{C_1} = \frac{V_{\text{bus}}}{2} - V_{m\_C}\sin(2\omega t - \theta) \\ v_{C_2} = \frac{V_{\text{bus}}}{2} + V_{m\_C}\sin(2\omega t - \theta) \end{cases} \tag{41}$$

where V_{m_C} is the amplitude of capacitors' voltage ripple and can be derived from the integration of dv_{C1}/dt and dv_{C2}/dt shown in the left column of Table I

$$V_{m\_C} = \frac{V_m I_m}{2\omega(C_2 - C_1)V_{\text{bus}}}.$$

Substituting (41) into the input current expression (3), i_{in} can be derived as follows:

$$i_{\text{in}} = \frac{V_{\text{bus}}I_{\text{bus}}}{V_{\text{in}}} + \frac{I^2{}_{\text{bus}}}{V_{\text{in}}\omega\cos^2\theta}\frac{C_1+C_2}{(C_1-C_2)^2}\sin(4\omega t - 2\theta). \tag{42}$$

As seen, the fourth-harmonic current appears. The input current ripple suppression ratio is defined as follows:

$$\varepsilon = 1 - \frac{\Delta i_{\text{in\_dif}}}{\Delta i_{\text{in\_con}}} \tag{43}$$

where $\Delta i_{\text{in\_dif}}$ is the current ripple in the differentiated-capacitance design, and $\Delta i_{\text{in\_con}}$ is the current ripple in traditional design.

According to (10) and (42), ε can be derived as follows:

$$\varepsilon = 1 - \frac{1}{2\cos\theta}\left(\frac{1+C_1/C_2}{1-C_1/C_2}\right)^2. \tag{44}$$

From the above-mentioned equation, ε is only related to C_1/C_2 after the working condition is determined. Fig. 12 shows the relationship curve between ε and C_1/C_2 under the resistive load. The maximum of ε is 0.5, indicating that the input current ripple can be reduced up to 50% of the traditional design. The boundary-value of $\varepsilon > 0$ can be calculated as follows:

$$C_1/C_2 < 0.17. \tag{45}$$

Hence, the main circuit's parameter should meet (45) to get the suppression effect of ripple current.

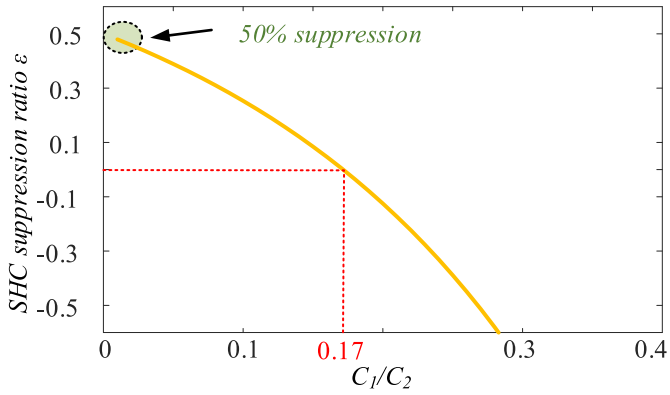

Fig. 12. Relationship curve between SHC suppression ratio ε and C_1/C_2.

C. Parameter Optimization Scheme

From the above-mentioned analysis, the suppression ratio λ and ε are both dependent on the main circuit parameters.

Therefore, a general optimization scheme can be built for the selection of the main circuit parameters C_1/C_2 and L_k.

This scheme should make the best use of the semiconductor's current-carrying capacity to suppress the second harmonic. As can be seen in Fig. 11, the suppression effect close to 100% can be obtained by increasing $i_{\text{out\_max}}$ to slightly more than twice the value of I_{bus}. Therefore, the parameters ought to lie in the upper right of the yellow curve in Fig. 11. Moreover, C_1/C_2 must meet the constraint of (45) for getting a smaller input current ripple. Apart from the low-frequency ripple, the high-frequency switching ripple also needs to be considered, which requires C_1/C_2 not be too small.

Based on the above-mentioned considerations, the parameters' preferred zone is summarized and drawn in Fig. 11 with shadow, which makes a great tradeoff between voltage and current ripple suppression effect and low-frequency and high-frequency ripple suppression effect. Furthermore, the parameters' optimal scheme is designed as follows.

1) First of all, selecting the voltage suppression ratio λ between 70% and 100%.
2) Calculating the sum of dc bus capacitance using the definition of voltage suppression ratio

$$(C_1+C_2)_{\text{con\_min}}=\frac{2MI_m}{\omega\frac{(\Delta V_{\text{bus}})_r}{1-\lambda}} \tag{46}$$

where $(\Delta V_{\text{bus}})_r$ is the amplitude of SHV required by the application.
3) Finding the curve that intersects with the selected λ. The parameter L_k can be obtained using the $i_{\text{out\_max}}/I_{\text{bus}}$ of this curve

$$L_k=\frac{nV_{\text{in}}}{8f_s\left(\frac{i_{\text{out\_max}}}{I_{\text{bus}}}\right)I_{\text{bus}}}. \tag{47}$$

4) The abscissa corresponding to the intersection is the optimal $(C_1/C_2)_o$. C_1 and C_2 can be calculated as follows:

$$\begin{cases} C_1=(C_1+C_2)_{\text{con\_min}}\frac{(C_1/C_2)_o}{1+(C_1/C_2)_o} \\ C_2=(C_1+C_2)_{\text{con\_min}}\frac{1}{1+(C_1/C_2)_o} \end{cases}. \tag{48}$$

5) Taking the optimal parameters into (38) and (42) and calculating the voltage ripple and current ripple. If the design objectives are not met, decrease λ in step (1), and do steps (2)–(4) again.

V. Experiment Verification

A. Prototype Design

To verify the validity of the proposed differentiated-capacitance design, a 625-W IPOS DAB fed VSI prototype is built in the lab, as shown in Fig. 13. The design procedure of the main circuit parameters would be conducted based on the proposed parameter optimal scheme. The design objective is shown in Table II. As can be seen, the required dc bus voltage ripple coefficient $(\Delta V_{\text{bus}}/V_{\text{bus}})_r$ is extremely small (2%) to prove the second-harmonic suppression capability of the differentiated-capacitance design.

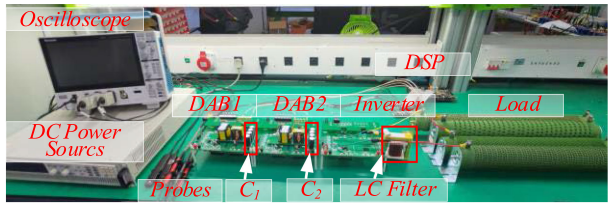

Fig. 13. Experimental setup of the IPOS DAB fed VSI.

TABLE II
Design Objective of the Prototype

Parameter	*Meaning*	*Value*
p_{ac}	rated power	625W
V_{in}	input voltage	125V
V_{bus}	dc bus voltage	250V
v_{ac}	output voltage	200Vp
n	turns ratio	1:1
f_s	switching frequency	50kHz
$(\Delta V_{bus}/V_{bus})_r$	ripple coefficient	2%

1) Selecting the SHV suppression ratio $\lambda=0.85$, which means that the SHV in the differentiated-capacitance design can be reduced to 15% of the traditional design theoretically.
2) Calculating the minimum dc bus capacitance according to the required ripple coefficient

$$(C_1+C_2)_{\text{con\_min}}=\frac{2MI_m}{\omega\frac{1}{1-\lambda}\left(\frac{\Delta V_{\text{bus}}}{V_{\text{bus}}}\right)_r V_{\text{bus}}}\approx 1000\,\mu\text{F}. \tag{49}$$

3) From Fig. 11, the curves that can intersect with $\lambda=0.85$ in the parameter preferred zone should have $2<i_{\text{out\_max}}/I_{\text{bus}}<2.12$. Selecting $i_{\text{out\_max}}/I_{\text{bus}}$ as 2.08, and calculating the main circuit parameter L_k

$$L_k=\frac{nV_{\text{in}}}{8f_s\left(\frac{i_{\text{out\_max}}}{I_{\text{bus}}}\right)I_{\text{bus}}}\approx 60\,\mu\text{H}. \tag{50}$$

From (48), the main circuit parameters C_1 and C_2 can be calculated as follows:

$$\begin{cases} C_1=(C_1+C_2)_{\text{con\_min}}\frac{(C_1/C_2)_o}{1+(C_1/C_2)_o}\approx 100\,\mu\text{F} \\ C_2=(C_1+C_2)_{\text{con\_min}}\frac{1}{1+(C_1/C_2)_o}\approx 900\,\mu\text{F} \end{cases}. \tag{51}$$

4) Taking the design result L_k, C_1, and C_2 into (38), the theoretical result of ripple coefficient is $\Delta V_{\text{bus}}/V_{\text{bus}}=1.84\%$. These optimal parameters can meet the design objective with a little margin.

B. Experimental Results

The experimental waveforms for the IPOS DAB fed VSI under differentiated-capacitance design ($C_1=100\ \mu$F and $C_2=900\ \mu$F) is shown in Fig. 14. It can be seen that the voltage ripple in v_{C1} and v_{C2} is 21.6 V, which is consistent with the

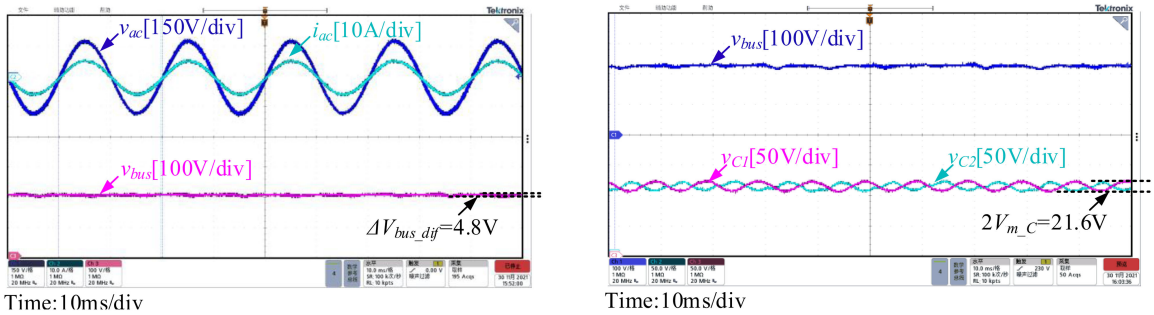

Fig. 14. Experimental waveforms for the IPOS DAB fed VSI of the differentiated-capacitance design ($C_1 = 100\ \mu$F and $C_2 = 900\ \mu$F). (a) ac voltage $v_{\rm ac}$, ac current $i_{\rm ac}$, and dc bus voltage $v_{\rm bus}$. (b) dc bus voltage $v_{\rm bus}$ and capacitor voltages v_{C1} and v_{C2}.

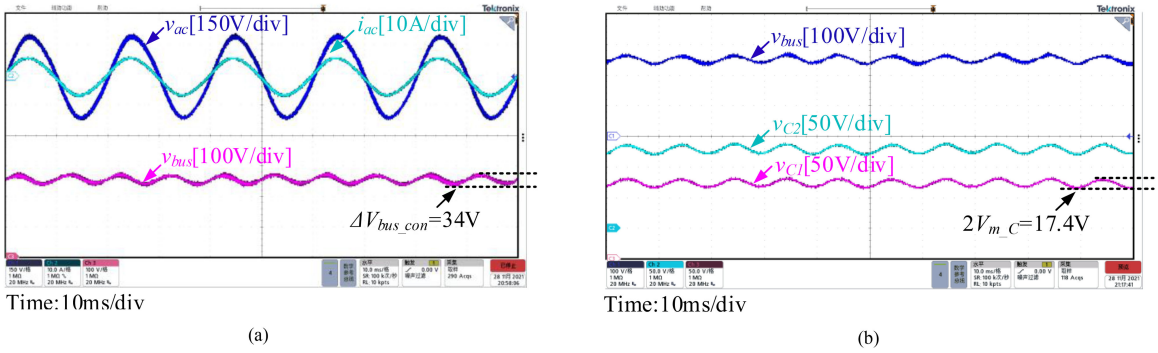

Fig. 15. Experimental waveforms for the IPOS DAB fed VSI of the traditional design ($C_1 = 500\ \mu$F, $C_2 = 500\ \mu$F). (a) ac voltage $v_{\rm ac}$, ac current $i_{\rm ac}$, and dc bus voltage $v_{\rm bus}$. (b) dc bus voltage $v_{\rm bus}$ and capacitor voltages v_{C1} and v_{C2}.

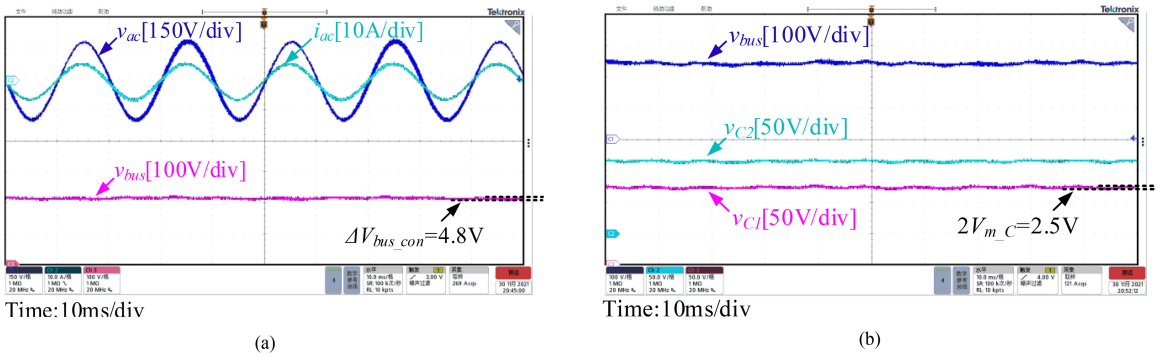

Fig. 16. Experimental waveforms for the IPOS DAB fed VSI of the traditional design ($C_1 = 3500\ \mu$F and $C_2 = 3500\ \mu$F). (a) ac voltage $v_{\rm ac}$, ac current $i_{\rm ac}$, and dc bus voltage $v_{\rm bus}$. (b) dc bus voltage $v_{\rm bus}$ and capacitor voltages v_{C1} and v_{C2}.

result (19.89 V) calculated from (41). The voltage ripple is complementary except for the uncontrollable interval, indicating that the ripple-complementary algorithm works well. The SHV in dc bus is 4.8 V and satisfies the design objective (5 V). The quality of VSI's output voltage is great, and the total harmonic distortion (THD) of it is only 1.8%. The results have proved the validity of the proposed parameter optimal scheme.

For comparison, the experimental waveforms for the IPOS DAB fed VSI under the traditional design ($C_1 = 500\ \mu$F and $C_2 = 500\ \mu$F) are shown in Fig. 15. The SHV in dc bus increases to 34 V, which is seven times larger than the differentiated-capacitance design. At the same time, the THD of $v_{\rm ac}$ increases to 6.3%. In fact, there is a positive correlation between the output distortion of VSI and the dc bus SHV, so the THD in traditional design ought to be higher than in the proposed method.

Fig. 16 shows the experimental waveforms for the IPOS DAB fed VSI under the traditional design ($C_1 = 3500\ \mu$F and $C_2 = 3500\ \mu$F) with the same SHV (4.8 V) as the differentiated-capacitance design. The dc bus capacitance requirement increases to 7 mF. Hence, larger capacitors are required in the

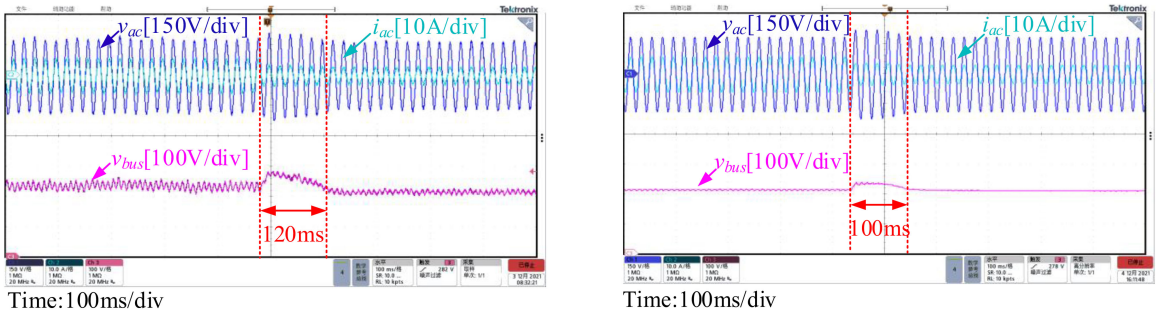

Fig. 17. Dynamic waveforms for the IPOS DAB fed VSI of the traditional design ($C_1 = 500\ \mu$F and $C_2 = 500\ \mu$F) and the differentiated-capacitance design ($C_1 = 100\ \mu$F and $C_2 = 900\ \mu$F) under the load step change from 32 (full load) to 64 Ω (50% load). (a) ac voltage $v_{\rm ac}$, ac current $i_{\rm ac}$, and dc bus voltage $v_{\rm bus}$ in the traditional design. (b) ac voltage $v_{\rm ac}$, ac current $i_{\rm ac}$, and dc bus voltage $v_{\rm bus}$ in the differentiated-capacitance design.

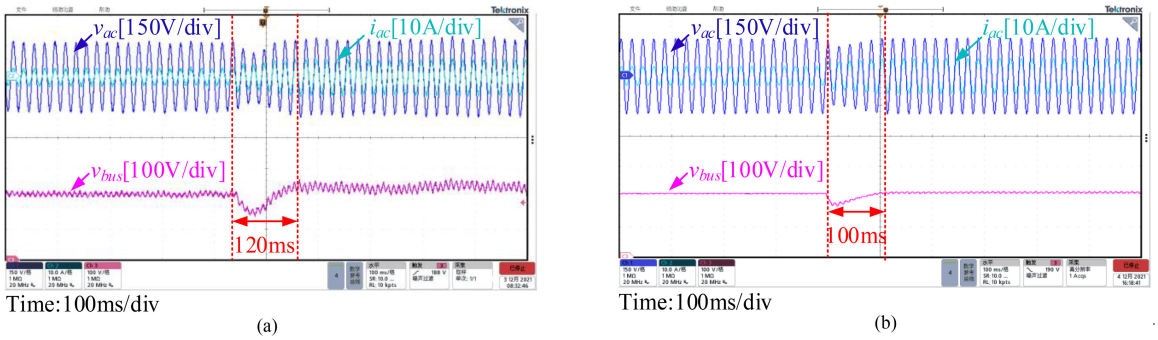

Fig. 18. Dynamic waveforms for the IPOS DAB fed VSI of the traditional design ($C_1 = 500\ \mu$F and $C_2 = 500\ \mu$F) and the differentiated-capacitance design ($C_1 = 100\ \mu$F and $C_2 = 900\ \mu$F) under the load step change from 64 (50% load) to 32 Ω (full load). (a) ac voltage $v_{\rm ac}$, ac current $i_{\rm ac}$, and dc bus voltage $v_{\rm bus}$ in the traditional design. (b) ac voltage $v_{\rm ac}$, ac current $i_{\rm ac}$, and dc bus voltage $v_{\rm bus}$ in the differentiated-capacitance design.

traditional design to achieve low voltage ripple in dc bus. In addition, although the high-density E-Caps are used at the expense of lifespan, the decoupling circuit's volume is still 1.4 times larger than the proposed method.

Fig. 17 shows the dynamic waveforms for IPOS DAB fed VSI under the traditional design and the differentiated-capacitance design when the load is step changed from 32 (full load) to 64 Ω (50% load). Fig. 18 shows the dynamic waveforms when the load is step changed from 64 (50% load) to 32 Ω (full load). As seen, the SHV in dc bus is greatly suppressed under different loads, and the dynamic response time of the proposed strategy is almost the same as the traditional design, indicating that the ripple-complementary strategy does not affect the traditional control loop structure too much as mentioned above.

Fig. 19 presents the spectrums of two-stage inverter's input current $i_{\rm in}$ under the differentiated-capacitance design ($C_1 = 100\ \mu$F and $C_2 = 900\ \mu$F) and the traditional design ($C_1 = 500\ \mu$F, $C_2 = 500\ \mu$F). After the proposed method is adopted, the SHC in $i_{\rm in}$ reduces to 13.67%, and there is an eightfold increase in the fourth-harmonic current, which is consistent with the theoretical analysis. Considering the output resistance of the dc source, the harmonic current propagating into the source is derived as (52). To make the source's harmonic current equal, the input capacitance needed by the traditional design is 1.6 times larger than the proposed method, which demonstrates the advantages

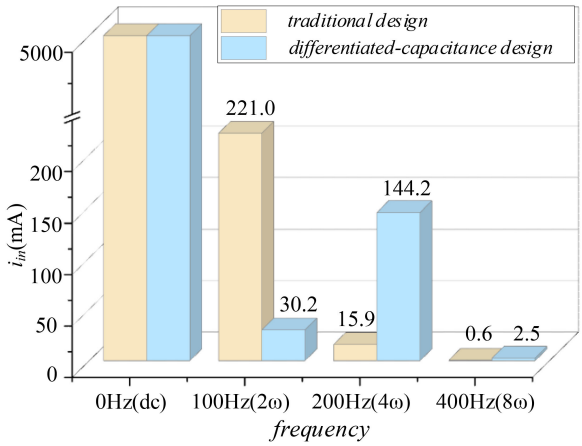

Fig. 19. Spectrums of input current with the traditional design ($C_1 = 500\ \mu$F and $C_2 = 500\ \mu$F) and the differentiated-capacitance design ($C_1 = 100\ \mu$F and $C_2 = 900\ \mu$F).

of differentiated-capacitance design again

$$|i_{s\_k\omega}| = \frac{1}{\sqrt{1 + (k\omega)^2 R^2 {C_{\rm in}}^2}} |i_{\rm in\_k\omega}|. \tag{52}$$

TABLE III
PERFORMANCE COMPARISON OF SOME COMMON POWER DECOUPLING METHODS

Methods	*L-C filter [22]*	*Buck [27]*	*Half-bridge [29]*	*Full-bridge [32]*	*Proposed method*
Fundamental frequency f_0	50Hz	50Hz	60Hz	50Hz	50Hz
Rated power P_0	2.5kW	1kW	1kW	600W	625W
DC bus capacitor C/ Operating voltage V	200μF/400V	50μF/380V	45μF/380V 45μF/380V	220μF/450V	100μF/125V 900μF/125V
Decoupling capacitor C/ Operating voltage V	1400μF/400V 1.81mH/6.25A	100μF/360V	180μF/380V	1000μF/50V	0
Efficiency loss	0.3%	1.2%	2.3%	2.6% (estimate)	1.4%
Additional cost	Capacitor+ 1 inductor	Capacitor+2 switches+ 1 inductor	Capacitor+2 switches+ 1 inductor	Capacitor+4 switches+ 1 inductor	0
$\frac{f_0 \sum (CV^2+LI^2)}{P_o}$	80.43	6.34	5.89	14.78	7.85 (adjustable)

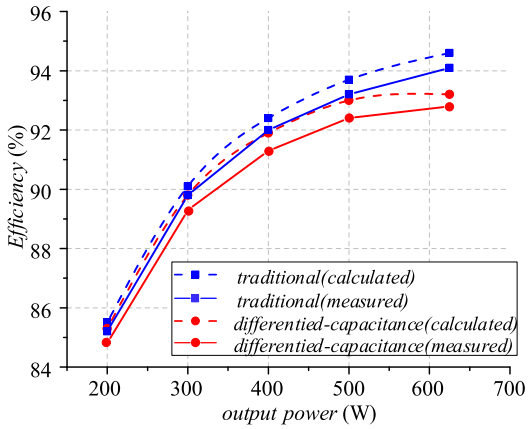

Fig. 20. Calculated and measured efficiency of the IPOS DAB fed VSI with the traditional design ($C_1 = 500\ \mu$F and $C_2 = 500\ \mu$F) and the differentiated-capacitance design ($C_1 = 100\ \mu$F and $C_2 = 900\ \mu$F).

The system efficiencies of the proposed and traditional designs are calculated based on the methods proposed in [2] and [3] considering the conduction loss, turn-OFF loss, transformer loss and inductor loss. The calculated result is shown in Fig. 20 with dashed lines. After the differentiated-capacitance method is adopted, the peak efficiency reduces by 1.4% due to the increase in component's current stress caused by the modified pulsating output current of DAB modules. The experimental efficiencies of the proposed and traditional designs are shown in Fig. 20 with solid lines. The peak efficiency of the differentiated-capacitance method is 92.8%. The difference with calculated results is mainly due to the assumption of small turn-ON loss in the non-ZVS interval.

C. Comparison With Existing Methods

To further demonstrate the effectiveness of the proposed method, the performance of the differentiated-capacitance design is compared with the passive method using an *L–C* resonant filter [22] and the active methods using an additional power semiconductor circuit [27], [29], [32] in component volume, cost, and efficiency loss. Considering the different roles and working conditions of the decoupling components in these methods, the volume is compared through the following ratio [29]:

$$\frac{f_0 \sum CV_{\rm dc}^2 + LI_{\rm dc}^2}{P_o} \tag{53}$$

where $V_{\rm dc}$ is the operating voltage of capacitors and $I_{\rm dc}$ is the operating current of inductors, P_o is the rated power, and f_0 is the fundamental line frequency. In fact, this ratio represents the total energy storage requirement in the whole system and gives a great view of the decoupling components' volume.

It should be noted that the proposed method utilizes the DABs' output capacitors to compensate the low-frequency ripple power without any other decoupling components. But for the SHCC and SHVC, the dc bus capacitors are still needed to ensure the normal operation of the main circuit after the decoupling circuit is used. Hence, the dc bus capacitors and decoupling capacitors are both considered in this comparison as shown in Table III. The total capacitance needed by the proposed method seems to be slightly larger than the methods proposed in [27] and [29], but it can be adjusted by the selected suppression ratio in as (46). The closer λ gets to 1, the smaller dc bus capacitance can be obtained, which gives designers the freedom to make tradeoff according to their applications. Compared with other methods, the main contribution of the proposed method is providing an original idea to compensate the instantaneous power without any additional components and minimizes the efficiency effect to original circuit.

VI. CONCLUSION

The pulsating instantaneous output power of the two-stage single-phase inverter leads to the SHV in dc bus, and the bulky short-life electrolytic capacitors are needed to stabilize the dc bus voltage in the traditional design. This article presents an IPOS DAB under the differentiated-capacitance design as the front-end dc–dc stage to decouple the pulsating power. The

ripple-complementary algorithm and controller are derived from the small-signal model of IPOS DAB fed VSI, which injects the second-harmonic component into the traditional control algorithm as a feed-forward item. For the uncontrollable interval existing in this algorithm, the physical mechanism and quantitative analysis are conducted. Furthermore, the suppression effect of SHV and SHC is calculated, based on which, the preferred zone and optimization scheme of the main circuit parameters are designed. A 625-W IPOS DAB fed VSI design example is presented. The experimental results show that the capacitance requirements can be reduced at least seven times without any additional components, which is meaningful to achieve E-Cap free in the two-stage inverter system.

The differentiated-capacitance design method can also be extended to other modular dc–dc converters whose dc bus capacitors are connected in series. In fact, after changing the IPOS structure to ISOP, this method is still effective to absorb the pulsating power generated by the front-end rectifier, which will be studied in future research work.

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