Gate Capacitance Characterization of Silicon Carbide and Silicon Power MOSFETs Revisited

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***Abstract*—Capacitance–voltage (C–V) gate characteristics of power metal-oxide-semiconductor field-effect transistors (MOSFETs) play an important role in the dynamic device performance. C–V characterization of the MOSFET gate structure is a necessary step for evaluating the MOSFET switching behavior and calibrating lumped equivalent capacitances of MOSFET compact models. This article presents a comprehensive analysis on gate C–V measurements of silicon (Si) and silicon carbide (SiC) power MOSFETs leading to clear measurement guidelines. The requirements on the measurement setup, the selection of equivalent models used for the MOSFET capacitance extraction, and the measurement frequency range are defined and supported by an accurate C–V characterization of several Si- and SiC power MOSFETs. The results show that the gate-source and gate-drain capacitances should be extracted at a frequency of some 10 kHz rather than at 1 MHz, as typically adopted in datasheets, to avoid parasitic effects introduced by the measurement setup and package. Furthermore, analytical expressions for C_{dg} and C_{sg} were derived based on a lumped equivalent circuit, which explain the influence of the measurement setup and the package parasitics on the C–V measurements. Nonideal measurement conditions are identified and correlated to the differences in C–V extraction with either parallel or series-equivalent model. A new method is proposed to estimate the ratio of the MOSFET's ON-state resistance components R_{ch} and R_{drift} based on the presented C–V measurement guidelines, which are applicable to all three- and four-terminal power MOSFETs.**

***Index Terms*—Commercial off-the-shelf devices (COTS), gate-drain capacitance, gate-source capacitance, input capacitance, internal gate resistance, ON-state resistance, power MOSFET, silicon, silicon carbide.**

I. Introduction

POWER metal-oxide-semiconductor field-effect transistors (MOSFETs) have been used for many years as active switch for various power converter topologies. Today, state-of-the-art silicon carbide (SiC) power MOSFETs are gradually replacing silicon (Si) insulated-gate bipolar transistors (IGBTs) in medium- to high-voltage and high-temperature power electronic applications [1]–[3]. Current–voltage (I–V) and capacitance-voltage (C–V) characteristics of power MOSFETs are important for evaluating their electrical performances, optimizing fabrication processes, improving device design, and calibrating compact device models [4]. Accurate device models are a valuable tool for predicting device switching dynamics, power losses, and electromagnetic interference noise generation in a computationally efficient and accurate way [5], [6]. Compact models based on the equivalent circuit shown in Fig. 1 have successfully been used for modeling both dynamic and static behavior of power MOSFETs [7]. A compact model describes the power MOSFET's macroscopic I–V characteristics, C–V characteristics, and thermal behavior. The output (C_{oss}), input (C_{iss}), and reverse transfer (C_{rss}) capacitance as function of the drain–source voltage (V_{ds}) for zero gate-source voltage (V_{gs}) can be measured on standard impedance analyzers and are specified in the datasheet of the respective device. The lumped equivalent interterminal capacitances, C_{gs}, C_{gd}, and C_{ds}, of compact models are then typically derived from measured C_{oss}, C_{iss}, and C_{rss} characteristics, as $C_{oss} = C_{gd} + C_{ds}$, $C_{iss} = C_{gd} + C_{gs}$, and $C_{gd} = C_{rss}$.

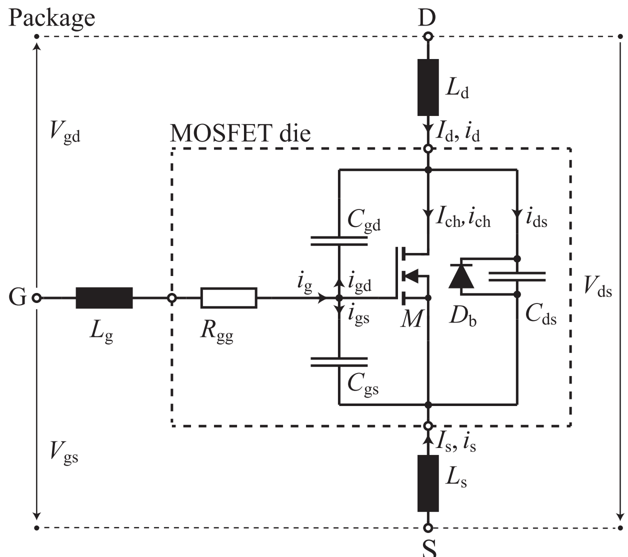

Fig. 1. Electrical equivalent circuit of a power MOSFET.

The importance of considering that the MOSFET C–V characteristics depend on both V_{ds} and V_{gs} for modeling was reported in [5], [8]–[11], showing that the capacitance trajectories during turn-ON and turn-OFF transients differ from the C–V curves derived dependent on V_{ds} only. Accordingly, the

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C–V characterization of power MOSFETs goes beyond the measurements of $C_{\rm oss}(V_{\rm ds})$, $C_{\rm iss}(V_{\rm ds})$, and $C_{\rm rss}(V_{\rm ds})$ at $V_{\rm gs} = 0$. Since power MOSFETs are controlled by $V_{\rm gs}$, the $V_{\rm gs}$ dependence of $C_{\rm gs}$ and $C_{\rm gd}$ should be evaluated in addition to their $V_{\rm ds}$ dependence. The $V_{\rm gs}$-dependent characteristics of $C_{\rm gs}$ and $C_{\rm gd}$ at $V_{\rm ds} = 0$ V, used in compact models as shown in, e.g., [4], [12]–[16], are often not consistent in the full range of $V_{\rm gs}$ with the relation $C_{\rm iss} = C_{\rm gs} + C_{\rm gd}$ resulting from the lumped electrical equivalent circuit of a power MOSFET depicted in Fig. 1. As consequence, $C_{\rm gs}$ and $C_{\rm gd}$ are modeled incorrectly, which leads to inaccurate simulations of switching transients.

A sophisticated measurement setup for C–V characterization of high-voltage power devices beyond datasheets was shown in [17]. The accuracy of the proposed measurement setup was assessed by capacitance measurements of three test capacitors connected in the same delta configuration as the voltage-dependent MOSFET interterminal capacitances, $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$. However, such a measurement setup only imitates the MOSFET equivalent circuit in the OFF-state, i.e., at $V_{\rm gs}$ below the threshold voltage ($V_{\rm th}$). Additionally, the C–V measurements were shown only for Si-IGBTs. The difference between Si and SiC power MOSFETs with respect $C_{\rm gd}(V_{\rm gs})$ and $C_{\rm gs}(V_{\rm gs})$ was explained in [18]; however, neither the measurement setup nor the devices under test were shown. Namely, for a strong channel inversion, i.e., $V_{\rm gs} \gg V_{\rm th}$, $C_{\rm gd}$ of SiC power MOSFETs is in the range of $C_{\rm gs}$, while for Si power MOSFETs, $C_{\rm gs} \gg C_{\rm gd}$. As a consequence, $C_{\rm gs}$ and $C_{\rm gd}$ measurements of SiC power MOSFETs are more sensitive to gate current sharing between the source and the drain current paths in the $V_{\rm gs}$ measurement range and it has to be ensured that a measurement setup does not affect this current sharing.

Accordingly, this article focuses on the characterization of $C_{\rm iss}(V_{\rm gs})$, $C_{\rm gs}(V_{\rm gs})$, and $C_{\rm gd}(V_{\rm gs})$ in the range of $(V_{\rm gs,off}, V_{\rm gs,on})$, where $V_{\rm gs,off}$ and $V_{\rm gs,on}$ are the maximum recommended turn-OFF and turn-ON gate-source control voltages. This is of high importance for emerging SiC power MOSFETs with respect to 1) designing the gate circuit [12], [19], 2) evaluating gate bias instability [20], 3) extracting electrically active traps and defects at the MOS interface [21]–[23], and 4) parametrization of compact device models by including $V_{\rm gs}$-dependent capacitance models, as suggested in [4], [5], [14], [15], [24].

The article is organized as follows. In Section II, a theoretical background of the commonly used relationship between $C_{\rm iss}$, $C_{\rm gs}$, and $C_{\rm gd}$ is given and the $V_{\rm gs}$ dependence of $C_{\rm iss}$, $C_{\rm gs}$, and $C_{\rm gd}$ is briefly explained starting from the lumped equivalent circuit of a power MOSFET. In Section III, the requirements on the measurement setup for accurate C–V characterization are described. An analytical description of $C_{\rm gd}$ and $C_{\rm gs}$ as function of the circuit parameters of the equivalent power MOSFET model is derived in Section V. Furthermore, based on this analytical model, a new method is proposed for extracting the ratio ($R_{\rm ch}/R_{\rm drift}$) between the MOSFET's ON-state resistance ($R_{\rm ds,on}$) components, $R_{\rm ch}$ and $R_{\rm drift}$, based on the measurements of $C_{\rm gd}$ and $C_{\rm gs}$. In Section IV, the C–V measurement results of commercial off-the-shelf (COTS) Si and SiC power MOSFETs are analyzed showing the differences between Si and SiC power MOSFETs. Section VI addresses the selection of appropriate measurement instruments and a correct connection of the MOSFET to the test fixture for accurate characterization of interterminal gate capacitances. Finally, Section VII concludes this article.

II. Power MOSFET Lumped Equivalent Model

A. *Power MOSFET Capacitance Relations*

The gate, drain, and source terminals of a packaged power MOSFET are denoted by G, D, and S, respectively, in the equivalent circuit shown in Fig. 1. DC bias voltages ($V_{\rm ds}, V_{\rm gs}$) and the drain, source conduction currents ($I_{\rm d}, I_{\rm s}$) are represented by capital, whereas time-dependent small-signal voltages ($v_{\rm d}$, $v_{\rm s}$, and $v_{\rm g}$) and charging currents ($i_{\rm d}$, $i_{\rm s}$, and $i_{\rm g}$) are denoted by lowercase symbols. The MOSFET symbol (M) represents the voltage-controlled current source. The diode ($D_{\rm b}$) models the MOSFET's internal body-diode. The lumped resistors $R_{\rm gg}$ represent the resistance of the MOSFET's distributed gate, whereas $L_{\rm g}, L_{\rm d}$, and $L_{\rm s}$ represent a simplified model of the package parasitic stray inductances [6]. The capacitors $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ are defined according to

$$C_{\rm ij} = \frac{\partial q_{\rm i}}{\partial v_{\rm j}}|_{\rm i=j} \tag{1a}$$

$$C_{\rm ij} = -\frac{\partial q_{\rm i}}{\partial v_{\rm j}}|_{\rm i\neq j} \tag{1b}$$

where a capacitor $C_{\rm ij}$ between the terminals drain, gate, and source, i.e., $i, j \in \{\rm d, g, s\}$, defines the change of charge $\partial q_{\rm i}$ at terminal *i*, induced by a change of potential $\partial v_{\rm j}$ at terminal *j*. $C_{\rm ij}$ with $i = j$ are denoted as terminal capacitances (self-capacitance) and $C_{\rm ij}$ with $i \neq j$ as interterminal capacitances (trans-capacitances). For the extraction of the equivalent lumped interterminal capacitances used in power MOSFET compact models, typically their reciprocity, $C_{\rm ds} = C_{\rm sd}$, $C_{\rm gd} = C_{\rm dg}$, and $C_{\rm gs} = C_{\rm sg}$ [25]–[27], has been assumed. Based on (1a) and (1b), reciprocity, and the Kirchhoff's system of equations for the power MOSFET equivalent circuit shown in Fig. 1, the relationship between $C_{\rm ij}$, $i, j \in \{\rm d, g, s\}$, $C_{\rm oss}$, $C_{\rm iss}$, and $C_{\rm rss}$ can be derived [25], [27] as

$$C_{\rm oss} = C_{\rm dd} = C_{\rm gd} + C_{\rm ds} \tag{2}$$

$$C_{\rm iss} = C_{\rm gg} = C_{\rm gs} + C_{\rm gd} \tag{3}$$

$$C_{\rm rss} = C_{\rm gd}. \tag{4}$$

This article focuses on gate capacitance characterization based on relation (3) as function of $V_{\rm gs} = V_{\rm gd}$. Thus, the notation $C_{\rm gg}$ is used instead of $C_{\rm iss}$ and the interterminal gate capacitances are denoted as drain-gate ($C_{\rm dg}$) and source-gate ($C_{\rm sg}$) according to (1b), as will be explained in more detail in Section III.

B. *V_{gs} Dependence of Power MOSFET Capacitances*

A power MOSFET turns ON or OFF by applying a gate-source voltage $V_{\rm gs}$ above or below $V_{\rm th}$, which in turn controls the charge carrier distribution at the oxide–semiconductor interface [28]. The channel of the power MOSFET is closed for $V_{\rm gs} < V_{\rm th}$ and opened for $V_{\rm gs} \geq V_{\rm th}$. The equivalent electric circuits of turned-OFF and turned-ON power MOSFETs are illustrated in Fig. 2(a) and (c), using a schematic for a half-cell structure of a vertical

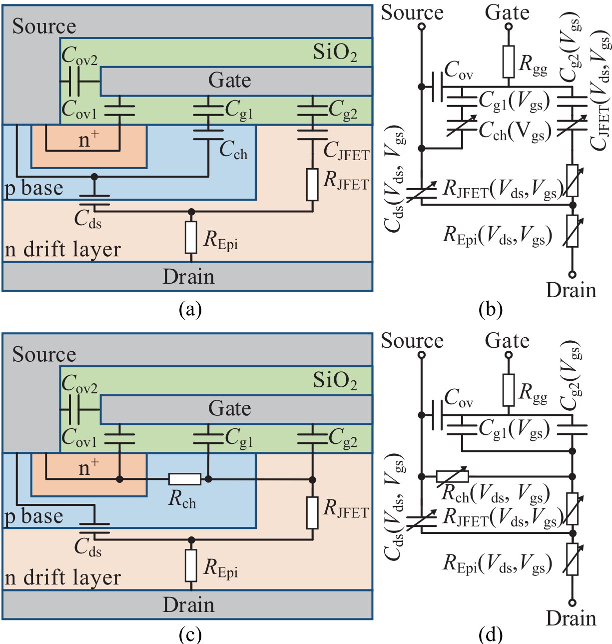

Fig. 2. Simplified electrical equivalent circuit of a vertical double-diffused power MOSFET half-cell structure for (a) a closed channel ($V_{gs} < V_{th}$), and (c) open channel ($V_{gs} \gg V_{th}$). The corresponding small-signal equivalent circuits (b) and (d) indicate the voltage dependencies of the capacitances and resistances.

double-diffused power MOSFET. The corresponding small-signal equivalent circuits of Fig. 2(a) and (c) are given in Fig. 2(b) and (d), indicating the voltage dependencies of the capacitances and resistances. In Fig. 2(a), the gate capacitance is split into the overlap capacitance C_{ov2} between the gate and the source metallization, C_{ov1} between the gate and the n$^+$ contact, $C_{\text{g1}}(V_{\text{gs}})$ in series to $C_{\text{ch}}(V_{\text{gs}})$ of the MOSFET channel, and $C_{\text{g2}}(V_{\text{gs}})$ connected to the JFET depletion capacitance $C_{\text{JFET}}(V_{\text{ds}}, V_{\text{gs}})$. Based on (3), the input capacitance C_{gg} is divided into C_{sg} composed of the sum of $C_{\text{ov}} = C_{\text{ov1}}+C_{\text{ov2}}$ and C_{g1} in series to C_{ch}, whereas C_{dg} consists of the series connection of C_{g2} and C_{JFET}. C_{ds} depicts the junction capacitance between the p base and the n drift layer, whereas $R_{\text{Epi}}(V_{\text{ds}}, V_{\text{gs}})$ and $R_{\text{JFET}}(V_{\text{ds}}, V_{\text{gs}})$ model the resistance of the epitaxial- (Epi-) and JFET-layer, respectively. This epitaxial layer is especially characteristic for SiC devices, where a low-doped high-quality crystalline layer is grown on a higher doped substrate. The sum of $R_{\text{JFET}} + R_{\text{Epi}}$ is denoted here for further use as drift resistance

$$R_{\text{drift}} = R_{\text{JFET}} + R_{\text{Epi}}. \tag{5}$$

The resistance of the n$^+$ substrate is accounted in R_{Epi}. The small resistances of the n$^+$ source and package electrodes are neglected, as well as the resistance of the p base.

By applying $V_{\text{gs}} \geq V_{\text{th}}$, the depletion capacitance C_{ch} in Fig. 2(a) changes into an inversion layer resistance $R_{\text{ch}}(V_{\text{ds}}, V_{\text{gs}})$ in Fig. 2(c), forming a channel between the n$^+$ contact and the JFET region. A current conducting path between the drain and source contacts is formed by R_{ch} in series with R_{drift}. At $V_{\text{gs}} > V_{\text{th}}$ and $V_{\text{ds}} = 0$ V, C_{JFET} is the accumulation capacitance in the JFET region, which is much larger than the oxide capacitance C_{g2}, and, therefore, can be neglected for the following discussion.

III. Small-Signal Gate Characterization Methodology

Characterization of voltage-dependent MOSFET capacitances is typically performed by two measurement methods. The first method, referred to as ramp rate technique in [29], is based on voltage ramp measurements in the time-domain, where the capacitance is extracted as $C = \frac{I}{dV/dt}$. The main challenge of ramp rate measurements is to keep the dV/dt relatively low to minimize transient effects and, at the same time, avoid pronounced self-heating. Accordingly, the circuit layout of the measurement setup can have a significant impact on the C–V extraction.

The second approach is based on small-signal measurements [30] in the frequency domain (ω), where C is extracted either from the complex impedance $\bar{Z}$ by using polar coordinates (mag$(\bar{Z}) = |\bar{Z}|$, phase $(\bar{Z}) = \varphi(\bar{Z})$) as

$$C_{\text{s}} = \frac{-1}{\Im\{\bar{Z}\}\omega} = \frac{-1}{\omega|\bar{Z}|\sin(\varphi(\bar{Z}))} \tag{6}$$

using a series-equivalent model $C_{\text{s}} - R_{\text{s}}$, or from the complex admittance $\bar{Y}$ as

$$C_{\text{p}} = \frac{\Im\{\bar{Y}\}}{\omega} = \frac{-\sin(\varphi(\bar{Z}))}{\omega|\bar{Z}|} \tag{7}$$

using a parallel-equivalent model $C_{\text{p}}||G_{\text{p}}$. From (6) and (7), the relation between C_{s} and C_{p} is found to be

$$C_{\text{s}}\sin^2(\varphi(\bar{Z})) = C_{\text{p}}. \tag{8}$$

Equation (8) shows that the difference between C_{s} and C_{p} is solely caused by $\varphi(\bar{Z})$, i.e., by $\sin^2(\varphi(\bar{Z}))$.

Small-signal measurements are typically performed on standard impedance analyzers selecting a low dc bias sweep rate to accurately extract C–V characteristics. Moreover, to perform C–V measurements during the MOSFET's ON state as function of both V_{ds} and V_{gs}, external bias-Ts have to be added to the MOSFET's terminals [31], [32]. There, a trade-off between the small-signal measurement frequency and self-heating effects has to be considered [5].

To avoid the side effects of auxiliary measurement components (e.g., bias-Ts), the C–V characterization in this work is performed based on the small-signal method as function of V_{gs} at $V_{\text{ds}} = 0$ V, using a Keysight E4990A impedance analyzer. The Keysight E4990A is based on an autobalancing bridge measurement technique. It has a bias range of $\pm$40 V/$\pm$20 mA or $\pm$25 V/$\pm$100 mA and a frequency range of 20 Hz to 120 MHz. The test fixture Keysight 16047E rated for a maximum frequency range of 120 MHz is used to mount the *DUTs*. All *DUTs* are packaged in a TO-247 3-pin package. The 16047E allows the measurements of 3-, or 4-pin packaged power MOSFETs, which must be connected to its high-side (AC$^+$), low-side (AC$^-$), and guard (ACG) electrodes, respectively, as illustrated in Fig. 3. The advantage of the autobalancing bridge technique is that the current i_{ac} on the the low-side AC$^-$ is measured in the negative

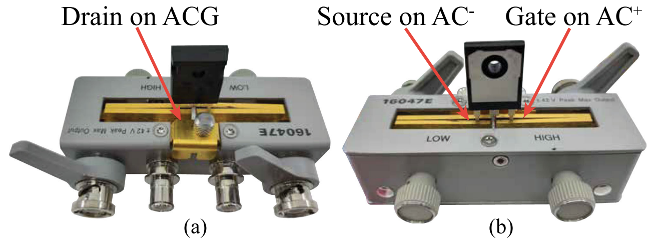

Fig. 3. Picture of the Keysight fixture 16047E, on which a *DUT* is mounted for a C_{sg} measurement. (a) Connection of the drain terminal to ACG at the back. (b) Gate and source terminals connected to AC⁺, AC⁻, respectively.

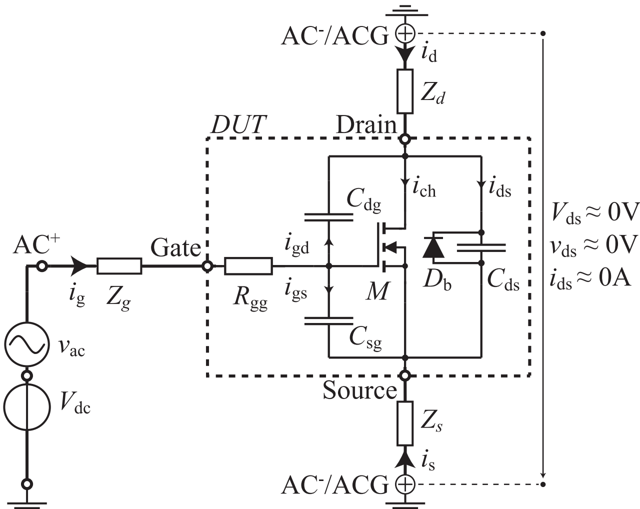

Fig. 4. Electrical equivalent circuit of the gate capacitance small-signal setup, which is used for the characterization of the input capacitance C_{gg}, the internal gate resistance R_{gg}, and the interterminal capacitances $C_{\mathrm{dg}}, C_{\mathrm{sg}}$. The MOSFET (*DUT*) is represented by its three interterminal capacitance model. The small signal terminal currents are denoted by $i_{\mathrm{g}}, i_{\mathrm{d}}$, and i_{s}, and the interterminal charging currents as $i_{\mathrm{gd}}, i_{\mathrm{gs}}$, and i_{ds}. Z_{g}, Z_{d}, and Z_{s} model the stray impedances of the setup connections AC⁺, AC⁻, and ACG, including the *DUT* package parasitic inductances in series.

feedback loop after the common virtual ground potential [30], which eliminates the influence of the ampere meter on the measured current.

A. Electrical Equivalent Circuit of the Setup

The electrical equivalent circuit of this small-signal gate capacitance characterization setup is illustrated in Fig. 4. It includes the MOSFET's equivalent circuit introduced in Fig. 1. The high-side (AC⁺) of the small-signal voltage source (v_{ac}) and the dc bias voltage (V_{DC}) are superposed by the internal bias-T at the gate terminal. Both the drain and source terminals are connected to the dc ground potential (V_{GND}). The small-signal current (i_{ac}) is measured at the low-side (AC⁻) of v_{ac}, which is coupled to either the drain or the source terminal. The impedance $\bar{Z} = \bar{v}_{\mathrm{ac}}/\bar{i}_{\mathrm{ac}}$ is derived from the voltage $\bar{v}_{\mathrm{ac^+-ac^-}}$ measured across AC⁺ and AC⁻, and the current $\bar{i}_{\mathrm{ac}}$ at AC⁻. Hereafter, complex impedances ($\bar{Z}$), voltages ($\bar{v}$), and currents ($\bar{i}$) will be denoted without macron for simplicity.

Setting up the measurements of the interterminal capacitances $C_{\mathrm{ij}}|_{(\mathrm{i}\neq\mathrm{j})}$ of 3-, or 4-pin packaged power MOSFETs require a special attention. The third terminal of the MOSFET must be connected to ac guard (ACG) [33], in order to avoid capacitive coupling over the floating third terminal in parallel to C_{ij}.

Z_{g}, Z_{d}, and Z_{s} in Fig. 4 represent the stray impedances of the setup connections AC⁺, AC⁻, and ACG, including L_{g}, L_{d}, and L_{s} of the *DUT* package depicted in Fig. 1. These impedances influence the measurement of *Z* between AC⁺–AC⁻, since they are connected in series with the *DUT* terminals.

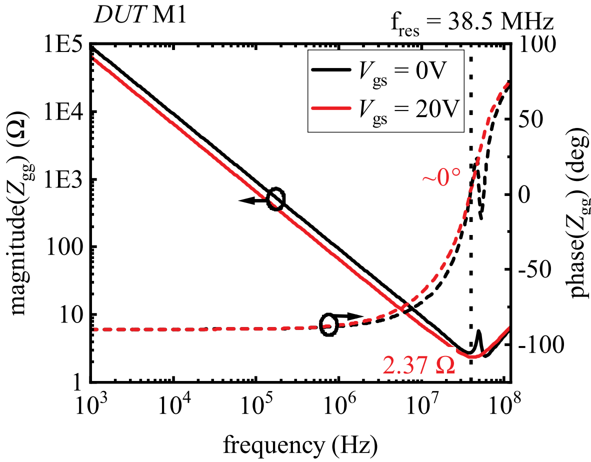

Fig. 5. (Z_{gg}) magnitude and phase of M1 measured for $V_{\mathrm{gs}} = 0$ V and $V_{\mathrm{gs}} = 20$ V with a pin length of 7 mm.

B. Extraction of C_{gg}

For the extraction of the input capacitance C_{gg}, defined by (1a), the gate terminal is connected to AC⁺, and the drain and source terminals are connected both to AC⁻, so that the sum of the currents i_{gd} and i_{gs} is measured at AC⁻; see Fig. 4. According to the MOSFET's equivalent circuit, a series-equivalent model $C_{\mathrm{s}} - R_{\mathrm{s}}$ is intuitively used to model the gate circuit, and hence, the $C_{\mathrm{s}} - R_{\mathrm{s}}$ model was used to extract C_{gg} from the imaginary part of the input impedance Z_{gg} based on (6), whereas the real part $\Re\{Z_{\mathrm{gg}}\}$ can be used to extract the lumped equivalent gate resistance, R_{gg}. The Z_{gg} measurements of a planar-gate SiC power MOSFET M1, listed in Table I, is used here as an example to better explain the recommended measurement settings for the C_{gg} extraction. The magnitude-phase measurements of $Z_{\mathrm{gg,M1}}$ are presented in Fig. 5 for $V_{\mathrm{gs}} = 0$ V and $V_{\mathrm{gs}} = 20$ V. At high frequencies > 1 MHz, a series-equivalent model has to be extended to a $C_{\mathrm{s}} - R_{\mathrm{s}} - L_{\mathrm{s}}$ equivalent model, where L_{s} is used to explain the Z_{gg} resonance in Fig. 5. Namely, the inductive reactance $X = \omega L$ determined by the package parasitic inductances, which in turn depends on the length of the package pins above the test fixture, shifts the phase of Z_{gg} positively [34]. Accordingly, the input capacitance C_{gg} is preferably measured at lower frequencies, e.g., 30 kHz, to reduce $X = \omega L$, and to achieve a high measurement accuracy, i.e., $0.1\,\%$ accuracy of the measurement instrument is specified for $|Z_{\mathrm{meas}}|$ in the range of (1 –100 kΩ) [35].

At the resonance frequency (f_{res}), the magnitude of the measured impedance (Z_{meas}) $|Z_{\mathrm{meas}}| = \Re\{Z_{\mathrm{meas}}\}$. Hence, $|Z_{\mathrm{gg}}(f_{\mathrm{res}})|$

TABLE I
LIST OF COTS SIC AND SI POWER MOSFETS USED IN THIS STUDY (*DUTS*) ALONG WITH THEIR NOMINAL PARAMETERS $V_{\rm DS}$, $I_{\rm d}$, AND $R_{\rm ds,on}$

Manufacturer	Number	*DUT*	Type	$V_{\rm ds}$ [V]	$I_{\rm d}$ [A]	$R_{\rm ds,on}$
Wolfspeed	C2M0080120D	M1	planar SiC Power MOSFET	1200	36	80 mΩ
Rohm	SCT2080KE	M2	planar SiC Power MOSFET	1200	40	80 mΩ
Infineon	IPW60R070P6	M3	Si superjunction CoolMOS	650	156	70 mΩ
IXYS	IXFH6N120P	M4	Si Polar HiPerFET	1200	6	<= 2.75 Ω

represents the lumped value of the internal gate resistance of the MOSFET's compact model. For the $Z_{\rm gg,M1}$ two resonance frequencies ($\varphi = 0$ deg) can be observed for $V_{\rm gs} = 0$ V, which can be simulated using a MOSFET compact model equivalently to Fig. 1. For $V_{\rm th} \ll V_{\rm gs} = 20$ V, only a single resonance peak appears, since the open channel of the MOSFET almost provides an AC short of the internal drain–source contacts and leads to a series-equivalent connection of $(R - C - L) \approx L_{\rm g} - R_{\rm gg} - C_{\rm gg} - L_{\rm d}||L_{\rm s}$; see Fig. 2(c) and (d). Therefore, for $V_{\rm gs} \gg V_{\rm th}$, e.g. $V_{\rm gs} = 20$ V, the direct extraction of measured $\Re\{Z_{\rm gg}\} = R_{\rm gg}$ is possible, which is not necessarily true for $V_{\rm gs} = 0$ V.

Both $C_{\rm gg}$ and $R_{\rm gg}$ are frequency-dependent. For example, $R_{\rm gg}(V_{\rm gs} = 20\,{\rm V})$ shows a difference of +44 % between the values of 2.37 Ω at $f = 38.5$ MHz and 3.42 Ω at $f = 1$ MHz. The main contribution at higher frequencies above 1 MHz is due to the distributed $R_{\rm gg} - (C_{\rm gg}||G_{\rm p})$ (parallel conductance $G_{\rm p}$) behavior of the MOSFET's distributed gate layout [36] and package parasitics. The frequency dependence of $C_{\rm gg}$ for frequencies below 1 MHz is very small, whereas $R_{\rm gg}$ might be strongly affected by oxide interface states, gate leakage current, and insufficient accuracy of the $Z_{\rm gg}$ phase measurement. However, the detailed discussion of such frequency dependence is not in focus of this article and, hence, is omitted for the sake of brevity.

C. Extraction of C_{dg} and C_{sg}

In a $C_{\rm dg}$ measurement, the MOSFET's D and S terminals are connected to AC$^-$ and ACG, respectively (see Fig. 4), where $Z_{\rm s} = j\omega L_{\rm s} + Z_{\rm ACG}$ and $Z_{\rm d} = j\omega L_{\rm d} + Z_{\rm AC^-}$. In contrast, in a $C_{\rm sg}$ measurement the D and S terminals are connected to ACG and AC$^-$, respectively, so that $Z_{\rm s} = j\omega L_{\rm s} + Z_{\rm ac^-}$ and $Z_{\rm d} = j\omega L_{\rm d} + Z_{\rm ACG}$. The ampere meter (A) (always at AC$^-$ of the Keysight E4900A), which is located in the current path of $i_{\rm d}$ for $C_{\rm dg}$ or in the current path of $i_{\rm s}$ for $C_{\rm sg}$, indicates the position at which $i_{\rm d}$ or $i_{\rm s}$ are measured.

The small-signal voltage $v_{\rm ds}$ between AC$^-$/ACG and the DC bias voltage $V_{\rm ds}$ are ideally equal to 0 V. However, it will be shown that the effective condition $V_{\rm ds} \neq 0\,V$ has significant impact on the measurement of the interterminal drain-gate impedance, $Z_{\rm dg}$, and source-gate impedance, $Z_{\rm sg}$, from which $C_{\rm dg}$ and $C_{\rm sg}$ are extracted based on (7) or (6), respectively.

During $Z_{\rm dg}$ and $Z_{\rm sg}$ measurements, the small-signal current $i_{\rm g}$ is divided into two components, $i_{\rm d}$ and $i_{\rm s}$, flowing into the drain and source terminals, respectively.

Starting from the MOSFET's small-signal equivalent circuit shown in Fig. 2(b), the $i_{\rm d} = -i_{\rm gd}$ path in the OFF-state is via $C_{\rm g2}, C_{\rm JFET}$, and $R_{\rm JFET}$, while the current path of $i_{\rm s} = -i_{\rm gs}$ is defined by $C_{\rm g1}||C_{\rm ov}$. The current path between the drain and source terminals is split into the channel current, $i_{\rm ch}$, which is 0 A in the OFF-state, and the current $i_{\rm ds}$ via $C_{\rm ds}$. The voltage difference across $C_{\rm ds}$ and the current $i_{\rm ds}$ can be neglected since 1) the impedances $|Z_{\rm d} + R_{\rm Epi}|, |Z_{\rm s}| \ll 1/(\omega C_{\rm dg}), 1/(\omega C_{\rm sg}),\ 1/(\omega C_{\rm ds})$ at frequencies $f < 10$ MHz ($C_{\rm ij} \sim 1\,nF$ and $R_{\rm Epi} \leq 1\,\Omega$), hence, the corresponding voltages $|v_{\rm ac}| \gg |i_{\rm d}(Z_{\rm d} + R_{\rm Epi})| \approx |i_{\rm s}Z_{\rm s}| \approx 0$ V, and 2) $v_{\rm ac} \gg v_{\rm ds}$ between AC$^-$/ACG ≈ 0 V. The small-signal electrical equivalent circuits of the measurement setups for $C_{\rm dg}$ and $C_{\rm sg}$ in the ON-state are shown in Fig. 6(a) and (b). The power MOSFET model for the condition of a strong inversion is shown in Fig. 2(d), based on which the interterminal gate capacitances are defined as

$$C_{\rm dg,on} = C_{\rm g2} \tag{9}$$

$$C_{\rm sg,on} = C_{\rm g1} + C_{\rm ov}. \tag{10}$$

During measurements, the gate current $i_{\rm g}$ is divided into $i_{\rm ov}$, flowing through the overlap capacitance $C_{\rm ov}$, and into $i_{\rm g'} = i_{\rm g} - i_{\rm ov}$, flowing through the parallel capacitances $C_{\rm g1}$ and $C_{\rm g2}$, which is defined here as

$$C_{\rm g'} = C_{\rm g1} + C_{\rm g2} = C_{\rm gg} - C_{\rm ov}. \tag{11}$$

In addition to the terminal currents $i_{\rm d}$ and $i_{\rm s}$, a current source $i_{\rm g_{ch}}$ needs to be modeled in parallel to $R_{\rm ch}$. This current source $i_{\rm g_{ch}}$ results due to the MOSFET's channel transconductance ($g_{\rm ch}$) [26]. Since the total transconductance $g_{\rm m}$ is mainly determined by $g_{\rm ch}$, the contributions of the JFET- and Epi-layer transconductances are neglected here for the sake of simplicity. The transconductance $g_{\rm m}$ of M1 obtained from quasi-static $I_{\rm d} - V_{\rm gs}$ measurements is shown for $V_{\rm ds} = 50$ mV and $V_{\rm ds} = 0$ V in Fig. 7(a).

During measurements of $Z_{\rm dg}$ and $Z_{\rm sg}$ for $V_{\rm gs} \geq V_{\rm th}$, the product of the internal gate-source voltage $v_{\rm gs}$ (across the oxide/semiconductor interface) and $g_{\rm ch}$, where $g_{\rm ch} \sim V_{\rm ds}$ for small $V_{\rm ds}$, leads to a current flow $i_{\rm g_{ch}} = g_{\rm ch}v_{\rm gs}$ (in phase with $v_{\rm gs}$) between the drain-source terminals (AC $^-$/ACG) in the case of $V_{\rm ds} \neq 0$ V. This current flow only occurs due to the failure of guarding [30], when the open MOSFET channel creates a low-resistive connection ($R_{\rm ds,on}$) between AC$^-$ and ACG. This is demonstrated in the following on the example of the planar-gate SiC power MOSFET, M1, listed in Table I. Finite values of $V_{\rm ds}$ were measured in the range of 350 –50 μV with the digital multimeter Keithley DMM6500 [37] for $V_{\rm th} < V_{\rm gs} \leq 20$ V. The product of this measured $V_{\rm ds}$ and normalized transconductance $g_{\rm m,norm}$ ($g_{\rm m,norm}V_{\rm ds}$), where $g_{\rm m,norm} = g_{\rm m}/(50\,{\rm mV})$ [as measured in Fig. 7(a)], is compared with the absolute conductance $|G_{\rm sg}|$ and $\omega C_{\rm sg,s}$ from the $Z_{\rm sg}$ measurement. The conductance peak of $g_{\rm m,norm}V_{\rm ds}$ clearly correlates with the peak of $|G_{\rm sg}|$ and $\omega C_{\rm sg}$, as shown in Fig. 7(b).

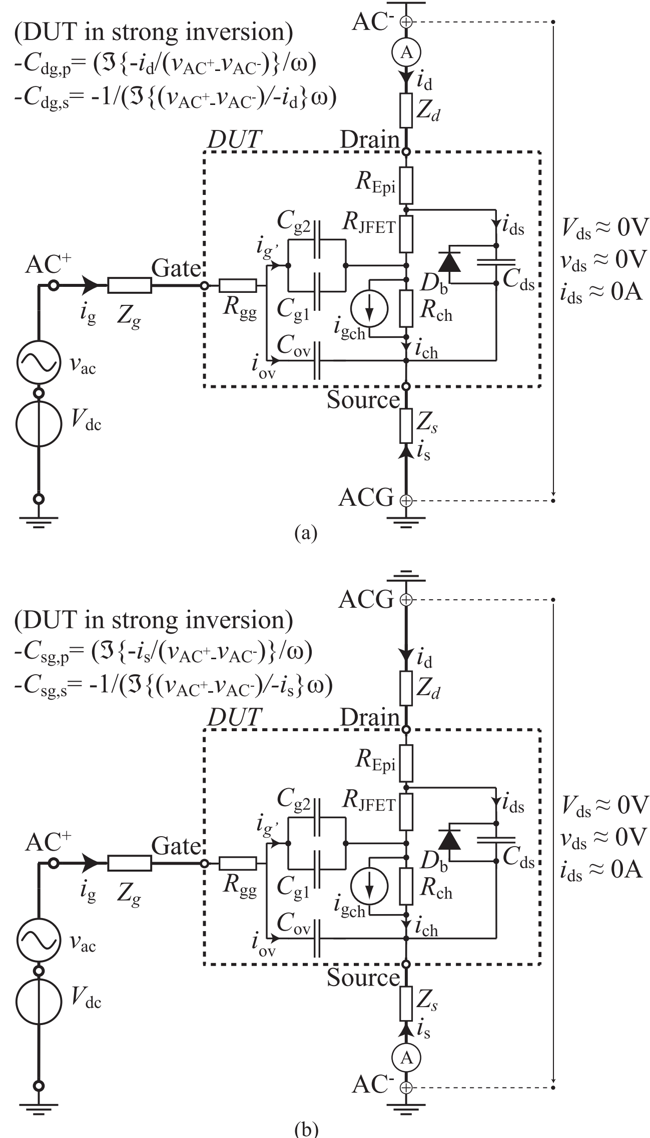

Fig. 6. Electrical equivalent circuits of the small-signal characterization setups for (a) C_{dg} and (b) C_{sg}. The MOSFET is modeled in strong inversion to emphasize the path of the small-signal currents during the measurements.

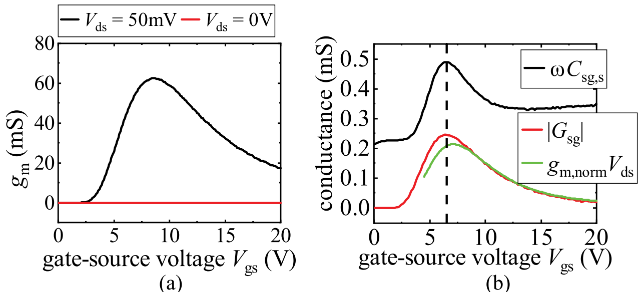

Fig. 7. (a) Transconductance g_{m} of M1 extracted from quasi-static $I_{\mathrm{d}} - V_{\mathrm{gs}}$ measurements at $V_{\mathrm{ds}} = 50$ mV, $V_{\mathrm{ds}} = 0$ V. (b) Comparison of the conductance $|G_{\mathrm{sg}}|$ and $\omega C_{\mathrm{sg,s}}$ (series-equivalent model C_{s}) measured at $f = 30$ kHz versus $g_{\mathrm{m,norm}} V_{\mathrm{ds}}$.

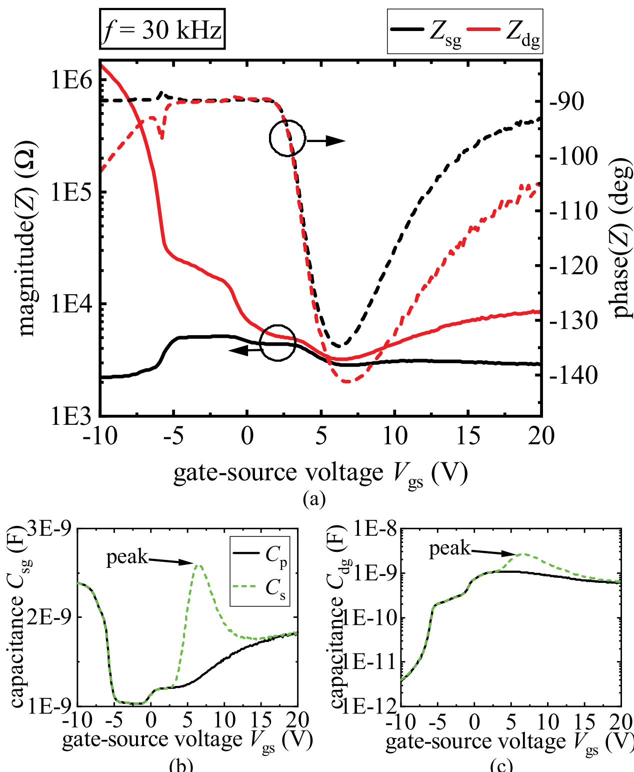

Fig. 8. (a) Magnitude and phase of the impedances Z_{sg} (black) and Z_{dg} (red) of M1 measured at $f = 30$ kHz, $T = 25$ °C. Parallel C_{p} (in black) and series C_{s} (in green) equivalent capacitances of (b) C_{sg} (c) C_{dg} extracted from Z_{sg} and Z_{dg} of (a).

The effect of $i_{g_{\mathrm{ch}}} = g_{\mathrm{ch}} v_{\mathrm{gs}}$ results mainly in a deviation of the phase Z_{dg} ($\varphi(Z_{\mathrm{dg}})$) and the phase Z_{sg} ($\varphi(Z_{\mathrm{sg}})$) from -90 deg, as shown in Fig. 8(a), at $f = 30$ kHz. Note that $\varphi(Z_{\mathrm{dg}})$ and $\varphi(Z_{\mathrm{sg}})$ deviate from -90 deg starting from $V_{\mathrm{gs}} \approx V_{\mathrm{th}}$ and reach a negative peak value of -141 and -137 deg, respectively. This value of deviation from -90 deg is proportional to g_{ch} and, hence, to V_{ds}, i.e., the voltage between AC$^-$ and ACG. With increasing frequency, the amplitudes of $i_{\mathrm{d}} = v_{\mathrm{ac}}/Z_{\mathrm{dg}}$ and $i_{\mathrm{s}} = v_{\mathrm{ac}}/Z_{\mathrm{sg}}$ increase for a constant value of v_{ac} due to the reduction of $|Z_{\mathrm{dg}}| \approx |\frac{1}{\omega C_{\mathrm{dg}}}|, |Z_{\mathrm{sg}}| \approx |\frac{1}{\omega C_{\mathrm{sg}}}|$. As a result, the ratios of $|i_{\mathrm{d}}|/|i_{g_{\mathrm{ch}}}|, |i_{\mathrm{s}}|/|i_{g_{\mathrm{ch}}}|$ increase with increasing frequency until $|i_{\mathrm{d}}|, |i_{\mathrm{s}}| \gg |i_{g_{\mathrm{ch}}}|$, for which the influence of $g_{\mathrm{ch}} v_{\mathrm{gs}}$ becomes negligible.

The impact of this phenomena ($i_{g_{\mathrm{ch}}} = g_{\mathrm{ch}} v_{\mathrm{gs}}$) is further analyzed by the extraction of C_{dg} and C_{sg} using both series- and parallel-equivalent circuits and (6) and (7), respectively. It should be noted that a series-equivalent circuit is typically selected since the equivalent circuits of the gate current paths can be described by a series connection of resistance and capacitance, without prior knowledge of the distortions introduced by the measurement setup. Fig. 8(b) and (c) shows the parallel (C_{p}) and series (C_{s}) equivalent capacitances for C_{dg} and C_{sg}, which are extracted from Z_{dg} and Z_{sg} of Fig. 8(a). The comparison between C_{p} and C_{s} shows that the deviations in $\varphi(Z_{\mathrm{dg}})$ and $\varphi(Z_{\mathrm{sg}})$ only affect C_{s}, indicated by the capacitance peaks in Fig. 8(b) and (c). The extracted parallel capacitances C_{p} of C_{dg}

and C_{sg} are not affected by these phase distortions, even though C_p is extracted from the same impedance as C_s. This is explained by the parallel-equivalent circuit used for the extraction of C_p in (7). The transconductance contributes only to the in-phase current represented by the parallel conductance G_p (the real part of the admittance $Y = 1/Z$) and, therefore, leaves C_p unaffected. On the contrary, the series-equivalent model $R_s - C_s$ cannot correctly represent this effect, since the in-phase current $i_{g_{ch}} = g_{ch} v_{gs}$ ($\varphi(i_{g_{ch}}) = 0°$) would lead to an increase of the differential capacitance C_s by $\Delta C \sim \partial q/\partial v_{gs} \sim i_{g_{ch}}/(\omega v_{gs}) \sim g_{ch}/f$, resulting in the observed capacitance peak, which does not correctly represent the underlying device physics. Thus, C_{dg} and C_{sg} should be extracted from the measured impedances Z_{dg}, Z_{sg} or admittance Y_{dg}, Y_{sg} as parallel equivalent capacitance C_p.

Another interesting observation is the deviation of $\varphi(Z_{dg})$ from -90 deg toward increasing negative values for decreasing $V_{gs} \leq -5$ V, as depicted in Fig. 8(a). This effect is not due to the failure in guarding between AC^- and ACG, but it can be explained by the formation of an inversion layer of holes at the oxide–JFET interface, cf. Fig. 2(a). This inversion layer of holes forms a resistive connection between the oxide–JFET interface and the p base [38], while it is separated by a depletion region from the conducting Epi-layer of the drain current path. As a result, a part of the current i_{ac} ($i_{g'}$) is bypassed through the p base into the source instead of the drain terminal, which causes this deviation in $\varphi(Z_{dg})$ for negative V_{gs}.

IV. C–V Measurement Results

In this section, the measurement results of gate capacitance characteristics are presented for SiC and Si power MOSFETs. The measurements are performed at $f = 30$ kHz and at room temperature ($T = 25$ °C) if not otherwise stated. The properties of the *DUTs*, such as label, type, V_{ds} rating, nominal drain current I_d, and ON-state resistance $R_{ds,on}$, are listed in Table I.

Prior to all measurements, open- and short- compensation of the test fixture were performed. During each measurement, V_{gs} was swept from negative to positive polarity with a point delay of 1 s.

C_{gg} measurements at $f = 30$ kHz, $f = 100$ kHz, and $f = 1$ MHz of two SiC (M1,M2) and two Si (M3, M4) power MOSFETs are shown in Fig. 9. Only a small frequency dependence is visible, except for M2, which shows a difference of up to 7.5 % for $V_{gs} < -5$ V at $f = 1$ MHz in comparison to $f = 30$ kHz and $f = 100$ kHz. The frequency dependence of $C_{sg,M1}$ and $C_{dg,M1}$ is shown in Fig. 10(a) and (b), respectively, for $f = \{30$ kHz, 100 kHz, 1 MHz$\}$. At $f = 30$ kHz (black) and $f = 100$ kHz (red), a difference is observable in C_{dg} of up to 10 % at $V_{gs} = 20$ V, whereas C_{sg} differs only by 1 %. Yet, C_{dg} at $f = 1$ MHz is higher by (112 %) and C_{sg} lower by (30 %) in comparison to $f = 30$ kHz.

The characteristics of $C_{dg,M1}$ and $C_{sg,M1}$ at $f = 30$ kHz measured at $T = \{25\,°C, 125\,°C, 175\,°C\}$ are shown in Fig. 11(a) and (b). The C_{dg} decreases and the C_{sg} increases with increasing temperature, which is due to the temperature dependance of the ON-state resistance components, $R_{ch}(T)$ and $R_{drift}(T)$ [39], as it is further explained in Section V. In addition, a reduction of

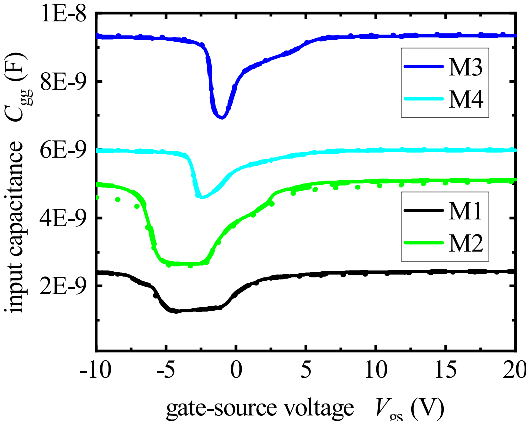

Fig. 9. Input capacitance C_{gg} of M1, M2, M3, and M4 listed in Table I, measured at $f = 30$ kHz (solid), $f = 100$ kHz (dashed), and $f = 1$ MHz (dotted line). All *DUTs* are connected with a spacing of 7 mm between *DUT* package and electrodes of the test fixture 16047E.

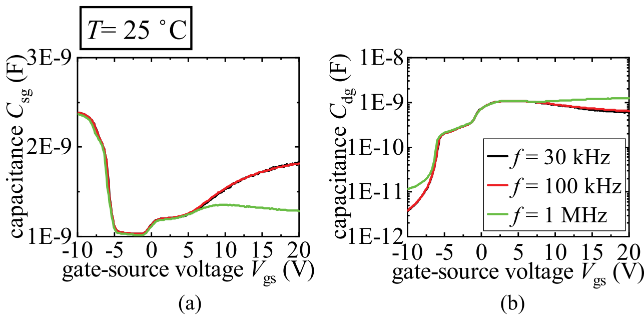

Fig. 10. (a) C_{sg} and (b) C_{dg} frequency dependence of M1 measured for $V_{ds} = 0$ V at $T = 25$ °C, $f = \{30$ kHz, 100 kHz, 1 MHz$\}$.

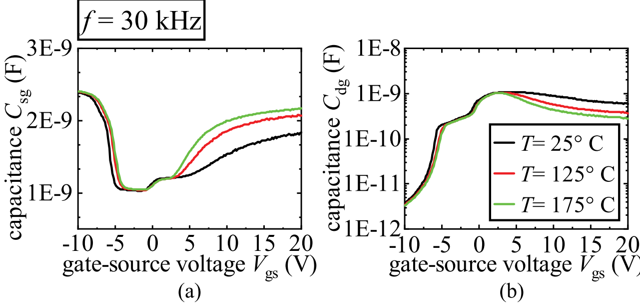

Fig. 11. (a) C_{sg} and (b) C_{dg} temperature dependence of M1 measured for $V_{ds} = 0$ V at $f = 30$ kHz, $T = \{25$ °C, 125 °C, 175 °C $\}$.

V_{th} (the value of $V_{gs} > 0$ V at which the curves for different temperatures start to diverge) is observable at the onset of inversion for $T = 125$ °C and $T = 175$ °C. The V_{th} values of each *DUT* at room temperature are specified in Table II for the conditions of $V_{gs} = V_{ds}$ and $I_d = 5$ mA. The gate capacitance characteristics C_{gg} (C_s) and C_{dg}, C_{sg} (C_p) of M1 are plotted in solid lines as functions of V_{gs} at $V_{ds} = 0$ V, for $f = 30$ kHz and $f = 1$ MHz in Fig. 12.

The measurement accuracy of C_{dg} and C_{sg} can be verified by comparing ($C_{dg} + C_{sg}$) with C_{gg} according to (3). In the case of M1, ($C_{dg} + C_{sg}$) matches C_{gg} at $f = 30$ kHz, as shown in

TABLE II
DUTs THRESHOLD VOLTAGE VALUES V_{TH}, AND ESTIMATIONS OF THE OVERLAP CAPACITANCES C_{OV}, ACCORDING TO (23), MEASURED $C_{\text{dg,on}}/C_{\text{sg,'on}}$, $R_{\text{ds,on}}$, AND ESTIMATED R_{CH} AND R_{DRIFT} ACCORDING TO (26)

DUT	V_{th} [V] ($V_{\text{gs}} = V_{\text{ds}}$, I_{d} =5 mA)	C_{ov} [nF]	$V_{\text{gs}}\|_{C_{\text{ov}}}$ [V]	$C_{\text{dg,on}}/C_{\text{sg',on}}$ (V_{gs} =20 V)	$R_{\text{ds,on}}$ [Ω] (V_{ds} =50 mV, V_{gs} =20 V)	R_{ch} [Ω]	R_{drift} [Ω]
M1	3.23	1.03	-1.6	0.73	0.079	0.033	0.046
M2	3.34	1.80	3.5	0.96	0.082	0.04	0.042
M3	4.08	2.54	4.1	0.15	0.062	0.008	0.054
M4	4.19	1.73	3.65	0.006	2.15	0.013	2.137

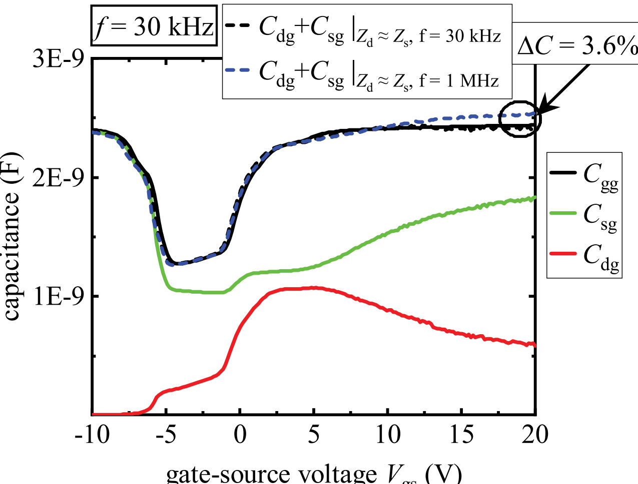

Fig. 12. Gate capacitance characteristics C_{gg} (C_{s}) and C_{dg}, C_{sg} (C_{p}) of M1 measured at f = 30 kHz, $V_{\text{ds}} = 0$ V. The black dashed line depicts the sum of $C_{\text{dg}} + C_{\text{sg}}$ at f = 30 kHz and the blue dashed line $C_{\text{dg}} + C_{\text{sg}}$ at f = 1 MHz.

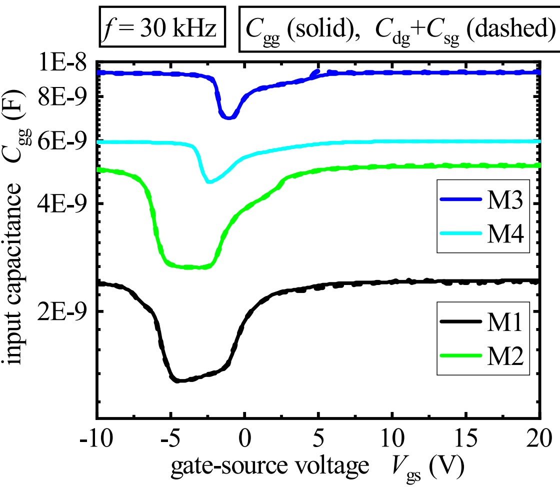

Fig. 13. Input capacitance C_{gg} (solid lines) in comparison to the sum $C_{\text{dg}} + C_{\text{sg}}$ (dashed lines). The measurements are performed at $V_{\text{ds}} = 0$ V, f = 30 kHz.

Fig. 12. On the other hand, the ($C_{\text{dg}} + C_{\text{sg}}$) measured at f = 1 MHz starts to diverge from C_{gg} for $V_{\text{gs}} > V_{\text{th}}$ up to a relative difference of 3.6 % at V_{gs} = 20 V. This difference is caused by an increase of $|Z_{\text{d}}| \sim wL_{\text{d}}$ and $|Z_{\text{s}}| \sim wL_{\text{s}}$ of the package parastic inductances at f = 1 MHz ($L_{\text{d}} \neq L_{\text{s}}$ [34], [40]), which leads to an increase of C_{dg} and a decrease of C_{sg}, as shown in Fig. 10(a) and (b), respectively.

A. Comparison of SiC vs. Si Power MOSFETs

A comparison between the measured input capacitance C_{gg} (solid lines) and ($C_{\text{dg}} + C_{\text{sg}}$) (dashed lines) is shown in Fig. 13 for Si- and SiC-power MOSFETs specified in Table I. For all *DUTs*, the extracted ($C_{\text{dg}} + C_{\text{sg}}$) match the extracted C_{gg}, which verifies the accuracy of the proposed measurement procedure.

The measured C_{sg} and C_{dg} of all *DUTs* are plotted in Figs. 14 and 15, respectively. For large negative V_{gs}, the JFET region below the gate oxide is in inversion, resulting in a very small depletion capacitance C_{JFET}, as depicted in Fig. 2(a), and hence, C_{dg} is small [18]. C_{dg} increases with increasing V_{gs} corresponding to the change from inversion to accumulation and reaches the highest value for V_{gs} around V_{th}. C_{sg} is equal to C_{gg} until the channel region starts to deplete. For $V_{\text{gs}} \geq V_{\text{th}}$, C_{sg} increases.

The main difference between Si and SiC power MOSFETs in terms of C_{sg} and C_{dg} characteristics is apparent in strong inversion: While the C_{sg} values in inversion and accumulation are very close for Si power devices, the inversion and accumulation values of C_{sg} are different for SiC power MOSFETs. With respect to the C_{dg} characteristics in inversion, it can be observed that the values of C_{dg} are much smaller than C_{sg} for Si power devices. On the other hand, C_{dg} of SiC power MOSFETs is of the same order as C_{sg} in inversion. This difference between Si and SiC power MOSFETs can be further explained by the following analysis based on an analytical derivation of C_{dg} and C_{sg}, shown in Section V-B.

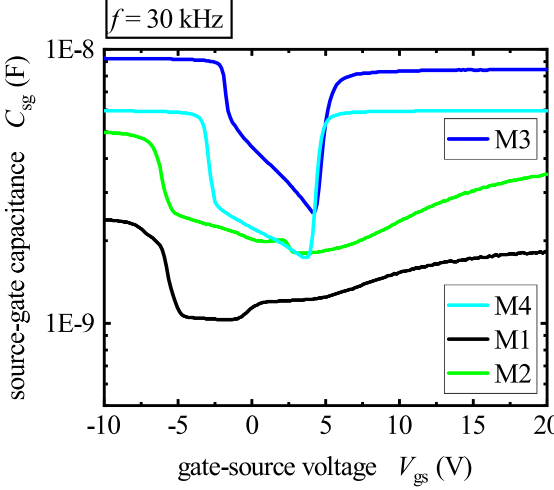

Fig. 14. Source-gate capacitance C_{sg} measured at $V_{\text{ds}} = 0$ V, f = 30 kHz.

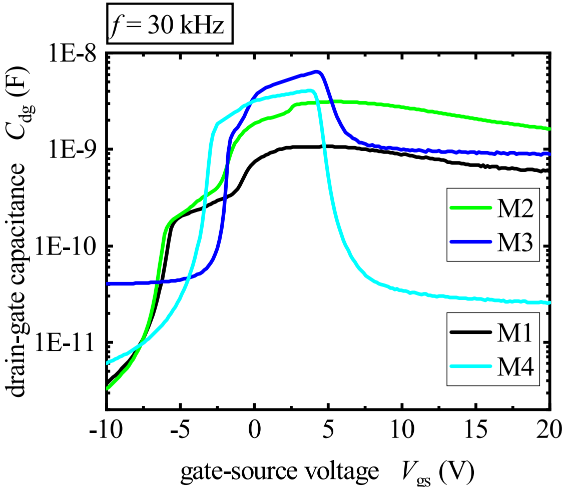

Fig. 15. Drain-gate capacitance C_{dg} measured at $V_{\mathrm{ds}}=0$ V, $f=30$ kHz.

V. A Proposed Method for the Extraction of $R_{\mathrm{ds,on}}$ MOSFET Components

In this section, a new method for the extraction of $R_{\mathrm{ds,on}}$ MOSFET components is presented. First, analytical models of C_{sg} and C_{dg} are derived as function of the MOSFET's equivalent circuit parameters of Fig. 6(a) and (b), similar to the procedure presented in [26]. However, in [26], analytical models for $C_{\mathrm{gd}}/C_{\mathrm{dg}}$ and for $C_{\mathrm{gs}}/C_{\mathrm{sg}}$ were derived based on a small-signal equivalent circuit of a double-diffused MOSFET, but without considering the MOSFET's overlap capacitance C_{ov} and without the series impedances Z_{s}, Z_{d} of the measurement setup.

The derivation presented here illustrates the differences between the parallel ($C_{\mathrm{p}}||G_{\mathrm{p}}$) and series ($C_{\mathrm{s}}-R_{\mathrm{s}}$) equivalent capacitance models.

A. Analytical Derivation of C_{dg} and C_{sg}

The electrical equivalent circuits in Fig. 6(a) and (b) are solved by Kirchhoff's circuit laws for the terminal currents i_{d} and i_{s}. Based on the solutions of i_{d} and i_{s}, the applied voltage ($v_{\mathrm{AC^+}}-v_{\mathrm{AC^-}}$), and the parallel-equivalent model (7), the interterminal capacitances can be derived by

$$C_{\mathrm{dg,p}} = -\Im\left\{\frac{-i_{\mathrm{d}}}{v_{\mathrm{AC^+}}-v_{\mathrm{AC^-}}}\right\}/\omega \tag{12}$$

and

$$C_{\mathrm{sg,p}} = -\Im\left\{\frac{-i_{\mathrm{s}}}{v_{\mathrm{AC^+}}-v_{\mathrm{AC^-}}}\right\}/\omega. \tag{13}$$

In order to derive analytical forms of $C_{\mathrm{dg,p}}$ (12) and $C_{\mathrm{sg,p}}$ (13), the following assumptions of the small-signal circuit elements in Fig. 6(a) and (b) are used:

1) $1/(\omega C_{\mathrm{g'}}), 1/(\omega C_{\mathrm{ov}}), 1/(\omega C_{\mathrm{ds}}) \gg R_{\mathrm{ch}}, R_{\mathrm{drift}}, |Z_{\mathrm{d}}|, |Z_{\mathrm{s}}|$
2) $C_{\mathrm{g'}}, C_{\mathrm{ov}}, R_{\mathrm{ch}}, R_{\mathrm{drift}}, |Z_{\mathrm{d}}|, |Z_{\mathrm{s}}| \leq 1$
3) $1/(\omega C_{\mathrm{gg}}) \gg R_{\mathrm{gg}}+|Z_{\mathrm{g}}|$.

The solutions of (12) and (13) based on the Assumptions 1–3 are given in (14) and (15), shown at the bottom of this page. Here, two approximations for $C_{\mathrm{dg,p}}$ and $C_{\mathrm{sg,p}}$ are presented from (14) and (15). In the first approximation A1, $g_{\mathrm{ch}}=0$ S is assumed, based on which $C_{\mathrm{dg,on,p}}$ and $C_{\mathrm{sg,on,p}}$ can be expressed in ON-state as

$$C_{\mathrm{dg,on,p}}|_{g_{\mathrm{ch}}=0} \approx \Re\left\{\frac{C_{\mathrm{ov}}Z_{\mathrm{s}}+C_{\mathrm{g'}}(R_{\mathrm{ch}}+Z_{\mathrm{s}})}{R_{\mathrm{drift}}+R_{\mathrm{ch}}+Z_{\mathrm{d}}+Z_{\mathrm{s}}}\right\} \tag{16}$$

$$C_{\mathrm{sg,on,p}}|_{g_{\mathrm{ch}}=0} \approx \Re\left\{\frac{C_{\mathrm{g'}}(R_{\mathrm{drift}}+Z_{\mathrm{d}})+C_{\mathrm{ov}}(R_{\mathrm{ch}}+R_{\mathrm{drift}}+Z_{\mathrm{d}})}{R_{\mathrm{drift}}+R_{\mathrm{ch}}+Z_{\mathrm{d}}+Z_{\mathrm{s}}}\right\}. \tag{17}$$

In the second approximation A2, $Z_{\mathrm{d}}=0$ and $Z_{\mathrm{s}}=0$ are assumed, which corresponds to low-frequency measurement conditions, and leads to

$$C_{\mathrm{dg,on,p}}|_{Z_{\mathrm{d}}=Z_{\mathrm{s}}=0} \approx \frac{C_{\mathrm{g'}}R_{\mathrm{ch}}(R_{\mathrm{ch}}+R_{\mathrm{drift}}+g_{\mathrm{ch}}R_{\mathrm{ch}}R_{\mathrm{drift}})}{(R_{\mathrm{drift}}+R_{\mathrm{ch}})^2} \tag{18}$$

$$C_{\mathrm{sg,on,p}}|_{Z_{\mathrm{d}}=Z_{\mathrm{s}}=0} \approx C_{\mathrm{ov}}+\frac{C_{\mathrm{g'}}R_{\mathrm{drift}}(R_{\mathrm{ch}}+R_{\mathrm{drift}}+g_{\mathrm{ch}}R_{\mathrm{ch}}R_{\mathrm{drift}})}{(R_{\mathrm{drift}}+R_{\mathrm{ch}})^2}. \tag{19}$$

It was mentioned in Section III-C that the parallel-equivalent capacitance C_{p} is not affected by $i_{g_{\mathrm{ch}}}=g_{\mathrm{ch}}v_{\mathrm{gs}}$. Even though (18) and (19) depend on g_{ch}, the term $g_{\mathrm{ch}}R_{\mathrm{ch}}R_{\mathrm{drift}} \ll (R_{\mathrm{ch}}+R_{\mathrm{drift}})$ for $g_{\mathrm{ch}} \ll 1$. Thus, $g_{\mathrm{ch}}R_{\mathrm{ch}}R_{\mathrm{drift}}$ can be neglected in (18) and (19) for very small values of V_{ds}. For Z_{d}, $Z_{\mathrm{s}} \neq 0$, and $g_{\mathrm{ch}}=0$ S, analytical solutions for $C_{\mathrm{dg,on,s}}$ and $C_{\mathrm{dg,on,s}}$ exist similarly to (16)–(17), which are not explicitly mentioned here for the sake of brevity. In contrast to (18)–(19), which are derived using the parallel equivalent model C_{p}, no analytical solution can

$$\begin{aligned}C_{\mathrm{dg,p}} = \Re\{&(C_{\mathrm{ov}}(1+g_{\mathrm{ch}}R_{\mathrm{ch}})(Z_{\mathrm{s}}(R_{\mathrm{ch}}+R_{\mathrm{drift}}+Z_{\mathrm{d}}+Z_{\mathrm{s}})+C_{\mathrm{g'}}(R_{\mathrm{ch}}+Z_{\mathrm{s}}+g_{\mathrm{ch}}R_{\mathrm{ch}}Z_{\mathrm{s}})\\&(R_{\mathrm{ch}}+R_{\mathrm{drift}}+Z_{\mathrm{d}}+Z_{\mathrm{s}}+g_{\mathrm{ch}}R_{\mathrm{ch}}(R_{\mathrm{drift}}+Z_{\mathrm{d}}+Z_{\mathrm{s}})))/\\&(R_{\mathrm{drift}}+Z_{\mathrm{d}}+Z_{\mathrm{s}}+R_{\mathrm{ch}}(1+g_{\mathrm{ch}}Z_{\mathrm{s}}))^2\}\end{aligned} \tag{14}$$

$$\begin{aligned}C_{\mathrm{sg,p}} = \Re\{&(C_{\mathrm{ov}}(R_{\mathrm{ch}}+R_{\mathrm{drift}}+Z_{\mathrm{d}})(R_{\mathrm{ch}}+R_{\mathrm{drift}}+Z_{\mathrm{d}}+Z_{\mathrm{s}})+C_{\mathrm{g'}}(R_{\mathrm{drift}}+Z_{\mathrm{d}})\\&(R_{\mathrm{ch}}+R_{\mathrm{drift}}+Z_{\mathrm{d}}+Z_{\mathrm{s}}+g_{\mathrm{ch}}R_{\mathrm{ch}}(R_{\mathrm{drift}}+Z_{\mathrm{d}}+Z_{\mathrm{s}})))/\\&(R_{\mathrm{drift}}+Z_{\mathrm{d}}+Z_{\mathrm{s}}+R_{\mathrm{ch}}(1+g_{\mathrm{ch}}Z_{\mathrm{s}}))^2\}.\end{aligned} \tag{15}$$

be found when using Assumptions 1–3 and approximation A2 ($g_{\rm ch} \neq 0$ S) for the series-equivalent model $C_{\rm s}$ (6). In this case, the deviations in $\varphi(Z_{\rm dg})$ and $\varphi(Z_{\rm sg})$ increase with decreasing frequency. Both $C_{\rm dg,on,s}$ and $C_{\rm sg,on,s}$ diverge to infinity for the frequency f approaching zero ($C_{\rm s} \sim g_{\rm ch}/f$). In consequence, the interterminal capacitances $C_{\rm dg}$ and $C_{\rm sg}$ must be extracted by the parallel equivalent model $C_{\rm p}$.

Equations (16)–(19) can further be simplified assuming $|Z_{\rm d}|$, $|Z_{\rm s}| \ll R_{\rm ch}$, $R_{\rm drift}$, and $i_{g_{\rm ch}} \ll i_{\rm d}$, $i_{\rm s}$ into

$$C_{\rm dg,on}\big|_{|Z_{\rm d}|,|Z_{\rm s}|\ll R_{\rm ch},R_{\rm drift};g_{\rm ch}=0} = \frac{C_{g'}R_{\rm ch}}{R_{\rm ch}+R_{\rm drift}} \tag{20}$$

and

$$C_{\rm sg,on}\big|_{|Z_{\rm d}|,|Z_{\rm s}|\ll R_{\rm ch},R_{\rm drift};g_{\rm ch}=0} = \frac{C_{g'}R_{\rm drift}}{R_{\rm ch}+R_{\rm drift}} + C_{\rm ov}. \tag{21}$$

From (20) and (21) and the assumptions taken above, the ratio of $C_{\rm dg,on}/(C_{\rm sg,on} - C_{\rm ov})$ can be expressed as

$$\frac{C_{\rm dg,on}}{C_{\rm sg,on} - C_{\rm ov}} = \frac{i_{\rm d}}{i_{\rm ch}} = \frac{R_{\rm ch}}{R_{\rm drift}}. \tag{22}$$

B. *Extraction of R_{ch} and R_{drift} From C_{dg} and C_{sg}*

The ratio of $R_{\rm ch}$ to $R_{\rm drift}$ can be calculated based on (22) from the values of the MOSFET's $C_{\rm dg}$ and $C_{\rm sg}$ characteristics, which are shown in Figs. 14 and 15. To solve (22) for $R_{\rm ch}$ and $R_{\rm drift}$, the value of $C_{\rm ov}$ is approximated at the minimum of $C_{\rm sg}$ by

$$C_{\rm ov} \approx \min(C_{\rm sg}). \tag{23}$$

The approximation (23) is based on the assumption that in the MOSFET's OFF-state $C_{\rm sg} = C_{\rm ov}||(C_{\rm g1} - C_{\rm ch})$, as shown in Fig. 2(a) and (b). In depletion of the channel region, $C_{\rm ch}$ becomes minimal and, thus, the capacitance of the series connection $C_{\rm g1} - C_{\rm ch} \approx C_{\rm ch} \ll C_{\rm ov}$. Hence, in depletion, $C_{\rm sg} = C_{\rm ov}||(C_{\rm g1} - C_{\rm ch}) \approx C_{\rm ov}$. Although the estimation (23) is not precise, it is a good approximation which can be obtained solely from measured $C_{\rm sg}(V_{\rm gs})$. The estimated $C_{\rm ov}$ and the corresponding $V_{\rm gs}$ values of each *DUT* are listed in Table II. From (10) and (23), it follows that in strong inversion

$$C_{\rm sg,'on} = C_{\rm sg} - \min(C_{\rm sg}) \approx C_{\rm sg} - C_{\rm ov}. \tag{24}$$

Based on the definition of the drain–source resistance

$$R_{\rm ds} = R_{\rm ch} + R_{\rm drift} \tag{25}$$

and together with (3), (22), and (24), the following expression can be derived for $V_{\rm gs} \gg V_{\rm th}$:

$$\frac{C_{\rm gg} - \min(C_{\rm sg})}{R_{\rm ds}} \approx \frac{C_{\rm sg,'on}}{R_{\rm drift}} \approx \frac{C_{\rm dg,on}}{R_{\rm ch}}. \tag{26}$$

$C_{\rm dg,on}/C_{\rm sg,'on}$ is plotted for $V_{\rm gs} > 0$ V in Fig. 16 for all *DUTs* listed in Table I. When $V_{\rm gs}$ is reduced below $V_{\rm th}$ toward depletion, the values of $C_{\rm dg,on}/C_{\rm sg,'on}$ rapidly increase due to (23). The comparison of $C_{\rm dg,on}/C_{\rm sg,'on}$ at higher $V_{\rm gs}$, e.g., at 20 V, shows the difference between SiC and Si power MOSFETs. For M1 and M2, $C_{\rm dg,on}/C_{\rm sg,'on} = \{0.73, 0.96\}$, respectively, which is comparable to the simulation results presented in [41]. $C_{\rm dg,on}/C_{\rm sg,'on}$ of M3 (0.15) and M4 (0.006) are much lower, which means that their $R_{\rm ds,on}$ is mainly determined by $R_{\rm drift}$.

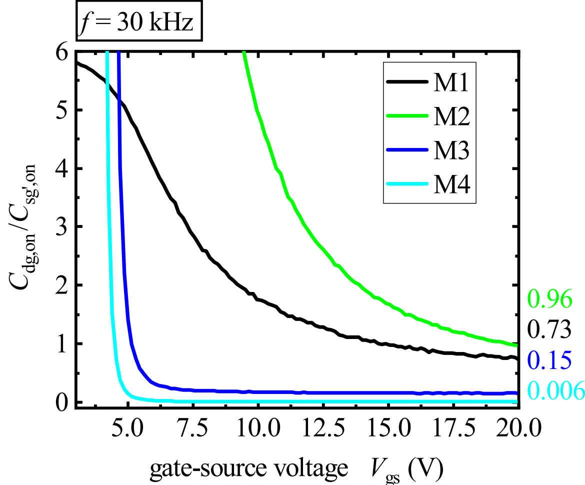

Fig. 16. Plot of $C_{\rm dg,on}/C_{\rm sg,'on}$ based on the $C_{\rm dg}$ and $C_{\rm sg}$ characteristics shown in Figs. 15 and 14. The values of each *DUT* are indicated at $V_{\rm gs} = 20$ V.

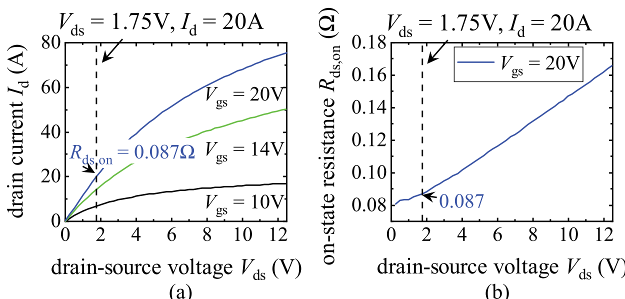

Fig. 17. (a) Output characteristic ($I_{\rm d} V_{\rm ds}$) of M1 measured at room temperature for $V_{\rm gs}$ =10, 14, 20 V using a Keithley PCT-4B. (b) ON-State resistance $R_{\rm ds,on}$ extracted at $V_{\rm gs}$ =20 V.

Overall, thes data demonstrate that SiC power MOSFETs have a thinner active device (epitaxial) layer, and thus, achieve a much smaller $R_{\rm ds,on}$ compared to Si power MOSFETs rated for the same nominal $V_{\rm ds}$ blocking capability of, e.g., 1.2 kV, but also that the channel region of the SiC should be further optimized. Fig. 17(a) shows the output characteristic ($I_{\rm d} - V_{\rm ds}$) of M1 for $V_{\rm gs} = \{10, 14, 20\}$ V, and Fig. 17(b) $R_{\rm ds,on}$ at $V_{\rm gs} = 20$ V. At $V_{\rm ds} = 50$ mV and $V_{\rm gs} = 20$ V, a drain current of $I_{\rm d} = 0.63$ A is measured and $R_{\rm ds,on} = 0.079\ \Omega$ is calculated. Based on $C_{\rm dg,on}/C_{\rm sg,'on} = 0.73$ measured at $V_{\rm gs} = 20$ V, $V_{\rm ds} = 0$ V, a channel resistance $R_{\rm ch} = 0.033\ \Omega$ and a drift resistance $R_{\rm drift} = 0.046\ \Omega$ are calculated from (26); see Table II. The same approximation is valid for application relevant conditions of, e.g., $I_{\rm d} = 20$ A, $V_{\rm ds} = 1.75$ V, and $R_{\rm ds,on} = 0.087\ \Omega$, as shown in Fig. 17, which results in values of $R_{\rm ch} = 0.037\ \Omega$ and $R_{\rm drift} = 0.05\ \Omega$.

VI. Impact of Measurement Setup on the Measurement Accuracy

The influence of the measurement setup on the C–V extraction can be described by $Z_{\rm d}$ and $Z_{\rm s}$ of the *DUT* fixture as analytically derived in Section V-A.

TABLE III

IMPACT OF $|Z_\mathrm{d}| = |Z_\mathrm{s}| \approx R_\mathrm{CH}, R_\mathrm{DRIFT}$ ON C_DG AND C_SG VALUES OF DUT M1 FOR $V_\mathrm{GS} = 20$ V AND $f = 30$ KHZ, 100 KHZ

fixture/extension	f [kHz]	$\|Z\|$ [mΩ]	$\varphi(Z)$ [deg]	C_dg [nF]	$e_\mathrm{r}(C_\mathrm{dg})$ [%]	C_sg [nF]	$e_\mathrm{r}(C_\mathrm{sg})$ [%]
16047E	30	-	-	0.584	-	1.835	-
wire 11 cm	30	22	54.9	0.927	59	1.647	10
wire 40.5 cm	30	93	57.2	1.016	74	1.465	20
16047E	100	-	-	0.643	-	1.819	-
wire 11 cm	100	63	78.4	0.957	49	1.533	16
wire 40.5 cm	100	268	79	1.121	74	1.327	27

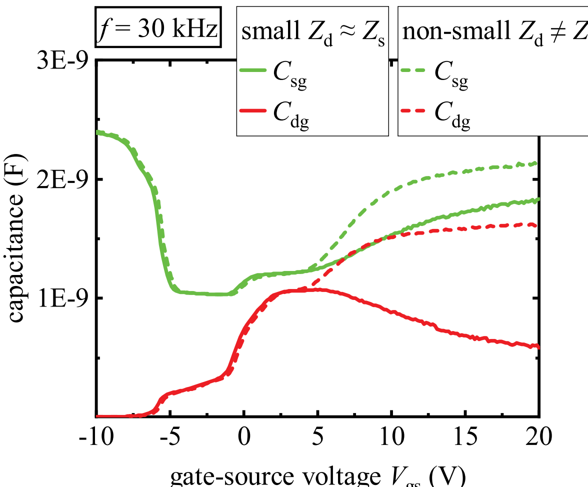

Fig. 18. Plot of C_dg and C_sg (cf. Fig. 12), in which the pins are fixed with 7 mm spacing to the fixture 16047E, such that $|Z_\mathrm{g}| \approx |Z_\mathrm{d}| \approx |Z_\mathrm{s}| \ll R_\mathrm{ch}, R_\mathrm{drift}$, whereas the dotted red and green lines represent measurement results of C_dg, C_sg with additional copper wire of length = 40.5 cm for $|Z_\mathrm{ACG}| \gg |Z_\mathrm{AC^-}|$, $|Z_\mathrm{d}| \neq |Z_\mathrm{s}| \sim R_\mathrm{ch}, R_\mathrm{drift}$.

To evaluate the impact of Z_d and Z_s, the conditions $|Z_\mathrm{d}| = |Z_\mathrm{s}| \approx R_\mathrm{ch}, R_\mathrm{drift}$ are first addressed. The MOSFET package terminals were extended with copper wires of a diameter of 0.4 mm and length of 11 or 40.5 cm, resulting in $|Z_\mathrm{wire}| \approx |Z_\mathrm{d}| = |Z_\mathrm{s}|$ and $\varphi(Z_\mathrm{wire}) \simeq \varphi(Z_\mathrm{d}) \approx \varphi(Z_\mathrm{s})$. The changes in measured values of C_dg and C_sg are listed in Table III. The relative differences to using the fixture 16047E alone (see Fig. 3), are indicated by e_r.

Next, the case $|Z_\mathrm{d}| \neq |Z_\mathrm{s}| \approx R_\mathrm{ch}, R_\mathrm{drift}$ is considered. For the measurement of C_sg, the same copper wire with a length of 40.5 cm (cf. Table III) was inserted only between the drain terminal and ACG ($|Z_\mathrm{ACG}| \approx |Z_\mathrm{wire}| \gg |Z_\mathrm{s}|$), cf. Fig. 6(b), whereas the source terminal was directly connected to AC$^-$ of the fixture 16047E. For the measurement of C_dg, the source terminal was connected to ACG by the copper wire ($|Z_\mathrm{ACG}| \approx |Z_\mathrm{wire}| \gg |Z_\mathrm{d}|$) and the drain terminal directly to AC$^-$. As a consequence of $|Z_\mathrm{ACG}| \gg |Z_\mathrm{AC^-}|$, C_dg and C_sg increase 179 % and 16 % at $V_\mathrm{gs} = 20$ V. This effect of nonsmall $|Z_\mathrm{ACG}| \neq |Z_\mathrm{AC^-}|$ is shown in Fig. 18 by the C–V results marked as nonsmall $|Z_\mathrm{d}| \neq |Z_\mathrm{s}|$.

From (16) and (17) and the results in Table III, it can be concluded that if a test fixture has nonsymmetric impedances, e.g., $|Z_\mathrm{d}| > |Z_\mathrm{s}|$ marked in Fig. 4, the division of $i_{\mathrm{g}'}$ leads to $i_\mathrm{d} < i_\mathrm{s}$, which in turn leads to a measured C_sg higher than a measured C_dg. Similarly, the same holds for $|Z_\mathrm{s}| > |Z_\mathrm{d}|$. In the case of $|Z_\mathrm{ACG}| \gg |Z_\mathrm{AC^-}|, R_\mathrm{ch}, R_\mathrm{drift}$, the values of C_sg and C_dg converge both to the value of C_gg, since $-i_\mathrm{s} = i_\mathrm{g}$ for the configuration of C_sg and $-i_\mathrm{d} = i_\mathrm{g}$ for the configuration of C_dg measurements. Thus, for a strongly unequal $|Z_\mathrm{ACG}| \gg |Z_\mathrm{AC^-}|, R_\mathrm{ch}, R_\mathrm{drift}$, the measurements lead to $(C_\mathrm{dg} + C_\mathrm{sg}) = 2\ C_\mathrm{gg}$. If $|Z_\mathrm{d}| \approx |Z_\mathrm{s}| \gg R_\mathrm{ch}, R_\mathrm{drift}$, then Z_d and Z_s dominate in (16), (17) and cause an equal division of C_gg into $C_\mathrm{dg} = C_\mathrm{sg} = 0.5\ C_\mathrm{gg}$. This is typically the case in measurement setups which use longer cable extensions due to$|Z_\mathrm{cable}| \gg R_\mathrm{ch}$, R_drift.

Ideally, the magnitudes of $|Z_\mathrm{d}|, |Z_\mathrm{s}|$ must be as small as possible, i.e., $|Z_\mathrm{d}| \approx |Z_\mathrm{s}| \ll R_\mathrm{ch}, R_\mathrm{drift}$. The influence of wL_d and wL_s of the drain and source package reactances is considered small at low frequencies such as 30 kHz. Accordingly, the disagreement of the gate capacitance characteristics with the relation (3) observed in [4], [12]–[16] can be ascribed to improper *DUT* connections, i.e., leaving the drain or source terminal floating, or high impedances $|Z_\mathrm{d}|, |Z_\mathrm{s}| \gg R_\mathrm{ch}, R_\mathrm{drift}$ of the *DUT* fixture.

To verify the accuracy of C–V measurements, the extracted C_sg can be compared for the bias conditions in accumulation, e.g., at $V_\mathrm{gs} = -10$ V, and in inversion, e.g., $V_\mathrm{gs} = 20$ V. In accumulation, $C_\mathrm{sg} \approx C_\mathrm{gg}$, but in inversion, C_sg is typically smaller than C_gg for SiC power MOSFETs (M1, M2), as it can be observed in Fig. 14. On the other hand, in the case of Si power MOSFETs (M3, M4), in inversion $C_\mathrm{sg} \approx C_\mathrm{gg}$, which can be related to a relatively large R_drift and correspond to the small extracted ratios $R_\mathrm{ch}/R_\mathrm{drift} \approx 0.15, 0.006$ (21).

The impact of Z_d and Z_s imposes criteria for selecting a measurement instrument. The measurement setup must provide a possibility to equivalently connect the 3- or 4-pins of the *DUT*, such that $|Z_\mathrm{d}|, |Z_\mathrm{s}| \ll R_\mathrm{ch}, R_\mathrm{drift}$. In addition, the instrument's ampere meter must not add to Z_d or Z_s.

The selection of the Keysight E4990A in combination with the test fixture 16047E provides a setup for minimal stray impedances Z_d and Z_s, which can almost be limited to the parasitic inductances of the MOSFET package. In comparison, direct RF-IV impedance analyzers such as the Keysight E4991B are not recommended for measurements of C_dg or C_sg since the condition $|Z_\mathrm{d}|, |Z_\mathrm{s}| \ll R_\mathrm{ch}, R_\mathrm{drift}$ cannot be achieved. A similar challenge arises when using network analyzers due to the characteristic impedance and impedance matching of the transmission line to typically 50 Ω, as shown in [13], which requires correct de-embedding. Finally, when using on-wafer gate capacitance measurements of MOS transistors, the impedances of the coaxial cables severely influence the current divider of $i_\mathrm{d}/i_\mathrm{s}$ during the MOSFET's ON-state.

The use of parametric curve tracers such as the Keithley 2600-PCT-4B [42] in combination with the impedance measurement unit Keithley 4210-CVU [43] or the Keysight B1505A, including the B1520A MFCMU [44], requires the use of external bias-Ts [10], [30], which distort the extracted capacitance values.

It should be noted that the deviation of $\varphi(Z_{\mathrm{dg}})$ and $\varphi(Z_{\mathrm{sg}})$ from -90 degree, shown in Section III-C, is insignificant if the lumped equivalent MOSFET gate capacitances are extracted from C_{gd} and C_{gs} measurements. In reverse polarity of v_{ac}, i.e., by connecting the gate to AC$^-$ and drain/source on either AC$^+$/ACG, the MOSFET's reverse transconductance ($\partial i_{\mathrm{g}}/\partial v_{\mathrm{sg}}|_{V_{\mathrm{ds}}}$) is negligible. This was confirmed by using a Keithley 4210-CVU [43] with a Keysight 16047E test fixture, which allows to apply a reverse polarity of the v_{ac} without changing the DC bias polarity. The Keithley 4210-CVU is a capacitance voltage unit, based on the autobalancing bridge measurement technique similar to Keysight E4990A, however, operating in a narrower frequency range from 1 kHz to 10 MHz.

VII. Conclusion

This article reviews the requirements and specifies the conditions for accurate characterization of the interterminal gate capacitances of power MOSFETs, which is highly useful for device design optimization and accurate parametrization of device compact models. A measurement method for extracting the ratio $R_{\mathrm{ch}}/R_{\mathrm{drift}}$ of power MOSFETs is proposed, which can be used to increase the knowledge on the design of COTS discrete SiC power MOSFETs. The main conclusions are summarized in the following. 1) Capacitance measurements of packaged power MOSFETs should not predominantly be performed at 1 MHz, as typically specified in datasheets, but rather at lower frequencies in the order of some 10 kHz to minimize the influence of the parasitic effects.

2) The influence of the MOSFET's transconductance leads to a deviation in $\varphi(Z_{\mathrm{dg}})$ and $\varphi(Z_{\mathrm{sg}})$ for $V_{\mathrm{gs}} \geq V_{\mathrm{th}}$, which results in distorted capacitance values when extracted by the series-equivalent model C_{s}. Therefore, the lumped equivalent capacitances of the MOSFET should be modeled by the parallel equivalent capacitance model C_{p} when extracted from measured Z_{dg} and Z_{sg} characteristics.

3) The contributions of R_{ch} and R_{drift} to the overall $R_{\mathrm{ds,on}}$ of power MOSFETs can be directly derived for any 3- and 4-pin device from the values of the MOSFET's C_{dg} and C_{sg} characteristics.

4) The measurement accuracy can significantly be hampered by the impedance of the measurement setup, i.e., unsuitable connection of the *DUT* or the test fixture. Consequently, only specific standard measurement instruments employing an autobalancing bridge measurement technique are recommended for characterization of interterminal gate capacitances of MOS transistors.

The presented analysis represents a valuable input toward standard guidelines on the C–V characterization of power MOSFETs.

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