Design of High Step-Down Ratio Isolated Three-Level Half-Bridge DC–DC Converter With Balanced Voltage on Flying Capacitor

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***Abstract*—A high step-down ratio three-level half-bridge (TLHB) dc–dc converter with a current-doubler rectifier is presented for power conversion from a 48-to-60-V input to a 0.5-to-1-V output. The proposed TLHB topology and operation employed on the primary side improve the power-conversion efficiency by reducing the switching loss while minimizing the turn ratio of the transformer by converting the input voltage down to one quarter on the primary side. Moreover, it reduces the voltage stress on switches by half, thereby enabling the converter to be implemented with Si transistors with low breakdown voltage. The designed TLHB gate-driver IC minimizes the delay mismatches in gate drivers and mitigates the effect of the leakage inductance of the transformer, reducing the voltage imbalance on the flying capacitor without any balancing scheme in the controller. The proposed dc–dc converter implemented with 40-V Si transistors for the primary-side switches achieves 92.8% peak efficiency while supporting the maximum load current of 60 A and the maximum input voltage of 60 V. The converter with the proposed TLHB gate driver IC shows less than 0.8% voltage imbalance on the flying capacitor.**

***Index Terms*—Data center power, DC-DC power converters, driver circuits, gate drivers, integrated circuits, multilevel converters, power conversion.**

I. Introduction

USE of 48-V dc voltage has been increasing recently for server, telecommunication, and automotive applications. Compared with the traditional 12-V system, the 48-V system has a lower distribution loss since the current is reduced by a factor of four; therefore, the distribution loss is reduced by 16 times. Moreover, the 48-V system can support higher power and offers a comparable safety requirement [1]. As a result, researchers of the companies such as Google and Facebook have announced an open rack standard using 48-V dc power-delivery architecture for the server application [2], [3].

Fig. 1 shows several rack architectures with estimated power-conversion efficiencies [2], [4], [5]. Typically, the data center consumes about 15 kW per rack and the rack power density will continue to increase in the future [4], [6]. Therefore, the traditional 12-V system in Fig. 1(a) requires a large current of thousands of amperes to power the servers, which increases the overall power cost significantly due to the large distribution loss. The 48-V power-delivery architectures shown in Fig. 1(b) and 1(c) can reduce the power distribution loss significantly. The cascade architecture in Fig. 1(b) can be implemented readily since the existing 12-V system can be used. It requires only an intermediate bus converter (IBC) to convert the bus voltage of 48 V down to 12 V. Although it reduces the distribution loss, the overall power-conversion efficiency is not optimal due to the additional power-conversion stage. To overcome such a drawback, many research results that improved the efficiency of the IBC have been reported, showing peak efficiencies of about 97% or more [6]–[9]. However, even with the high-efficiency IBC, further improvement in overall efficiency is limited due to the inherent structural limitation of the cascade topology [10].

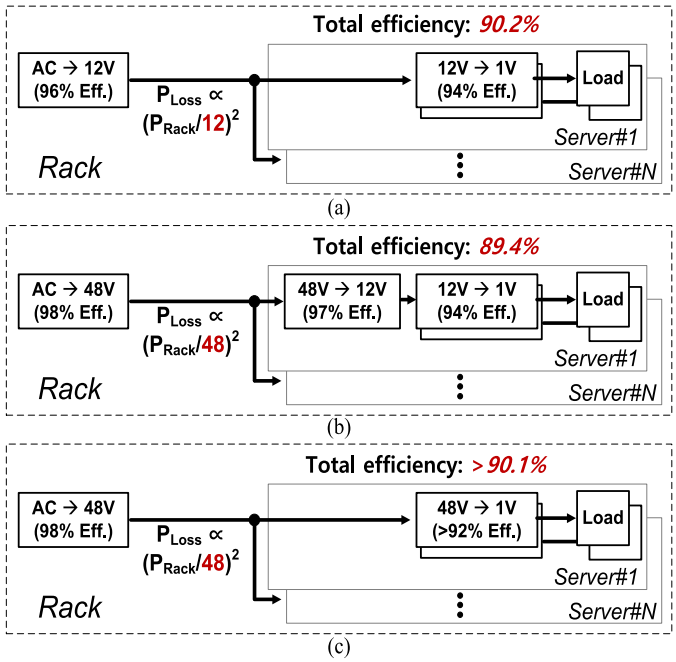

Fig. 1. Power delivery architectures with the estimated power-conversion efficiencies for server applications.

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Recently, the direct conversion from 48 V to the load supply voltage such as 1 V has emerged to improve the overall energy efficiency. As shown in Fig. 1(c), if high-efficiency 48-V point-of-load (PoL) dc–dc converters are employed, the overall power-conversion efficiency can be improved while the distribution loss is minimized. However, the 48-V PoL dc–dc converter has significant design challenges due to the high step-down conversion ratio and the high output current required. Thanks to the recent development of wide bandgap devices, various high-efficiency dc–dc converters using high-quality GaN transistors have been employed for the 48-V PoL converter [10]–[17]. The previous work presented in [11] shows the possibility of a buck converter with GaN transistors at 48 V, but it still shows a low peak efficiency of 82.9% and supports a low output current of 12 A.

To improve the efficiency, several nonisolated hybrid converters have been proposed to reduce the switching loss [10], [12]–[15], [18]. The hybrid converter uses capacitors as a capacitive divider for the input voltage, reducing the switching loss and increasing the duty cycle. Although the hybrid converter requires many passive devices and switches and increases the design complexity, it can provide a high power density thanks to the higher energy density of capacitors than magnetic components [12]. The double step-down converter [10] is similar to the two-phase buck converter except for an additional capacitor. With the additional capacitor, the voltage stresses and the switching voltages of the switches are reduced by half, reducing the switching loss compared to the conventional buck converter. However, halving the switching voltage at 48 V is still not sufficient to support the high output current of tens of amperes or more, since the switches of the converter should support half of the load current; it requires large-size switches, resulting in high switching losses. As a result, the converter provides the maximum current of only up to 1.5 A. A dual inductor hybrid converter based on the Dickson switched-capacitor converter [13] employs five flying capacitors to reduce the switching voltage and thus the voltage stress to one-sixth of the input voltage. However, the split-phase control to improve efficiency increases the controller complexity and the converter provides a low load current of 10 A. A dual-phase multi-inductor hybrid converter is proposed to raise the maximum output current of the nonisolated hybrid converter [14]. It achieves the maximum output current of 100 A and a power density of 440 W/in^3 using four inductors, three flying capacitors, and eight GaN switches while showing a moderate peak efficiency of 90.9%.

A two-stage 48-V converter using a dual active bridge derived hybrid switched capacitor in the first stage and a three-phase buck converter in the second stage is proposed in [15]. The first stage based on the hybrid architecture converts the input to a low voltage with minimal switching losses, and the second stage with the low input voltage is implemented with multiphase architecture to support a high output current. It achieves a peak efficiency of 91.9% and a maximum output current of 55 A. Another two-stage hybrid 48-V converter with an interleaved charge pump in the first stage and multiphase series-capacitor buck converters in the second stage achieves a peak efficiency of 93.7%, a maximum current of 400 A [18]. The two-stage converters in [15] and [18] achieve high power densities of 470 W/in^3 and 341.9 W/in^3, respectively, although the converters require many capacitors, inductors, and switches and use two or more controllers for each stage.

On the other hand, several isolated dc–dc converters with high output current capability have been proposed for 48-V PoL converters [16], [17], [19]–[22]. The transformer provides galvanic isolation and converts the input voltage to a low secondary voltage while the secondary-side transistors with low breakdown voltage can support high output current with low power loss. Although a sigma converter using GaN transistors [16] achieves a high peak efficiency of 93.4% and supports 80-A output current, it uses a transformer with a high turn ratio of 40:1 and requires many switches, which limits the conversion ratio. Besides, although the GaN transistor promises higher performance than the Si transistor, it entails higher cost and suffers from reliability issues [23], [24]. An isolated active-clamp forward converter in [19] is implemented with high breakdown-voltage Si transistors and a transformer with a 12:1 turn ratio and provides a 60-A maximum current but shows a low peak efficiency of 89.5%. A quasi-resonant full-bridge converter in [21] shows a high peak efficiency of 93.2% using Si transistors. The phase-shift full-bridge converter with the additional resonant inductor and capacitor provides zero-voltage switching (ZVS) and zero-current switching (ZCS) for both the primary and secondary side transistors. However, the converter is implemented with a transformer with a high turn ratio of 9:1 and the ZVS and ZCS require additional control schemes. An isolated stacked half-bridge (HB) converter in [22] is implemented with a hybrid architecture on the primary-side HB converter to simplify the transformer implementation and to reduce voltage ratings of switches. The proposed primary-side hybrid HB converter can reduce the primary-side transformer voltage by a quarter, as a result, the turn ratio of the transformer can be minimized. However, it requires two more capacitors for the HB converter and two switches operate simultaneously in one switching event, resulting in increased switching power loss. The converter achieves a 92% peak efficiency and a 45-A maximum output current using both Si and GaN transistors.

This article presents a high-efficiency three-level HB (TLHB) dc–dc converter with a current-doubler rectifier [25]. The proposed TLHB topology based on the hybrid architecture allows the use of switches with lower breakdown voltage, and a current-doubler rectifier provides high output current with low power loss. With the proposed TLHB operation of the converter, the TLHB converter generates a quarter of the input voltage at the primary-side transformer in contrast with half of the input of the conventional TLHB operation, and as a result, it can support a high step-down ratio dc–dc conversion with a low turn-ratio transformer and minimize the hard-switching losses without ZVS. The proposed TLHB gate-driver IC is designed for minimizing the voltage imbalance of the flying capacitor and supporting straightforward implementation using off-the-shelf HB solutions. The remainder of this article is organized as follows. Section II introduces the background of this work. In Section III, the operational principle and analysis of the proposed dc–dc converter architecture are presented. Section IV describes

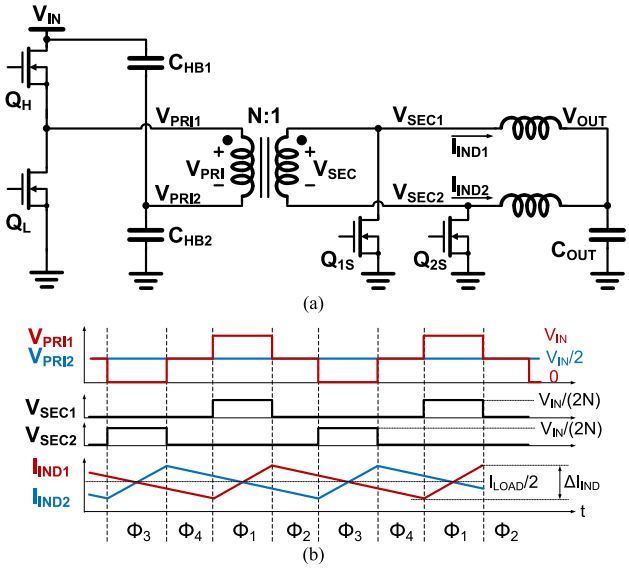


Fig. 2. Conventional HB dc–dc converter with a current-doubler rectifier. (a) Block diagram. (b) Timing diagram.

the circuit implementation of the proposed TLHB gate-driver IC. The measurement results are provided in Section V and a conclusion is given in Section VI.

II. Background

A. HB DC–DC Converter With a Current-Doubler Rectifier

One of the well-known architectures for the high step-down ratio dc–dc converter with a high output current capability is an HB dc–dc converter with a current-doubler rectifier as shown in Fig. 2(a) [17], [26], [27]. Instead of the full-bridge architecture, the converter is implemented with an HB topology on the primary side. For the secondary side, the current-doubler rectifier, which is similar to a two-phase interleaved buck converter, is employed to support high output current. The converter operates in four steps of Φ_1, Φ_2, Φ_3, and Φ_4 as shown in the timing diagram of Fig. 2(b). While the voltage on the primary-side capacitors, C_{HB1} and C_{HB2}, keeps half of the input voltage, the voltage of the primary-side switching node V_{PRI1} changes between 0 V, 1/2·V_{IN}, and V_{IN}. With the primary-side operations, the two secondary-side inductors are magnetized and demagnetized, and the output voltage is regulated. Since the primary-side transformer voltage V_{PRI} is reduced by half, the HB can reduce the turn ratio of the transformer and increase the duty ratio of the converter. As a result, one of the previous works achieved a 90.7% peak efficiency using GaN transistors [17]. However, as shown in the power-loss breakdown of the conventional HB dc–dc converter with a current-doubler rectifier using Si transistors in Fig. 3, it still has room for improvement in minimizing the switching losses of the primary side.

B. GaN Transistors Versus Si Transistors

It is well known that GaN transistors have better figure-of-merits (FoMs) compared with the Si transistors for high-voltage applications [28], [29]. However, the GaN transistor is generally

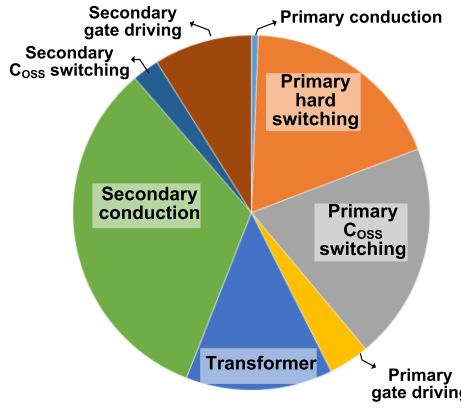


Fig. 3. Power-loss breakdown of the conventional HB dc–dc converter with a current-doubler rectifier at the condition of $V_{\mathrm{IN}} = 48$ V, $V_{\mathrm{OUT}} = 1$ V, $I_{\mathrm{LOAD}} = 20$ A, and a switching frequency of 400 kHz.

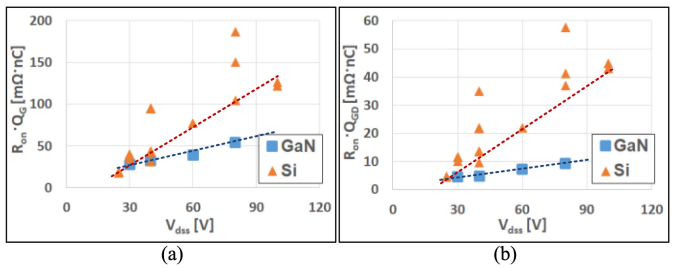


Fig. 4. Comparison of Si and GaN transistors of Infineon and EPC according to the breakdown voltages. (a) Q_{G} ·R_{on}. (b) Q_{GD}·R_{on}.

expensive and has a reliability issue. The FoM comparison according to the breakdown voltages of transistors is depicted in Fig. 4. The graphs show that the lower the breakdown voltage is, the smaller the benefit of GaNs is. Therefore, if the converter is implemented with Si transistors with lower breakdown voltages like 30 or 40 V instead of 60 or 80 V, it can achieve a competitive performance without using GaN transistors. In this work, discrete Si transistors are employed for the power switches of the dc–dc converter instead of discrete GaN transistors.

C. TLHB DC–DC Converter

To minimize the voltage stress of the switch, various TLHB topologies have been proposed in [30]–[36], and a flying capacitor TLHB converter is shown in Fig. 5. With the four-step operation in Fig. 5(b), the conventional TLHB converter generates three output voltages V_{IN}, 1/2·V_{IN}, and 0 V, which are the same as the conventional HB converter in Fig. 2. Since the flying capacitor keeps the voltage of 1/2·V_{IN}, the voltage stresses of the four switches, $\mathrm{Q_{H1}}$, $\mathrm{Q_{H2}}$, $\mathrm{Q_{L2}}$, and $\mathrm{Q_{L1}}$, are reduced to half of the input voltage, and as a result, the TLHB converter can be implemented with the lower breakdown-voltage transistors compared to the conventional HB converter. Furthermore, the TLHB converter can employ ZVS to all switches eliminating turn-ON losses and $\mathrm{C_{OSS}}$ switching losses that are dominant losses of the conventional HB dc–dc converter, as shown in Fig. 3. However, supporting ZVS requires complicated control circuits and the large leakage inductance of the transformer for

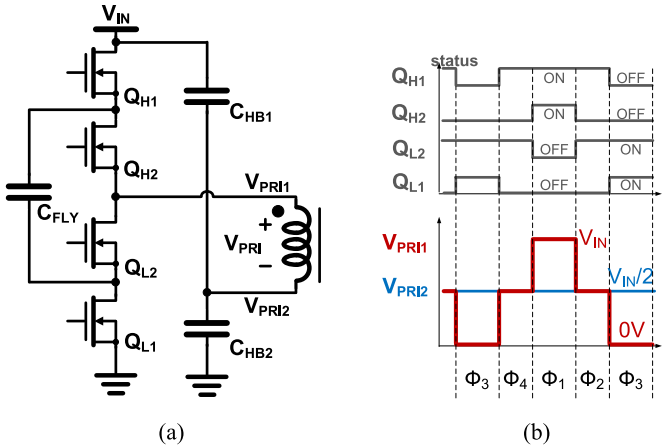


Fig. 5. (a) Flying-capacitor TLHB topology of the primary side. (b) Conventional operation of the TLHB converter.

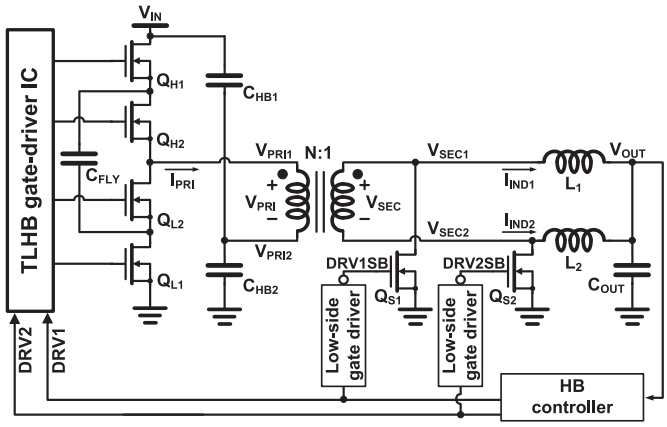


Fig. 6. Overall system architecture of the proposed dc–dc converter.

a wide ZVS range causes a large circulating power loss [32], [34]–[36]. Since the conversion ratio of 1/2 of the primary-side TLHB with the conventional operation is the same as that of the conventional HB converter, the conventional TLHB does not have an additional advantage for a high step-down ratio dc–dc conversion.

III. Proposed System Architecture

A. System Architecture and Operation

The proposed TLHB dc–dc converter with a current-doubler rectifier is shown in Fig. 6. The proposed converter is similar to the previous HB dc–dc converter with a current-doubler rectifier except for the primary-side topology. The current-doubler rectifier on the secondary side is incorporated to support the high-output current. The flying-capacitor TLHB architecture is employed for the primary side so that the primary-side switches are implemented with transistors with low-breakdown voltages. To support the proposed TLHB operation of the primary side, the TLHB gate-driver IC is proposed and designed in this work. A loop-controller IC and two low-side gate drivers for the secondary-side switches are implemented with the off-the-shelf commercial ICs used for the conventional HB architecture. Discrete Si transistors are employed for power switches of both the primary side and the secondary side.

Compared with the four-step operation of the conventional HB and TLHB, the proposed TLHB operation requires the eight-step operation to charge and discharge the flying capacitor and to generate the primary-side transformer voltage V_{PRI} of $1/4{\cdot}V_{\mathrm{IN}}$ as shown in Fig. 7. The timing diagram of the proposed converter with the eight-step operation is depicted in Fig. 8. Compared with the conventional TLHB with ZVS, the proposed TLHB operates with the hard-switching scheme.

During Φ_1, C_{FLY} is charged according to I_{IND1} while C_{HB1} and C_{HB2} are discharged and charged, respectively. On the secondary side, L_1 and L_2 are magnetized and demagnetized, respectively. The voltages of C_{FLY} and V_{PRI2} become $1/2{\cdot}V_{\mathrm{IN}}$ and $1/4{\cdot}V_{\mathrm{IN}}$, respectively, in the steady state over many cycles of operation. Therefore, the primary-side transformer voltage V_{PRI} becomes $1/4{\cdot}V_{\mathrm{IN}}$, which is halved compared with the conventional HB topology. During Φ_2, the converter demagnetizes two inductors. In this period, the primary side and the transformer do not affect the overall operation of the converter. The behavior of Φ_3 works almost in the opposite of Φ_1. During Φ_3, L_1 and L_2 are demagnetized and magnetized, respectively, whereas C_{HB1} and C_{HB2} are charged and discharged, respectively, according to I_{IND2}. However, C_{FLY} is not affected during Φ_3 and V_{PRI} becomes $-1/4{\cdot}V_{\mathrm{IN}}$. The operation of Φ_4 is almost the same as Φ_2 while the different switch is turned ON at the primary side. The next four steps, Φ_5, Φ_6, Φ_7, and Φ_8, are repeated almost identically to the previous four steps Φ_1, Φ_2, Φ_3, and Φ_4 except for discharging C_{FLY}. For the charge balance, C_{FLY} is discharged according to I_{IND1} during Φ_5. As a result, charging and discharging C_{FLY} are related to the current of L_1 only; it is advantageous for the voltage balance of C_{FLY}. In the case of C_{HB1} and C_{HB2}, charging and discharging are related to both L_1 and L_2; it is the same as the conventional HB converter. Through the proposed eight-step operation, the proposed dc–dc converter regulates the output voltage while satisfying the charge balance of C_{FLY}, C_{HB1}, and C_{HB2} and the volt–second balance of L_1 and L_2.

Compared to the conventional TLHB operation, which generates three-level voltages of V_{IN}, $1/2{\cdot}V_{\mathrm{IN}}$, and 0 V, the proposed TLHB converter generates $1/2{\cdot}V_{\mathrm{IN}}$, floating, and 0 V, and as a result, the primary-side transformer voltage becomes $1/4{\cdot}V_{\mathrm{IN}}$. It means that the primary-side TLHB converts the input voltage down to $1/4{\cdot}V_{\mathrm{IN}}$ in contrast with $1/2{\cdot}V_{\mathrm{IN}}$ of the conventional HB and TLHB. Therefore, the proposed isolated TLHB converter can further reduce the turn ratio of the transformer and is suitable for the dc–dc converter with a high step-down ratio.

B. DC Characteristics

The timing diagram in Fig. 8 shows the voltage and current characteristics in the steady state according to the driving signals, DRV1 and DRV2, from the controller. According to the volt-second balance law of L_1 and L_2 during Φ_1–Φ_8

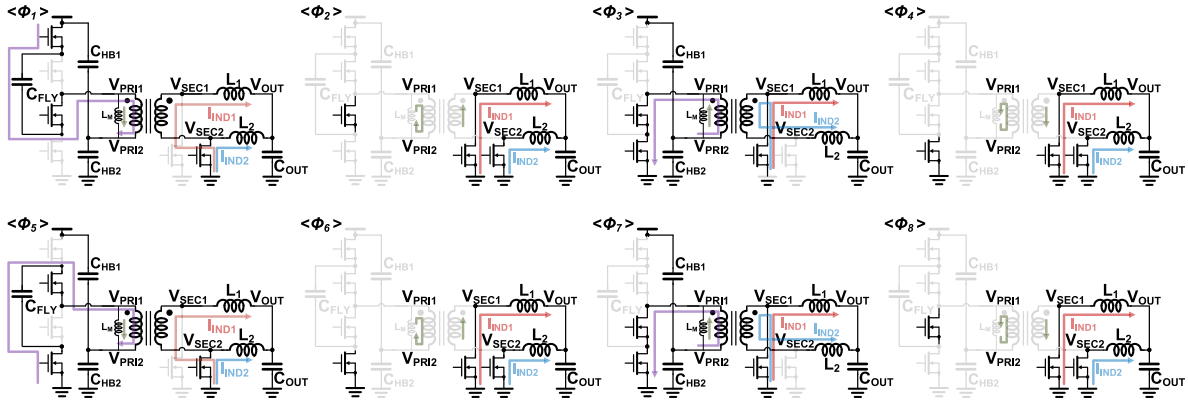


Fig. 7. Operation of the proposed converter in eight steps of Φ_1, Φ_2, Φ_3, Φ_4, Φ_5, Φ_6, Φ_7, and Φ_8.

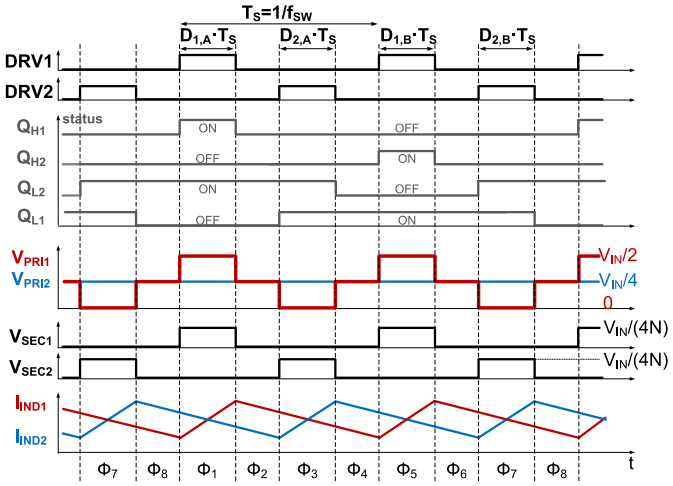


Fig. 8. Timing diagram of the proposed dc–dc converter.

$$\left(\frac{V_{\rm IN}-V_{\rm CFLY}-V_{\rm PRI2}}{N}-V_{\rm OUT}\right)D_{1,A}-V_{\rm OUT}\left(1-D_{1,A}\right)$$
$$=-\left(\frac{V_{\rm CFLY}-V_{\rm PRI2}}{N}-V_{\rm OUT}\right)D_{1,B}+V_{\rm OUT}\left(1-D_{1,B}\right) \quad (1)$$

$$\left(\frac{V_{\rm PRI2}}{N}-V_{\rm OUT}\right)D_{2,A}-V_{\rm OUT}\left(1-D_{2,A}\right)$$
$$=-\left(\frac{V_{\rm PRI2}}{N}-V_{\rm OUT}\right)D_{2,B}+V_{\rm OUT}\left(1-D_{2,B}\right) \quad (2)$$

where $V_{\rm CFLY}$ is the voltage of $C_{\rm FLY}$ and N is the turn ratio of the transformer. Note that the average currents of both inductors, L_1 and L_2, are assumed to be the same and the resistances of all components are ignored for simplicity of the analysis. From (1) and (2), the output voltage is determined as

$$V_{\rm OUT}=\frac{D_{1,A}V_{\rm IN}-\left(D_{1,A}-D_{1,B}\right)V_{\rm CFLY}-\left(D_{1,A}+D_{1,B}\right)V_{\rm PRI2}}{2N} \quad (3)$$

$$V_{\rm OUT}=\frac{\left(D_{2,A}+D_{2,B}\right)V_{\rm PRI2}}{2N}. \quad (4)$$

Besides, according to the volt–second balance law of the magnetizing inductance L_M

$$\left(V_{\rm IN}-V_{\rm CFLY}-V_{\rm PRI2}\right)D_{1,A}+\left(V_{\rm CFLY}-V_{\rm PRI2}\right)D_{1,B}$$
$$=V_{\rm PRI2}\ \left(D_{1,B}+D_{2,B}\right) \quad (5)$$

$$V_{\rm PRI2}=\frac{D_{1,A}}{D_{1,A}+D_{1,B}+D_{2,A}+D_{2,B}}$$
$$V_{\rm IN}-\frac{D_{1,A}-D_{1,B}}{D_{1,A}+D_{1,B}+D_{2,A}+D_{2,B}}V_{\rm CFLY}. \quad (6)$$

In the steady state of the proposed converter, the duty ratio $D=D_{1,A}=D_{1,B}=D_{2,A}=D_{2,B}$, and as a result

$$V_{\rm PRI2}=\frac{1}{4}\,V_{\rm IN}. \quad (7)$$

Therefore, $V_{\rm PRI2}$ is determined by the input voltage regardless of the values and ratio of $C_{\rm HB1}$ and $C_{\rm HB2}$ as with the conventional HB topology; the ratio of $C_{\rm HB1}$ and $C_{\rm HB2}$ determines a peak-current level of the input. From (4) and (7)

$$V_{\rm OUT}=\frac{1}{4N}\,D\cdot V_{\rm IN}. \quad (8)$$

The output voltage is determined by the turn ratio of the transformer and the duty cycle, similar to the conventional HB or the full-bridge dc–dc converter, while the input voltage is divided by four due to the TLHB topology.

C. Topology Comparison and Power-Loss Breakdown

Table I compares the proposed TLHB topology with the conventional primary-side topologies with the same transformer turn ratio N: a full bridge, an HB, and the conventional TLHB. Thanks to the three-level architecture, the voltage stress of the primary-side transistors is reduced by half compared to the full-bridge and HB topologies. As a result, 40-V Si transistors are employed instead of 80-V GaN transistors for the primary-side switches in this work. The proposed TLHB generates the primary-side voltage $V_{\rm PRI}$ as $1/4{\cdot}V_{\rm IN}$, which means the primary-side TLHB converter operates as a 4:1 voltage divider. While the full bridge and the conventional TLHB can reduce the turn-ON and $C_{\rm OSS}$ switching losses by ZVS, the proposed TLHB minimizes switching losses with a hard-switching scheme by

TABLE I
PRIMARY-SIDE TOPOLOGY COMPARISON

	Full bridge	Half bridge	Conventional TLHB	Proposed TLHB
Voltage stress of switch	V_{IN}	V_{IN}	$1/2 \cdot V_{IN}$	**$1/2 \cdot V_{IN}$**
Primary-side V_{PRI} (Conversion ratio)	V_{IN}	$1/2 \cdot V_{IN}$	$1/2 \cdot V_{IN}$	**$1/4 \cdot V_{IN}$**
Primary-side switching loss	$\propto f_{SW} \cdot 1/2 \cdot V_{IN} \cdot I_{PRI}$ (ZVS)	$\propto f_{SW} \cdot 1/2 \cdot V_{IN} \cdot I_{PRI}$ (hard switching)	$\propto f_{SW} \cdot 1/4 \cdot V_{IN} \cdot I_{PRI}$ (ZVS)	**$\propto f_{SW} \cdot 1/4 \cdot V_{IN} \cdot I_{PRI}$ (hard switching)**
# of switches	4	2	4	**4**
Secondary-side V_{SEC}	$1/N \cdot V_{IN}$	$1/(2N) \cdot V_{IN}$	$1/(2N) \cdot V_{IN}$	**$1/(4N) \cdot V_{IN}$**
Required f_{sw} (or Required N)	High	Medium	Medium	**Low**

Bold values shows the proposed work.

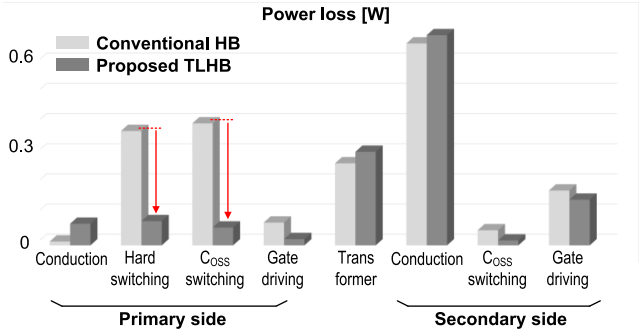


Fig. 9. Power-loss comparison at the condition of $V_{\mathrm{IN}} = 48$ V, $V_{\mathrm{OUT}} = 1$ V, and $I_{\mathrm{LOAD}} = 20$ A.

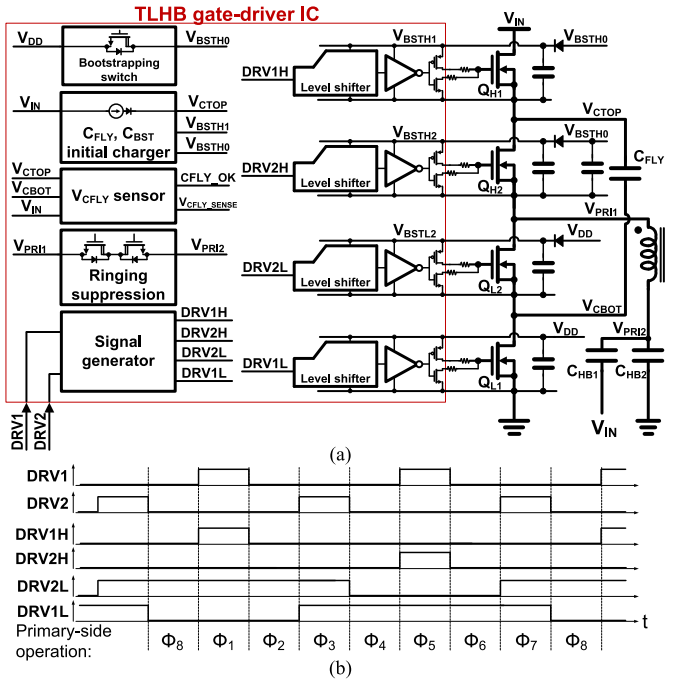


Fig. 10. (a) Block diagram of the proposed TLHB gate driver IC with primary-side switches and bootstrap circuits. (b) Input and output timing diagram of the signal generator.

reducing turn-ON and turn-OFF switching voltages down to $1/4 \cdot V_{\mathrm{IN}}$; since the ZVS converter has the turn-OFF switching loss, the primary-side switching loss of the proposed TLHB is similar with the conventional TLHB with ZVS. Moreover, since the required switching frequency is lower with the same the transformer turn ratio N, the switching losses of both the primary side and secondary side can be further minimized; the inductor current ripple is reduced due to the low secondary-side voltage V_{SEC}, and as a result, the required switching frequency is reduced. Overall, the proposed TLHB topology can improve the efficiency by reducing switching losses without soft-switching schemes.

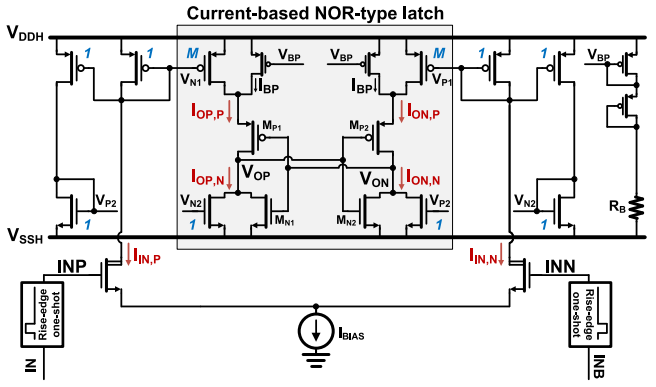
The power loss of the proposed TLHB dc–dc converter with a current-doubler rectifier is compared with the power loss of the conventional HB converter, as shown in Fig. 9. For a fair comparison, the calculations are based on 80-V Si transistors, BSZ070N08LS5, for the conventional HB and 40-V Si transistors, BSC059N04LS6, for the proposed TLHB, while the 25-V Si transistors are used for the secondary sides of both HB and TLHB topologies. The turn ratios of the transformers are 5:1 and 4:1 and switching frequencies are 400 kHz and 333 kHz for the HB and the TLHB, respectively, taking into account the current ripples of the inductors. The conduction loss of the TLHB dc–dc converter is slightly increased due to the series connection of the primary-side switches and the high duty ratio; the high duty ratio increases the periods of Φ_1, Φ_3, Φ_5, and Φ_7, when only one of the secondary-side switches, Q_{S1} or Q_{S2}, is turned ON. As shown in Fig. 7, the current flows through only one of the secondary-side switches during these periods, so the conduction loss of the secondary-side switches is increased. However, the switching loss is greatly decreased, thereby overall efficiency is increased sufficiently; in this calculation, the efficiency of the proposed converter is improved by 2.7%.

IV. PROPOSED TLHB GATE-DRIVER IC

A. Design Considerations and Overall Architecture

In this work, the TLHB gate-driver IC is designed for the proposed dc–dc converter. All other components including the HB controller are implemented with the off-the-shelf commercial ICs. The block diagram of the proposed gate-driver IC is shown in Fig. 10(a). It includes four gate drivers controlling four switches and the signal generator that converts two input signals, DRV1 and DRV2, from the conventional HB controller into four output signals, DRV1H, DRV2H, DRV2L, and DRV1L, for the three-level operation, as shown in Fig. 10(b). The TLHB gate-driver IC operates with a supply voltage V_{DD} of 5 V used as the controller power of the proposed dc–dc converter.

Since the three-level architecture requires keeping the voltage of C_{FLY} at half of the input voltage for the output-regulation quality and reliability of the converter, the voltage balance on C_{FLY} should be taken into account in the circuit design. Previous works monitor the flying-capacitor voltages or inductor currents and adapt the pulse width to balance the voltages of flying capacitors [37]–[39]. Since these schemes require adjusting the loop control, the controller should be modified. The proposed converter with the TLHB gate-driver IC is designed to minimize the voltage imbalance of C_{FLY} without redesigning the conventional HB loop controller. The major cause of the voltage imbalance on C_{FLY} is the timing mismatch between gate-driver signals



(a)

INP	INN	$I_{OP,P}$	$I_{OP,N}$	$I_{ON,P}$	$I_{ON,N}$	V_{OP}	V_{ON}
L	L	I_{BP}	0	I_{BP}	0	latch	latch
L	H	I_{BP}	I_{BIAS}	$M \cdot I_{BIAS}$	0	L	H
H	L	$M \cdot I_{BIAS}$	0	I_{BP}	I_{BIAS}	H	L
H	H	$M \cdot I_{BIAS}/2$	$I_{BIAS}/2$	$M \cdot I_{BIAS}/2$	$I_{BIAS}/2$	latch	latch

* $I_{BIAS} \gg I_{BP}$

** Logical states of M_{P1}, M_{P2}, M_{N1}, and M_{N2} are ignored

(b)

Fig. 11. Proposed fully differential dynamic level shifter using the current-based NOR-type latch. (a) Block diagram. (b) Relationship between input and output.

[40]–[42], especially due to the combination of the level-shifter delay mismatch and the bootstrapped voltage mismatch [43]. In this work, if the periods of Φ_1 for charging C_{FLY} and of Φ_5 for discharging C_{FLY} are not the same, the voltage imbalance on C_{FLY} occurs, resulting in the flying capacitor voltage not being kept at $1/2 \cdot V_{IN}$. Moreover, the transformer leakage inductance can exacerbate the voltage imbalance in the proposed topology. Therefore, the proposed gate-driver IC is designed to minimize the delay mismatch and the effect of leakage inductance. Furthermore, the initial charging circuit of C_{FLY} and bootstrapping capacitors and the appropriate start-up sequence are designed for the reliability of the proposed converter.

B. High-Reliable Dynamic Level Shifter

Since the operating voltages of the four-level shifters in the gate-driver IC are all different, the delay mismatches in level shifters can occur, resulting in voltage imbalance on C_{FLY}. To minimize the delay mismatch, this work proposes a fully differential current-based level shifter, as shown in Fig. 11(a). To reduce the delay of the level shifter, the bias current should be increased, causing large power consumption. Therefore, the pulsed input signals with a large bias current are employed and the output latch stage is used to maintain the output voltage when both input signals are low. However, the conventional output latch stage using the voltage-based cross-coupled inverters may be subject to malfunction due to the high dv/dt slope of V_{DDH} and V_{SSH}; during the voltage transition with the high dv/dt slope, the latch operates as if both input signals are high. Although several level shifters have been proposed to overcome the difficulties, the speed of the level shifter is limited by the maximum dv/dt slope; the level shifter in [44] includes several stages from input to output, causing the increased overall delay. While the level

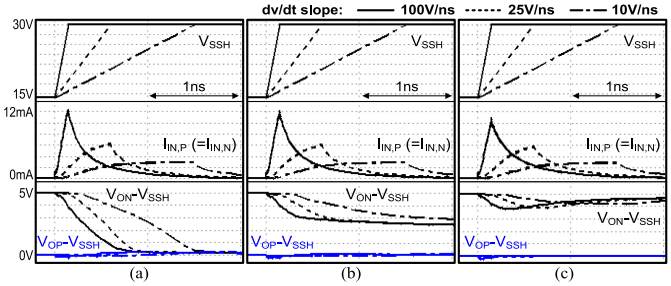


Fig. 12. Postlayout simulation results of the proposed level shifter according to the various dv/dt slopes of V_{DDH} and V_{SSH} for (a) $M = 0.5$, (b) $M = 1$, and (c) $M = 2$.

shifter in [45] proposes the use of a large damping resistor, which supports a high dv/dt slope, the delay is increased.

In this work, the current-based NOR-type latch is proposed, and the input-and-output relationship of the latch is shown in Fig. 11(b). When the input signals are different, the output is changed by flowing the sinking current, $I_{OP,N}$ or $I_{ON,N}$, not the sourcing current, $I_{OP,P}$ or $I_{ON,P}$. Since $I_{OP,N}$ and $I_{OP,P}$ ($I_{ON,N}$ and $I_{ON,P}$) are differential current according to the differential input, if $I_{OP,N}$ ($I_{ON,N}$) flows, $I_{OP,P}$ ($I_{ON,P}$) blocks. When both inputs are low, all currents do not flow. The proposed latch works like the conventional cross-coupled NOR latches, thus holding the output. Small current I_{BP} generated by current mirrors and a resistor R_B flows to prevent the floating nodes. When both inputs are high, both sinking currents and sourcing currents flow simultaneously. However, the proposed latch can hold the output, since the sourcing currents are M times larger than the sinking currents. The simulation results during V_{DDH} and V_{SSH} transitions according to the value of M are shown in Fig. 12. Due to the high dv/dt slope of V_{DDH} and V_{SSH}, the same amount of large $I_{IN,P}$ and $I_{IN,N}$ flows simultaneously. In the case of $M = 0.5$, the logical value of V_{ON} or V_{OP} is switched as shown in Fig. 12(a). As M increases, the voltage fluctuation of V_{ON} or V_{OP} is reduced, so the level shifter can maintain the output as shown in Fig. 12(c). Moreover, since the delay of the sinking current path is longer than the sourcing current path, the proposed level shifter can operate properly for any dv/dt slope such as 100 V/ns while the delay is around 0.9 ns.

C. Bootstrap Circuit

Designing bootstrap circuits for the proposed TLHB is a challenge since there is no way of directly delivering the power from V_{DD} to the high-side bootstrapping capacitor C_{H1}. In the conventional cascade bootstrap circuit for a multilevel converter as shown in Fig. 13(a), the diode voltage is accumulated, therefore, the bootstrapped voltage is determined as

$$\begin{aligned}(V_{BSTH1} - V_{SSH1}) &= (V_{BSTH2} - V_{SSH2}) - V_{DIODE} \\ &= V_{DD} - 3V_{DIODE} \end{aligned} \quad (9)$$

where V_{DIODE} is the voltage dropped by the diode. Due to the voltage drop by the diode, all bootstrapped voltages of C_{H1}, C_{H2}, C_{L2}, and C_{L1} are different, resulting in the delay mismatches

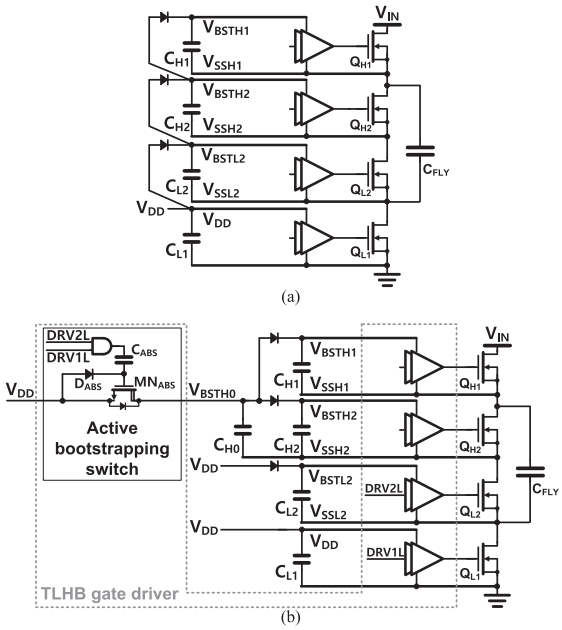


Fig. 13. Implementation of (a) the conventional cascade bootstrap circuit and (b) the proposed bootstrap circuit with an active switch.

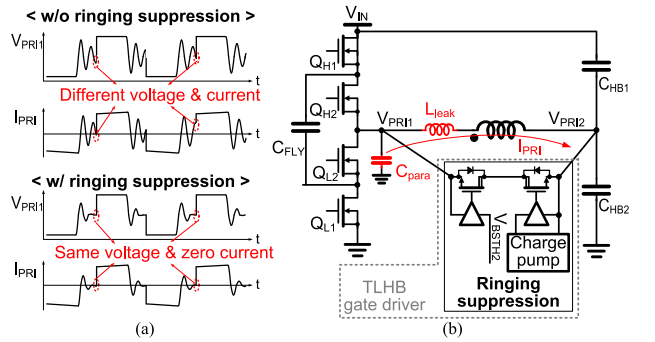


Fig. 14. (a) Waveforms of V_{PRI1} and I_{PRI} without and with the ringing suppression. (b) Implementation of the ringing suppression circuit of the TLHB gate-driver IC.

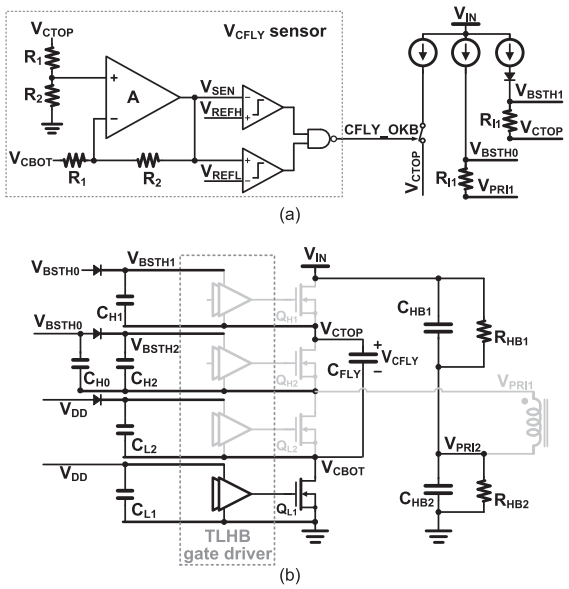


Fig. 15. (a) Implementation of the initial charger circuit in the TLHB gate-driver IC. (b) Primary-side operation of the converter in the disabled state.

in gate drivers. Therefore, the previous work in [43] employs external LDOs to make the bootstrapped voltages all the same.

In this design, the bootstrap circuit with an intermediate capacitor C_{H0} and an active bootstrapping switch is proposed as shown in Fig. 13(b). With the proposed circuit, the bootstrapped voltages are determined as

$$(V_{\mathrm{BSTH1}} - V_{\mathrm{SSH1}}) \approx (V_{\mathrm{BSTH2}} - V_{\mathrm{SSH2}}) = V_{\mathrm{DD}} - V_{\mathrm{DIODE}}. \tag{10}$$

As a result, the proposed circuit generates the same bootstrapped voltages for C_{H1} and C_{H2}, minimizing the voltage imbalance on C_{FLY}. In this work, since the only delay mismatch between driving Q_{H1} and Q_{H2} affects the voltage imbalance on C_{FLY}, V_{DD} is directly applied to the gate driver of Q_{L1}; an additional diode to C_{L1} can produce the same bootstrapped voltages of all the gate drivers. The active bootstrapping-switch circuit is implemented in the gate-driver IC. The LDMOS transistor MN_{ABS} is used for the switch while the switch is driven by the bootstrapping driver using a capacitor C_{ABS} and a diode D_{ABS}.

D. Ringing Suppression

The voltage imbalance on C_{FLY} can occur in the proposed dc–dc converter due to the leakage inductance of the transformer. As shown in Fig. 14(a), the voltage ringing at V_{PRI1} and the current ringing of I_{PRI} are caused by the leakage inductance of the transformer L_{leak} and the parasitic capacitance of the switches C_{para}, and they appear during Φ_2, Φ_4, Φ_6, and Φ_8. The ringing current can flow until the beginning of the next steps, Φ_1, Φ_3, Φ_5, and Φ_7. Especially, the ringing current at the beginning of Φ_1 and Φ_5 can affect the amount of charging and discharging current of C_{FLY}. Since the time duration of Φ_4 and Φ_8 can be varied by the control signals and the values of C_{para} are different for Φ_4 and Φ_8 due to the switch state, I_{PRI} at the beginning of Φ_1 and Φ_5 can be different. As a result, the difference in the ringing current at the beginning of Φ_1 and Φ_5 causes the voltage imbalance on C_{FLY}. To minimize the voltage and current ringing, this design employs the ringing suppression circuit in the TLHB gate-driver IC as shown in Fig. 14(b). The ringing suppression circuit implemented with two LDMOS transistors and a charge pump shorts the two input terminals of the primary-side transformer, V_{PRI1} and V_{PRI2}, during Φ_2, Φ_4, Φ_6, and Φ_8. Thus, the proposed converter minimizes the voltage and current ringings, resulting in $I_{\mathrm{PRI}} = 0$ at the beginning of Φ_1, Φ_3, Φ_5, and Φ_7.

E. Initialization Circuit and Startup Sequence

Even though the converter is disabled, C_{FLY} should keep the voltage at the proper level for the reliability of the switches with low breakdown voltage. Moreover, to activate the gate drivers, the bootstrapping capacitors should be charged. Fig. 15(a) shows the initial charger circuit of the proposed TLHB gate-driver

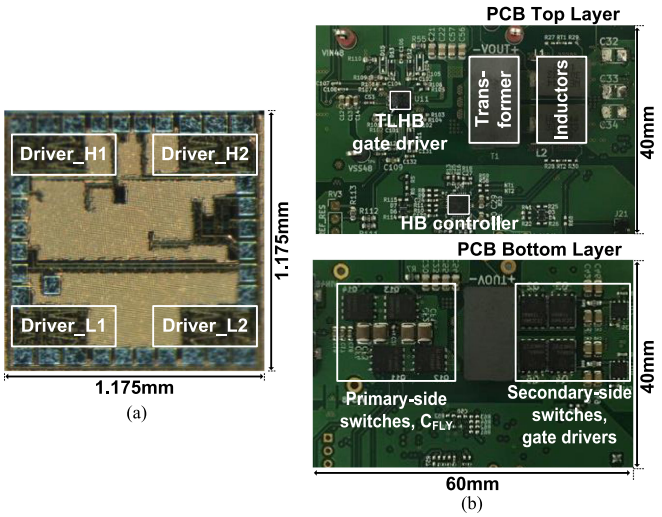


Fig. 16. (a) Chip photomicrograph of the TLHB gate-drive IC. (b) Photos of the PCB of the proposed TLHB dc–dc converter with a current-doubler rectifier.

IC. Simple current sources are used for charging the capacitors, C_{FLY}, C_{H0}, and C_{H1}, when the converter is disabled. To generate the appropriate voltage of C_{FLY}, the V_{CFLY} sensor is implemented with an analog subtractor. The output of the V_{CFLY} sensor is determined as $V_{\mathrm{SEN}} = (R_2/R_1) \cdot V_{\mathrm{CFLY}}$. Using two comparators and two reference voltages, V_{REFH} and V_{REFL}, the voltage of C_{FLY} is kept between V_{REFH} and V_{REFL}. The V_{CFLY} sensor operates not only in the disabled state but also in the normal operation to monitor the voltage of C_{FLY}. Besides, resistors R_{I1} and R_{I2} are employed to generate the appropriate voltages for the high-side bootstrapping capacitors C_{H0} and C_{H1}.

Fig. 15(b) shows the primary-side operation of the proposed dc–dc converter in the disabled state. With the proposed TLHB gate-driver IC, the low-side switch $\mathrm{Q_{L1}}$ is turned on to charge C_{FLY} and also the low-side bootstrapping capacitors, C_{L2} and C_{L1}, in the disabled state. R_{HB1} and R_{HB2} are employed to charge C_{HB1} and C_{HB2} in the disabled state for the reliable operation of the converter during the startup. At the beginning of the startup, the proposed level shifter first turns on the low-side switches, $\mathrm{Q_{L1}}$ and $\mathrm{Q_{L2}}$; namely, the converter starts at Φ_3. Therefore, C_{H0} and C_{H2} are charged first before driving $\mathrm{Q_{H2}}$. Then, C_{H1} is charged during Φ_5 before $\mathrm{Q_{H1}}$ is first driven.

V. Measurement Results

A prototype TLHB gate-driver IC is implemented in the 0.18-μm BCD process and Fig. 16(a) shows the photomicrograph of the chip with a die area of 1.38 mm^2. The test PCB of the proposed dc–dc converter is shown in Fig. 16(b). The proposed converter uses 40-V Si transistors for the primary side and 25-V Si transistors for the secondary side to support the maximum input voltage of 60 V while employing two 330-nH inductors, the flying capacitors of 40 μF total, and a 4:1 planar transformer on an 8-layer PCB. A commercial HB controller with the current-balancing function that minimizes the current mismatch between two inductor currents of the secondary side

TABLE II
Components List

Item	Part information
Primary-side switches	BSC059N04LS6 (40 V, 5.9 mΩ)
Secondary-side switches	BSC009NE2LS5I (25 V, 0.95 mΩ)
Secondary-side gate drivers	UCC27512
Controller	TPS53632G
C_{FLY}	10 uF x 4
C_{OUT}	47 uF x 8
HB capacitors	4.7 uF x 8
Inductors	330nH (0.37 mΩ) x 2
Transformer	ER18/3/10 (PC200)

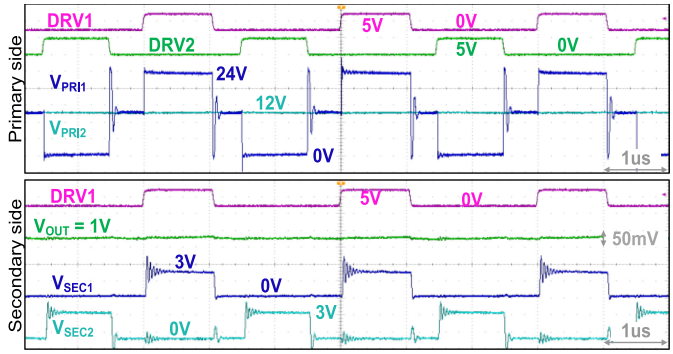


Fig. 17. Measured steady-state waveforms of the proposed dc–dc converter.

is implemented for the loop control. The controller senses the secondary-side average inductor currents and balances the currents of each inductor by adjusting the duty cycles of each phase [46]. Two commercial low-side gate-driver ICs are used for driving secondary-side switches. The dead time between driving signals of the primary-side switches and the secondary-side switches is designed by adjusting the delay of the control signal from the HB controller using resistors, capacitors, and diodes on the PCB. The components used in the design are detailed in Table II.

The steady-state key-nodes waveforms of the proposed converter at the condition of 48-V input, 1-V output, and a switching frequency of 333 kHz are shown in Fig. 17. The primary-side switch node V_{PRI1} varies from 0 V to 24 V, whereas the secondary-side switch nodes, V_{SEC1} and V_{SEC2}, vary from 0 V to 3 V according to the control signal, DRV1 and DRV2, from the HB controller. Fig. 18 shows the measured transient waveforms of the converter. The transient response to a high slew-rate load current is measured by the load generator implemented on the PCB. Under a 10-A/μs load step up and a 5-A/μs load step down, the converter shows a voltage recovery time of around 17 μs, undershoot voltage of 80 mV, and overshoot voltage of 35 mV. Since the maximum duty ratio of the current-doubler architecture is 0.5, the transient response of load-step up can be limited by the maximum duty ratio. In this design, the steady-state duty ratios are 0.33 and 0.13 at the condition of 48-V input and 1-V output and 60-V input and 0.5-V output, respectively. The transformer turn ratio is selected taking into account the tradeoff between the conversion range and the transient response.

The proposed converter achieves a stable and competitive transient response using the off-the-shelf controller IC without

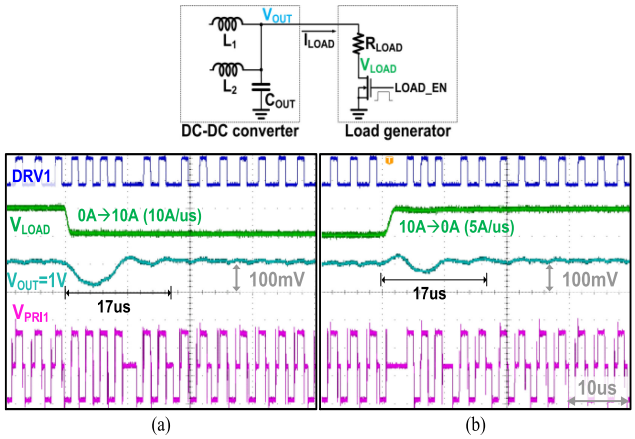


Fig. 18. Measured transient waveforms with the measurement setup on the PCB for the high slew load-current generation. (a) Under a load step-up transient. (b) Under a load step-down transient.

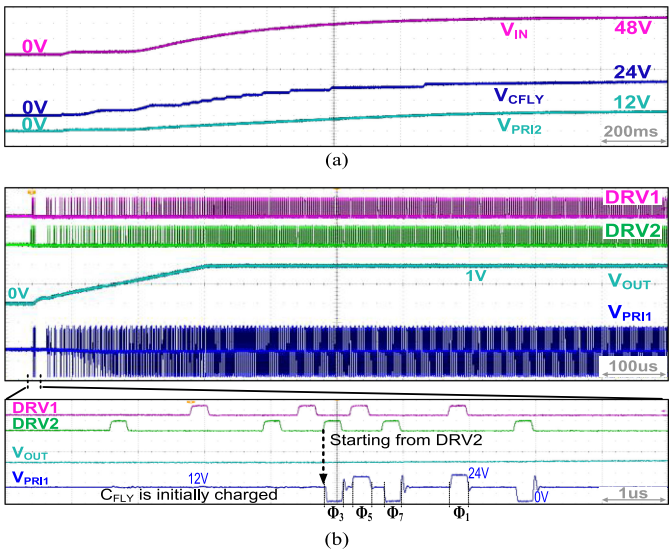


Fig. 19. (a) Measured precharging waveforms when $V_{\rm IN}$ is applied. (b) Measured start-up waveforms.

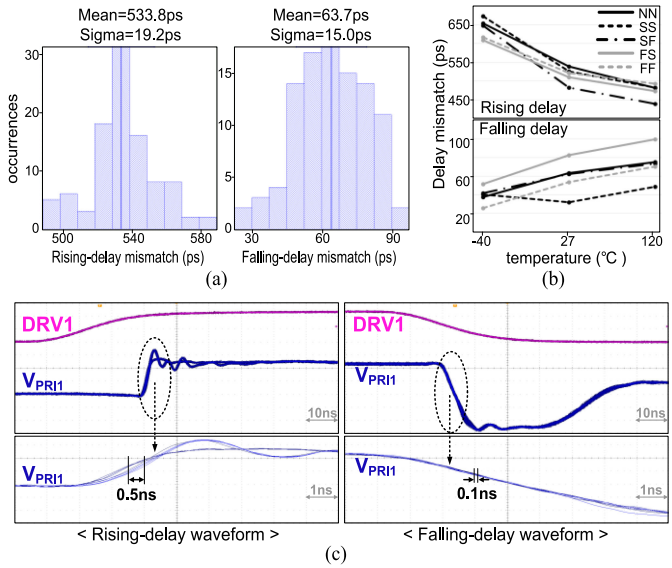


Fig. 20. Rising and falling delay variations. (a) Monte Carlo simulation results with 100 replications. (b) Five-corner simulation results according to the temperature variation. (c) Measured waveforms of the proposed dc–dc converter.

any customized control scheme for the proposed TLHB architecture.

Fig. 19(a) shows the precharging waveforms of $C_{\rm FLY}$ and HB capacitors, $C_{\rm HB1}$ and $C_{\rm HB2}$. When $V_{\rm IN}$ is just applied with a voltage slew rate of 60 V/s, $C_{\rm FLY}$ is charged by the initial charger circuit of the TLHB gate-driver IC and $C_{\rm HB1}$ and $C_{\rm HB2}$ are charged by the external resistors. For the reliability of the transistors, the input-voltage slew rate is limited by the driving capability of the initial charger circuit; in this work, the maximum slew rate of $V_{\rm IN}$ is around 125 V/s. Fig. 19(b) shows the measured start-up waveforms of the converter. The flying capacitor is initially charged to the predetermined voltage, around $1/2{\cdot}V_{\rm IN}$. The operation of the TLHB gate driver IC starts at Φ_3 to turn ON the low-side switches first for charging the bootstrapping capacitor of Q_{H2}. Then, the gate driver turns ON Q_{H2} during Φ_5 for charging the bootstrapping capacitor of Q_{H1}.

The rising-delay and falling-delay mismatches from DRV1 to $V_{\rm PRI1}$ are verified by Monte Carlo simulation and process corner simulation according to temperature variation as shown in Fig. 20(a) and 20(b), respectively. The rising-delay mismatch shows the mean value of 533.8 ps and one sigma of 19.2 ps and varies around 210 ps when the temperature changes from -40 °C to 120 °C. The falling-delay mismatch shows the mean value of 63.7 ps and one sigma of 15.0 ps and varies around 50 ps according to the temperature variation. The measured delay variations of the TLHB gate-driver IC are shown in Fig. 20(c). The measured rising-delay and falling-delay variations of the high-side gate drivers show around 0.5 ns and 0.1 ns, respectively. Since the minimum ON time of the converter in the steady state is 399 ns in the condition of $V_{\rm IN} = 60$ V, $V_{\rm OUT} = 0.5$ V, and a switching frequency of 333 kHz, the delay variation of the converter shows less than 0.2% of the minimum ON time. Although the proposed TLHB gate-driver cannot compensate for the parasitic-capacitance mismatch between power transistors, the estimated delay mismatch of this design due to the 10% capacitance mismatch is only about 0.33 ns, less than 0.1% of the minimum on time.

Fig. 21(a) and (b) shows the improvement of the voltage balance on $C_{\rm FLY}$ with the proposed schemes. With the ringing suppression and the proposed bootstrap circuit enabled, the voltage imbalance on $C_{\rm FLY}$ is reduced down to about 0.8% as shown in Fig. 21(c). The dynamic performance of $C_{\rm FLY}$ voltage balance during the input voltage transient is measured as shown in Fig. 22. When the input voltage changes from 48 V to 60 V, the voltage of $C_{\rm FLY}$ keeps balanced without any balancing scheme in the controller.

Fig. 23 shows the power-conversion efficiency of the proposed converter according to switching frequencies, output voltages, and input voltages. The efficiency is measured including the power consumption of all devices such as gate drivers and the HB controller. The proposed converter achieves 92.8% and 92.0% peak efficiencies at 48-V and 60-V inputs, respectively, to a 1-V

TABLE III
PERFORMANCE COMPARISON

		TI [17]	APEC 2017 [16]	TPEL 2020 [19]	TPEL 2020 [22]	This work
Structure		HB + current doubler	Sigma converter	Active clamp forward converter	Stacked HB + current doubler	TLHB + current doubler
V_{IN} [V]		36 - 75	48	12, 48	36 - 60	48 - 60
V_{OUT} [V]		0.5 - 1.5	0.8 - 1	0.7 - 1.1	0.8 - 1.2	0.5 - 1
I_{MAX} [A]		50	80	60	45	60
f_{SW} [kHz]		600	1000 / 600	325	500	333
Switches		GaN	GaN	MOSFET	GaN & MOSFET	MOSFET
V_{IN}=48V	Peak Eff. [%]	90.7 (V_{OUT}=1V, I_{LOAD}=20A)	93.4 (V_{OUT}=1V, I_{LOAD}=40A*)	89.5 (V_{OUT}=1V, I_{LOAD}=35A)	92.0 (V_{OUT}=1V, I_{LOAD}=20A)	92.8 (V_{OUT}=1V, I_{LOAD}=17A)
	Eff. [%] at I_{LOAD}=I_{MAX}	87.7 (V_{OUT}=1V)	91.6 (V_{OUT}=1V)	88.0 * (V_{OUT}=1V)	88.5 * (V_{OUT}=1V)	85.0 (V_{OUT}=1V)
V_{IN}=60V	Peak Eff. [%]	89.8 * (V_{OUT}=1V, I_{LOAD}=20A)	-	-	89.3 (V_{OUT}=1.2V, I_{LOAD}=25A)	92.0 (V_{OUT}=1V, I_{LOAD}=20A)
	Eff. [%] at I_{LOAD}=I_{MAX}	87.7 * (V_{OUT}=1V)	-	-	86.5 * (V_{OUT}=1.2V)	86.1 (V_{OUT}=1V)
Load step up	V_{OUT} undershoot [mV]	30 *	-	-	57	80 (10A/μs load slope)
	t_{settle} [μs]	5 *	-	-	16	17
Load step down	V_{OUT} overshoot [mV]	20 *	-	-	63	35 (5A/μs load slope)
	tsettle [μs]	5 *	-	-	18	17
Primary-side conversion ratio (V_{PRI}/V_{IN})		1/2	1	1	1/4	1/4
Turn ratio of transformer		5:1	4 × (10:1)	12:1	2:1	4:1
# of magnetics		3	5	2	3	3
# of capacitors **		3	3	2	5	4
# of switches		4	14	4	6	6

*estimated from the article.
**excluding input capacitor.

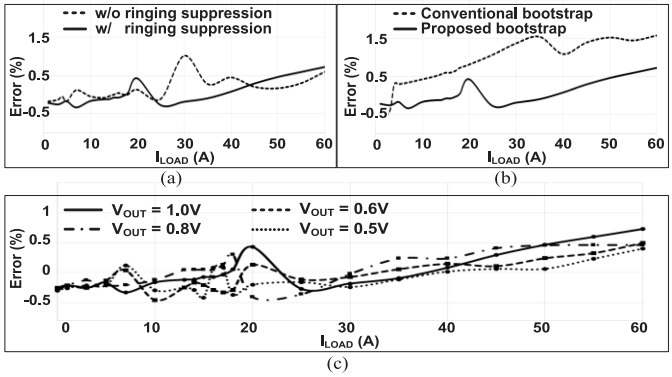


Fig. 21. Measured voltage imbalance according to the load current at V_{IN} = 48 V. (a) With and without the ringing suppression. (b) With and without the proposed bootstrap circuit. (c) With different output voltage.

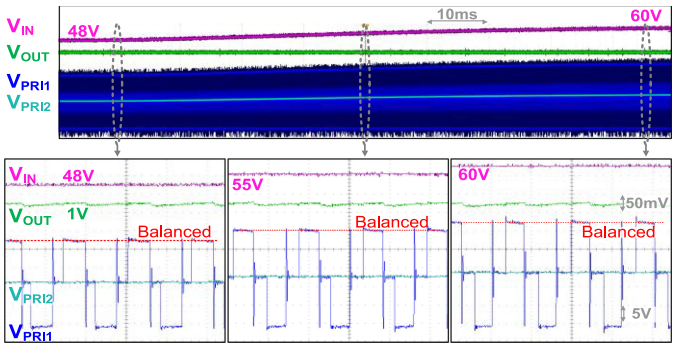


Fig. 22. Measured waveforms during the input voltage transient from 48 V to 60 V.

output. Table III compares the performance of this work with the previously reported isolated dc–dc converters with similar power levels and conversion ratios.

Compared with the baseline HB dc–dc converter with GaN transistors in [17], this work achieves a higher peak efficiency with Si transistors. Although the sigma converter in [16] shows

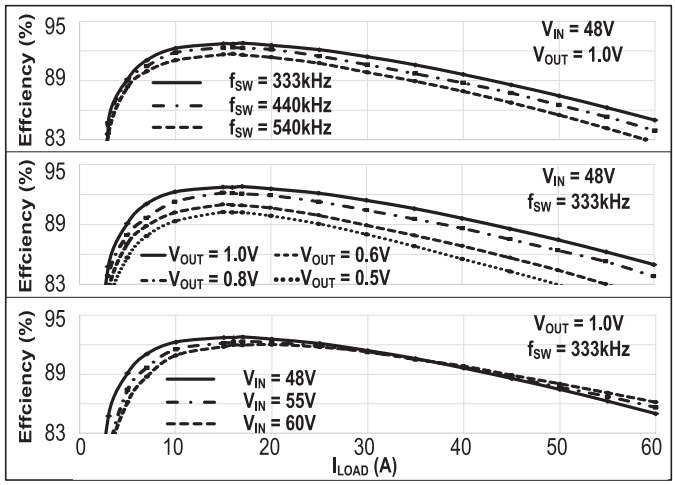


Fig. 23. Measured power conversion efficiency under different switching-frequency, output-voltage, and input-voltage conditions.

a superior peak efficiency, it requires a 40:1 turn-ratio transformer and employs GaN transistors. The primary-side stacked HB converter in [22] similarly converts the input voltage by a quarter, however, it is implemented with one more capacitor and GaN transistors. Although the active clamp forward converter in [19] is implemented with Si transistors, it shows a lower peak efficiency. In summary, the proposed TLHB converter with additional two switches and one capacitor offers a higher peak efficiency using reliable and low-cost Si transistors instead of GaN transistors while supporting the maximum input voltage of 60 V and the minimum output voltage of 0.5 V using a transformer with a low turn ratio of 4:1.

VI. CONCLUSION

This article describes the design of a TLHB dc–dc converter with a current-doubler rectifier for high step-down ratio power

conversion. The proposed TLHB topology and the overall operation of the converter reduce the hard-switching loss sufficiently while reducing the voltage stress on switches by half and switching voltages by a quarter. Since the primary-side TLHB with the proposed operation converts the input voltage by a quarter, thus increasing the overall duty cycle and reducing the required turn ratio of the transformer for a high step-down ratio dc–dc conversion. The TLHB gate-driver IC is designed for supporting the proposed three-level operation of the converter and straightforward implementation of the primary side. The level shifter, the bootstrap circuit, and the ringing suppression circuit reduce the voltage imbalance on C_{FLY} down to 0.8% with the proposed design principle. As a result, the existing HB-converter system can be easily replaced with the proposed TLHB converter employing the TLHB gate driver without additional controller ICs. The entire dc–dc converter implemented with Si transistors exhibits comparable or superior power-conversion efficiency compared with the state-of-the-art dc–dc converters with GaN transistors.

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