# Control Strategy of AC-DC Converter Based on Dual Active Bridge With Minimum Current Stress and Soft Switching

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***Abstract*—This article presents a control strategy for the single-stage dual active bridge (DAB) ac-dc converters. To reduce the conduction loss and achieve zero voltage switching (ZVS), the global optimal working modes are reviewed. Based on the global optimal working modes, the input current of the DAB ac-dc converter is analyzed for the sinusoidal input voltage. The control algorithm of the DAB ac-dc converter is proposed to achieve the unit power factor with the minimum current stress and ZVS. The range of the working modes is analyzed to meet the wide load power. The working mode is varied with the line-frequency angle and load power, which guarantees that the DAB ac-dc converter works in the optimal working modes. The conduction loss in the converter with the variation of the series inductance and the turns ratio of the transformer is analyzed. The series inductance and the turns ratio of the transformer are designed to further improve the conduction loss. The proposed control strategy is applied to a 1 kW DAB ac-dc converter with 220 V/50 Hz input voltage and 200 V output voltage. The experimental results demonstrate the working mode, the soft switching performance, fast dynamic response, high efficiency, and high power quality.**

***Index Terms*—Dual active bridge (DAB) ac-dc, global optimal working modes, unit power factor.**

## I. Introduction

Single-phase isolated ac-dc converters are becoming a favorable choice in the modern power supply, especially for the battery charger in electrical vehicles, energy storage systems, and solid-state transformers. The prevalent solution is the non-isolated PFC plus the isolated dc-dc converter [1][2], in which the PFC regulates the ac voltage to a constant dc bus voltage and the dc-dc converter adjusts the output voltage or current. The two-stage converter can decouple the ac power factor and the dc output voltage regulation [3].

With the advantages of galvanic isolation and soft switching, dual active bridge (DAB) converters are becoming a universal solution for the bidirectional power supply, especially for the energy storage system [4][5]. DAB converters can work in single-phase-shift control, in which the output voltages of the two full bridges are square waveforms and the phase shift angle is adjusted for the output regulation. In this strategy, the converter can achieve high efficiency when the effective conversion ratio is close to one, but the efficiency will be degraded in the wide conversion ratio. Extended phase shift (EPS) [6], dual-phase-shift (DPS) [7], and triple-phase-shift (TPS) [8][9] control strategies presented in the previous works can extend the efficiency of the DAB converters in a wide voltage range. These control strategies are based on the optimization of the current stress and soft switching. A TPS control is investigated to achieve the minimum peak current in the transformer by the Karush–Kuhn–Tucker (KKT) method [8]. The TPS control with the minimum root means square (RMS) current in the transformer is derived by the Lagrange multiplier method [9]. In [10], a modulation scheme with the minimum conduction loss on the premise of zero-voltage-switching (ZVS) is proposed. Meanwhile, the multiple working modes can be switched seamlessly to avoid oscillation. The comparisons of the TPS strategies with the peak current and RMS current in the transformer are presented in [11], which reveals that the control strategy with minimum RMS current is more complicated than that with minimum peak current. Therefore, the TPS by optimizing the peak current is easier to be implemented in the digital control.

A single-stage isolated ac-dc converter, composed of a four-diode rectifier and a DAB converter, has been used to achieve the unit power factor in the 1990s [12]. The line-frequency current has large distortion by only using the SPS control. After the control strategies with more degrees of freedom have been proposed, the DAB converter can meet the wide voltage conversion requirement. Therefore, it possesses a better performance in isolated ac-dc applications. In [13], a single-phase, single-stage, bidirectional, isolated DAB ac–dc converter is proposed. It consists of a synchronous rectifier cascaded with a DAB converter. The extra inductor and the magnetizing inductor of the transformer are used to extend the ZVS range. Although the converter can achieve higher efficiency compared with the two-stage converters, the working modes of the DAB in [13] are not globally optimal. Furthermore, the extra inductor current will cause more conduction loss. A trapezoidal modulation can reduce the conduction loss in the single-stage DAB ac-dc

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converter [14], but the converter can not work in ZVS. The switching loss also degrades the efficiency, so the converter can not work in high-frequency cases. A DAB ac/dc converter based on the half-bridge matrix structure is proposed in [15], and it can not achieve ZVS in all the working modes. To improve the efficiency, a phase-shift and frequency modulation of a DAB ac–dc converter with matrix switches is proposed to optimize the conduction loss and the ZVS [16]. The look-up table for the required output voltage is calculated offline and stored in the digital controller. The off-line optimization scheme is not flexible to meet the wide output voltage regulation. To simplify the control strategy, a single H-bridge modulation scheme is proposed to achieve the unit power factor in the DAB ac-dc converter [17]. The duty cycle of the full-bridge on the ac side is adjusted, while the voltage of the full-bridge on the dc side is a square waveform. The working mode can be viewed as the triangular current modulation (TCM) [18], which will cause large peak currents to meet the required load power and some switches can not work in ZVS. They are not optimal working modes. In [19], a control strategy using pulse frequency modulation (PFM) and DPS is applied in the DAB ac-dc converter to avoid the current distortion at the zero-crossing. A modulation scheme hybrid with the DPS and TPS can improve the line current distortion and efficiency [20]. However, the DPS and TPS only can meet soft switching and sinusoidal line current constraints, the conduction loss is not minimum. A single-stage single-phase solid-state transformer based on the DAB converters is proposed in [21]. The proposed optimal control is based on the EPS control. Although the control strategy losses a degree of freedom, the implementation is simplified. In [22], multiple operating modes are utilized in the DAB ac-dc converter, but the magnetizing current in the transformer is necessary for the ZVS performance. It also causes large conduction loss. For the full-operating-range zero voltage modulation, the nonlinear parasitic output capacitance is analyzed for the DAB ac-dc converter [23]. The article [24] also reveals that the ZVS of the switches is associated with the working modes in DAB converters. The nonidealities that existed in the circuit may cause the error of the theoretical analyses. A modeling approach of the DAB ac-dc converter is presented in [25] to reduce the modeling errors.

For the DAB dc-dc converters, the global optimal working modes with the minimum current stress and the ZVS have been discussed in many previous articles, and it is easy to be derived and implemented for the specific range of the conversion ratio in dc-dc converters. When the DAB converter is interfaced to the folded ac voltage, the conversion ratio is varied with the line-frequency voltage, which causes the difficult implementation of the global optimal working modes in the whole line-frequency voltage. In the previous works of the ac-dc DAB converters, to meet the unity power factor and low THD of the input current, the converter can not work in the optimal working modes. Therefore, the minimum conduction loss and the ZVS can not be achieved simultaneously. Although some articles present the ZVS modulation scheme, it is at the expense of more conduction loss. To optimize the modulation scheme for the DAB ac-dc converter, the following aspects should be taken into account.

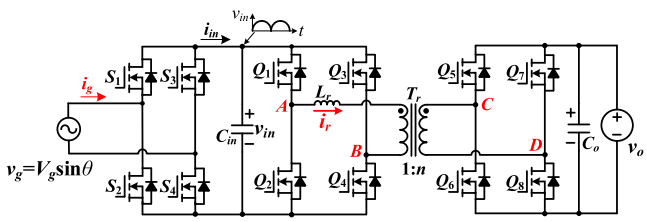



Fig. 1. Circuit of the single-stage DAB ac-dc converter.

1) All the switches should work in ZVS without any auxiliary circuit. The auxiliary circuit will cause more conduction loss. The article [10] shows that the optimal working modes of the DAB dc-dc converters can face all the load power with ZVS. Therefore, the auxiliary circuit is unnecessary for the ZVS in dc-dc DAB converters. In ac-dc DAB converters, all the switches have the potential to achieve ZVS without any auxiliary circuit.
2) The optimal working modes for the DAB dc-dc converters have been addressed in many previous works for the specific conversion ratio and load power. For DAB ac-dc converters, the conversion ratio is varied with the sinusoidal grid voltage in a very wide range. It is more difficult to distribute the optimal working modes of the DAB converters in the line-frequency period. To reduce the conduction loss, the current stress of the DAB ac-dc converter should be optimized in the whole line-frequency period.
3) The control loop can regulate both the output voltage and the line-frequency current. The line current should be sinusoidal waveform and in phase with the line voltage for the unit power factor.

The article presents an improved single-loop control for the single-stage DAB ac-dc converter. The contribution of this work is that a control strategy for the ac-dc DAB converter is proposed by combining four optimal working modes with minimum current stress for lower conduction loss and ZVS for lower switching loss is proposed. The article is organized as follows. In Section II, the global optimal working modes of the DAB converter are reviewed. They can achieve soft switching and minimum current stress. In Section III, the input current of the DAB converter based on the optimal working modes is analyzed, and the relationship between the global optimal working modes and the unit power factor is derived. Section IV presents a control strategy of the DAB ac-dc converter for regulating the output voltage and input unit factor. Meanwhile, the converter works in the optimal working mode to improve efficiency. The range of the working mode is analyzed. The design of the series inductance and turns ratio of the transformer is introduced. Section V gives the experimental results, which verify the analysis and control strategy. Finally, Section VI concludes the article.

## II. Optimal Working Mode for DAB Converter in TPS

Fig. 1 shows the circuit of the single-phase single-stage DAB ac-dc converter. Referred to [26], there are four optimal working

TABLE I
OPTIMAL TPS CONTROL FOR DAB CONVERTERS WITH MINIMUM CURRENT STRESS AND SOFT SWITCHING

| Working mode | | Range of $\varphi_s$ (where $\varphi_s$=2$\varphi/\pi$) | Expression of the duty cycle of the two full bridges | Expression of the output power |
|---|---|---|---|---|
| $M\leqslant 1$ | Mode 1 | $0<\varphi_s\leqslant\varphi_{b1}$ where $\varphi_{b1}=1-M$ | $\begin{cases} D_1=\frac{M}{1-M}\left(\varphi_s+\frac{4L_rI_{ZVS1}}{v_oT_s}\right) \\ D_2=\frac{D_1}{M}+\frac{4n^2L_rI_{ZVS2}}{v_oT_s} \end{cases}$ (1) | $P_o=\frac{v_{in}v_oT_s}{4nL_r}\varphi_sD_1$ (2) |
| | Mode 2 | $\varphi_{b1}<\varphi_s\leqslant 1$ | $\begin{cases} D_1=\frac{2M-1}{M}+\frac{1-M}{M}\varphi_s \\ D_2=1 \end{cases}$ (3) | $P_o=\frac{v_{in}v_oT_s}{8nL_r}\left(2\varphi_s-D_1^2+2D_1-\varphi_s{}^2-1\right)$ (4) |
| $M>1$ | Mode 3 | $0<\varphi_s\leqslant\varphi_{b2}$ where $\varphi_{b2}=1-\frac{1}{M}$ | $\begin{cases} D_2=\frac{1}{M-1}\left(\varphi_s+\frac{4L_rI_{ZVS2}}{v_{in}T_s}\right) \\ D_1=MD_2+\frac{4L_rI_{ZVS1}}{v_{in}T_s} \end{cases}$ (5) | $P_o=\frac{v_{in}v_oT_s}{4nL_r}\varphi_sD_2$ (6) |
| | Mode 4 | $\varphi_{b2}<\varphi_s\leqslant 1$ | $\begin{cases} D_2=2-M+(M-1)\varphi_s \\ D_1=1 \end{cases}$ (7) | $P_o=\frac{v_{in}v_oT_s}{8nL_r}\left(2\varphi_s-D_2^2+2D_2-\varphi_s{}^2-1\right)$ (8) |

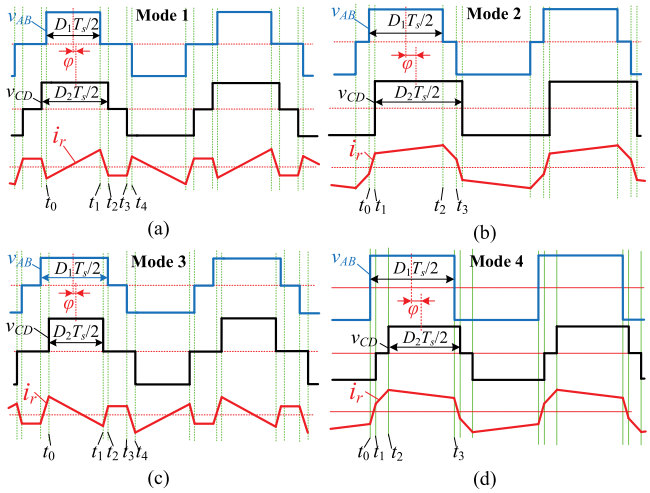



Fig. 2. Key waveforms DAB converter: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4.

modes for the DAB dc-dc converters in forward power flow, which cover the conversion ratio of both larger than one and less than one. Fig. 2 shows the four global optimal working modes in forward power for the DAB converter. The detailed derivation procedures of the optimal working modes are referred to the appendix in [26]. Fig. 2(a) and Fig. 2(b) correspond to the working modes when the converter ratio is less than 1. The conversion ratio $M$ is defined as $M = v_o/(n\cdot v_{in})$, where $v_{in} = |v_g|$. $v_g$ is the input ac voltage. Fig. 2(c) and Fig. 2(d) correspond to the working modes when the converter ratio is larger than 1.

By setting the peak current in the transformer and ZVS conditions as the optimized objectives and using Karush–Kuhn–Tucker (KKT) condition [26], the optimal working modes are derived as shown in Table I. If $D_1$ and $D_2$ in the equations of Table I is larger than one, $D_1$ and $D_2$ should be set as the maximum value, i.e., one. The maximum value of $\varphi$ is $\pi/2$, so the maximum value of $\varphi_s$ is also one. $I_{ZVS1}$ is the current amplitude for the ZVS of $Q_1$-$Q_4$, and $I_{ZVS2}$ is the current amplitude for the ZVS of $Q_5$-$Q_8$. $I_{ZVS1}$ and $I_{ZVS2}$ are associated with the output capacitance of the switches. To achieve ZVS, the current at the commutation time should meet $|i_r(t_x)|\geq I_{ZVS1}$ or $|i_r(t_x)|\geq I_{ZVS2}$, where $t_x$ is the turn-ON time of the corresponding switches. Referred to [27] and [28], the output capacitor of the switches is nonlinearly varied with the drain-source voltage. Therefore, $I_{ZVS1}$ and $I_{ZVS2}$ are difficult to regulate for the wide conversion ratio. To fully charge and discharge the junction capacitors during the commutation, $I_{ZVS1}$ and $I_{ZVS2}$ can be set a little larger so that the current in the series inductor can flow through the body diode of the switch before the switch is turned on. Taking $Q_1$-$Q_4$ for example, the current amplitude is expressed as

$$I_{zvs1}\geq\sqrt{\frac{1}{L}\left(4Q_{oss}(V_{ds})\frac{V_o}{n}-2Q_{oss}(V_{ds})V_{in}\right)} \quad (9)$$

The derivation of Equ. (9) can be referred to [28]. In this work, the switches are selected as C3M0120065J (@Cree), whose output capacitance is 60 $p$F (@300 V drain-source voltage). For the series inductance of 20 $\mu$H, $V_{in}$ = 300 V, and $V_o/n$ = 200 V, $I_{ZVS1}$ should be larger than 0.024A. The calculation is based on a constant input voltage. For ac-dc DAB converters, the output capacitor of the switches is varied with the sinusoidal input voltage, which complicates the implementation of the control algorithm. To overcome the nonlinearity of the output capacitance, $I_{ZVS1}$ is selected as 1A. Similarly, $I_{ZVS2}$ is also selected as 1A. The current amplitude guarantees the complete ZVS. Although the conduction loss becomes larger, the more conduction loss is very low because $I_{ZVS1}$ and $I_{ZVS2}$ are still selected as very low values. The boundary ZVS condition for the full-bridge circuit has been analyzed in many previous papers [27][28], and it is not the key concern in this article. Therefore, it is not derived in detail.

## III. Input Current Analysis for the Optimal Working Modes

As seen in Fig. 1, $S_1$-$S_4$ are the synchronous rectifier (SR). They are driven according to the line ac voltage $v_g(t)$. If $v_g(t)>0$, $S_1$ and $S_4$ are on, and $S_2$ and $S_3$ are off. If $v_g(t)<0$, $S_1$ and $S_4$ are off, and $S_2$ and $S_3$ are on. Because of the state of the synchronous switches, the ac line voltage is folded into a dc voltage $v_{in}$, which is pulsating twice the line-frequency, i.e., $v_{in}=|v_g|=V_g|\sin\theta|$, where $\theta$ is the phase angle of the input ac voltage. The input current of the DAB converter $i_{in}$ is expressed as $i_{in}=|i_g|$, where $i_g$ is an alternating current. If $i_{in}$ is in phase with $v_{in}$, $i_g$ is in phase with $v_g$. In this case, the ac-dc converter can achieve the unit PF.

### A. Mode 1

If the converter works in the unit power factor, the ac input current can be expressed as $i_g=I_g\sin\theta$, where $I_g$ is the amplitude of $i_g$. The input current of the DAB converter is expressed as $i_{in}=I_g|\sin\theta|$. According to Table I, the input current of the DAB converter is expressed as

$$i_{in}=\frac{P_o}{v_{in}}=\frac{v_oT_s}{4nL_r}D_1\varphi_s=I_g\,|\sin\theta| \tag{10}$$

Defining $I_{base}=v_oT_s/(8nL_r)$, $y$ is defined as the amplitude of the grid current in per unit (*p.u.*) and it is expressed as $I_g/I_{base}$. Equ. (10) is rewritten as

$$2D_1\varphi_s=y\,|\sin\theta| \tag{11}$$

Substituting (1) into (11), the phase shift angle is expressed as

$$\varphi_s=\sqrt{\frac{1-M}{2M}y\,|\sin\theta|+\left(\frac{2nL_rI_{ZVS1}}{v_oT_s}\right)^2}-\frac{2nL_rI_{ZVS1}}{v_oT_s} \tag{12}$$

Substituting (12) into (1), the duty cycle of the two full bridges is derived. If the converter works in Mode 1 and the duty cycle and phase shift angle meet (12) and (1), the ac input current must be the same phase with the ac line voltage.

### B. Mode 2

Similar to Mode 1, when the converter works in Mode 2, the following condition is satisfied for the unit power factor.

$$i_{in}=\frac{P_o}{v_{in}}=\frac{v_oT_s}{8nL_r}\left(2\varphi_s-D_1^2+2D_1-{\varphi_s}^2-1\right)=I_g\,|\sin\theta| \tag{13}$$

Rearranging (13), the following expression is derived, where $y$ is also defined as $I_g/I_{base}$.

$$2\varphi_s-D_1^2+2D_1-{\varphi_s}^2-1=y\,|\sin\theta| \tag{14}$$

Substituting (3) into (14), the phase shift angle is expressed as (15) by solving (14).

$$\varphi_s=1-\sqrt{\frac{1-y\,|\sin\theta|}{2-2/M+1/M^2}} \tag{15}$$

Substituting (15) into (3), the duty cycle of the two full bridges for Mode 2 is derived. If the converter meets (15) and (3) in Mode 2, the ac input current is also in the same phase with the ac line voltage.

### C. Mode 3

To achieve the unit power factor in Mode 3, the analysis is similar to Mode 1. The input current of the DAB converter is expressed as

$$i_{in}=\frac{P_o}{v_{in}}=\frac{v_oT_s}{4nL_r}\varphi_sD_2=I_g\,|\sin\theta| \tag{16}$$

Substituting (5) into (16), the phase shift angle is expressed as

$$\varphi_s=\sqrt{\frac{(M-1)\,y\,|\sin\theta|}{2}+\left(\frac{2L_rI_{ZVS2}}{v_{in}T_s}\right)^2}-\frac{2L_rI_{ZVS2}}{v_{in}T_s} \tag{17}$$

The conversion ratio $M$ is expressed as $v_o/(n\cdot V_g|\sin\theta|)$. Therefore, (17) can be rewritten as

$$\varphi_s=\sqrt{\frac{1}{2}\left(\frac{M}{nV_g}-|\sin\theta|\right)y+\left(\frac{2L_rI_{ZVS2}}{v_{in}T_s}\right)^2}-\frac{2L_rI_{ZVS2}}{v_{in}T_s} \tag{18}$$

Substituting (18) into (5), the duty cycle of the two full bridges for Mode 3 is derived. If the converter works in Mode 3 and the duty cycle and phase shift angle meet (18) and (5), the ac input current must be the same phase with the ac line voltage.

### D. Mode 4

The input current analysis in Mode 4 is similar to Mode 2. The input current of the DAB converter in Mode 4 is expressed as

$$i_{in}=\frac{P_o}{v_{in}}=\frac{v_oT_s}{8nL_r}\left(2\varphi_s-D_2^2+2D_2-{\varphi_s}^2-1\right)=I_g\,|\sin\theta| \tag{19}$$

Substituting (7) into (19), the phase shift angle in Mode 4 is expressed in (20)

$$\varphi_s=1-\sqrt{\frac{1-y\,|\sin\theta|}{M^2-2M+2}} \tag{20}$$

If the converter in Mode 4 meets (20) and (7), the ac input current is also in the same phase with the ac line voltage.

### E. Working Mode in the Zero-Crossing Point

Mode 3 handles the light power in $M>1$. For the sinusoidal input current, the light load occurs in the range near the zero-crossing point of the input voltage. In this case, the input voltage $v_{in}$ in the DAB is very low. The value of $\varphi_s$ must be very large in terms of (18), while the value of $D_1$ and $D_2$ must be larger than 1 in terms of (5). Therefore, $\varphi_s$, $D_1$, and $D_2$ must be set as the maximum value, i.e., 1. In this case, the working modes may not meet the conditions in Mode 3, and the input current will not be the sinusoidal waveforms at the zero-crossing point. Therefore, the current in the zero-crossing point will become distorted. To overcome the distortion, the triangular current modulation (TCM) is selected as the working mode in the zero-crossing point. When $I_{ZVS1}$ and $I_{ZVS2}$ in Mode 3 are set as zero, the

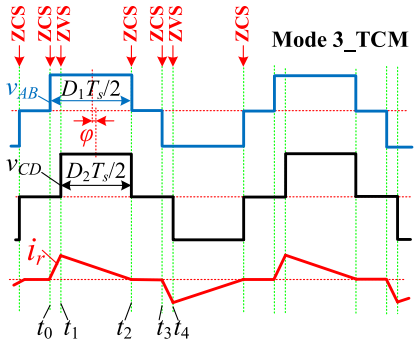



Fig. 3. Working mode in zero-crossing point.

working mode becomes the TCM. The key waveforms in TCM are shown in Fig. 3. Mode 3_TCM is the special case in Mode 3. Setting $I_{ZVS1}$ and $I_{ZVS2}$ in the equations of Section III C to zero, the expression of Mode 3_TCM to achieve sinusoidal input current is derived in (21).

$$\begin{aligned} \varphi_s &= \sqrt{\frac{1}{2}\left(\frac{M}{nV_g} - |\sin\theta|\right) y} \\ D_2 &= \frac{1}{M-1}\varphi_s \\ D_1 &= MD_2 \end{aligned} \tag{21}$$

In Mode 3_TCM, only $Q_7$ and $Q_8$ can achieve ZVS, $Q_1$ to $Q_6$ can not achieve ZVS but ZCS. The voltage at the zero-crossing point is very low. Even if $Q_1$ to $Q_4$ work in hard switching, the turn-ON loss of $Q_1$ to $Q_4$ is ignored because of very low drain-source voltage. Only $Q_5$ and $Q_6$ generate some turn-ON loss. However, the turn-ON and turn-OFF current are zero for $Q_5$ and $Q_6$. The switching loss is also very low in this case. The input voltage is too low to generate enough current amplitude for the ZVS. It is the reason why the working mode in the zero-crossing point can not meet Mode 3 in Fig. 2. When the grid phase angle is within $\pm6°$ and $180\pm6°$, the converter is selected to work in Mode 3_TCM.

## IV. Single Loop Control and Performance Analyses

### A. Control Strategy

In Section III, the input currents of the global optimal working modes are analyzed. As seen in (10), (13), (16), (19), and (21), $y$ determines the input current amplitude, i.e., the output power. Therefore, $y$ can be used to regulate the output power. $\theta$ and $V_g$ are gotten by the phase-locked loop (PLL). The strategy in Section III is derived from the optimal working modes in Section II, so the converter must work in the minimum current stress and soft switching. However, only one working mode can not meet a specific output power in a line-frequency cycle. There must be more than one working mode in a line-frequency cycle to regulate the output voltage. As seen in Table I, the range of $\varphi_s$ determines the working modes. In terms of the analyses in Section III, the flow chart of the modulation scheme is shown

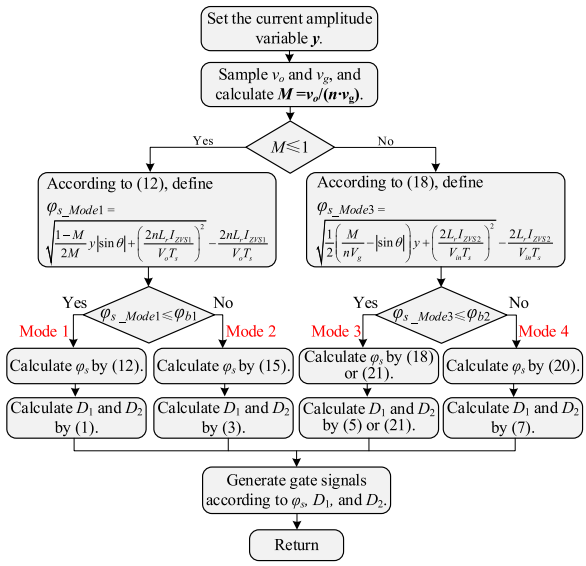



Fig. 4. Flow chart of the modulation scheme.

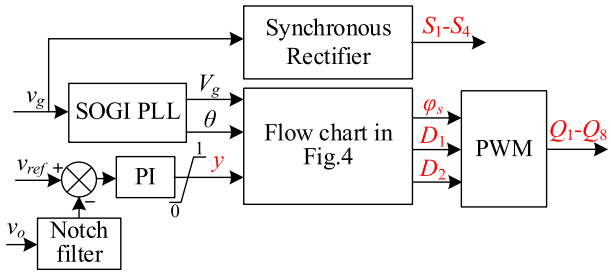



Fig. 5. Control loop of the single-stage ac-dc converter.

in Fig. 4. The input voltage of the DAB converter is the folded sinusoidal waveform, so the conversion ratio is varied with the input voltage. As seen in Fig. 4, the input voltage and output voltage are sampled, and the conversion ratio is obtained. If $M$ is less than one, the converter must work in Mode 1 or Mode 2. Assuming the converter works in Mode 1, the phase shift angle $\varphi_s$, i.e., $\varphi_{s\_\mathrm{Mode1}}$ in Fig. 4 can be calculated in terms of (12). As seen in Table I, the range of $\varphi_s$ for Mode 1 is $0<\varphi_s\leq\varphi_{b1}$. If $\varphi_{s\_\mathrm{Mode1}}$ is in the range of $0<\varphi_s\leq\varphi_{b1}$, the converter is selected to work in Mode 1. If $\varphi_{s\_\mathrm{Mode1}}$ is larger than $\varphi_{b1}$, the working mode derived from (12) is nonexistent. Therefore, the converter must work in Mode 2. If $M$ is larger than one, the converter must work in Mode 3 or Mode 4. If the converter works in Mode 3, the phase shift angle $\varphi_s$, i.e., $\varphi_{s\_\mathrm{Mode3}}$ in Fig. 4 can be calculated in terms of (18). If $\varphi_{s\_\mathrm{Mode3}}$ is in the range of $0<\varphi_s\leq\varphi_{b2}$, the converter works in Mode 3. Otherwise, the converter works in Mode 4. According to the definition of $y$ in Section III A, $y$ is the grid current amplitude in per unit, i.e., $y=I_g/I_{base}$. The grid current is expressed as $yI_{base}\sin\theta$. Therefore, $y$ is in the range from 0 to 1.

The control loop is shown in Fig. 5. For single-phase ac-dc converters, there is a twice line-frequency voltage ripple in the output voltage. A notch filter is used to filter out the twice line-frequency voltage ripple. Therefore, the output voltage sampling

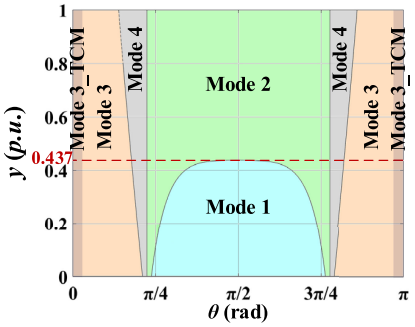



Fig. 6. Range of working modes.

is a dc value. By using a proportional-integral (PI) controller, the output of the controller is set as $y$, which is also a dc value. The grid voltage amplitude and phase angle $V_g$ and $\theta$ are gotten by using the second-order generalized integrator (SOGI) PLL. $\varphi_s$, $D_1$, and $D_2$ are calculated in terms of the flow chart in Fig. 4. Then the gate signals are generated to drive the power stage. For 50 Hz line frequency, the bandwidth of the ac-dc converter is selected as 10 Hz to 20 Hz.

### B. Analyses of the Control Strategy

According to the control strategy in Section IV A, the range of the working modes for the single input voltage is shown in Fig. 6, where the input voltage is 220 V/50 Hz, $v_o = 200$ V, $n = 1.1$, $L_r = 20$ $\mu$H, $I_{ZVS1} = I_{ZVS2} = 1$A, and $T_s = 10$ $\mu$s. In a half-line-frequency cycle, the converter is switched among several working modes. When $y$ is less than 0.437, the working mode in a half-line-frequency cycle contains the four working modes in Fig. 2. With the increase of $y$, the converter works in Mode 3, Mode 4, and Mode 2 but not Mode 1 in a half-line-frequency cycle.

Fig. 7 shows the three-dimensional (3D) modulation surfaces of $D_1$, $D_2$, and $\varphi_s$ versus the phase angle $\theta$ and $y$. $D_1$, $D_2$, and $\varphi_s$ are varied with $\theta$ and $y$, and they cover all the required conversion ratios and load power. Fig. 8 shows the curves of $D_1$, $D_2$, and $\varphi_s$ versus the phase angle $\theta$ for different $y$. The figures in Fig. 8 are the cross-section of the surfaces in Fig. 7. When $y$ is equal to 0.2 or 0.4, the converter works in the four working modes in Section II. For $y = 0.8$ or 1.0, the converter works in Mode2, Mode 3, and Mode 4. Fig. 8 also demonstrates the range of the working modes in Fig. 6. The normalized grid currents are derived from (10), (13), (16), and (19), and they are shown in Fig. 9. When $\theta$ is close to 0 or $\pi$, the converter works in Mode 3. As the conversion ratio is just greater than 1, the converter works in Mode 4. When the conversion ratio is less than 1, the converter works in Mode 1 and Mode 2. When $y$ is very low, the converter works in Mode 1 nearby the peak grid current. With the increase of $y$, the converter only works in Mode 2 in the range nearby $\pi/2$. The calculated grid normalized currents in Fig. 9 are derived from the grid current formulas in Section III. They are sinusoidal waveforms by using the proposed control strategy, which demonstrates the analyses in Section III.

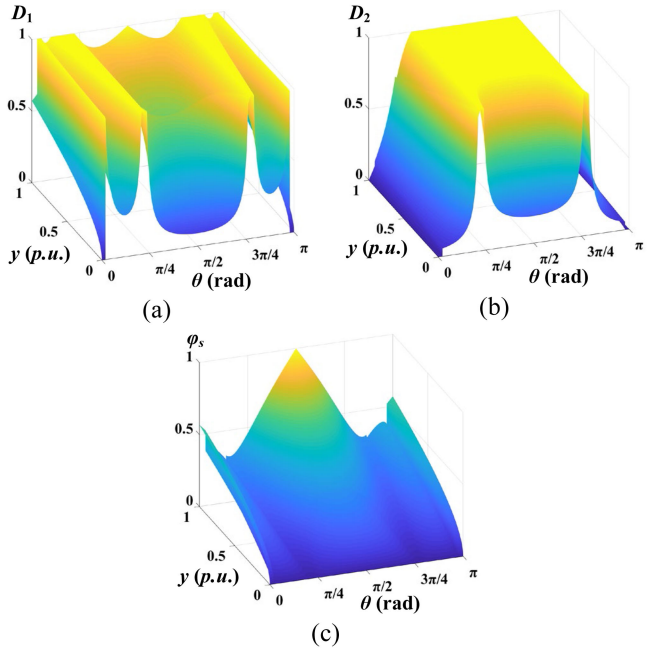



Fig. 7. 3D modulation surfaces of $D_1$, $D_2$, and $\varphi_s$ versus the phase angle $\theta$ and $y$.

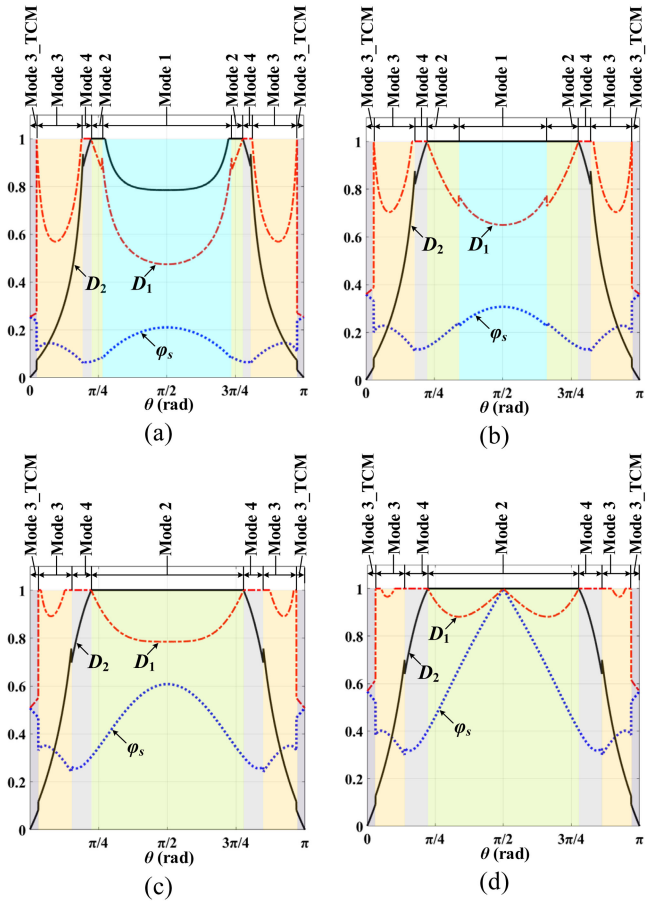



Fig. 8. Curves of $D_1$, $D_2$, and $\varphi_s$ versus the phase angle $\theta$ for different $y$: (a) $y = 0.2$; (b) $y = 0.4$; (c) $y = 0.8$; (d) $y = 1.0$.

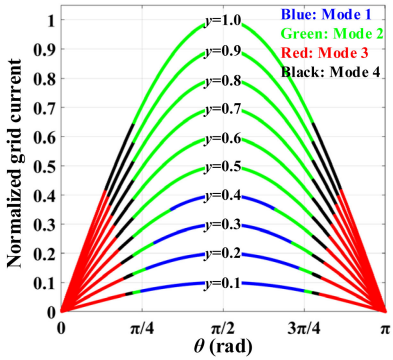



Fig. 9. Normalized grid current waveform versus the phase angle $\theta$.

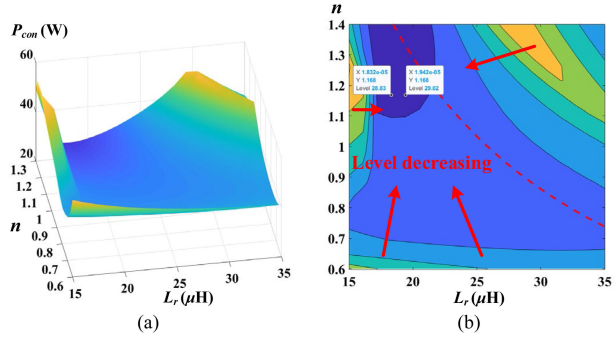



Fig. 10. (a) Surface of the conduction loss versus the turns ratio of the transformer and the series inductance; (b) Contour lines of the conduction loss.

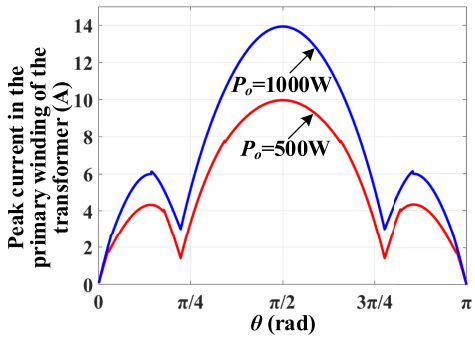



Fig. 11. Peak current in the transformer versus the grid angle $\theta$.

### C. Design of the Series Inductance and the Turns Ratio of the Transformer

As seen in Table I, the output power of the DAB converter is associated with the series inductor and turns ratio of the transformer. When $y = 1$, $\theta = \pi/2$, $D_1 = 1$, $D_2 = 1$, and $\varphi_s = 1$, the peak grid current gets the maximum value. It is expressed as

$$i_{g\_peak\_\max} = \frac{v_o T_s}{8nL_r} \tag{22}$$

Therefore, the maximum RMS grid current is expressed as $i_{g\_peak\_max}/\sqrt{2}$. The maximum input power capacity should be larger than the maximum load power, which can be expressed as follows.

$$P_{in\_\max} = \frac{V_g}{\sqrt{2}} \frac{i_{g\_peak\_\max}}{\sqrt{2}} = \frac{V_g v_o T_s}{16nL_r} > P_{o\_\max} \tag{23}$$

The following constraint can be derived.

$$n \cdot L_r < \frac{V_g v_o T_s}{16 P_{o\_\max}} \tag{24}$$

The conduction loss in the DAB ac-dc converter includes the conduction loss in the synchronous switches and DAB stage. The conduction loss in the synchronous switches is expressed as

$$P_{con\_SR} = {i_{g(rms)}}^2 \cdot 2 \cdot R_{dson\_SR} \tag{25}$$

where $R_{dson\_SR}$ is the turn-ON resistance of the synchronous switches $S_1$-$S_4$.

The conduction loss in the DAB stage is expressed as

$$\begin{aligned} &P_{con\_DAB} \\ &= \left(\tfrac{1}{\pi} \cdot \int_0^{\pi} {i_{r(rms)}}^2 d\theta\right) \cdot (2 \cdot R_{dson\_Q} + + R_{ESR\_Lr2} \\ &+ R_{ESR\_Tr\_pri} + \tfrac{2 \cdot R_{dson\_Q} + R_{ESR\_Tr\_sec}}{n^2}\Big) \end{aligned} \tag{26}$$

where $R_{dson\_Q}$ is the turn-ON resistance of $Q_1$-$Q_8$, and $R_{ESR\_Lr}$ is the equivalent series resistance (ESR) of $L_r$. $R_{ESR\_Tr\_pri}$ is the ESR of the winding of the transformer on the primary side, and $R_{ESR\_Tr\_sec}$ is the ESR of the winding of the transformer on the secondary side. The conduction loss $P_{con}$ is expressed as

$$P_{con} = P_{con\_DAB} + P_{con\_SR} \tag{27}$$

The working mode in each switching period is associated with the phase angle of the input ac voltage. Meanwhile, $i_r$ is also related to the turns ratio of the transformer and the series inductance. Therefore, the conduction loss is related to the turns ratio of the transformer, the series inductance, and the working modes. For 220 V/50 Hz input voltage, 200 V output voltage, and 1 kW load power, the surface of the conduction loss versus the turns ratio of the transformer and the series inductance is shown in Fig. 10(a), where $R_{dson\_SR} = R_{dson\_Q} = 0.12\ \Omega$, $R_{ESR\_Lr} = 0.05\ \Omega$, $R_{ESR\_Tr\_pri} = 0.1\ \Omega$, $R_{ESR\_Tr\_sec} = n$•$0.1\ \Omega$, $I_{ZVS1} = 1$A, $I_{ZVS2} = 1$A, $T_s = 10\ \mu$s. The conduction loss can reach the minimum value by selecting the turns ratio of the transformer and the series inductance. As seen in the expression of the output power in Table I, the maximum output power of the DAB converter is associated with the input and output voltage and the series inductance. If the output power of the DAB converter just meets the rated load power, the converter may lose the regulation capacity in the rated load power. Especially for the transient procedure, the output of the regulator may be saturated in this case. Therefore, the rated power is 1 kW, and the maximum load power $P_{o\_max}$ is selected as 1.3 kW. The contour lines of the conduction loss are shown in Fig. 10(b). According to (24), the boundary condition of the series inductance and the turns ratio of the transformer is plotted as the dashed line in Fig. 10(b). The series inductance and the turns ratio of the transformer should be selected in the range below the dashed line. When $n$ is equal to 1.1 and $L_r$ is equal to 20 $\mu$H, the conduction loss is close to the minimum value.

In terms of the parameters of $L_r$ and $n$, the peak current in the transformer versus the grid angle $\theta$ is shown in Fig. 11, where the input voltage is 220 V/50 Hz, $v_o = 200$ V, $n = 1.1$, $L_r = 20\ \mu$H,

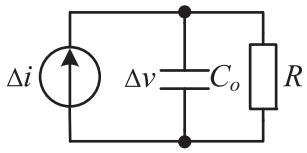



Fig. 12. Equivalent output circuit in the ac component.

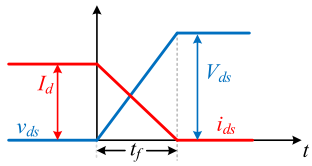



Fig. 13. Switch turn-OFF process.

$I_{ZVS1} = I_{ZVS2} = 1$A, and $T_s = 10$ $\mu$s. When the load power is 1000 W, the peak current in the transformer at $\pi/2$ phase angle is approximately 14 A. When the load power is 500 W, the peak current in the transformer at $\pi/2$ phase angle is approximately 10 A.

### D. Output Capacitor Design

The twice-input line frequency current ripple is caused by the sinusoidal input voltage. Assuming the input current is in the same phase with the input voltage and the output power is equal to the input power, the output power is expressed as

$$\begin{aligned} P_o = P_{in} &= V_g \sin(\omega t) \cdot I_g \sin(\omega t) \\ &= V_g I_g \frac{1-\cos(2\omega t)}{2} = P_{ave} - P_{ave}\cos(2\omega t) \end{aligned} \tag{28}$$

The integral of cos(2$\omega t$) in a line frequency period is equal to zero. Therefore, the average power $P_{ave}$ is defined as $V_g I_g/2$. $P_{ave}$cos(2$\omega t$) is the twice-line frequency power ripple. The equivalent output circuit in the ac component is shown in Fig. 12, where $\Delta v$ is the output voltage, and $\Delta i$ is defined as $P_{ave}$cos(2$\omega t$)/$V_o$. According to (28), the output power ripple in twice line-frequency is increased with the increase of the average output power.

The transfer function of the output current ripple to the voltage ripple is shown in (29). The amplitude of $\Delta i$ in the twice line frequency is 5A, where $P_o = 1000$ W, $V_o = 200$ V, and $2\omega = 2\times 2\pi \times 50$. If the voltage ripple is less than 4V in the twice line frequency, the constraint in (30) can be derived. For $R = 40\,\Omega$, $C_o$ should be larger than 1990 $\mu$F. In the experimental verification, $C_o$ is selected as 2200 $\mu$F.

$$G_{vi}(s) = \frac{\Delta v(s)}{\Delta i(s)} = \frac{R}{sC_oR + 1} \tag{29}$$

$$\begin{aligned} |G_{vi}(j2\pi 100)| &= \left|\frac{\Delta v(j2\pi 100)}{\Delta i(j2\pi 100)}\right| \\ &= \frac{R}{\sqrt{1 + (2\pi 100 C_o R)^2}} < \frac{4}{5} \end{aligned} \tag{30}$$

### E. Turn-OFF Loss Analysis

The control strategy can achieve ZVS in all the switches, so the turn-ON loss is ignored. The turn-OFF waveforms for the MOSFETs are shown in Fig. 13.

The turn-OFF loss expression is approximately evaluated as

$$P_{off\_loss\_Qx} = \int_0^{t_f} v_{ds} i_{ds} dt \approx \frac{V_{ds} I_d t_f}{6T_s} \tag{31}$$

where $t_f$ is the turn-OFF time, and $x = 1$ to 8. The turn-OFF loss is associated with the turn-OFF current and drain-source voltage.

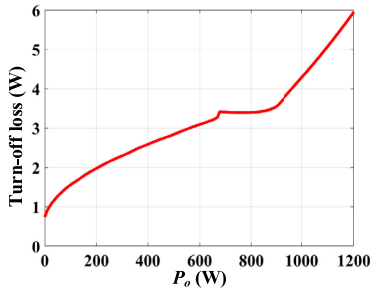



Fig. 14. Average turn-OFF loss in a line-frequency period versus the output power.

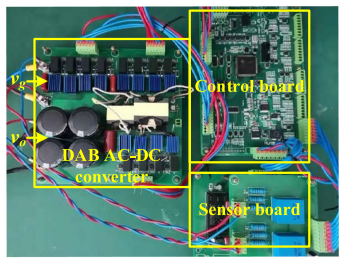



Fig. 15. Experimental prototype for test.

In each switching period, the current at the commutation time is associated with the working modes and output power, so turn-OFF loss in a switching period is the function of the phase angle $\theta$ and load power. The average turn-OFF loss in the line-frequency period is expressed in (32). Based on the numerical calculation, the average turn-OFF loss in the line-frequency period versus the output power is shown in Fig. 14, where the input voltage is 220 V/50 Hz, $v_o = 200$ V, $n = 1.1$, $L_r = 20$ $\mu$H, $I_{ZVS1} = I_{ZVS2} = 1$A, $T_s = 10$ $\mu$s, and $t_f = 30$ns. The turn-OFF loss in 1000 W rated output power is 4.315W.

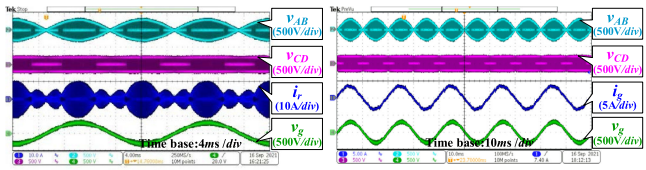
$$\begin{aligned} P_{off\_loss} = \frac{1}{\pi}\int_0^{\pi} &(P_{off\_loss\_Q1} + P_{off\_loss\_Q4} \\ &+ P_{off\_loss\_Q5} + P_{off\_loss\_Q8})\, d\theta \end{aligned} \tag{32}$$

## V. Experimental Validation

A prototype with 1 kW rated load power is built to verify the control strategy. The detailed specifications are shown in Table II. The control strategy and control algorithm are calculated online in the digital signal processor (DSP) TMS320F28335. Fig. 15 shows the experimental prototype. The switching frequency is 100 $k$Hz, and the sampling and control frequency is 50 $k$Hz.

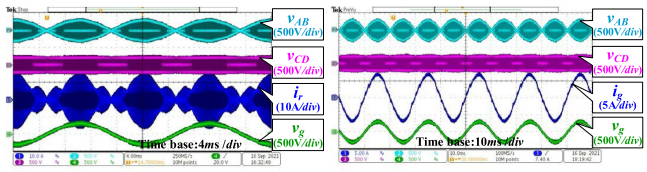
TABLE II
DETAILED SPECIFICATIONS

| Items | Symbol | Parameter |
|---|---|---|
| **Input AC voltage** | $v_g$ | 220V/50Hz |
| **Output voltage** | $V_o$ | 200 V |
| **Turns ratio of the transformer** | $n$ | 1.1 |
| **Core size of the transformer** | | PQ40/40 |
| **Switching frequency (period)** | $f_s\,(T_s)$ | 100$k$Hz (10 $\mu$s) |
| **Switches** | $S_{1\text{-}4}$, $Q_{1\text{-}8}$ | C3M0120065J (Cree) |
| **Series inductor** | $L_r$ | 20$\mu$H |
| **Core size of the series inductor** | | PQ32/30 |
| **Output filter capacitance** | $C_o$ | 2200 $\mu$F |
| **Input filter capacitance** | $C_{in}$ | 4.7$\mu$F |




(a) (b)

Fig. 16. Waveforms in 500 W load power: (a) Full bridge voltages and transformer current; (b) Line-frequency voltage and current.

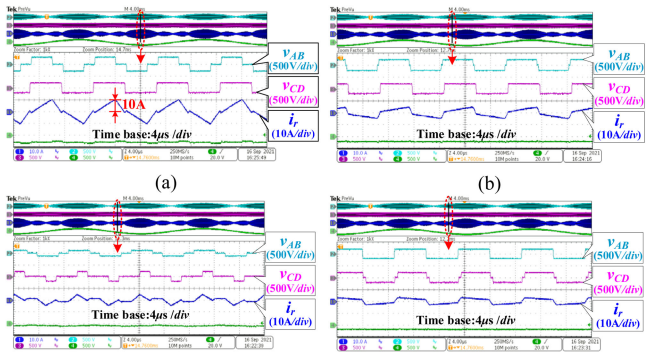



(a) (b)

Fig. 17. Waveforms in 1000 W load power: (a) Full bridge voltages and transformer current; (b) Line-frequency voltage and current.

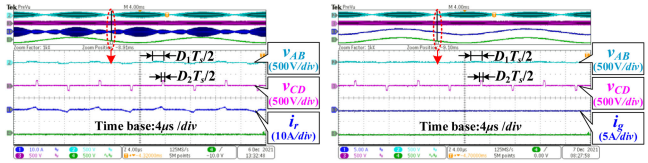
Fig. 16 shows the waveforms in 500 W load power. Fig. 16(a) shows the full-bridge voltages and the transformer current, the envelope curve of $v_{AB}$ is the line-frequency voltage. Fig. 16(b) shows the line-frequency voltage and current. The line-frequency current is in the same phase as the line-frequency voltage, which illustrates the unit power factor. Fig. 17 shows the waveforms in 1000 W load power. With the increase of the load power, the converter also can achieve the unit power factor. The envelope of $i_r$ illustrates the peak current of the transformer. The shapes of the envelope of $i_r$ in Figs. 16 and 17 are identical with the peak current curves shown in Fig. 11.

Fig. 18 shows the zoomed-in waveforms in 500 W load power. As seen in Fig. 18(a), the converter works in Mode 1 at the peak or valley grid voltage voltage. The peak current in the transformer in this case is 10 A, which is the same as the analysis of Fig. 11. In Fig. 18(b), the effective conversion ratio is less than one, and the phase of the line-frequency voltage is not in the range of the peak voltage or valley voltage. Therefore, the converter works in Mode 2. Fig. 18(c) and (d) show the converter



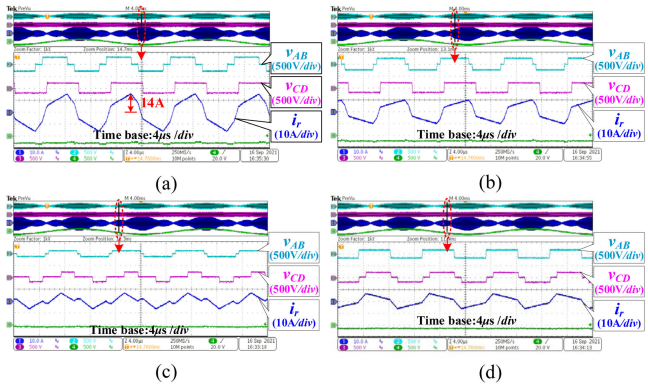

(a) (b) (c) (d)

Fig. 18. Zoomed-in waveforms in 500 W load power: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.




(a) (b)

Fig. 19. Zoomed-in waveforms of the zero-crossing point in 500 W load power: (a) Zoomed-in transformer current; (b) Zoomed-in grid current.




(a) (b) (c) (d)

Fig. 20. Zoomed-in waveforms in 1000 W load power: (a) Mode 2; (b) Mode 2; (c) Mode 3; (d) Mode 4.

works in Mode 3 and Mode 4, when the conversion ratio is larger than one.

Fig. 19 shows the zoomed-in waveforms of the zero-crossing point in 500 W load power. Fig. 19(a) shows zoomed-in transformer current. The current in the transformer is a triangular waveform, which demonstrates the waveforms of Mode 3_TCM in the zero-crossing point. In this case, the input voltage is very low, so the voltage amplitude of $v_{AB}$ is very low. Therefore, the switching loss in $Q_1$ to $Q_4$ is negligible. Fig. 19(b) shows the grid current in the zero-crossing point, which illustrates a smooth grid current without distortions in the zero-crossing point.

Fig. 20 shows the zoomed-in waveforms in 1000 W load power. Fig. 20(a) and 20(b) illustrate that the converter works in Mode 2. Fig. 20(a) shows the key waveforms in the peak grid voltage. In this case, the peak current in the transformer

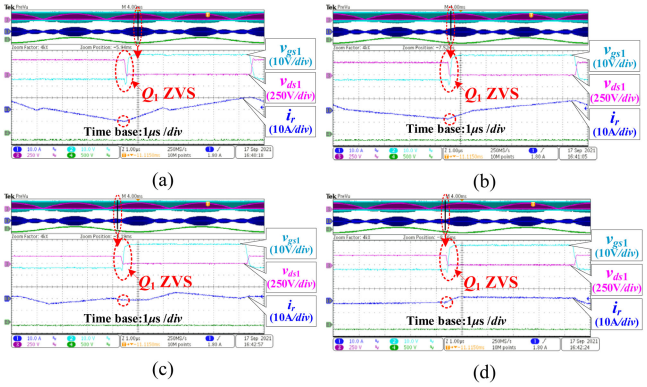



Fig. 21. Gate signal and drain-source voltage of switch $Q_1$: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.

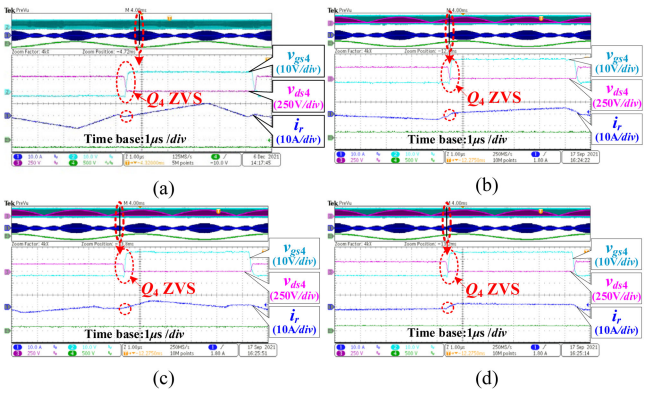



Fig. 22. Gate signal and drain-source voltage of switch $Q_4$: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.

is 14 A, which is also the same as the peak current shown in Fig. 11. Therefore, the experimental result in Figs. 18 and 20 demonstrates the analyses in Section IV.C. Fig. 20(c) and (d) show the working modes in Mode 3 and 4, when the effective conversion ratio is larger than one. With the increase of the load power, the working modes do not include Mode 1. The experimental results demonstrate the analyses in Section IV.B.

Fig. 21 shows the zoomed-in gate signal and drain-source voltage of switch $Q_1$ in 500 W load power. The four figures in Fig. 21 show the ZVS performance in Mode 1–4, which illustrates $Q_1$ can achieve ZVS in all the working modes.

Fig. 22 shows the zoomed-in gate signal and drain-source voltage of switch $Q_4$ in 500 W load power. The four figures also illustrate that $Q_4$ can achieve ZVS in the four working modes.

The zoomed-in gate signal and drain-source voltage of switch $Q_5$ in Fig. 23 demonstrate the ZVS performance of switch $Q_5$ in the four working modes.

Fig. 24 shows the ZVS performance of switch $Q_8$ in the four working modes. The above experimental results of gate signal and drain-source voltage demonstrate all the switches can meet the ZVS conditions, so the switching loss is reduced.

Fig. 25 shows the dynamic waveforms under the load step change from no load to 800 W load power. Before the load step change, the control strategy also can meet the no-load case. During the dynamic procedure, the line-frequency current is in

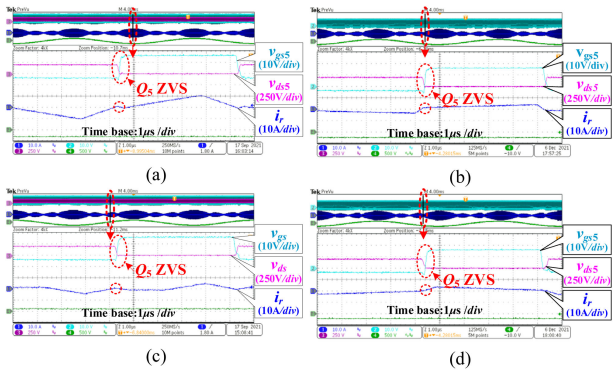



Fig. 23. Gate signal and drain-source voltage of switch $Q_5$: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.

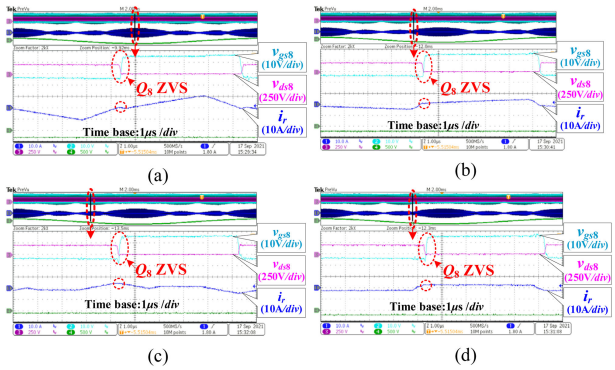



Fig. 24. Gate signal and drain-source voltage of switch $Q_8$: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.

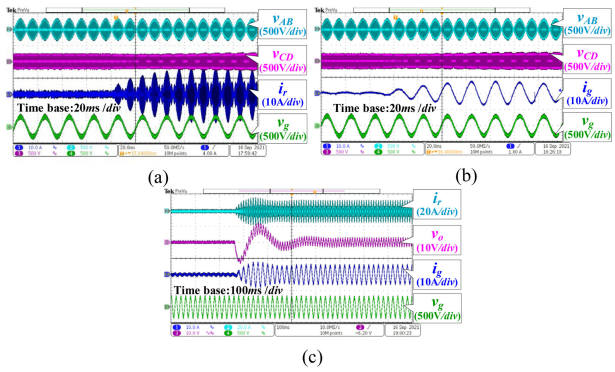



Fig. 25. Dynamic waveforms under the load step change from no load to 800 W load power.

the same phase as the line-frequency voltage. The experimental results verify the good dynamic response.

Fig. 26 shows the output voltage step-changed waveforms. Before $t_m$, the output voltage is 200 V, and the load power is 1000 W for the resistive load. At $t_m$, the output voltage reference is changed to 150 V. The output voltage is decreased, while the grid current amplitude and the transformer current amplitude are decreased. For different output voltages, the grid current is also a sinusoidal waveform, which demonstrates the effectiveness of the control strategy. Therefore, the proposed control strategy has a wide output voltage regulation capacity.

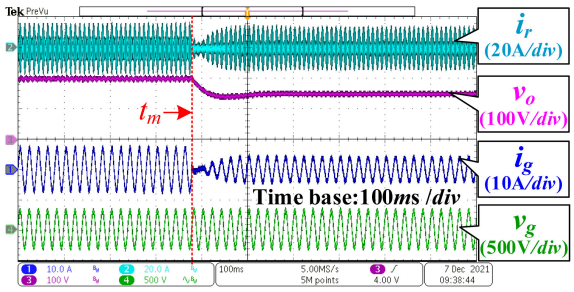



Fig. 26. Output voltage step-changed waveforms.

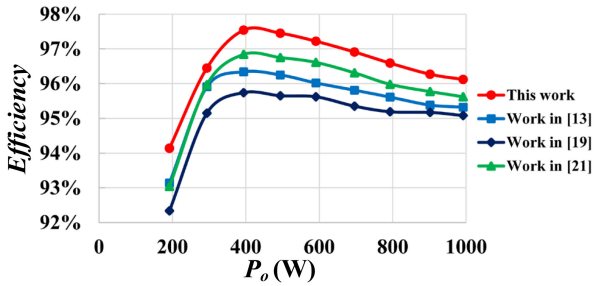



Fig. 27. Measured efficiency curve versus output power.

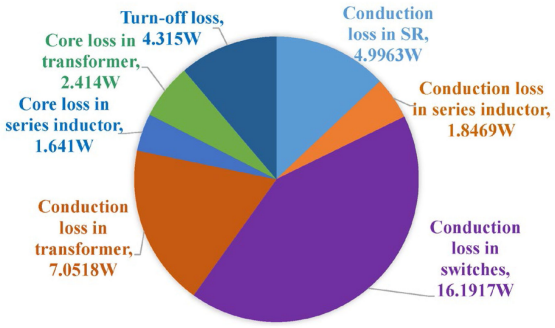



Fig. 28. Breakdown of calculated loss for rate load power.

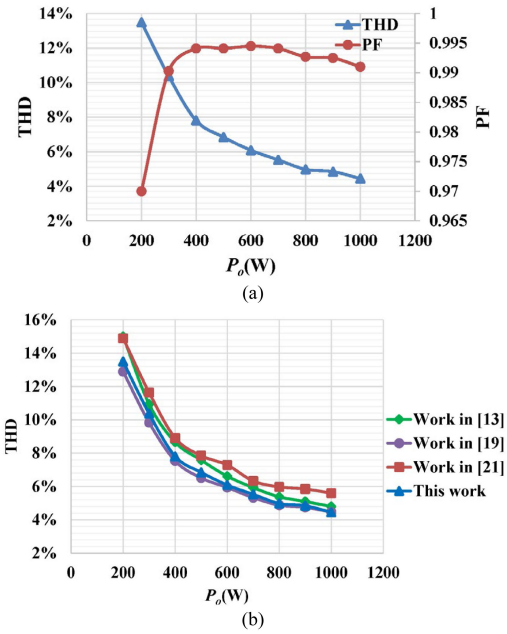



Fig. 29. (a) Measured PF and THD of the grid current; (b) THD comparison.

TABLE III
COMPARISONS OF CONTROL STRATEGIES FOR THE DAB AC-DC CONVERTERS

| | [13] | [19] | [21] | This work |
|---|---|---|---|---|
| **Switching frequency** | Variable frequency | Variable frequency | Constant frequency | Constant frequency |
| **Control strategy** | TPS+PFM | DPS+PFM | TPS | TPS |
| **Solution of the strategy** | Off-line Calculation | Real-time | Real-time | Real-time |
| **Working modes** | Not optimal | Not optimal | Locally optimal | Globally optimal |
| **Soft switching strategy** | Auxiliary component | Not global Soft Switching | Magnetizing inductance | Inherent |
| **Design complexity** | High | Low | Moderate | Moderate |
| **Wide conversion ratio capacity** | Moderate | Low | Moderate | High |

Because the converter works in the global optimal working modes with the minimum current stress and the ZVS, the conduction loss and the switching loss are greatly reduced. Therefore, the converter can achieve high-efficiency performance. Fig. 27 shows the efficiency curves versus the load power. The peak efficiency reaches 97.5% in 400 W load power. In 1000 W rated load power, the efficiency is 96.1%. The distribution of the calculated loss for the rated load power is shown in Fig. 28. Almost most of the losses are the conduction loss in the switches and the magnetizing components. Fig. 29(a) shows the measured power factor (PF) and total harmonic distortion (THD) of the grid current. In the rated 1000 W load power, the power factor is 0.991, and the THD is 4.45%. It illustrates the proposed control strategy can guarantee a high power factor and low total harmonic distortion in wide load power. Testing in the same bench, Fig. 29(b) shows the THD comparisons with the previous works. The THD of the grid current in the proposed control strategy is not lower than in the previous works.

Table III shows the comparisons of the control strategies for DAB ac-dc converters. The control strategies in [13] and [19] are based on TPS plus PFM and DPS plus PFM, so the switching frequency is varied in a wide range. It will be difficult in EMC design. The working modes in [13], [19], and [21] are not globally optimal, which causes more conduction loss. The ZVS performance in [13] and [21] can be achieved with the aid of the auxiliary component or the magnetizing inductance of the transformer, which also causes more conduction loss. As shown in Fig. 27, the efficiency curves of some previous works tested in the same test bench demonstrate that the proposed control strategy can achieve higher efficiency than the above previous works. The modulation scheme in [13] is based on the off-line calculation, so the design is more complex and less flexible for a wide conversion ratio. The proposed control strategy can achieve ZVS inherently without the need for any auxiliary components. The modulation scheme is implemented in real-time without off-line calculation. Therefore, the design and implementation of the control strategy are easier.

## VI. Conclusion

In this article, a control strategy with minimum current stress and ZVS is proposed for the DAB ac-dc converter. According to the global optimal working modes, the algorithm of the input current of the DAB converter in phase with the sinusoidal input voltage is derived. The control strategy to achieve the unit power factor is proposed based on the global optimal working modes. The control strategy can achieve the minimum current stress in all the operating conditions, while all the switches work in soft switching. Therefore, the conduction loss and switching loss are reduced. The working modes range is analyzed, and it demonstrates the control strategy can meet wide load power. The conduction loss as the function of the series inductance and the turns ratio of the transformer is analyzed to optimize the parameter of the magnetizing component. The prototype is built to test the performance of the control strategy. The experimental results verify the working modes and soft-switching performance. The proposed converter can achieve a good dynamic response, high power factor, high power quality, and high efficiency.

## References


[1] S. Kim and F. Kang, "Multifunctional onboard battery charger for plug-in electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3460–3472, Jun. 2015.

[2] C. Oh, D. Kim, D. Woo, W. Sung, Y. Kim, and B. Lee, "A high-efficient nonisolated single-stage on-board battery charger for electric vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5746–5757, Dec. 2013.

[3] B. Li, Q. Li, F. C. Lee, Z. Liu, and Y. Yang, "A high-efficiency high-density wide-bandgap device-based bi-directional on-board charger," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1627–1626, Sep. 2018.

[4] Z. Guo, K. Sun, T. Wu, and C. Li, "An improved modulation scheme of current-fed bi-directional DC-DC converters for loss reduction," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4441–4457, May 2018.

[5] Y. R. Kafle, S. U. Hasan, and G. E. Town, "Quasi-Z-source based bidirectional DC-DC converter and its control strategy," *Chin. J. Elect. Eng.*, vol. 5, no. 1, pp. 1–1–10, Mar. 2019.

[6] G. Xu, L. Li, X. Chen, Y. Liu, Y. Sun, and M. Su, "Optimized EPS control to achieve full load range ZVS with seamless transition for dual active bridge converters," *IEEE Trans. Power Electron.*, vol. 68, no. 9, pp. 8379–8390, Aug. 2020.

[7] N. Hou, W. Song, and M. Wu, "Minimum-current-stress scheme of dual active bridge DC–DC converter with unified phase-shift control," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8552–8561, Dec. 2016.

[8] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.

[9] A. Tong, L. Hang, G. Li, X. Jiang, and S. Gao, "Modeling and analysis of a dual-active-bridge-isolated bidirectional DC/DC converter to minimize RMS current with whole operating range," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 174–188, Jun. 2018.

[10] Z. Guo, "Modulation scheme of dual active bridge converter for seamless transitions in multiworking modes compromising ZVS and conduction loss," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7399–7409, Sep. 2020.

[11] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148–3172, Mar. 2020.

[12] M. H. Kheraluwala and R. W. De Doncker, "Single phase unity power factor control for dual active bridge converter," in *Proc. IEEE Ind. Appl. Conf. 28th IAS Annu. Meeting*, 1993, pp. 909–916.

[13] J. Everts, F. Krismer, J. Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS modulation of single-phase single-stage bidirectional DAB AC–DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3954–3970, Aug. 2014.

[14] S. Zengin and M. Boztepe, "A novel current modulation method to eliminate low-frequency harmonics in single-stage dual active bridge AC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1048–1058, Feb. 2020.

[15] N. D. Dao and D. Lee, "Modulation of bidirectional AC/DC converters based on half-bridge direct-matrix structure," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12657–12662, Dec. 2020.

[16] F. Jauch and J. Biela, "Combined phase-shift and frequency modulation of a dual-active-bridge AC–DC converter with PFC," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8387–8397, Dec. 2016.

[17] N. D. Weise, G. Castelino, K. Basu, and N. Mohan, "A single-stage dual-active-bridge-based soft switched AC–DC converter with open-loop power factor correction and other advanced features," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4007–1016, Aug. 2014.

[18] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[19] Q. Tian and K. Bai, "Widen the zero-voltage-switching range and secure grid power quality for an ev charger using variable-switching-frequency single-dual-phase-shift control," *Chin. J. Elect. Eng.*, vol. 4, no. 1, pp. 11–19, Mar. 2018.

[20] A. Taylor, G. Liu, H. Bai, A. Brown, P. M. Johnson, and M. McAmmond, "Multiple-phase-shift control for a dual active bridge to secure zero-voltage switching and enhance light-load performance," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4584–4588, Jun. 2018.

[21] J. Zhang, D. Sha, and P. Ma, "A dual active bridge DC-DC based single stage AC-DC converter with seamless mode transition and high power factor," *IEEE Trans. Ind. Electron.*, vol. 69, no. 2, pp. 1411–1421, Feb. 2022.

[22] X. Sun, H. Wang, L. Qi, and F. Liu, "Research on single-stage high-frequency-link SST topology and its optimization control," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8701–8711, Aug. 2020.

[23] J. Everts, "Closed-form solution for efficient ZVS modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 11276–11287, Oct. 2017.

[24] Y. Yan, H. Gui, and H. Bai, "Complete ZVS analysis in dual active bridge," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1247–1252, Feb. 2021.

[25] A. Singh, A. K. Yadav, and A. Khaligh, "Steady-state modeling of a dual-active bridge AC–DC converter considering circuit nonidealities and intracycle transient effects," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11276–11287, Oct. 2021.

[26] S. Mu, Z. Guo, and Y. Luo, "Universal modulation scheme to suppress transient DC bias current in dual active bridge converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1322–1333, Feb. 2022.

[27] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[28] Y. Yan, H. Gui, and H. Bai, "Complete ZVS analysis in dual active bridge," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1247–1252, Feb. 2021.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