Chip-Level Electrothermal Stress Calculation Method of High-Power IGBT Modules in System-Level Simulation

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***Abstract*—Although with good robustness, insulated gate bipolar transistor (IGBT) modules suffer from catastrophic failures due to excessive electrothermal stress in field use. In view of the coupled and multitimescale electrothermal dynamics of IGBT modules, the conventional simulation methods are difficult to calculate the stresses accurately and efficiently. Therefore, this article proposes an artificial neural network (ANN) based method to calculate the chip-level stress of IGBT modules in system-level circuit simulation. The first contribution in this article is that the research focus goes from the entire device to chips within the device. Correspondingly, the uneven dynamic current and thermal coupling effects among chips are fully considered based on the established uneven power loss and three-dimensional (3-D) thermal models. The second one is to solve the contradiction between simulation efficiency and accuracy in multitimescale operation analysis through the joint application of IGBT physical model and ANN. The third one is to propose the complete chip-level stresses calculation and automated modeling processes, based on multisoftware cosimulation. An inverter experimental prototype was established to verify the accuracy of the proposed calculation method. The comparison results show that the method can accurately describe the transient junction temperature, overcurrent and overvoltage stresses, thus providing an effective support for the safety design of converters.**

***Index Terms*—Artificial neural network (ANN), finite-element method (FEM), insulated gate bipolar transistor (IGBT), thermal model.**

I. Introduction

As THE power rating of power electronic systems (PES) increases, power semiconductor devices suffer more serious overstress risk. The excessive electrical and thermal stress on chips within the device will cause the catastrophic failure for the PES, which should be strictly prohibited [1], [2]. Therefore, PES engineers tend to obtain the accurate electrothermal stress of chips as detailed as possible in the design stage, for the targeted device selection and protection circuit design. However, the conventional commercial circuit simulation software is difficult to achieve both efficient and accurate device stress calculation. Taking insulated gate bipolar transistor (IGBT) as an example, common circuit simulation software was investigated, as shown in Fig. 1. To the best of our knowledge, there are three types of IGBT model in commercial software: physical model refers to analytical model based on semiconductor physics, behavioral model without considering the physical mechanism of devices, and look-up table model.

For physical models, the most widely used one is undoubtedly Hefner model [3]–[5], which is the first complete one-dimensional (1-D) analytical, charge-controlled model suitable for circuit simulator implementation [6]. The analog circuit representation of Hefner model is shown as Fig. 1(a), where the nonlinear capacitances and non-quasi-static effects are fully considered. Therefore, the model can accurately describe the switching transient of device and has been integrated in Saber [7]. Besides, Kuang Sheng model and Kraus model are also accurate and mature ones [8], [9]. The latter has been implemented by Spice language and supported by Infineon Technologies according to the device characteristics [10], as shown in Fig. 1(b). For behavioral models, integrated hierarchical behavioral model, including average and dynamic models [11], was applied by ANSYS Simplorer to meet the needs of different simulation scenarios, as shown in Fig. 1(c). Another method is to simply model IGBT as a MOSFET-driven transistor, as shown in Fig. 1(d). The method was implemented in Simulink/Simscape as N-channel IGBT model to achieve a simplified and faster device simulation [12]. Further, PSIM/DSIM optimized this method by the combination of the discrete-state event-driven approach and the piecewise analytical transient (PAT) model, attaining awesome simulation efficiency especially in megawatt PES [13], [14]. For the look-up table model, the energy loss of IGBT device under certain conditions is stored in a table and called in the electrothermal simulation, as shown in Fig. 1(e). The model was applied in PLECS to implement fast power loss and thermal simulation [15].

The above models need to be comprehensively evaluated in terms of simulation effect and simulation speed, as illustrated

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TABLE I
COMMERCIAL CIRCUIT SIMULATION SOFTWARE INVESTIGATION

Software	IGBT Models	Types	Simulation effect		Simulation speed
			Switching transient	Thermal behavior	
LTspice				★	★
Pspice	Spice model supported by manufacturers	Physics	★★★★	★	★
SIMetrix/SIMPLIS				★	★★
Simplorer	Integrated average/ dynamic model	Behavioral	★★★	★★	★★
Saber	Integrated Hefner model	Physics	★★★★	★★	★★
PSIM/DSIM	Ideal model/ Piecewise analytical transient model	Behavioral	★★	★★★★	★★★★
PLECS	Ideal model	Look-up table	×	★★★★	★★★★
Simulink/Simscape	Ideal model/ N-Channel IGBT model	Behavioral	★★	★★★	★★★

★★★★— Excellent ★★★— Good ★★— General ★— Poor ×— None

★★★★— Excellent ★★★— Good ★★— General ★— Poor x— None

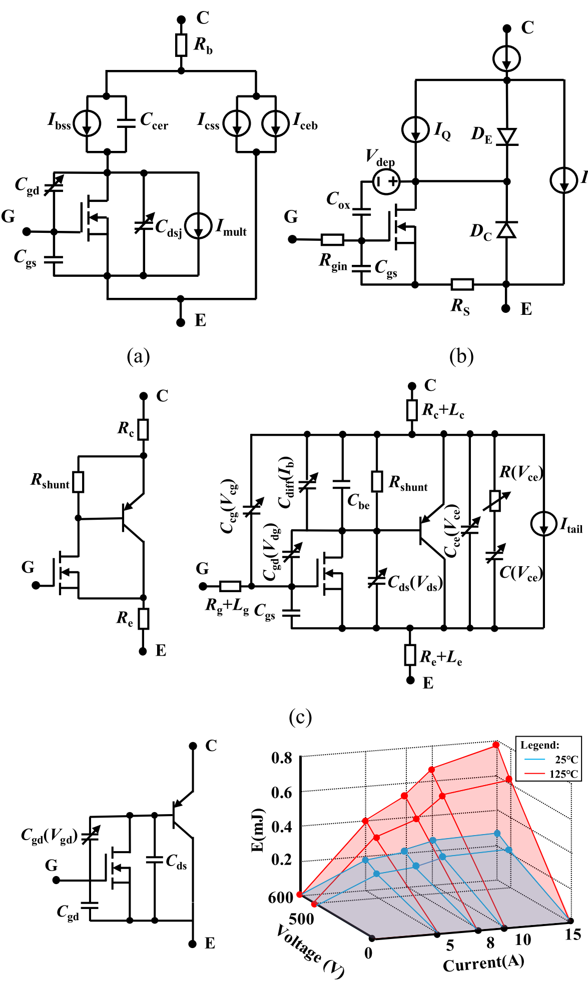

Fig. 1. Common IGBT model in commercial software. (a) Hefner model in Saber. (b) Kraus model in PSpice. (c) Average (left) and dynamic (right) behavioral models in Simplorer. (d) Simple behavioral model in Simscape and DSIM. (e) Look-up table in PLECS.

in Table I. Physical models undoubtedly have the best simulation effect under different dynamic switching conditions. However, fine simulation steps and complicated physical equations seriously reduce simulation efficiency, especially in the PES with numerous devices combination. In contrast, behavioral models simplify nonlinear equations based on curve-fitting methods rather than on device physics [6], which means the model has better simulation efficiency and convergence, but cannot maintain high calculation accuracy under various operation conditions. For example, the calculation accuracy of turn-ON and turn-OFF loss of PAT model under condition A (3000 V, 450 A) can reach 99.98% and 99.35%, respectively, whereas under condition B (3000 V, 200 A) can achieve only 66.63% and 80.42% [13]. In addition, since the time constant of the thermal behavior inside power device is normally up to several seconds under cooling system [16], look-up table model, combined with ideal device model ignoring switching transients, is proposed to attain long-term power loss and thermal simulation with higher speed [17], [18].

In addition to the IGBT device model, the thermal model also greatly affects the simulation accuracy and speed. Finite-element method (FEM) solving 3-D differential heat flow equation can accurately obtain the temperature distribution inside the device, but with massive calculation and limited time span [16]. By contrast, conventional 1-D *RC* lumped models are efficient and easily implemented in a circuit simulator with a relatively high simulation speed. However, ignoring thermal coupling effects might result in the underestimate of junction temperature prediction in multichip power modules [19]. The 3-D *RC* lumped models achieve a good compromise between the above two models, whereas the problem that limits its application is the complicated modeling process, including a large number of repeated data extraction and fitting [20], [21].

From the above analysis, it can be seen that the essence of current method solving the contradiction between simulation effect and efficiency is to sacrifice part of simulation accuracy in exchange for efficiency. However, the impact of reduced simulation accuracy of electrothermal stress on the safety design of PES is questionable. In addition to the common models in commercial software, other electrothermal models, such as models considering parallel device current sharing [22], [23], device rating information [24], and multitimescale thermal behaviors [25], [26], were proposed. But these models also cannot

reach the simulation accuracy of physical models, especially in terms of switching transient simulation. The article attempts to introduce the simulation accuracy of physical models into the system-level PES simulation with the aid of artificial neural networks (ANNs). In order to further apply this method to high-power multichip IGBT modules, this article has made the following contributions compared with the previous research [27].

1) Object: The research focus of this article goes further from the entire device to chips within the device, thus taking into account the effects of uneven dynamic current and thermal coupling.
2) Accuracy: The article applied the advanced IGBT physical model, which is lumped-charge IGBT model instead of Hefner model in [27]. Compared with the latter one, the model is with better accuracy and convergence in high power IGBT module simulation, due to its more accurate description on the carrier distribution.
3) Modeling efficiency: The article proposed an optimization training algorithm, which can greatly reduce the amount of data required for the training of ANNs, thus improving the modeling efficiency of ANNs.
4) Applicability: The core calculation processes of the proposed method were implemented automatically, including the optimization training algorithm of ANNs and parameters extraction of 3-D *RC* lumped models. The custom simulation-automation flow solves the limitation of complicated modeling of 3-D *RC* thermal models, improving the applicability of method.

The rest of this article is organized as follows. Section II introduces the IGBT electrical model from IGBT module to single chip, including the physical model for the entire IGBT module and the uneven dynamic current and switching loss ratio model for single chip. Section III describes the 3-D transient thermal model for the accurate junction temperature calculation of single chip. Section IV describes the modeling and training processes of ANN-based IGBT switching transient model. Based on the research works of previous chapters, Section V introduces the complete electrothermal stress calculation process from system to module to chip. The verification and application are also described in this chapter. Finally, Section VI concludes this article.

II. Electrical Model From IGBT Module to Chip

A. Introduction to the High-Power IGBT Module

To increase the power level of power electronic devices, IGBT modules are required to use more chips in parallel to improve the current capacity. To illustrate the application of the proposed method on high-power modules, this article focuses on the device rated 225 A and 1.2 kV. The device is a half-bridge IGBT module, which consists of six IGBT chips and six diode chips. Each arm is composed of three IGBT chips and three diode chips connected in parallel, as shown in Fig. 2(a). Thus, the electrothermal behavior of each chip is significantly different due to the asymmetric distribution of parasitic parameters shown in Fig. 2(b), increasing the overstress risk of single chip. The

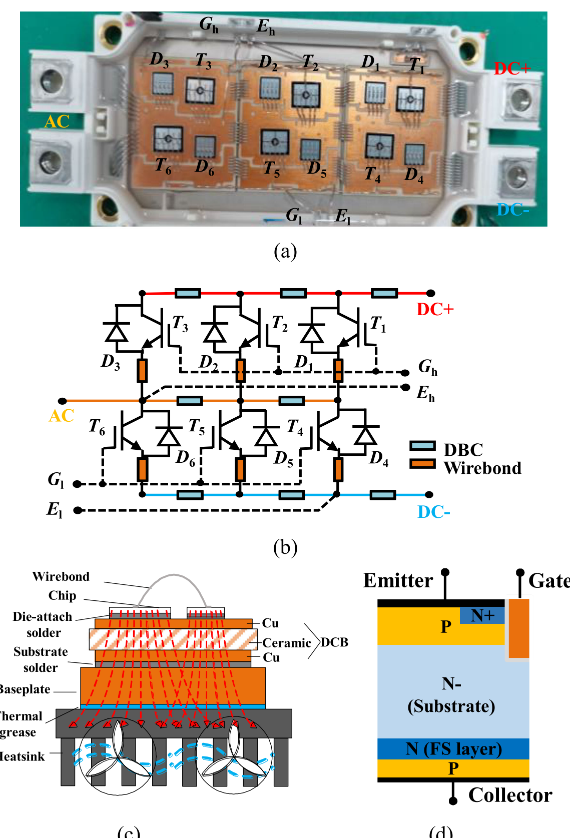

Fig. 2. Researched IGBT module. (a) Layout. (b) Parasitic parameters. (c) Cross section. (d) IGBT chip structure.

detailed cross section is shown in Fig. 2(c), where DCB refers to direct copper bonding substrate. In practical applications, the module is mechanically fixed on the heat sink to enhance heat dissipation efficiency. Between the heat sink and IGBT module, the thermal interface material such as thermal grease is used to reduce contact thermal resistance. It can be seen that there are thermal cross-coupling effects due to the partial overlap of the heat conduction paths between different chips inside the module. The IGBT chip is the trench field-stop (FS) structure, as shown in Fig. 2(d), where the FS layer can effectively reduce the thickness of the chip, and the trench gate enables a more pronounced carrier storage effect in N-region [28].

B. Physical Model for the IGBT Module

In this section, the researched IGBT module is considered as a whole, thus ignoring the uneven switching transient among the three parallel chips of one bridge arm. The lumped-charge IGBT model is applied to describe the dynamic behavior at switching transient, replacing the Hefner model in the previous research [27]. Compared with other physical models, the lumped-charge model does not need to solve the ambipolar diffusion equation in the drift region, so the complexity of the model is greatly reduced [29], [30]. The basic modeling process is introduced in Appendix A. Besides, the detailed part of the model referred to other references is not introduced in the article, including the extraction method of the model parameters [28], [31], [32], the

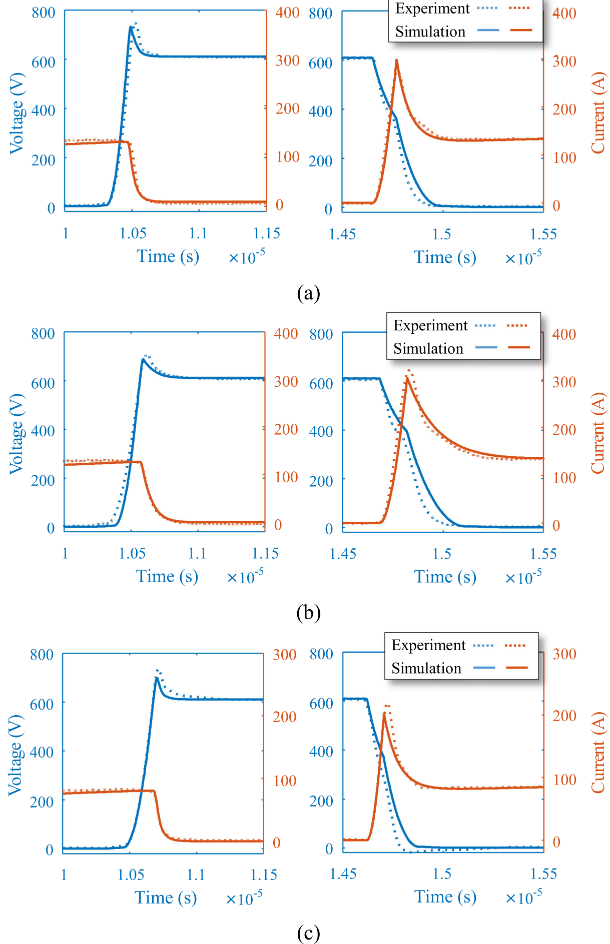

Fig. 3. Switching transient waveforms (left: turn OFF transient, right: turn ON) at (a) $V_{dc} = 600$ V, $I = 125$ A, $T_j = 20$ °C, $R_g = 2.5\ \Omega$; (b) $V_{dc} = 600$ V, $I = 125$ A, $T_j = 125$ °C, $R_g = 2.5\ \Omega$; and (c) $V_{dc} = 600$ V, $I = 80$ A $T_j = 20$ °C, $R_g = 5\ \Omega$.

temperature dependence of the model [3], [29], and the physical model of freewheeling diode [33], [34].

To verify the accuracy of the model, a series of double pulse tests (DPTs) under different load currents I, bus voltages V_{dc}, junction temperatures T_j, and gate resistances R_g are carried out. The test platform consists of power sources, measurement probes, signal generator, heating plate, and passive components. The turn-ON and turn-OFF IGBT collector current and collector–emitter voltage transient waveforms under three different test conditions are shown in Fig. 3, where the only processing was the smoothing on the original test data besides the necessary time calibration between the test and simulation data. It can be seen that the simulation waveforms are in good agreement with the experimental ones. Moreover, the results of extracted switching parameters in DPTs are shown in Fig. 4, where the switching loss includes turn-ON loss E_{on}, turn-OFF loss E_{off}, total switching loss E_{tot} and switching time includes rise time t_r and fall time t_f. V_{max} and I_{max} are the maximum voltage and current stresses on the device, respectively. It can be concluded that the model has high accuracy under different switching conditions with the maximum error of switching loss and time less than 10%. The comparison results verified the established lumped-charge IGBT model has a wide range of applicability in switching transient simulation.

C. Uneven Dynamic Current and Switching Loss Ratio Model for Single Chip

In the multichip IGBT module, the dynamic current sharing among parallel chips is quite uneven due to the asymmetric layout, as discussed in [35]–[38]. Fig. 5 shows the dynamic current of each IGBT chip measured by the Rogowski coil rated at 120 A under DPTs. It can be seen that among all switching processes, the uneven turn-ON losses of low-side chips are the most severe, which cannot be ignored at high-frequency inverter applications. Therefore, the model proposed in this section is for the low-side chips.

When the low-side chips turn ON, the current direction is shown as Fig. 6(a), considering the mutual inductances among different commutation loops. After detailed circuit analysis in our previous research [39], the mutual inductances can be decoupled, as shown in Fig. 6(b). The final calculation result is given as

$$\mathbf{I_{REF}} = \left(U_{GO} - U_{th} - \sqrt{\frac{I_\mathbf{C}}{12\beta}}\right)\left(\frac{\sqrt{3}}{2\sqrt{\beta I_\mathbf{C}}}\mathbf{E} + \mathbf{F}\right)^{-1}\mathbf{I} \tag{1}$$

where

$$\mathbf{F} = \begin{bmatrix} L_W/t_\mathbf{r} & -L_{EQC2}/t_\mathbf{r} & -L_{EQC2}/t_\mathbf{r} \\ 0 & (L_{EQC1} + L_W)/t_\mathbf{r} & L_{EQC1}/t_\mathbf{r} \\ 0 & L_{EQC1}/t_\mathbf{r} & (L_{EQC1} + L_W + L_{EQC})/t_\mathbf{r} \end{bmatrix}$$

$L_{EQC2} = L_{C2}–(M_{C2_2}+M_{C2_1})/2$, $L_{EQC1} = L_{C1}–(M_{C1_2}+M_{C1_1})/2$, and $L_{EQC} = L_C–(M_{C_2}+M_{C_1})/2$. $\mathbf{I_{REF}} = [I_{REF_4}, I_{REF_5}, I_{REF_6}]^T$.

Therefore, the ratio of turn-ON loss for each chip at low side on the total turn-ON loss can be approximately expressed as

$$n_k = \frac{\int_{t_1}^{t_2} i_k(t) \times U_\mathbf{CE}(t)dt}{\sum_{k=4}^{6}\int_{t_1}^{t_2} i_k(t) \times U_\mathbf{CE}(t)dt} \approx \frac{I_\mathbf{REF_k}}{\sum_{k=4}^{6} I_\mathbf{REF_k}}. \tag{2}$$

The detailed derivation process and verification of the model can refer to the previous research [39], where the comparison results between the proposed analytical model and DPTs verify the accuracy of the model under various operation conditions.

III. 3-D Transient Thermal Model for Single Chip

In this section, a 3-D thermal model based on Foster networks is established for single chip. The superiority of 3-D thermal model is that it considers the thermal coupling effects among chips, compared with the traditional 1-D one. For the considered chip, the temperature rise introduced by the adjacent chip needs to be also calculated besides itself. To improve the feasible of 3-D thermal model in practical engineering, the model was innovatively simplified in terms of calculation and modeling processes, respectively.

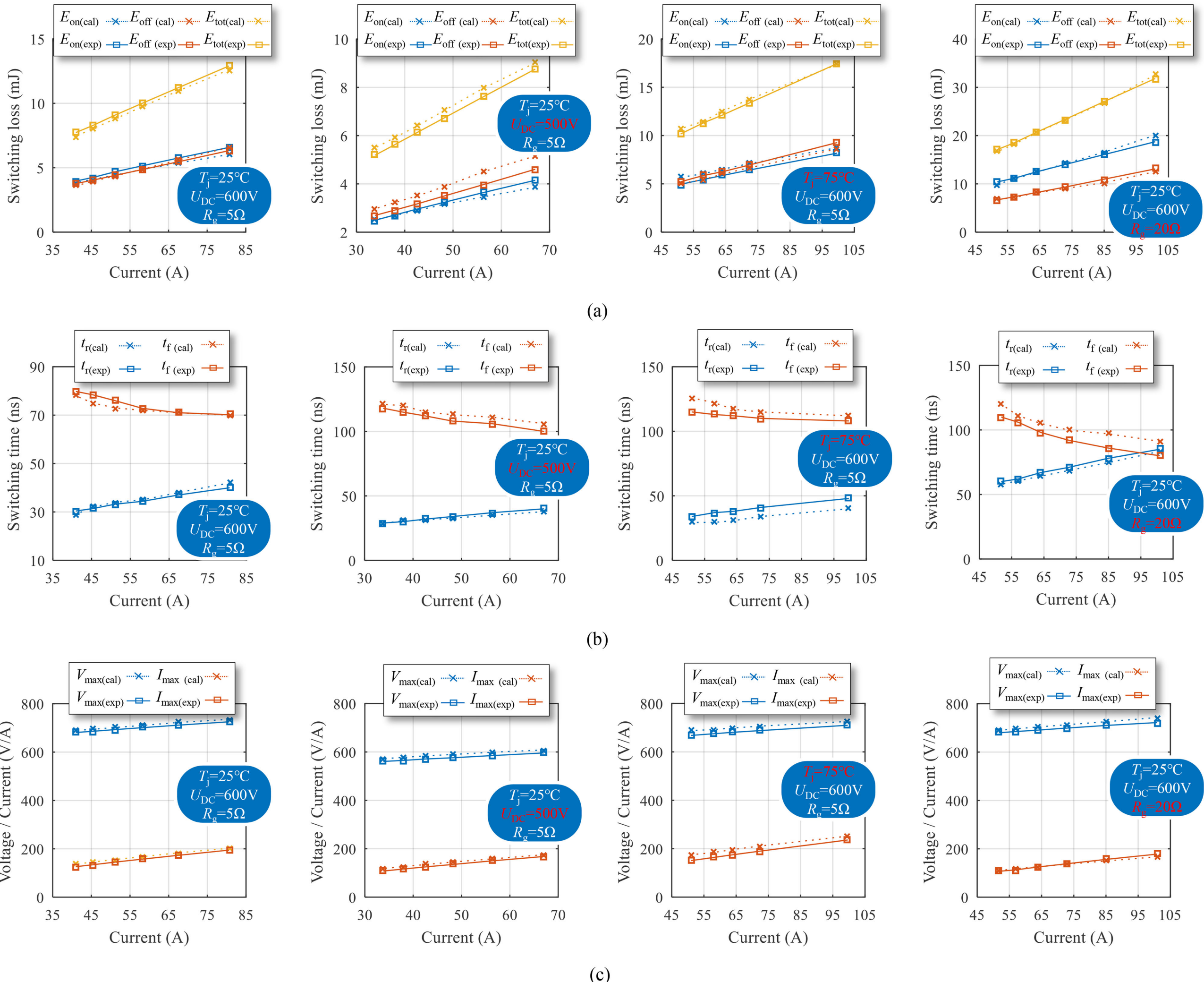

Fig. 4. Results of extracted switching parameters in DPTs: (a) switching loss, (b) switching time, and (c) voltage/current stresses.

A. Simplification in Calculation

The order of *RC* network for the thermal model is important to the calculation accuracy and efficiency, which is generally set to four. In order to set the order reasonably, an FEM model is built in COMSOL to study the transient thermal behavior of considered IGBT module, as shown in Fig. 7(a). The step size is set to ten times per decade of frequency under the logarithmic definition method. Besides, the boundary condition is set to convective heat transfer coefficient (htc) of 3000 W/(m^2·°C), to simulate the cooling performance of water-cooled heatsink. Applying 100 W step power loss on chip T_1, the temperature of chips T_1 and D_1 at each time step, $T_{\mathrm{j_1}}$ and $T_{\mathrm{j_2}}$ are extracted and shown in Fig. 7(b). The transient thermal impedances are defined as

$$Z_{\mathrm{th}m,m} = \frac{T_{\mathrm{j_}m} - T_{\mathrm{a}}}{P_m} \tag{3}$$

$$Z_{\mathrm{th}m,n} = \frac{T_{\mathrm{j_}n} - T_{\mathrm{a}}}{P_m} \tag{4}$$

where $Z_{\mathrm{th}m,m}$, $T_{\mathrm{j_}m}$, and P_m are the self-transient thermal impedance, junction temperature, and step power loss of *m*th chip, respectively. $Z_{\mathrm{th}m,n}$ is the mutual-transient thermal impedance, which represents the thermal impact of P_m on *n*th chip. T_{a} is the ambient temperature. According to the definition, the transient thermal impedances $Z_{\mathrm{th}11}$ and $Z_{\mathrm{th}12}$ are obtained and fitted by *n*th-order Foster network, as shown in Fig. 7(c). According to the root-mean-squared error (RMSE) of fitting results in Fig. 7(d), for the self-transient thermal impedance, the higher order can describe the more detailed thermal characteristics of multilayer structure shown in Fig. 2(c), thus increasing the fitting accuracy. As for the mutual-transient thermal impedance, the increase of the order has a limited impact in accuracy. Therefore, the optimal fitting orders of the self-transient and mutual-transient thermal impedances are four and one, respectively, considering both simulation accuracy and efficiency. The conclusion applies to most IGBT power modules with multilayer structure.

By the proposed theory, the total order of *RC* networks for the considered IGBT module is 180, including 48 of 12 sets of

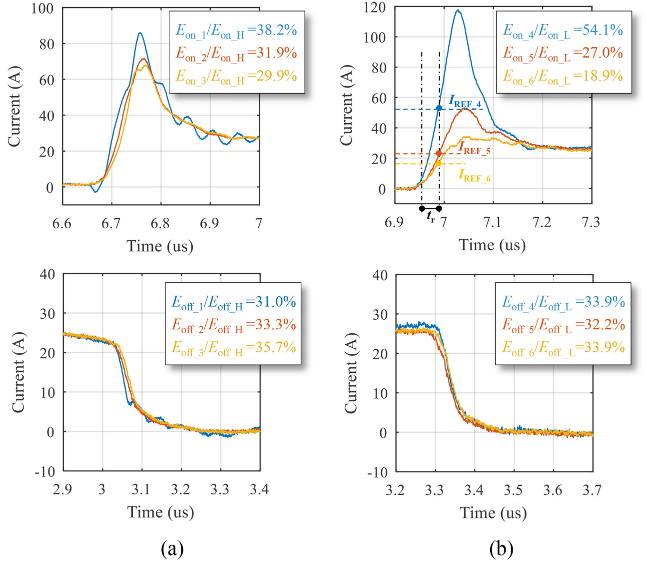

Fig. 5. Measured switching waveforms and energy losses of (a) high-side parallel chips and (b) low-side parallel chips.

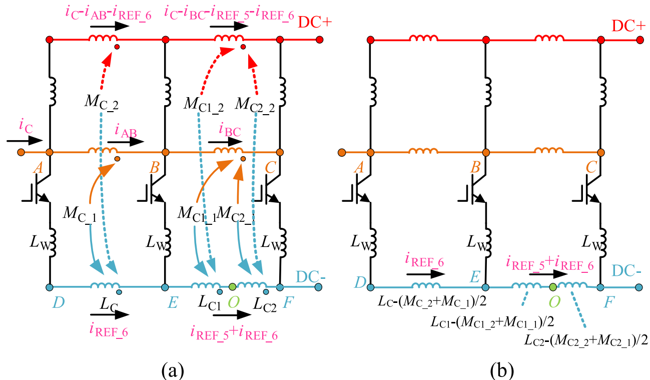

Fig. 6. Equivalent circuit diagrams at turn-ON transient of low-side parallel chips: (a) circuit considering mutual inductances and (b) decoupled circuit.

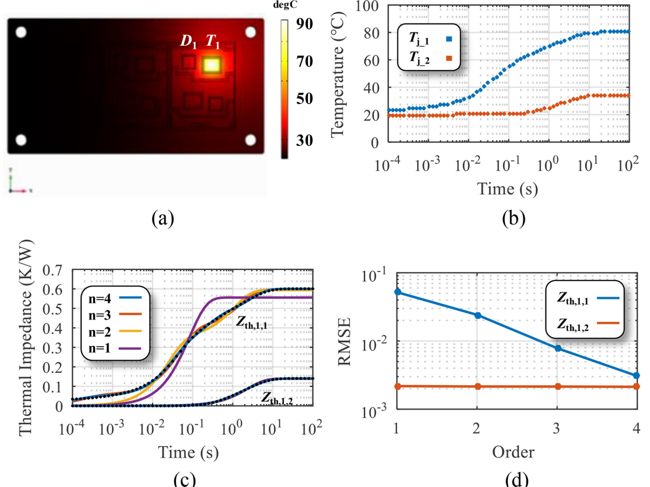

Fig. 7. Research on the transient thermal behavior of IGBT modules. (a) Transient FEM thermal model. (b) Transient temperature of chips. (c) Transient thermal impedance under different fitting orders. (d) RMSE of transient thermal impedance fitting results under different fitting orders.

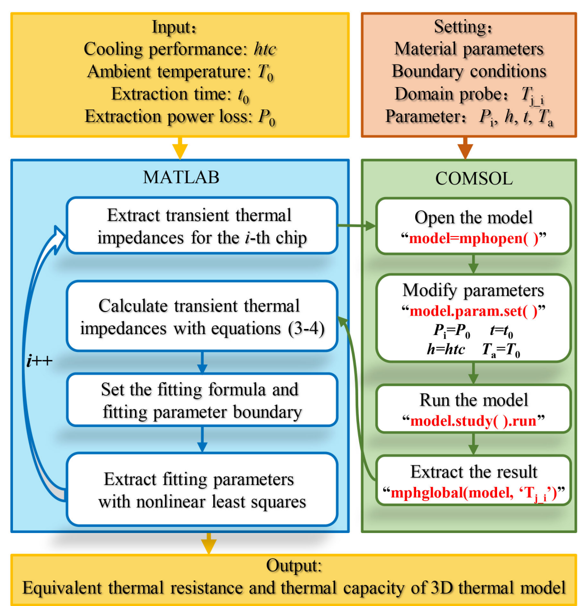

Fig. 8. Automated parameters extraction process for 3-D thermal model.

$Z_{thm,m}$ and 132 of 132 sets of $Z_{thm,n}$, which is much smaller than the 576 by the traditional theory (four orders for both each $Z_{thm,m}$ and $Z_{thm,n}$). Thus, the calculation efficiency of 3-D thermal model is significantly increased. After discretization, the complete calculation process of junction temperature for each chip inside IGBT modules is shown in Appendix B.

B. Simplification in Modeling

Although with better performance compared with 1-D thermal model, the modeling process of 3-D thermal model is too cumbersome especially for the power model with a large amount of chips. For the considered IGBT module with six IGBT chips and six diode chips, 12 transient thermal simulations in FEM software need to be performed first. Then, 144 fitting process with nonlinear least squares method on the simulation results need to be performed in MATLAB. Finally, 180 sets of thermal resistance and capacity of foster networks need to be extracted. To replace repetitive manual operations, an automatic parameters extraction process based on MATLAB-COMSOL cosimulation is proposed, as shown in Fig. 8. Before the extraction process starts, the corresponding settings need to be made in COMSOL in advance, including material parameters, boundary conditions, domain probes for chip temperatures, and so on. The realization of the automatic extraction process is to call COMSOL cyclically by MATLAB script, e.g., function "mphopen" for model opening and "mphglobal" for results extraction. Besides, the boundary of fitting parameters needs to be preset in the script to ensure good fitting results.

C. Model Verification

A transient FEM thermal model is performed to verify the accuracy of the proposed 3-D Foster network-based thermal model. The boundary condition settings of the two models are the same, which are 10 000 W/(m^2·°C), and the power losses applied

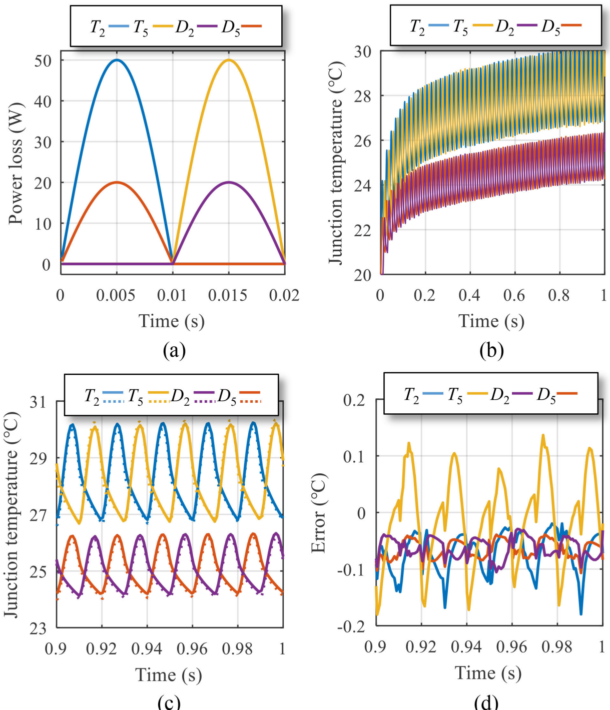

Fig. 9. Model verification of the proposed 3-D thermal model. (a) Power losses applied on each chip. (b) Simulation results of transient FEM thermal model. (c) Comparison results between the transient FEM thermal model (solid line) and the proposed model (dotted line). (d) Errors between the two models.

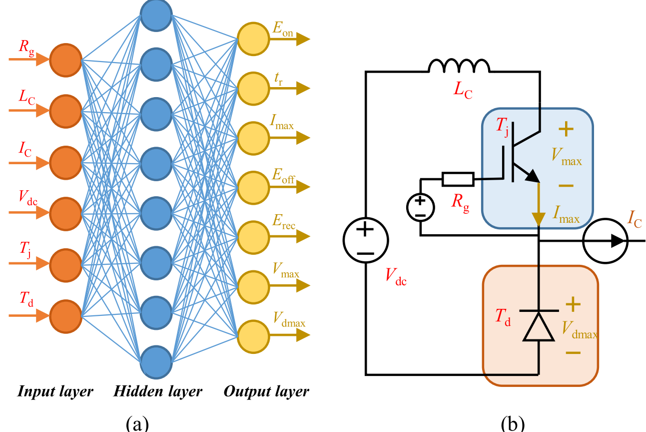

Fig. 10. Established ANN model. (a) Structure. (b) Parameter illustration.

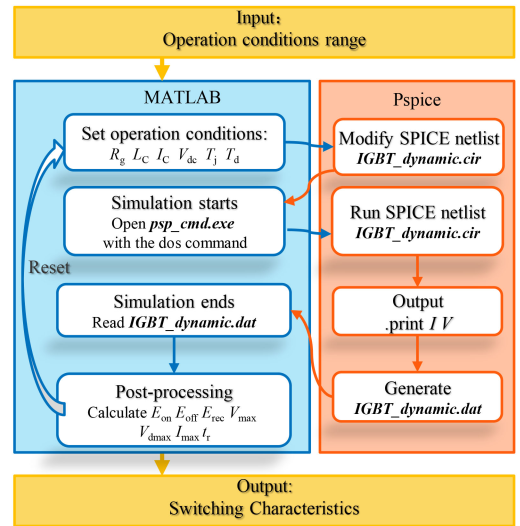

Fig. 11. Automated data extraction process for the training of ANN.

on each chip are shown in Fig. 9(a). The simulation results of transient FEM model are shown as Fig. 9(b), and it had to take 100 min execution time to simulate the 1 s transient temperature. By contrast, the simulation result of the proposed 3-D thermal model implemented by MATLAB is shown in Fig. 9(c) with the calculation time less than 10 s. Further, the error of the proposed model, compared with FEM model, is shown in Fig. 9(d). The comparison results show that the proposed 3-D thermal model can achieve the accuracy close to that of the FEM thermal model in the calculation of transient junction temperature, with a great increase in calculation efficiency.

IV. ANN-Based IGBT Switching Transient Model

A. Model Description

An ANN-based IGBT switching transient model is proposed to avoid excessive calculation for IGBT physical model in system-level simulation. Once the accurate mapping relationship between switching transient parameters and system parameters is established with the aid of ANN, the simulation software does not need to reduce the step size to solve the complex physical equations at each switching transient, thus greatly improving the simulation efficiency.

Since the main function of ANN is data fitting, a two-layer feedforward network with sigmoid hidden neurons and linear output neurons was used in this article, which can fit multidimensional mapping problems arbitrarily well given consistent data and enough neurons in its hidden layer. In detail, the structure of ANN is shown as Fig. 10(a), including input layer, hidden layer, and output layer. The number of sigmoid hidden neurons is set to 10. The feature illustration is shown as Fig. 10(b). For input layer, features are derived from system simulation, including the circuit constant loop parasitic inductance L_C and R_g, electrical variables I_C and V_{dc}, thermal variables T_j, and junction temperature of diode T_d. For output layer, features include the switching loss, maximum voltage and current stress, and rise time t_r for the calculation of (1). The lumped-charge IGBT model established in PSpice is applied as the data source for the ANN, and its accuracy has been verified in Section II. However, independent PSpice model is not suitable for the extensive data acquisition since the simulation waveform cannot be converted into the desired features automatically. In order to improve modeling efficiency, a MATLAB-PSpice cosimulation script is established, as shown in Fig. 11. Once operation condition range (e.g., V_{dc} from 200 to 800 V, once per 100 V) is determined, the script will automatically modify operation parameter in the SPICE netlist (e.g., IGBT_dynamic.cir) of switching transient simulation before each simulation. Then, the

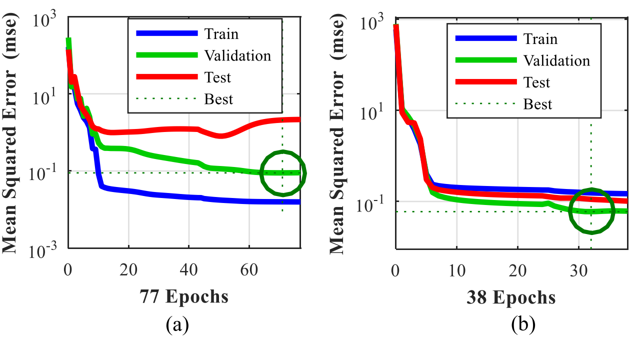

Fig. 12. Typical training performance with (a) 100 sets of data and (b) 700 sets of data.

netlist is run by the command prompt of PSpice (psp_cmd.exe). When the simulation ends, the current and voltage of devices are automatically exported and generated as a data file (e.g., IGBT_dynamic.dat). Finally, the data file is read by MATLAB script for the calculation of the switching characteristics. The established batch calculation script can realize automatic data acquisition under unsupervised situation.

B. Optimization Training Algorithm for ANN

The purpose of the optimization algorithm is to reduce the dataset size of ANN training to improve the modeling efficiency. Fig. 12 shows the typical training performance with different sets of data size. The increase in dataset will undoubtedly improve the prediction accuracy of the ANN model, but the calculation cost increases sharply since it takes dozens of seconds to obtain a set of data, including the time of physical model running and simulation data processing. On the contrary, the risk of overfitting for ANN will increase when the size of datasets is small, as shown in Fig. 12.

In the process of ANN modeling, the dataset acquisition and ANN training are both implemented based on MATLAB script, providing the ability of real-time training during the data acquisition process. Therefore, an optimization training algorithm for ANN is proposed, as shown in Fig. 13. When the operation condition range is determined, 100 sets of data are generated randomly. During the training process, K-fold cross-validation ($K = 10$) is applied to evaluate the performance of the ANN under the current dataset size. The dataset is randomly divided into K parts, (K–1) part is selected as the training set, and the remaining one part is used as the test set. The cross-validation is repeated K times, and the average of the accuracy is taken to evaluate the applicability of the current size of dataset, based on the following formulas:

$$\frac{MSE_test(i) - MSE_train(i)}{MSE_test(i)} < 0.1 \tag{5}$$

$$\frac{MSE_test(i) - MSE_test(i-1)}{MSE_test(i)} < 0.1 \tag{6}$$

where MSE_test and MSE_train are the average mean squared error (MSE) of test and train data in K-fold cross-validation, respectively. Formula (5) requires that the gap between the training error and the test error is small enough to ensure that the model has sufficient generalization ability. Formula (6) requires that the increase in dataset size will not bring significant improvement on the accuracy of ANN. In the training process, the dataset size will continue to increase until the above formulas are both satisfied.

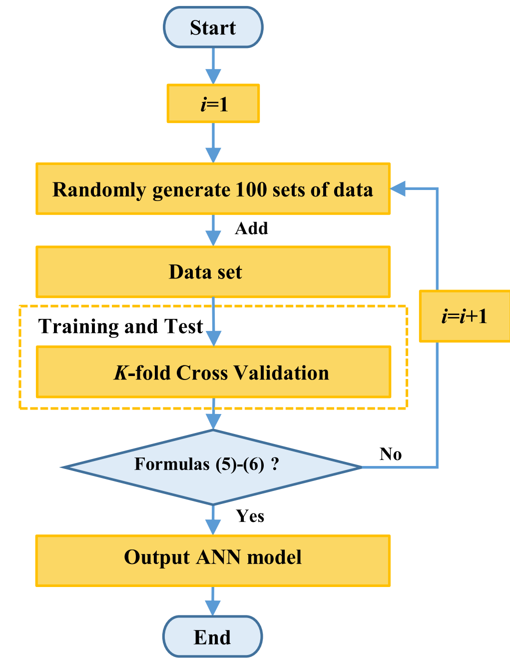

Fig. 13. Optimization training algorithm for ANN.

As a result, Fig. 14 shows the trend of MSE during the training process. When the size of the dataset is small at the beginning of training, MSE_test is significantly larger than MSE_train, illustrating that the generalization ability of ANN is poor. As the size of the dataset increases, MSE_test gradually decreases to approximately the same as MSE_train. According to Fig. 14, the final optimized size of dataset was 400, and the final MSEs of test data for switching loss (MSE_{SW}), maximum voltage and current stresses (MSE_{IV}), and rise time (MSE_{t}) were 0.17, 75, 1.8, respectively. The relative error can be approximately calculated by the following formula:

$$E_{sw} = \frac{\sqrt{MSE_{SW}}}{AVE_{SW}} = \frac{0.41\,mJ}{34.64\,mJ} \times 100\% = 1.184\% \tag{7}$$

$$E_{iv} = \frac{\sqrt{MSE_{IV}}}{AVE_{IV}} = \frac{8.67}{872} \times 100\% = 0.994\% \tag{8}$$

$$E_{t} = \frac{\sqrt{MSE_{t}}}{AVE_{t}} = \frac{1.34\,ns}{124\,ns} \times 100\% = 1.081\% \tag{9}$$

where AVE_{SW}, AVE_{IV}, and AVE_{t} are the average norm of switching losses, maximum voltage and current stresses, and rise time in the test dataset, respectively. It can be seen that the relative errors between the prediction of ANN and the actual value are close to 1%, which can verify that the trained ANN has quite high accuracy. Correspondingly, the proposed optimization training algorithm can achieve a good tradeoff between accuracy

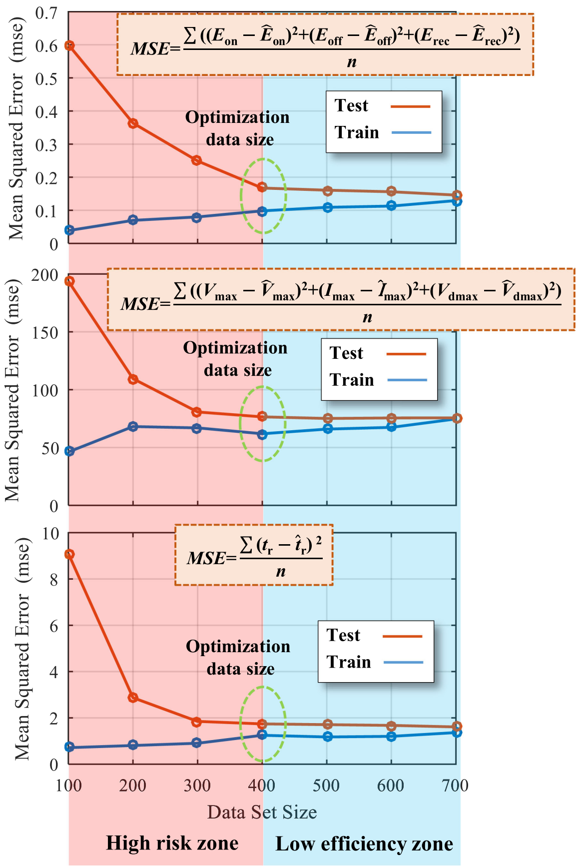

Fig. 14. Trend of MSE during the training process as the data size increases.

and efficiency for the modeling of ANN-based IGBT switching transient model.

Finally, the trained ANN model is implemented in Simulink, in form of diagram generated by MATLAB Neural Net Fitting Toolbox. In the proposed stress calculation method, the ANN model is used for the accurate and efficient description on the switching characteristic of the IGBT module, which will be introduced in detail in Section V.

V. Electrothermal Stress Calculation Method: From System to Module to Chip

A. Introduction

The electrothermal stress calculation method is implemented in Simulink, as shown in Fig. 15, also with the aid of other software as PSpice, ANSYS Q3D, and COMSOL.

In system-level simulation, the built-in ideal IGBT model in Simulink is applied by flexible control and modulation strategies. Besides, the electrical and thermal variables at each simulation step are transferred to the subsystem describing module and chip-level device behaviors, together with the set constants. In detail, the set constants include T_a, R_g, and L_C. The electrical variables include I_C, V_{dc}, and S. S is the flag indicating the operation status of the IGBT device, which is determined by the direction of I_C [shown in Fig. 10(a)] and the gate signals. The illustration of S is presented in Table II, where G^l and G^{l-1} are the

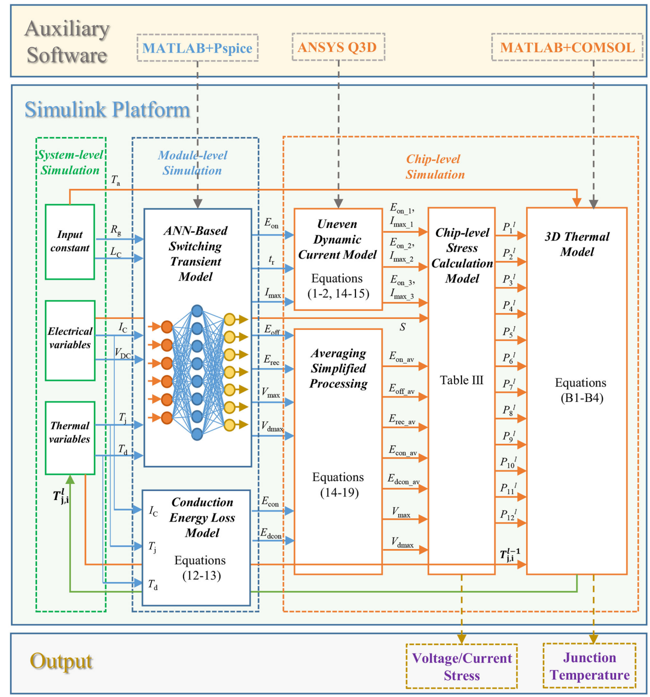

Fig. 15. Complete electrothermal stress calculation process.

TABLE II
Determination Rules of Flag

I_C	G^l	G^{l-1}	S	Description
≥ 0	1	0	1	High-side IGBT chips turn on Low-side diode chips turn off
	1	1	2	High-side IGBT chips conduct
	0	1	3	High-side IGBT chips turn off Low-side diode chips turn on
	0	0	4	Low-side diode chips conduct
< 0	1	0	5	Low-side IGBT chips turn off High-side diode chips turn on
	1	1	6	High-side diode chips conduct
	0	1	7	Low-side IGBT chips turn on High-side diode chips turn off
	0	0	8	Low-side IGBT chips conduct

gate signals of high-side chips at current (lth) and previous time steps, respectively. The thermal variables include the average temperature of parallel chips at each bridge, which are

$$T_j^l = \frac{T_{j,1}^l + T_{j,3}^l + T_{j,5}^l}{3} \text{ or } \frac{T_{j,8}^l + T_{j,10}^l + T_{j,12}^l}{3} \tag{10}$$

$$T_d^l = \frac{T_{j,2}^l + T_{j,4}^l + T_{j,6}^l}{3} \text{ or } \frac{T_{j,7}^l + T_{j,9}^l + T_{j,11}^l}{3} \tag{11}$$

where $T_{j,1}^l$, $T_{j,3}^l$, $T_{j,5}^l$ are the junction temperatures of high-side IGBT chips; $T_{j,8}^l$, $T_{j,10}^l$, $T_{j,12}^l$ are the junction temperatures of

low-side IGBT chips;$T^l_{j,2}$, $T^l_{j,4}$, $T^l_{j,6}$ are the junction temperatures of high-side diode chips; and $T^l_{j,7}$, $T^l_{j,9}$, $T^l_{j,11}$ are the junction temperatures of low-side diode chips.

In module-level simulation, the dynamic and static behaviors of the IGBT module are accurately described. For the dynamic behavior, the considerable features of switching transient are expressed by trained ANN model. For the static behavior, the conduction energy losses are calculated according to the datasheet [40], which are

$$E_{\text{con}}(I_C, T_{\mathbf{j}}) = I_C \times V_{CE}(I_C, T_{\mathbf{j}}) \times \Delta t \tag{12}$$

$$E_{\text{dcon}}(I_C, T_{\mathbf{d}}) = I_C \times V_F(I_C, T_{\mathbf{d}}) \times \Delta t \tag{13}$$

where V_{CE} and V_{F} are the output characteristics of parallel IGBT and diode chips, respectively.

In chip-level simulation, two different methods are adopted to express the ratio of electrical stress between each chip and the entire module. For the current stress and turn-ON energy loss of low-side chips, the unevenness is too obvious to be ignored, especially in the application of high-frequency inverters. For other characteristics, the slight differences among parallel chip are not considered in this article, thus averaging simplified process is adopted. Furthermore, corresponding expressions can be obtained as

$$E_{on_k} = \begin{cases} \frac{1}{3} E_{on}(R_g, L_C, I_C, V_{dc}, T_j, T_d), & k = 1,2,3 \\ n_k \cdot E_{on}(R_g, L_C, I_C, V_{dc}, T_j, T_d), & k = 4,5,6 \end{cases} \tag{14}$$

$$I_{max_k} = \begin{cases} \frac{1}{3} I_{max}(R_g, L_C, I_C, V_{dc}, T_j, T_d), & k = 1,2,3 \\ n_k \cdot I_{max}(R_g, L_C, I_C, V_{dc}, T_j, T_d), & k = 4,5,6 \end{cases} \tag{15}$$

$$E_{off_k} = \frac{1}{3} E_{off}(R_g, L_C, I_C, V_{dc}, T_j, T_d), \quad k = 1 \ldots 6 \tag{16}$$

$$E_{rec_k} = \frac{1}{3} E_{\text{rec}}(R_g, L_C, I_C, V_{dc}, T_j, T_d), \quad k = 1 \ldots 6 \tag{17}$$

$$V_{max_k} = V_{max}(R_g, L_C, I_C, V_{dc}, T_j, T_d), \quad k = 1 \ldots 6 \tag{18}$$

$$V_{\text{d}max_k} = V_{dmax}(R_g, L_C, I_C, V_{dc}, T_j, T_d), \quad k = 1 \ldots 6. \tag{19}$$

According to *S*, the types of electrical stress and energy loss can be determined, as illustrated in Table III, where E_{s}, V_{s}, and I_{s} are the energy loss, voltage and current stresses at current time step, respectively. Therefore, the instantaneous power loss of *i*th chip can be calculated by

$$P^l_{\text{i}} = \frac{E_{\text{s}}}{\Delta t}. \tag{20}$$

Further combining the previous temperature state of each *RC* network, the current junction temperature of each chip can be calculated by the proposed 3-D thermal model. In this way, the chip-level electrothermal stress at current time step can be fully calculated.

TABLE III
CHIP-LEVEL STRESS CALCULATION MODEL

S	T_1—T_3			D_1—D_3		T_4—T_6			D_4—D_6	
	E_s	V_s	I_s	E_s	V_s	E_s	V_s	I_s	E_s	V_s
1	E_{on}	0	I_{max}	0	0	0	V_{dmax}	0	E_{rec}	V_{dmax}
2	E_{con}	0	I_C	0	0	0	V_{dc}	0	0	V_{dc}
3	E_{off}	V_{max}	0	0	V_{max}	0	0	0	0	0
4	0	V_{dc}	0	0	V_{dc}	0	0	0	E_{dcon}	0
5	0	0	0	0	0	E_{off}	V_{max}	0	0	V_{max}
6	0	0	0	E_{dcon}	0	0	V_{dc}	0	0	V_{dc}
7	0	V_{dmax}	0	E_{rec}	V_{dmax}	E_{on}	0	I_{max}	0	0
8	0	V_{dc}	0	0	V_{dc}	E_{con}	0	I_C	0	0

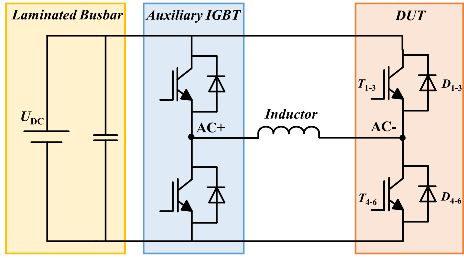

Fig. 16. Topology of the experimental setup.

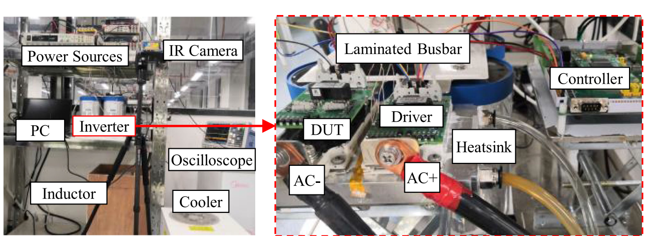

Fig. 17. Inverter experimental setup.

TABLE IV
PARAMETERS OF EXPERIMENT SETUP

Parameter	Value
Power source	1.2 kV /5A
IR camera	FLIR T650sc (30Hz)
Voltage probe	Tektronix P5200A
Rogowski coil	CWT UM 1
Cooling system	Water, 6L/min
DUT (IGBT)	FF225R12ME4
DC link capacitor	6.8mF 1200V
Load inductor	0.5 mH, 400A
Switching frequency	10 kHz
Output frequency	100 Hz

B. Verification

In order to verify the accuracy of the proposed method, an experiment setup was established, as shown in Figs. 16 and 17. The setup consists of an H-bridge inverter, a water-cooling system, and an infrared (IR) thermal camera, and the setup parameters are illustrated in Table IV. Five tests were carried out under different operation conditions, as illustrated in Table V.

TABLE V
VERIFICATION EXPERIMENT DESCRIPTION

Number	*IGBT*	*Stresses of Concern*	*Test Conditions:* R_g=5 L_C=45nH T_a=33℃ h=8000W/(m^2·℃)
I	A	Thermal Current	V_{dc}=250V I_{peak}=100A
II	A	Thermal Current	V_{dc} =250V I_{peak}=200A
III	A	Thermal	V_{dc} =250V 0~20s: I_{peak}=100A; 20~25s: I_{peak}=200A
IV	B	Voltage	V_{dc} =600V I_{peak}=100A
V	B	Voltage	V_{dc} =600V I_{peak}=200A

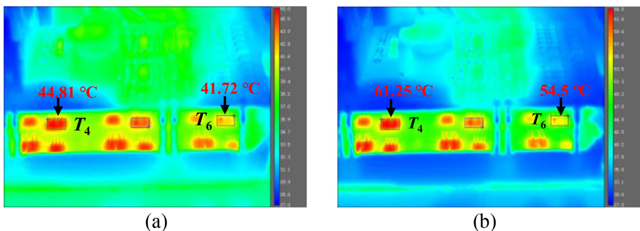

Fig. 18. Temperature distribution by IR camera at (a) Test I and (b) Test II.

On the one hand, an opened and black-painted IGBT module, numbered A, was used for the test of thermal and current stresses of IGBT chips. On the other hand, an intact IGBT module, numbered B, was used for the test of voltage stress at higher bus voltage, due to safety concerns.

For thermal stresses, the temperature distribution among parallel IGBT chips is quite uneven due to the imbalanced witching loss, which can be verified by IR picture in Fig. 18, and chip T_4 has the highest junction temperature. The comparison results between IR camera in Tests I, II, and III and the proposed method are shown in Fig. 19. For the comparison results, the calculated junction temperature fluctuates above and below the measured surface temperature, with a maximum error of less than 3 °C, which can verify the method can describe the transient junction temperature to a certain extent. Since the transient power loss of this article is unknown in advance, which is different from the papers that only focus on thermal models [19]–[21], the calculated junction temperature cannot be completely consistent with the test results. The errors mainly come from the lower sampling frequency of the IR camera on the one hand, and simplify processing of the method itself on the other hand, such as the averaging processing of power loss in parallel diode chips and the negligence on the initial voids of solder layers and thermal grease. However, the maximum temperature inside the IGBT module can be estimated by the method with acceptable error, thereby providing a strong support for the safe design of converters.

For current stresses, the currents of chip T_4 and T_6 inside the IGBT module are measured by Rogowski coil in Tests I and II, and the comparison results are shown in Fig. 20. It can be seen that the differences of transient current among chips can be accurately reflected by the proposed method. For voltage stresses, the comparison results between experiments in Tests IV and V and the method are shown in Fig. 21. The overvoltage stress of the IGBT module, especially at turn-OFF transient, also can be accurately calculated by the method.

TABLE VI
PARAMETERS OF MMC SIMULATION MODEL

Symbols	Meaning	Values
U_{DC}	DC-link voltage	4.5 kV
U_M	Phase voltage (Vrms) of three-phase source	330V
N	Number of SMs	5
L	Arm inductor	5 mH
R_O	Load resistor	0.3 Ω
L_O	Load inductor	3 mH
C_{SM}	SM capacitor	10mF
f_s	Switching frequency	600 Hz
f_{out}	Fundamental frequency	50 Hz

Based on the comparison results of thermal, current and voltage stresses, the accuracy of the proposed method can be fully verified.

C. Case Study

In this section, one case was studied by the proposed method, which is the IGBT module in modular multilevel converter (MMC) system. As far as we know, the electrothermal simulation of MMC system with a large number of series IGBT physical models and complex control algorithm is difficult to implement in Saber or PSpice. With the proposed method, a single-ended MMC simulation model is developed in Simulink. The schematics of MMC and submodule (SM) are presented in Fig. 22, and the system parameters are presented in Table VI. The modulation and control methods of the MMC are based on [41], including a modified phase-shifted carrier-based pulsewidth modulation scheme, a reduced switching-frequency voltage balancing algorithm, and a circulating current suppressing controller.

Fig. 23 shows the results of system-level simulation, including the upper arm, output and difference currents of phase a, voltages of five SM capacitors in the upper arm of phase a. It can be seen that the applied modulation and control strategies have achieved good effects. Fig. 24 shows the results of module-level simulation, including the current and voltage stresses of IGBT module in SM_1 of phase a. The stresses of low side device are significantly larger than high side due to the dc bias of the arm current. Furthermore, Fig. 25 shows the results of chip-level simulation. The junction temperature and current stresses of single IGBT chip can be obviously calculated by the proposed method.

Further, the efficiency of the method needs to be discussed. In detail, it will take approximately 6 h to complete all the modeling of a new IGBT module by the established automatic parameters extraction scripts, including 4 h for the collection of 400 set of data of ANN training, 2 h for the extraction of 3-D thermal impedance and parasitic inductance. Once the modeling of the considered IGBT module is completed, the model can be easily plug and play in any simulation model in Simulink as long as the gate drive signal, the bus voltage, and the bridge arm current

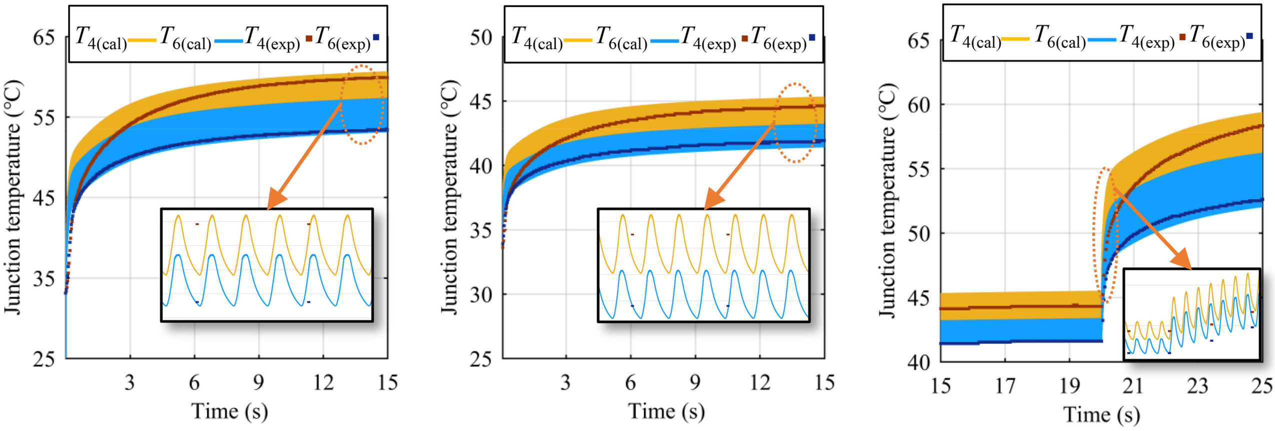

Fig. 19. Comparison results between IR camera (exp) and the proposed method (cal) in (a) Test I, (b) Test II, and (c) Test III.

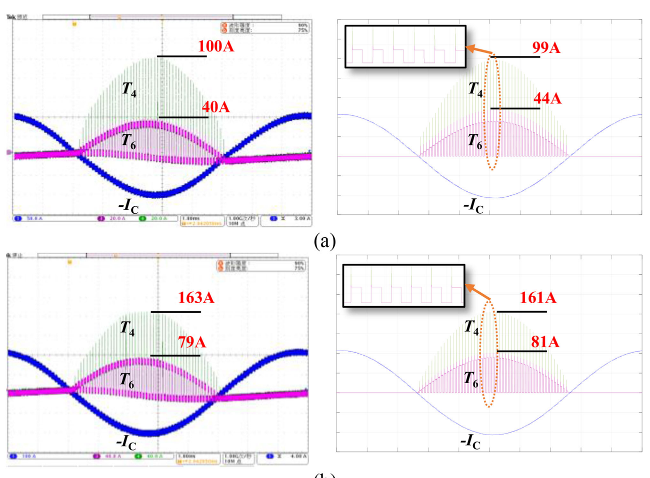

Fig. 20. Comparison results between current test (left) and the proposed method (right) in (a) Test I and (b) Test II.

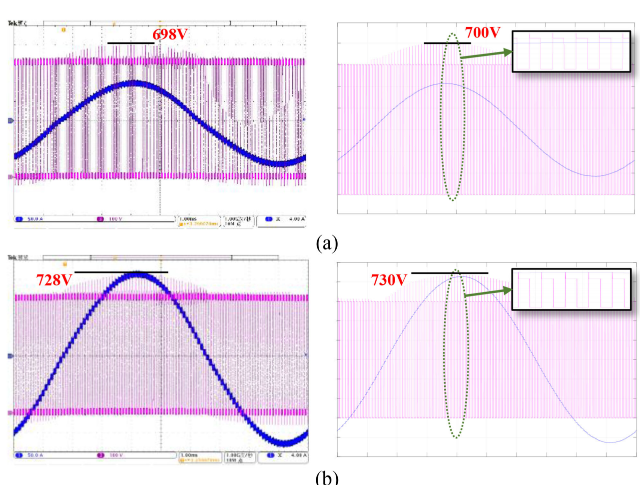

Fig. 21. Comparison results between voltage test (left) and the proposed method (right) in (a) Test IV and (b) Test V.

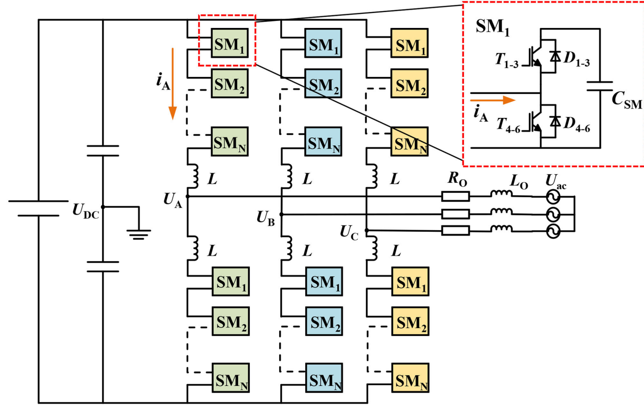

Fig. 22. Schematics of MMC and SM.

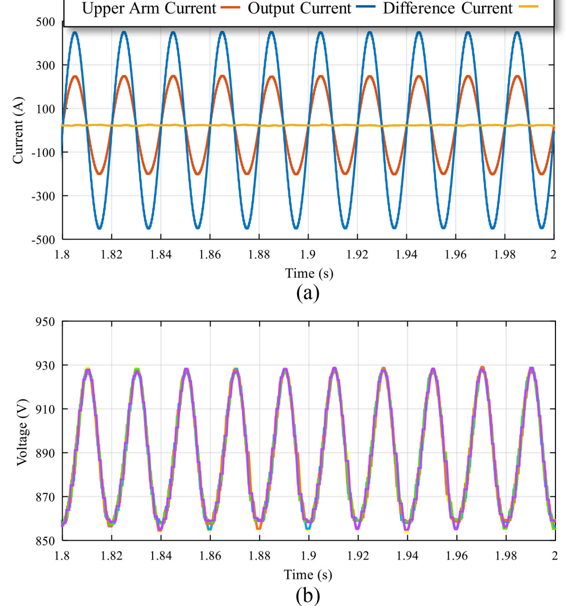

Fig. 23. Results of system-level simulation: (a) currents and (b) voltages of five SM capacitors.

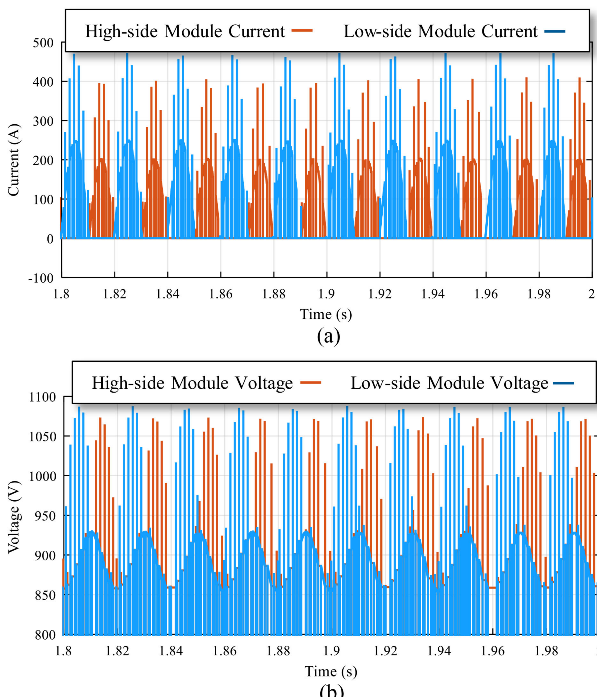

Fig. 24. Results of module-level simulation. (a) Currents. (b) Voltages.

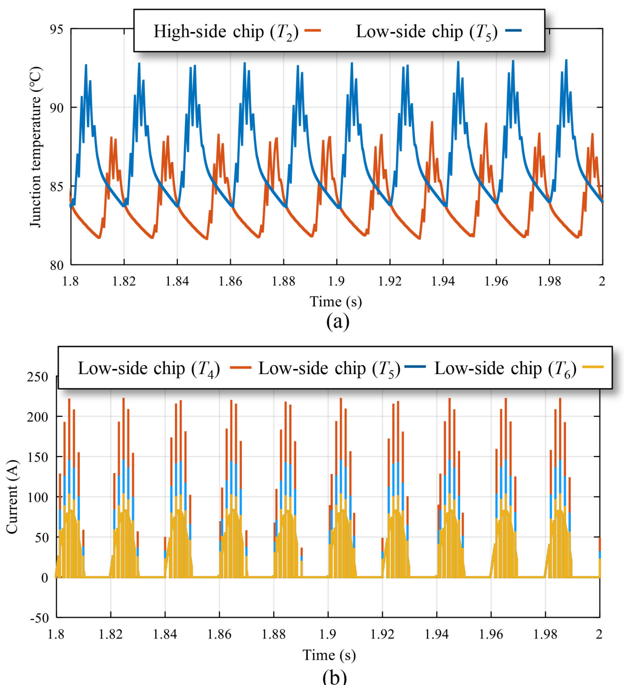

Fig. 25. Results of chip-level simulation. (a) Junction temperatures. (b) Chip currents.

in the original model are connected with the proposed stress calculation subsystem. Further, engineers can obtain quite accurate chip-level stresses at the speed of system-level simulation, with regardless of the topology types and control strategy of the PES. For this article, the method was gradually applied to each SM of phase a in a 2 s simulation with 1e–5 fixed-step size, and the simulation execution time was recorded at the same time, as illustrated in Table VII. The execution time gradually increased as the number of SMs simulated by the proposed method increases. However, the increased time is still within the acceptable range, compared with other circuit software. Besides, the proposed method can be run on a low-end personal computer (PC).

TABLE VII
EXECUTION TIME OF 2 S SIMULATION WITH 1E–5 STEP SIZE

PC Configuration	i7-7700 CPU @ 3.6GHz, 16.0GB RAM					
Number	0	1	2	3	4	5
Execution time	47s	84s	125s	169s	213s	225s

VI. CONCLUSION

This article proposes an ANN-based method to calculate the chip-level stress of IGBT modules in system-level circuit simulation. The accuracy of method has been fully verified by a series of test under inverter prototype. Compared with the conventional methods, the proposed one pays more attention to the chip-level stresses with the acceptable simulation speed. Further to improve the feasibility of the method in practical engineering, the automatic modeling processes of thermal and ANN are also introduced in the article. The method can help evaluate the safety of the device under transient overload conditions, which provides an accuracy and efficient tool for the design of PES. In the future, the simplification on the modeling process will continue to be improved, which is expected to bring greater convenience to engineers.

APPENDIX

A. Lumped-Charge IGBT Model

For the trench FS IGBT, four essential areas need to be accurately modeled, which are the p-n junctions, the lightly doped region (N-region), the FS layer, and the MOS region.

For N-region, the idea of spatial deconstruction is applied, and four subregions are established in the region, as shown in Fig. 26(a). γ_i is the partition coefficient, which satisfies

$$\gamma_2 + \gamma_B + \gamma_3 + \gamma_4 = 1. \tag{A1}$$

The charge concentration p_i at the center or edge of each subregion is used to approximate the charge concentration of the entire region, and a lumped charge node q_{pi} is put in the middle of each subregion to replace the total amount of the subregion, which satisfies

$$q_{pi} = qAp_i\gamma_i d \tag{A2}$$

where q is electronic charge, d is the width of N-region, and A is device active area. According to the current density equation, the hole current $i_{\mathrm{p2,B}}$ and the electron current $i_{\mathrm{n2,B}}$ flowing from

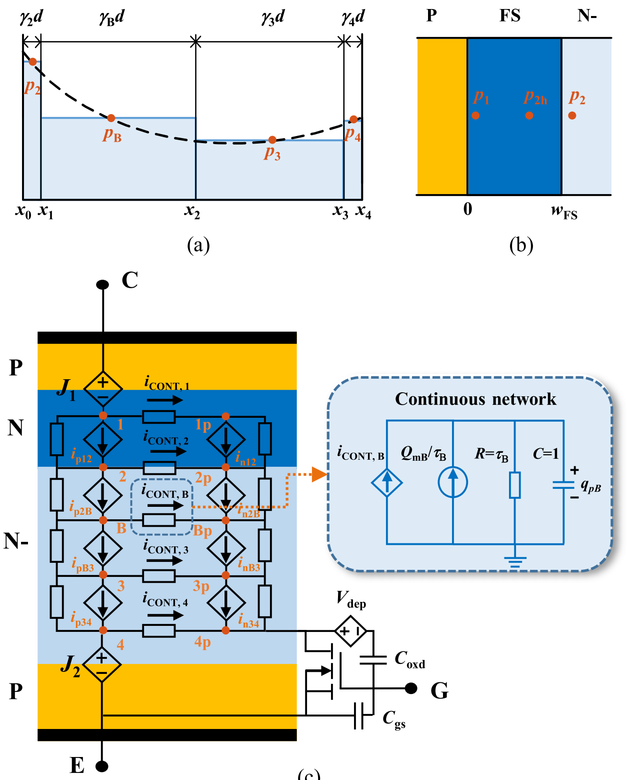

Fig. 26. Lumped-charge IGBT model. (a) Modeling method in N-region. (b) Modeling method in FS region. (c) Model implementation in PSpice.

nodes 2 to B are given as

$$\begin{cases} i_{p2B} = q_{pB}\frac{v_{2B}}{\phi_t \times T_{p2B}} + \frac{q_{p2}-q_{pB}}{T_{p2B}} \\ i_{n2B} = (q_{pB}+Q_{MB})\frac{v_{2B}}{\phi_t \times T_{n2B}} + \frac{q_{n2}-q_{nB}}{T_{n2B}} \end{cases} \tag{A3}$$

where v_{2B} is the potential difference between nodes 2 and B. $\phi_t$is thermal voltage. T_{p2B} and T_{n2B} are the transient transit time between nodes 2 and B, respectively, which are expressed as

$$\begin{cases} T_{p2B} = \frac{\gamma_2+\gamma_B}{2} \times \frac{d^2}{\phi_t \times \mu_p} \\ T_{n2B} = \frac{\gamma_2+\gamma_B}{2} \times \frac{d^2}{\phi_t \times \mu_n} \end{cases} \tag{A4}$$

where μ_p and μ_n are the mobility of electrons and holes, respectively. Furthermore, the recombination current $i_{CONT,B}$ can be derived from charge continuity equation, which is given as

$$i_{CONT,B} = i_{p2B} - i_{pB3} = \frac{dq_{pB}}{dt} + \frac{q_{pB}-Q_{mB}}{\tau_B} \tag{A5}$$

where τ_B is the average excess carrier lifetime in the base region. Q_{MB} and Q_{mB} are the amount of charge of majority and minority carries in subregion B under equilibrium conditions, respectively, which are expressed as

$$\begin{cases} Q_{MB} = qA\gamma_B dN_B \\ Q_{mB} = qA\gamma_B d\frac{{n_i}^2}{N_B} \end{cases} \tag{A6}$$

where N_B is the doping concentration of the N-region, and n_i is the intrinsic carrier concentration. The above equations are also applied to the other three subregions in the N-region.

For FS region, two lumped-charge nodes are placed, as shown in Fig. 26(b). The current density equation and the recombination current of this region follows the same rule as N-region, the only difference is the doping concentration. Therefore, the quasi-equilibrium simplification equation at the boundary is applied to combine the FS region and N-region [5], which is given as

$$p_{2h}(p_{2h}+N_{FS}) = p_2(p_2+N_B) \tag{A7}$$

where N_{FS} is the doping concentration of the FS region.

For the p-n junction, there is a space charge zone, which leads to the capacitance effect in the space charge region of the p-n junction. The capacitance of the p-n junction is classified as the barrier capacitance and the diffusion capacitance. To simplify the model, the barrier capacitance is only considered during the reverse state, whereas the diffusion capacitance is only considered during the forward state. Therefore, the model in J_1 is

$$U_{PN} = \begin{cases} \phi_t ln\left(q_{p1}/Q_{m,FS}\right), q_{p1} > Q_1^* \\ \phi_{PN} - (Q_1^* - q_{p1})^2 \Big/ 2A^2 q\varepsilon_{Si}N_{FS}, q_{p1} \leq Q_1^* \end{cases} \tag{A8}$$

where ϕ_{PN} is the built-in electric potential of the p-n junction, and $Q_1{}^*$ is the amount of charge in the space charge region of the p-n junction in the equilibrium state, which is expressed as

$$Q_1^* = Q_{m,FS}\exp(\phi_{PN}/\phi_t). \tag{A9}$$

The model of J_2 has a similar form.

For the MOS region, only the quasi-static model needs to be considered, since the dielectric relaxation time of the electron in the MOS region is too short compared with the switching time of IGBT. Therefore, a PSpice level-3 MOSFET device with a series voltage-controlled generator on the capacitance C_{oxd} is adopted to characterize the behavior of the MOS region, as shown in Fig. 26(c). The generator V_{dep} is used to represent the nonlinear behavior of the capacitance C_{oxd}, which is controlled by

$$V_{dep} = \begin{cases} V_{DG} + V_n(1 - \sqrt{1+\frac{V_{DG}}{V_n}}), V_{DG} \geq 0 \\ 0 \qquad\qquad\qquad\qquad\quad , V_{DG} < 0 \end{cases} \tag{A10}$$

where V_n is a normalization factor, and V_{DG} is the voltage between drain and gate of the MOS.

The above physical equations need to be converted into a subcircuit for the application in PSpice. According to the method in [30], the nonlinear controlled source is applied to build the IGBT lumped-charge equivalent circuit in the PSpice simulator, as shown in Fig. 26(c).

B. 3-D Thermal Model

Based on 3-D thermal model, the junction temperature for single chip can be calculated by the sum of self-heating temperature and mutual-heating temperature. The self-heating temperature T_{sj,i_k}^l at the lth time step can be calculated by

$$\begin{cases} C_{sth,i_k}\frac{dT_{sj,i_k}(t)}{dT_{sj,i_k}} + \frac{T_{sj,i_k}(t)}{R_{sth,i_k}} = {P_i}^l \\ T_{sj,i_k}(0) = T_{sj,i_k}^{l-1} \end{cases} \tag{B1}$$

where $C_{\mathrm{sth,i_k}}$ and $R_{\mathrm{sth,i_k}}$ are the equivalent thermal resistance and capacity of *k*th order foster network for *i*th chip, respectively. ${P_i}^l$ is the power loss of *i*th chip at *l*th time step. Assuming the simulation time step is Δt, the calculation result is

$$T_{sj,i_k}^{l} = T_{sj,i_k}(\Delta t) = T_{sj,i_k}^{l-1} e^{-\Delta t/\tau_{sth,i_k}} + {P_i}^l R_{sth,i_k}(1 - e^{-\Delta t/\tau_{sth,i_k}}) \quad \text{(B2)}$$

where $\tau_{\mathrm{sth,i_k}} = R_{\mathrm{sth,i_k}} C_{\mathrm{sth,i_k}}$.

Similarly, the mutual-heating temperature $T_{\mathrm{m}j,i_k}^{l}$ at the *l*th step, introduced by *k*th chip, can be calculated by

$$T_{\mathrm{m}j,i_k}^{l} = T_{mj,i_k}^{l-1} e^{-\Delta t/\tau_{mth,i_k}} + {P_k}^l R_{mth,i_k}(1 - e^{-\Delta t/\tau_{mth,i_k}}) \quad \text{(B3)}$$

where $\tau_{\mathrm{mth,i_k}} = R_{\mathrm{mth,i_k}} C_{\mathrm{mth,i_k}}$. $C_{\mathrm{mth,i_k}}$ and $R_{\mathrm{mth,i_k}}$ are the equivalent mutual thermal resistance and capacity of *k*th chip relative to *i*th chip, respectively. Considering the two types of temperature, the junction temperature of *i*th chip $T_{\mathrm{j,i}}$ can be calculated by

$$T_{j,i}^{l} = \sum_{k=1}^{4} T_{sj,i_k}^{l} + \sum_{k=1}^{i-1} T_{mj,i_k}^{l} + \sum_{k=i+1}^{n} T_{mj,i_k}^{l} + T_a \quad \text{(B4)}$$

where *n* is the total number of chips inside the IGBT module. According to (B2)–(B4), the temperature of one power step can be determined by the previous temperature state of each network and the present power loss of each chip.

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