Characterization of Partial Discharges in High-Frequency Transformer Under PWM Pulses

Zhicheng Guo, *Student Member, IEEE*, Alex Q. Huang, *Fellow, IEEE*, Robert E. Hebner, *Fellow, IEEE*, Gian Carlo Montanari, *Fellow, IEEE*, and Xianyong Feng, *Member, IEEE*

***Abstract*—Partial discharge (PD) is a phenomenon often occurring in insulation system defects (cavities), which can significantly affect life and reliability. While broad knowledge on PD phenomenology of high-frequency transformers (HFT) has been achieved under ac sinusoidal voltage, much less work has been done to infer PD behavior under emerging high frequency pulsewidth modulation (PWM) operation conditions. An impediment has been the limited appropriate test equipment. A recently developed novel ±5 kV GaN-based high-frequency PWM supply with controllable *dV/dt*, voltage level and frequency has been developed. This article explores the application of these measurements to the testing of materials in this electrical environment. Two commonly used windings for HFT were tested under different applied voltage magnitudes, frequencies, and slew rates. According to the test results, at high frequency (up to 50 kHz) the electric field generated by space charge deposited by PD occurring during previous PWM pulses plays an important role in PD behavior. The frequency dependent permittivity of the insulation material can also affect PD measurement results.**

***Index Terms*—High-frequency transformers (HFTs), high slew rate, high-frequency, partial discharge (PD), pulsewidth modulation (PWM) supply.**

I. Introduction

PARTIAL discharge (PD) is a local discharge phenomenon, occurring in defects present in insulation systems, which can increase the insulation aging rate [1], [2]. For line frequency transformers, mature standards and industrial practices are in place to guide the PD characterization under line-frequency voltage stress [3]–[5]. However, modern power electronics insulation systems, including the high frequency transformers (HFT) in isolated dc/dc converters, are subjected to high frequency pulsewidth modulation (PWM) voltage stress. With the introduction of wide bandgap power devices, such as SiC and GaN power switches in these power converters, the PWM voltage magnitude, slew rate (*dV/dt*) and frequency can be substantially higher than the Si-based power converters.

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Zhicheng Guo, Alex Q. Huang, and Xianyong Feng are with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78712 USA (e-mail: zcguo@utexas.edu; aqhuang@utexas.edu; x.feng@cem.utexas.edu).

Robert E. Hebner is with the Center for Electromechanics, University of Texas at Austin, Austin, TX 78758 USA (e-mail: r.hebner@ieee.org).

Gian Carlo Montanari is with the Center for Advanced Power Systems, Florida State University, Tallahassee, FL 32306 USA (e-mail: gmontanari@fsu.edu).

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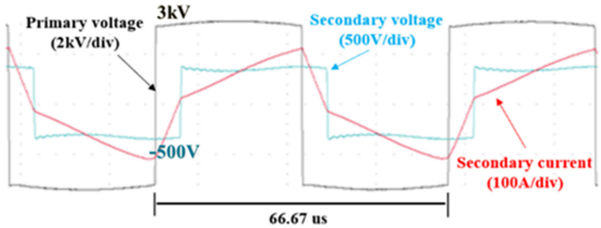

Fig. 1. Typical voltage and current waveforms in a high voltage HFT.

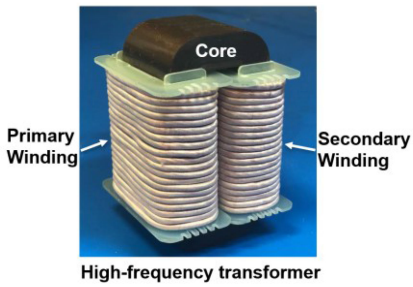

Fig. 2. Litz-wire-based HFT for a 12-kW DAB converter.

The HFT is an important component in any isolated power converter because it provides the galvanic isolation for the system. In most cases, the largest voltage stress of an HFT is between the primary and secondary windings. Fig. 1 shows typical HFT waveforms of a medium voltage SiC converter [6] where the primary voltage is ±3 kV square PWM pulse with a frequency of 15 kHz and the secondary is a phase shifted ±500 V square PWM pulse. Voltage stress on the primary to secondary insulation material is therefore as high as ±3.5 kV.

With the development of higher voltage power converters, such as the solid-state transformer based on medium voltage SiC power switches [7] or modular input series and output parallel converters [8], the voltage stress on the HFT is significantly increasing. Simultaneously, many applications limit the dimensions of HFT to achieve higher power densities. These two constraints together will result in higher electric field stress in the insulating material [9]. Therefore, it is helpful to investigate the PD behaviors in this emerging electrical environment and how the voltage magnitude, frequency and *dV/dt* affect the insulation performance. Different insulating materials can be used in an HFT. Fig. 2 shows a Litz wire winding HFT prototype for a 12

TABLE I
SUMMARY OF PD RESEARCH FOR POWER ELECTRONICS KEY COMPONENTS / SYSTEM AND THE WORK REPORT IN THIS ARTICLE

	DUT	PD Sensor	Waveform Shape	Investigate the effects of voltage changes	Investigate the effects of dv/dt changes	Investigate the effects of frequency changes*
VT(CPES) 2018 [16]	HFT	HFCT	Sinusoidal	YES	N/A	N/A (60 Hz)
EPFL 2019 [17]	HFT	HFCT	Sinusoidal	YES	N/A	N/A (60 Hz)
UT Austin 2020 [18]	HFT	HFCT	Sinusoidal	YES	N/A	N/A (60 Hz)
OSU 2021 [19]	Power module	HFCT/Antenna	PWM	YES	YES	YES (625-25 kHz)
SJTU/SUNY 2021 [15]	Power module	HFCT/Antenna	DC/PWM	YES	N/A	N/A (10 kHz)
VT(CPES) 2022 [20]	MV power converter	HFCT	Sinusoidal	YES	N/A	N/A (60 Hz)
UT Austin [This article]	**HFT**	**HFCT/Antenna**	**PWM**	**YES**	**YES**	**YES (10 kHz-50 kHz)**

*For sinusoidal signals, the frequency refers to the fundamental frequency. For PWM signals, the frequency refers to the pulse repetition frequency, The PWM frequency spectrum depends both on this and *dv/dt*.

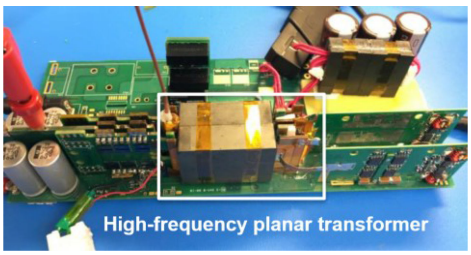

Fig. 3. PCB-winding-based high-frequency planer transformer for a 3.0 kW rated power *LLC* resonant converter.

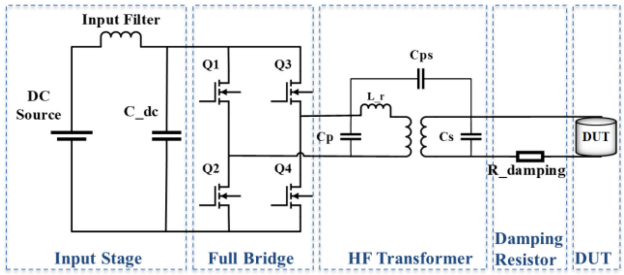

Fig. 4. Scheme of the high-voltage PWM waveform generator.

kW dual active bridge (DAB) converter. In this case, insulation is provided by the insulation on the Litz wire. Fig. 3 shows a printed circuit board (PCB) winding HFT prototype for a 3 kW *LLC* resonant converter [10]. Insulation is provided by the material placed between two PCBs.

To investigate the PD behaviors of HFT under PWM voltage stress, the twisted Litz wire and PCB windings are tested. PD characterization is done under high-frequency repetitive voltage impulses, emulating the electric stress characteristics of operating conditions. To this purpose, a ±5 kV GaN-based innovative high-frequency PWM wave PD tester has been developed [11] and was used in this investigation. There has been limited development of PWM pulse generators specifically for PD characterization. Billard *et al.* [12] and Benmamas *et al.* [13] deal with pulse generators based on insulated gate bipolar transistor (IGBT) devices, [14] and [15] describe high-voltage pulses generation using a 10 kV SiC power module. Compared with other published research, the main contributions of this article are the development and demonstration of a PD testing device that is based on low voltage GaN devices and a high-frequency transformer (HFT) to achieve a lower cost and compact design. The smart PWM generator provides various insulation testing waveforms which include adjustable *dV/dt* at rising and falling edges, with switching frequency up to 100 kHz and output voltage up to ±5 kV.

HFT/medium-frequency transformer (MFT) and semiconductor power module are key components in power electronic system. Recent PD test results relevant to HFT/MFT [16]–[18], high-voltage SiC power module [15], [19] and SiC medium-voltage power converter [20] are given in Table I. The PD behavior of HFT is systematically studied in this article. Comparing with literature work this article provides the following.

1) A comprehensive characterization of the PD behavior for the HFT under high frequency PWM waveforms (varying voltage magnitude, slew rate, and frequency).
2) Information on the effects on PD of with an applied PWM voltage repetition frequency up to 50 kHz which is closer to the actual high frequency operation.

II. HIGH-FREQUENCY HIGH-VOLTAGE PWM PD TEST PLATFORM

The novel high-voltage, PWM waveform generator, circuit topology is illustrated in Fig. 4. It consists of an GaN-based full-bridge inverter with a dc voltage source, a step-up HFT, a variable damping resistor and the device under test (DUT). The full-bridge inverter generates a low voltage PWM wave which is then stepped up in voltage by the HFT. The output voltage *dV/dt* and quality factor are controlled by the variable damping resistor.

Fig. 5 shows the PWM PD tester hardware. The GaN-based full-bridge inverter is realized using 600-V 12-A GaN FET (TI LMG3410R050) and controlled by the digital signal processor control card. The step-up HFT is designed with amorphous magnetic cores with a turns-ratio of 1:12.5. Three-dimensional

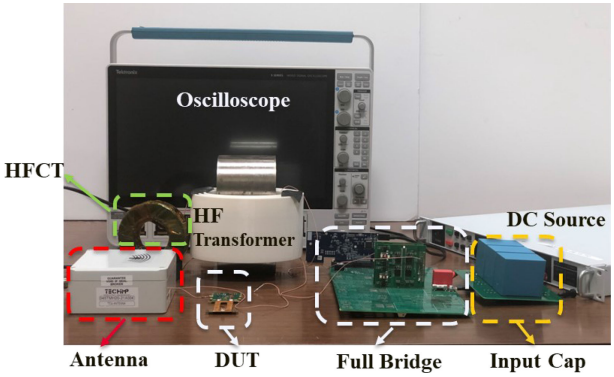

Fig. 5. High-frequency high-voltage PWM waveform PD test platform.

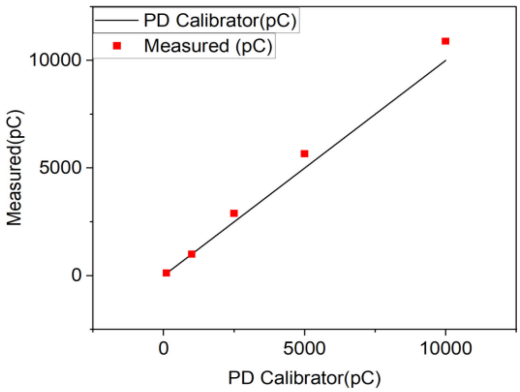

Fig. 6. Measured PD charge value and PD calibrator rating.

printed acrylonitrile butadiene styrene bobbins are used to construct the HFT winding structure. To achieve PD-free design and reduce the parasitic parameters, the HFT windings are potted with silicone gel.

For PD signal detection, a high-bandwidth, high-frequency current transducer (HFCT) (Pearson 6585) and an antenna (Techimp TEM antenna) are used. The TEM antenna and HFCT have a bandwidth of 100 MHz–3 GHz and 400 Hz–250 MHz, respectively. The test platform is remote from the other electric equipment that might induce electromagnetic noise. A comparison test by using a shielded box designed with aluminum foil has been done to verify the test environment is radiation-noise free. Besides, the setup was tested at higher voltage than ±5 kV to be confident that the operating voltage did not introduce spurious signals in the absence of PD in the DUT.

The use of two independent detection schemes to measure the same PD signals enhances reliability. If the two do not agree on the measurement of the small transient signals produced by PD, there will be an obvious inconsistency in the measured data. The system used in this investigation was sufficiently noise-free that consistent measurements were achieved routinely. In addition, the HFCT accuracy was calibrated using a Doble LDC-5/S2 PD calibrator, according to IEC 60270 procedure [4]. Fig. 6 shows the measured PD charge value and the PD calibrator rating. The HFCT was calibrated by a PD calibrator at five charge values (100 pC, 1000 pC, 2500 pC, 5000 pC, and 10000 pC). In time domain, the charge value results from the time integral over the

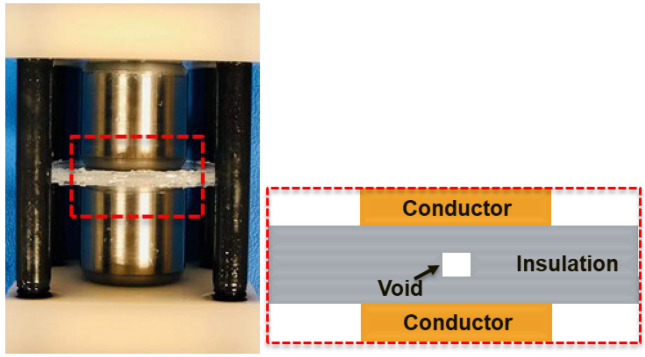

Fig. 7. Proposed benchmark test device.

PD current pulse. The PD charge is calculated as the integral of the first peak over time by applying the method in [21] and [22].

III. Typical Waveforms and PD Mechanism Under PWM Pulses

A. Typical Waveforms

Fig. 7 shows the proposed benchmark test device which include cylindrical electrodes and a three-layer test sample. The test fixture is designed with sufficient pressure to hold the test coupon between conductors. This pressure is sufficiently low to minimize geometry deformation. The material of the test samples is polypropylene (PP), and each layer has a thickness of 0.25 mm. One test sample that is free from significant defects has been tested up to ±5 kV to verify the test platform is PD free. Another test sample has a cylindrical defect with 0.25-mm thickness and 3-mm radius, as shown in Fig. 7. This is a typical setup to test the internal PD with a known geometry defect. It should be noted that the test sample can be immersed in the dielectric oil to remove the PD activity from the triple junctions at higher test voltage and the TEM antenna can still pick up strong signals when internal PD occurs.

Fig. 8 shows the test waveforms under 20 kHz peak-to-peak 7 kV PWM pulses. Fig. 8(a) shows the global waveforms of the first PD signal and followed falling edge and rising edge, the zoom-in waveforms is shown in Fig. 8(b)–(d). PD signals captured by the HFCT and the TEM antenna are presented. The PD occurrence timing and PD relative magnitudes captured by the HFCT and antenna match with each other well. Both the rising and falling edges show a repetitive commutation noise at the beginning of the switching time [23]. In this experiment, the first PD event happened at peak negative voltage.

In general, all PD signals occurred near a zero crossing or near the peak voltage of falling and rising edge. This raises the challenge of differentiating PD occurring in the vicinity of the rising and falling edges from commutation/switching noise. HFCT measurements shows that the frequency of the commutation noise during rising and falling edge is lower than the upper band of PD signals. Hence, when PD happen, the high frequency signal is superimposed on the low frequency waveform, as shown in the zoom-in waveforms of Fig. 8. Since TEM antenna has a bandwidth of 100 MHz–3 GHz, the lower

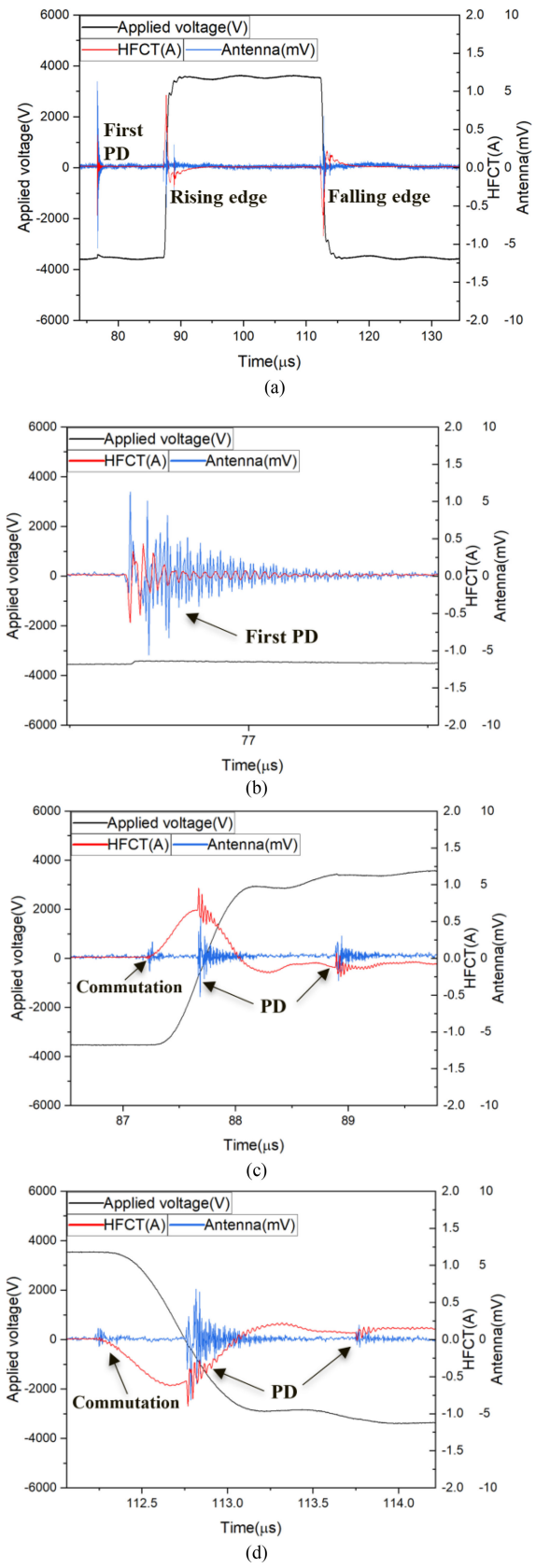

Fig. 8. Test waveforms under 20 kHz peak-to-peak 7 kV PWM pulses. (a) Global waveform. (b) First PD signal. (c) Rising edge. (d) Falling edge.

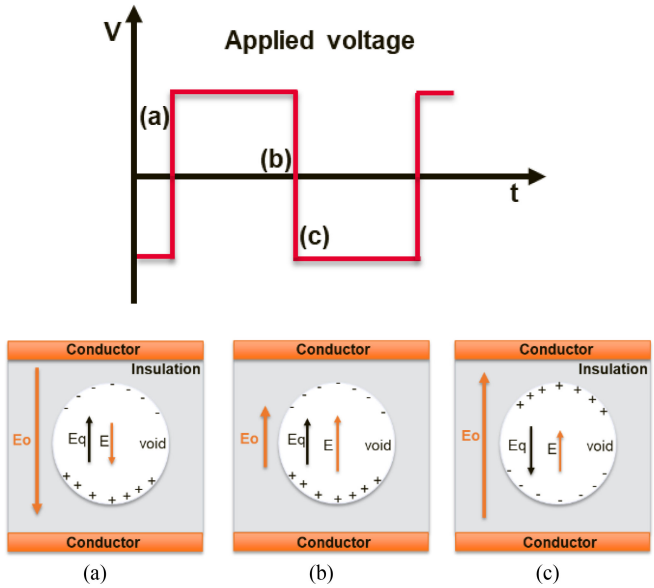

Fig. 9. Simplified model for PD occurrence. Square repetitive voltage waveform, simulating PWM voltage impulses and discharge during (a) Rising edge (positive voltage). (b) Falling edge (close to zero crossing). (c) Falling edge (negative voltage). E_q is the field caused by the space charge deposited by a discharge, E0 the geometric field and E the resulting field in the cavity.

frequency commutation noise will not appear in the antenna signals (see Fig. 8). The polarity of the first PD pulse indicates the polarity of the PD-induced charge. As the first PD event happens at peak negative voltage, the polarity of the first pulse detected from the HFCT is negative. When PD occurs at the rising edge, the first pulse in the PD event is positive indicating positive PD charge; when PD happens at the falling edge, the first pulse is negative indicating negative PD charge.

B. PD Mechanism Under PWM Voltage Stress

A gas-filled cavity/void within a solid dielectric insulation system, that can be created during manufacturing, installation, or aging, introduce an environment that can be conducive to PD in the insulation. A PD event is initiated when two basic conditions are met: a starting electron is available and the field inside the cavity is sufficiently high to generate an avalanche from the free electron [24]. This highlights the inherent stochastic nature of PD, which reflects into their variable amplitude and occurrence time.

Fig. 9 shows a simplified model which includes electrode, dielectric material, and spherical void. This representation is useful to provide insight into the occurrence of PD in an internal defect, as well as in an air gap between two insulated conductors. As noted in Fig. 8, the first PD occurs at the negative or positive peak voltage. The inception field for PDs in such a void (assumed the cavity is filled with air at ambient pressure) can be estimated, [25], as

$$E_{\text{inc}} = (E/p)_{cr} \left[1 + \frac{B}{(2pa)^n}\right]. \quad (1)$$

The parameters $(E/p)_{cr}$, B, and n characterize the ionization process in the gas. For air $(E/p)_{cr} = 25.2\ VPa^{-1}m^{-1}$ and $n = 0.5$, $B = 8.6\ m^{0.5}Pa^{0.5}$, p is gas pressure and a is the axis of an ellipsoid parallel to the background field E_o. The ellipsoidal representation is a more general form of a spherical representation.

When a PD occurs, a charge transfer happens at the cavity surface. Positive and negative charges will be deposited on void internal surfaces. The space charge deposited by an avalanche reduces the net field E in the void, allowing for the extinction of the PD event. The net field can be estimated as

$$E = f_E\, E_O - E_q \tag{2}$$

where E_o is the geometric field, E_q is the field induced by deposited charge, and f_E is the field enhancement factor depending on defect geometry and dielectric permittivity.

In the case of a PWM excitation, as in the simplification of Fig. 9, after a half switching cycle, the applied voltage starts decreasing and changing the polarity. However, the induced field E_q by the surface charge will remain longer (due to the longer relaxation time of surface charges [26], [27]), and it will enhance the electric field during the falling edge as shown in Fig. 9(b) [28]. Since such relaxation times are due to different factors than the temporal variation of the applied voltage, differences in the rate of change of the applied voltage and the time between PD events can produce differences in the size, shape, and initiation voltage of an individual PD event. In this case, it appears that the first PD affects the PD during the next edge (falling or rising), providing easy first electron availability and modifies the filed distribution in the void via deposited charge. Therefore, the first PD signal captured during next edge is close to a zero point in the applied voltage as shown in Fig. 8(c) and (d). The second PD signal is occurring at higher applied voltage (higher geometric field *Eo*), as shown in Fig. 9(c). Assuming PD occurs in a single cavity/air gap between two wires, then the total charge recorded due to the second PD event can be estimated [24], [29]

$$q = \varepsilon_{\text{void}}\, \pi r^2\, (1 + 2\varepsilon_r)\, \Delta E \tag{3}$$

where $\varepsilon_{\text{void}}$ is void permittivity, ε_r is the relative permittivity of the dielectric, r is the radius of the spherical void and ΔE is the field collapse in the void caused by the PD. This means that the larger the field drop, the higher the measured charge q.

IV. PD Phenomenology Under PWM Pulses

To reduce the randomness caused by external factors (e.g., temperature, relative humidity, surface condition of the specimen under test), each group of tests was completed within a sufficiently short-time that the test environment did not change appreciably [19]. Besides, since the PD apparent magnitude is related to the distance between the antenna and the DUT, for each group of tests, the relative positions of the antenna and the DUT were kept constant. Consequently, the relative response of the two sensors remained consistent. To help assess measurement reliability, the data captured by HFCT and antenna with and without the high pass filter were recorded.

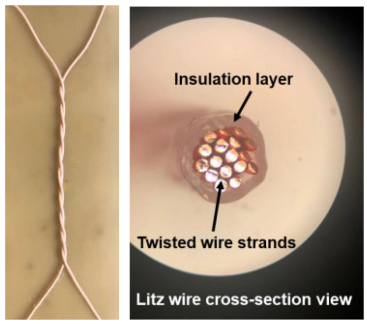

Fig. 10. Twisted Litz wire test sample and cross–section view.

PD sensors were verified to be PD-free over the full output voltage range by tests performed without connecting a DUT. Data from the voltage rising edge for ten pulses are presented in this article. PD measurements of each DUT were repeated at least ten times under each condition to obtain a statistical distribution. The time interval between each test was longer than 10 minutes to minimize the influence of residual space charge from the previous test [30]. To summarize results, PD magnitude values measured by the HFCT and the PD magnitude by the TEM antenna are plotted using boxplots. Each box summarizes a dataset by showing the median value (central line in the box), the 25th and 75th percentiles (the edges of the box), the data range (symbols outside the whiskers correspond to outlier). The connection line of the boxes corresponds to the mean value [31].

PWM voltage magnitude, *dV/dt* and PWM frequency are the factors that were investigated in relation to the PD phenomenology. The values of these parameters are selected based on the insulation capability and working conditions of DUT. To achieve an effective comparison, all other test parameters were kept the same when one of them was changed.

A. Devices Under Test

Litz wire is used in HFTs to reduce the skin effect and proximity effect in higher power HFT applications. PCB winding is widely used in lower power planar HFT design because it has excellent repeatability and consistent parameters. Fig. 10 shows the twisted Litz wire DUT and its cross-section. The structure of the Litz wire includes the twisted wire strands in the middle and an outer insulation layer. The conductor is made from copper and the insulation layer is nylon thread. Fig. 11 shows the 6-layer copper primary PCB winding and 12-layer copper secondary winding. The insulating material between the windings is a 0.01-mm thick lacquer-like layer of polymer. Fig. 12 shows the rising and falling voltage-impulse-waveform edges at peak-to-peak 2 kV voltage. To differentiate PD from disturbance signals, high pass filters were used. PD signals are composed of higher frequency components than is the commutation noise, so that most of the disturbance is filtered by the 50 MHz center-frequency and 150 MHz center-frequency high-pass filters (CHPFL-0050-BNC and CHPFL-0150-BNC, respectively). In this acquisition, both the HFCT and the antenna capture four PD signals with different magnitudes during the rising edge. The second PD signal has the largest magnitude

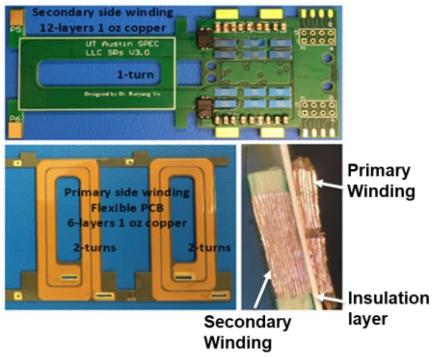

Fig. 11. Direct parallel PCB windings and cross–section view.

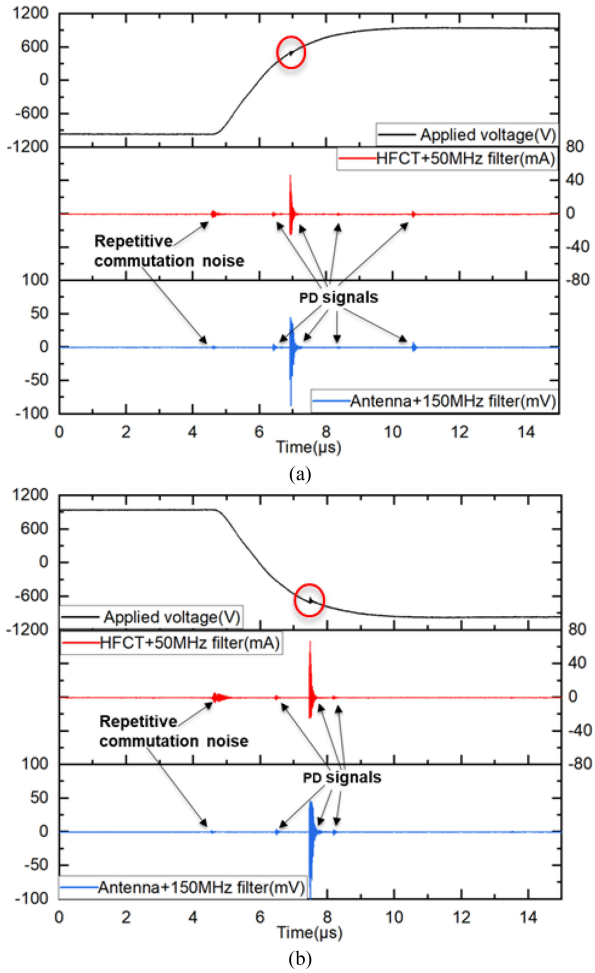

Fig. 12. Typical test waveforms under high-frequency PWM pulses. (a) Rising edge. (b) Falling edge. PD pulses are indicated, together with switching noise. The largest PD pulse induces a glitch in the voltage impulse.

which also induces a small spike in the voltage waveform. During the falling edge, there are three PD signals.

B. PD Behavior With Different PWM Voltage Values

For the Litz wire winding, the peak-to-peak applied voltage was increased from 1560 to 1680 V with the same frequency (10 kHz) and *dV/dt* (5.5 kV/μs). These values were chosen

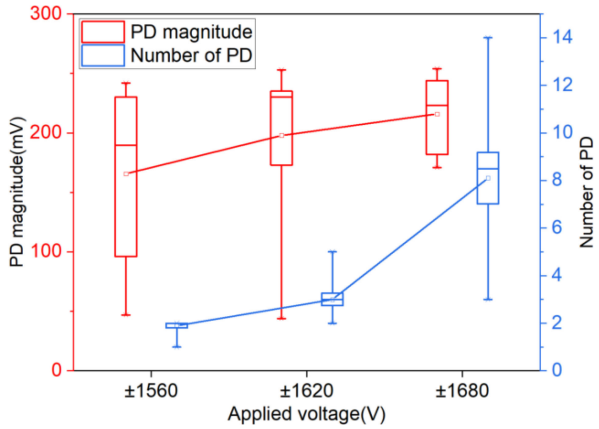

Fig. 13. Effects of applied voltage amplitude on PD magnitude and number of PD (Litz wire winding sample, f = 10 kHz, $dv/dt = 5.5$ kV/μs).

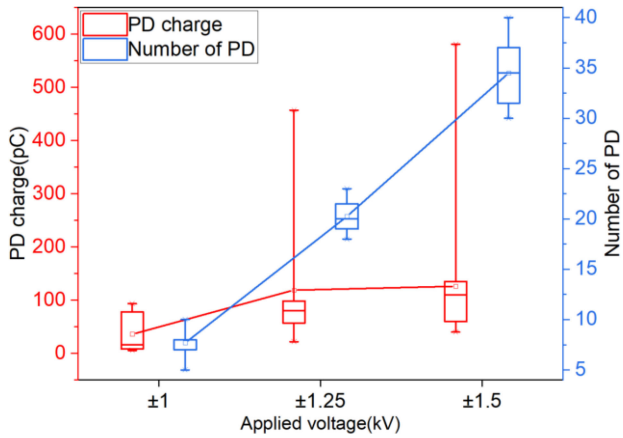

Fig. 14. Effects of applied voltage amplitude on PD charge and number of PD (PCB winding sample, $f = 10$ kHz and $dv/dt = 2.7$ kV/μs).

to explore the behavior near PD onset. As regards the PWM voltage, it needs to be higher than PDIV to initiate PD. But, the applied voltage cannot be too high otherwise it will trigger excessive PD or even a large leakage current. According to the test results, 1 to 1.5 kV are acceptable for PCB winding sample and 1560 to 1680 V are acceptable for Litz wire sample.

For the PWM frequencies, the frequency range of the PD tester is 5–100 kHz which is set by the limitation of the tester and capacitance of the DUT. Frequencies of 10, 20, and 50 kHz are the typical working frequencies for HFT design, and the range is wide enough for PD behavior characterization. The value of *dV/dt* is determined by the capacitance of DUT and the damping resistance. The *dV/dt* used in this research correspond to 5, 10, or 15 kΩ values of the damping resistance.

Fig. 13 shows that both the PD magnitude and number of PDs increase with increasing PWM peak voltage. For PCB winding, the peak-to-peak PWM voltage was increased from 1 to 1.5 kV at 10 kHz and a $dV/dt = 2.7$ kV/μs. The trend is the same as with the Litz wire, i.e., PD charge and number of PDs increase with PWM voltage value, as shown in Fig. 14.

The number of PD increases with rising PWM voltage because both additional PD may occur in same void [26] and/or more

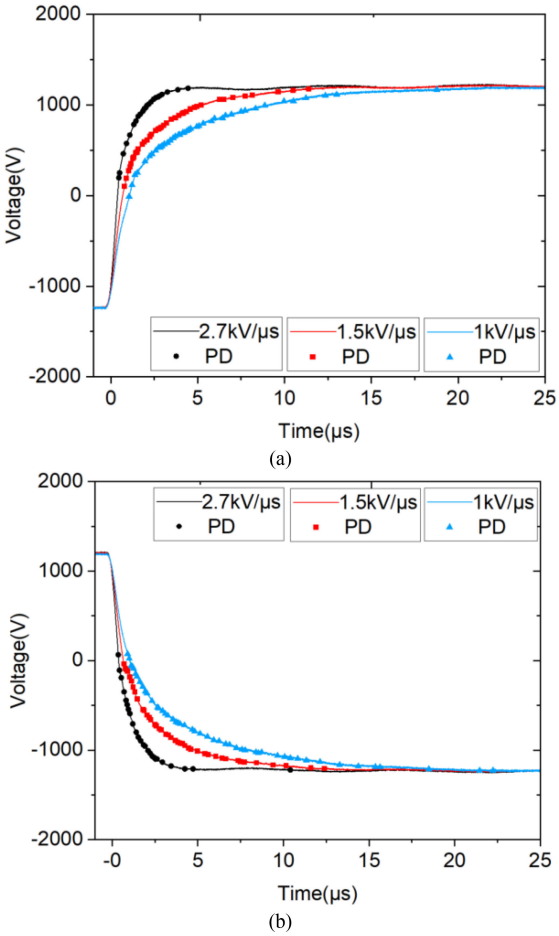

Fig. 15. PD-occurrence distribution with different *dV/dt* detected by HFCT and antenna (PCB winding sample, $f = 10$ kHz, and $v = \pm 1.25$ kV). (a) Rising edge. (b) Falling edge.

cavities are involved when voltage grows. The inception voltage of each cavity is, indeed, different due to varying geometries, so that more cavities meet the critical field emission threshold the larger the applied voltage [23], [24].

C. *PD Behavior With Different* DV/DT

Fig. 15 illustrates the effect on PD arising from varying *dV/dt* at the rising and falling edges of a PWM waveform. The PWM frequency is 10 kHz, and the voltage is 2.5 kV peak-to-peak. The PD-occurrence distribution moves closer to the switching time, and it becomes more concentrated in time as the *dV/dt* increases. This characterization can be explained by the model in Fig. 10, the principle is same for both rising and falling edge. When a PD occurs, a charge is deposited at the cavity surface. Positive and negative space charges can be resident on the void internal surfaces due to the discharge producing carriers of opposite polarity. After a half switching cycle, the applied voltage decreases, changing the polarity of the geometric electric field with different times for different values of *dV/dt*. However, the internal field(1) resulting from the surface charge, has a longer time constant for change.

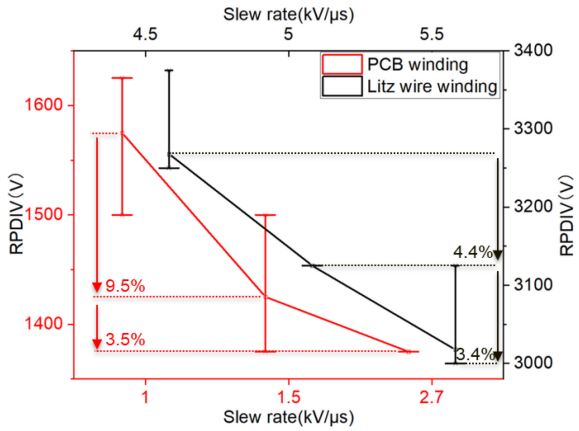

Fig. 16. RPDIV of test samples under different slew rates at rise/fall edge (Litz wire winding sample and $f = 10$ kHz).

For higher *dV/dt*, the net field E will reach the PD-occurrence threshold in shorter time. So, the PD-occurrence distribution would be expected to become more concentrated in time as the *dV/dt* increases as shown in Fig. 13.

The repetitive PD inception voltage (RPDIV) is defined as the minimum peak-to-peak impulse voltage at which more than five PD pulses occur during ten voltages impulses of the same polarity [27], [32]. Fig. 16 plots the RPDIV measurement results under different slew rates. The connecting line is the mean value of ten RPDIV results of each test condition. The percentage of mean value variation for each test condition are included. As can be seen, the RPDIV decreases with increasing *dV/dt*. This has been explained by a recombination/depletion time constant associated with surface charge (the electric field memory effect [30]). The defect-type represented by the twisted pair test object is different from a typical internal void since the defective volume in twisted pairs is not surrounded by the dielectric. Nevertheless, the defect in twisted pairs is an air gap between two conductors covered by dielectric, with air gap height not too dissimilar from real internal defects. The major difference is that a twisted pairs can be source of PD from sites spanning the Litz wire surface, and even simultaneous PD active sources, which is less common in embedded cavities.

Once PD occurs in the air gap between Litz wires, the induced charge decay mechanism is similar to that postulated for internal voids, including recombination at trapping charge sites and surface charge leakage, the latter most likely predominating on the former (while the opposite might occur in embedded cavities).

This difference could have some impact on memory effect of the PD-induced charge, which would influence a phase resolved PD pattern diagram. However, as regards the underlying physics and the PD mechanism, both test objects should exhibit similar behavior. Indeed, as *dV/dt* increases there is less time for surface charge decay, which makes the RPDIV lower.

D. *PD Behaviors With PWM Frequencies*

Fig. 17 reports the RPDIV values of both test objects at different modulation frequencies (10, 20, and 50 kHz) with the

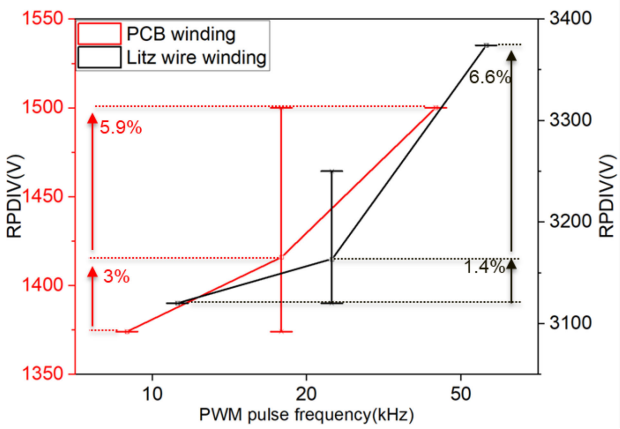

Fig. 17. RPDIV of tested objects under different frequency (litz wire winding sample, *dv/dt* = 5 kV/us, PCB winding, and *dv/dt* = 2.7 kV/us).

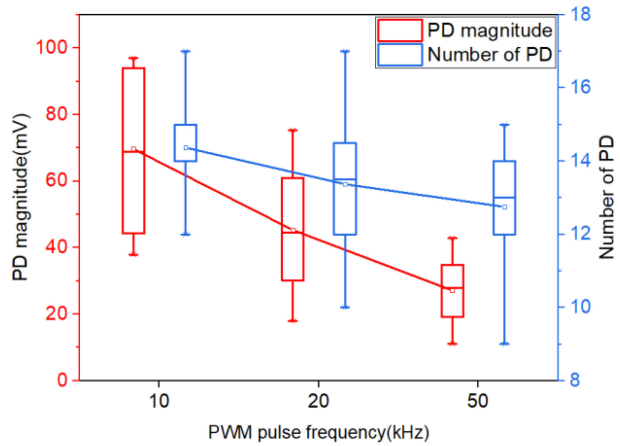

Fig. 18. Effect of applied voltage frequency on PD magnitude and number (PCB winding sample, *v* = 1.25 kV, and *dv/dt* = 2.7 kV/us).

same slew rate. Both the Litz wire and PCB winding show that the RPDIV increases slightly with increasing pulse repetition rates under these conditions. Figs. 18 and 19 summarize the effects of the PWM frequency on PD magnitude and number, for the PCB and Litz wire samples, respectively. With increased PWM frequency, the PD magnitude reduces as does the number of PDs (slightly).

An explanation for the above behavior is the frequency dependence permittivity of the insulation material. Under ac excitation, the geometric electric field is primarily determined by the relative permittivity ratio of the dielectric and gas in the void. The electrical field in gas-filled voids and cavities embedded in a solid dielectric is enhanced compared to the external field. The field in a spherical void embedded in a homogenous field has, indeed, field enhancement factor f_E, given by [33]

$$f_E = \frac{\varepsilon_r(f)}{1 + 2\varepsilon_r(f)}. \tag{4}$$

Then, the equation (2) can be rewritten as

$$E = \frac{\varepsilon_r(f) E_O}{1 + 2\varepsilon_r(f)} - E_q. \tag{5}$$

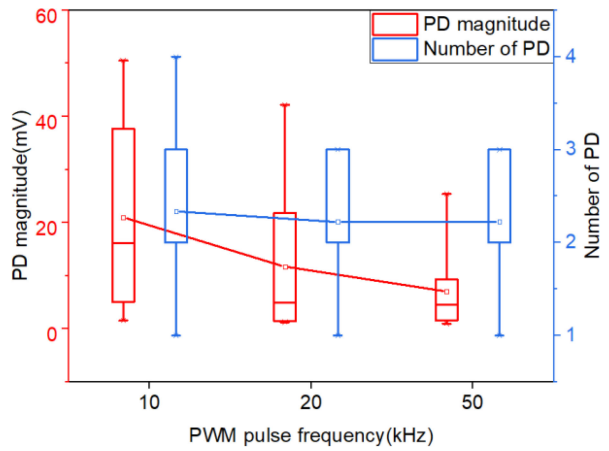

Fig. 19. Effects of applied voltage frequency on PD magnitude and number (Litz wire winding sample, *v* = 1.625 kV and *dv/dt* = 5.5 kV/us).

According to the dielectric constant curve as a function of the frequency for insulation materials used in the DUT samples, the dielectric constant decreases with the increase of frequency [34], [35]. Considering the threshold electric field is constant for a specific void, this frequency dependance of the dielectric constant requires higher applied voltage to meet the PD-occurrence criterion. Considering the defect geometry of the twisted pair has some level of uncertainty, two possible geometries could be assumed. One is the spherical geometry; the other could be parallel capacitor geometry. If we use parallel capacitor model to perform analysis, the voltage drops and E-field on the defect can be directly estimated using the relative permittivity of the dielectric material and the thickness of the insulation layers and the air gap. It would provide a slightly different value as compared with spherical defect.

Another factor that can contribute to or, in some cases, dominate, the reduction of charge magnitude and number is the memory effect [24]. The space charge decay time constant for the gas in the void is associated with charge drift and/or recombination rate. The range of charge decay times reported in [29] is 2–1000 ms. Considering the applied PWM range is 10–50 kHz, the charge decay time can be much longer than voltage impulse duration, and the availability of the first electron could be related approximately to the same value of geometric field (voltage).

V. Conclusion

This article developed and demonstrated a PWM power source to investigate the PD behavior of insulation material under high-frequency PWM pulses. RPDIV, number of PD, PD charge, and PD magnitude are determined to illustrate the PD behavior under different test conditions. The test results are discussed and analyzed to promote the understanding of PD mechanisms under high-frequency PWM voltage stress condition.

According to the test results, in addition to the PWM voltage amplitude, the *dV/dt* and PWM frequency exert considerable effect on PD phenomenology. Faster *dV/dt* lowers the RPDIV and leads to higher PD charges, while the opposite occurs increasing frequency. The information is a contribution both to

the design of reliable insulation systems which must withstand under repetitive voltage impulses with fast rise time and high carrier frequency and to the development of new standards for insulation testing in the new electrical environment enabled by wide band gap semiconductors.

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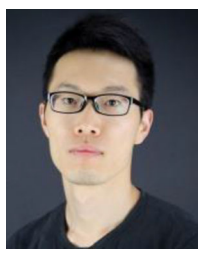


Zhicheng Guo (Student Member, IEEE) was born in Suzhou, China. He received the B.Sc. degree from Southeast University, Nanjing, China in 2013, and the M.S. degree from the National Tsing Hua University, Hsinchu, Taiwan, in 2016, both in electrical and computer engineering department of UT Austin. He is currently working toward the Ph.D. degree with the Semiconductor Power Electronics Center, the University of Texas at Austin, Austin, TX, USA.

His research interests include the high-voltage high-power magnetic design, power module packaging.

Alex Q. Huang (Fellow, IEEE) was born in Zunyi, Guizhou, China. He received the B.Sc. degree from Zhejiang University, Hangzhou, China in 1983 and the M.Sc. degree from Chengdu Institute of Radio Engineering, Chengdu, China in 1986, both in electrical engineering, and the Ph.D. degree from Cambridge University, Cambridge, U.K., in 1992.

From 1992 to 1994, he was a Research Fellow with Magdalene College, Cambridge, U.K. From 1994 to 2004, he was a Professor with the Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. From 2004 to 2017, he was the Progress Energy Distinguished Professor of Electrical and Computer Engineering, NC State University where he established and led the NSF FREEDM Systems Center. Since 2017, he has been the Dula D. Cockrell Centennial Chair in engineering with the University of Texas at Austin. Since 1983, he has been involved in the development of modern power semiconductor devices and power integrated circuits. He fabricated the first IGBT power device in China in 1985. He is the inventor and key developer of the emitter turn-off thyristor. He developed the concept of Energy Internet and the smart transformer based Energy Router technology. He has mentored and graduated more than 80 Ph.D. and master students, and has authored or coauthored more than 500 papers in international conferences and journals. He has also been granted more than 20 U.S. patents. His current research interests are power electronics, power management microsystems and power semiconductor devices.

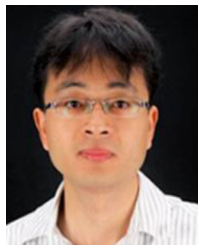
Dr. Huang is the recipient of the NSF CAREER award, the prestigious R&D 100 Award, the MIT Technology Review's 2011 Technology of the Year Award and the 2019 IEEE IAS Gerald Kliman Innovator Award. He is a fellow of National Academy of Inventors and IEEE.

Robert E. Hebner (Fellow, IEEE) received the B.S. degree in physics from Saint Mary's University, San Antonio, TX, USA, in 1967 and the M.S. and Ph.D. degrees in physics from the University of Missouri, Rolla, MO, USA, in 1969 and 1971, respectively.

He is the Director of the Center for Electromechanics, the University of Texas at Austin, TX, USA. The Center develops technology, primarily for novel motors, generators, and suspension components, and teams with companies to get the technology into the market.

Gian Carlo Montanari (Fellow, IEEE) is currently associated to the Center for Advanced Power Systems, Florida State University at Tallahasse, FL, USA. He has been a Full Professor of electrical technology with the Department of Electrical, Electronic and Information Engineering, University of Bologna, Bologna, Italy, teaching courses on Technology, Reliability and Asset Management. He has been working since 1979 in the field of aging and endurance of insulating materials and systems, diagnostics of electrical systems, asset management and innovative electrical materials (magnetics, electrets, superconductors, nanomaterials). He is author or co-author of about 800 scientific papers. He has been engaged also in the fields of power quality and energy market, power electronics, reliability and statistics of electrical systems, and smart grid.

Dr. Montanari has been recognized with several awards, including the IEEE Ziu-Yeda, Thomas W. Dakin, Whitehead, Eric Forster and IEC 1906 awards. He was founder and President of the spinoff Techimp, established in 1999.



Xianyong Feng (Member, IEEE) received the Ph.D. degree in electric power engineering from the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX, USA, in May 2012.

He is currently with the Center for Electromechanics, the University of Texas at Austin, TX, USA. Previously, he was with ABB, Raleigh, NC, USA, and ExxonMobil, Houston, TX, USA. His research interests include microgrids, shipboard power systems, and dc power system protection.