Carrier Selection Strategy of Generalized Discontinuous PWM Method for Current Reduction in DC-Link Capacitors of VSI

Junhyuk Lee, *Student Member, IEEE*, Myeong-Won Kim, *Student Member, IEEE*, and Jung-Wook Park, *Senior Member, IEEE*

***Abstract*—This article proposes a new carrier selection strategy of generalized discontinuous pulsewidth modulation (GDPWM) method for the two-level three-phase voltage source inverter to reduce the dc-link capacitor current under all operating conditions while keeping the minimum switching losses. First, the root-mean-square value of dc-link capacitor current is effectively reduced by selectively using both single and double carrier signals and modifying the switching patterns of existing GDPWM method. Although the proposed carrier selection strategy depends on the power factor (PF), the PF calculation is avoided because the multicarrier signals are properly chosen based on the information of three-phase modulation signals and measured three-phase currents. Also, the switching losses can be kept to a minimum as the modulation signals of conventional GDPWM method, which are optimal in terms of the switching losses, remain the same and the proposed carrier selection strategy has little effect on the total number of switching events. The operating principle of proposed GDPWM method is theoretically analyzed. Then, its practical effectiveness is verified by experimental tests on a motor drive system.**

***Index Terms*—Carrier selection strategy, dc-link capacitor, pulsewidth modulation (PWM), switching loss, two-level three-phase voltage source inverter (VSI).**

I. Introduction

THE two-level three-phase voltage source inverter (VSI) has been increasingly utilized in motor drive applications such as electric vehicles (EVs) and home appliances [1]–[5]. In general, the switching devices of VSI have been controlled by pulsewidth modulation (PWM) techniques due to their simplicity and effectiveness [6]. Although there are numerous PWM methods, it is important to choose a proper one because their unique switching patterns directly affect the input and output characteristics of VSI such as phase current quality, voltage linearity, switching losses, dc-link capacitor current, dc-link voltage ripple, and common-mode voltage (CMV) [7]–[10]. Among various PWM methods, the most widely utilized one has been the symmetrical space vector PWM (SVPWM) method [11], [12] due to its superior power quality. Many discontinuous PWM (DPWM) and generalized DPWM (GDPWM) methods [12]–[15] also have been investigated to reduce the switching losses as increasing efficiency has been a significant issue in the modern VSI [16]. In particular, it has been reported in [15] that the direct digital technique GDPWM (DDT-GDPWM) method generates the minimum switching losses under all operating conditions of VSI.

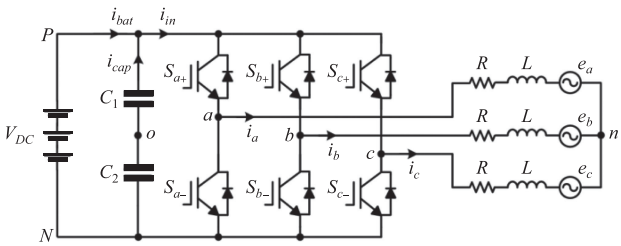

Fig. 1. Typical topology of battery-powered two-level three-phase VSI.

Another recent issue of the modern VSI is to reduce the dc-link capacitor current. As shown in Fig. 1, the typical battery-powered VSI system essentially requires the dc-link capacitors between the batteries and switching devices to provide a low impedance passage, through which the large harmonic current caused by the high-frequency switching events can flow [1], [17], [18]. Recently, the film capacitor has been primarily used as the dc-link capacitors instead of the electrolytic capacitor owing to its superiority [1]–[3], [19]. However, although the film capacitor is the reliable passive component, it is also susceptible to ageing because the current flowing through it causes power losses and raises temperature in it [20]–[22]. In fact, its root-mean-square (rms) value can reach up to about 65% of the rms value of phase currents. Moreover, this high rms value of dc-link capacitor current may increase its size and cost [25]. Therefore, it is required to reduce the dc-link capacitor current for improving the life expectancy, power density, and economic feasibility of VSI.

It is widely known that the instantaneous value of dc-link capacitor current is determined by the switching states of VSI.

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TABLE I
COMPARISON OF VARIOUS SCALAR DPWM METHODS DEVELOPED FOR DC-LINK CAPACITOR CURRENT REDUCTION

PWM method	Modulation signal	Carrier signal	Voltage linearity	DC-link capacitor current	Switching losses
TSPWM [23]	Same as DPWM1	Double	0–1.154	Low at very high PF High at low PF	Low
NSPWM [24]	Same as DPWM1	Double	0.770–1.154	Low at very high PF High at low PF	Low
DCPWM [25], [26]	Unique modulation signals (Table I in [25])	Double	0–1.154	Low at high PF High at low PF	Minimum at low MI Low at high MI
GTSPWM [27], [28]	Same as DDT-GDPWM [31]	Double	0–1.154	Low at high PF High at low PF	Minimum
MC-GDPWM	Same as DDT-GDPWM	Multi (Single and double)	0–1.154	Low in all ranges of PF	Minimum

To overcome the shortcoming of conventional PWM methods that produce relatively large fluctuation of the dc-link capacitor current, several PWM methods have been studied [23]–[29], which are divided into two types. The first type is the scalar DPWM methods using double carrier signals. In [23], the tristate PWM (TSPWM) method has been studied to reduce the CMV. The TSPWM method generates its switching pattern by using the modulation signals of DPWM1 method [12] and double carrier signals, which also brings about low dc-link capacitor current. However, its effect of reducing the dc-link capacitor current is valid only near unity power factor (PF), and it rather increases the dc-link capacitor current in the low PF range. Similarly, the near-state PWM (NSPWM) method defined only in the high modulation index (MI) range over 0.770 has been presented in [24] to reduce the CMV. In fact, the NSPWM method is the specific case of TSPWM method in the high MI range. In [25] and [26], the double carrier PWM (DCPWM) method has been proposed to reduce the dc-link capacitor current. The DCPWM method utilizes the unique discontinuous modulation signals decided by its own logical test (as explained in Table I of [25]) and double carrier signals as its nomenclature suggests. The DCPWM method can reduce the dc-link capacitor current more than the TSPWM method in a wider PF range. In [27] and [28], the generalized TSPWM (GTSPWM) method, which employs the modulation signals of DDT-GDPWM method and double carrier signals, has been introduced to reduce the CMV. Similar to the scalar DPWM methods described above, not only the CMV but the dc-link capacitor current is also reduced by the GTSPWM method. The GTSPWM method is identical to the DCPWM method when the MI is less than 0.667, otherwise it has smaller dc-link capacitor current than the DCPWM method in a wider PF range. However, the GTSPWM method also fails to reduce the dc-link capacitor current in all ranges of PF. The second type is the space-vector-based PWM methods using the voltage vector combinations that form obtuse triangles (originally, the scalar DPWM methods described above also have been devised based on the space vector approach. However, their scalar implementation has been presented together). In [29], the modified SVPWM method, which optimizes the voltage vector combinations for the reduced fluctuation of inverter input current in all ranges of PF, has been presented. Nevertheless, this PWM method results in more switching losses in the PF range below 0.866 than the DPWM methods because it partially adopts the existing symmetrical SVPWM method. In addition, the space vector approach is not preferred over the scalar approach from the implementation perspective because the computation effort required by the space vector theory is more burdensome [30].

On the basis of generalized scalar approach, which provides degrees of freedom in the choice of both zero-sequence and carrier signals [30], this article proposes a new carrier selection strategy for the DDT-GDPWM method to reduce the dc-link capacitor current under all operating conditions of VSI while maintaining the minimum switching losses [31]. The main difference between the previously studied scalar DPWM and proposed DPWM methods is how to utilize the carrier signals. The previously studied scalar DPWM methods employ only the double carrier signals, which lead to the dc-link capacitor current reduction only in the high PF range. On the other hand, the proposed DPWM method selectively uses the single and double carrier signals to adapt the switching pattern of DDT-GDPWM method, which makes the dc-link capacitor current reduction possible in all ranges of PF. Therefore, the proposed DPWM method is referred to as the multicarrier GDPWM (MC-GDPWM) method in below. Also, the DDT-GDPWM method is referred to as the single-carrier GDPWM (SC-GDPWM) method in below for the intuitive comparison with the proposed MC-GDPWM method. The proposed carrier signal selection strategy depends on the PF. However, the PF calculation is unnecessary because the carrier signals are appropriately chosen based on the information of three-phase modulation signals and measured three-phase currents. The switching losses caused by the proposed MC-GDPWM method are also kept to a minimum because the modulation signals of SC-GDPWM method remain the same, and the proposed carrier selection strategy has little effect on the total number of switching events. The featured characteristics between the scalar DPWM methods developed for the dc-link capacitor current reduction are summarized in Table I.

The remainder of this article is organized as follows. First, the principle of SC-GDPWM method is briefly reviewed in Section II. Second, the characteristics of dc-link capacitor current by the SC-GDPWM method are mathematically studied in Section III. Third, the detailed principle of proposed carrier selection strategy for the MC-GDPWM method is described in Section IV. Then, the performance of proposed MC-GDPWM method is theoretically analyzed in Section V. Thereafter, the practical effectiveness of proposed MC-GDPWM method is verified by experimental tests in Section VI. Finally, a conclusion is given in Section VII.

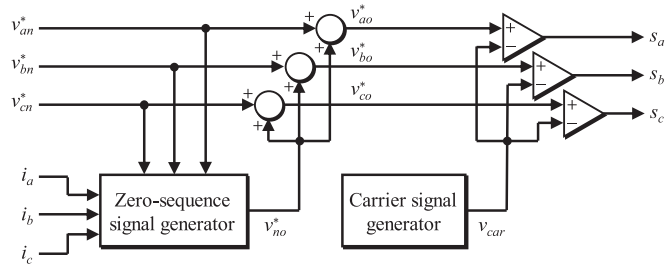

Fig. 2. Block diagram to implement the SC-GDPWM method.

II. Review of SC-GDPWM Method

In general, the scalar PWM method generates the binary switching functions, s_a, s_b, and s_c to control the six switching devices, $S_{a\pm}$, $S_{b\pm}$, and $S_{c\pm}$ by comparing the three-phase modulation signals with the single carrier signal, v_{car}. The high-frequency triangular signal, v_{tri} is usually used as v_{car}. In addition, it is widely known that the zero-sequence signal, v^*_{no} can be injected into the sinusoidal modulation signals, v^*_{an}, v^*_{bn}, and v^*_{cn} (which are the phase voltage references normalized to one-half of the dc-link voltage, V_{dc}) [30]. Accordingly, the nonsinusoidal modulation signals, v^*_{ao}, v^*_{bo}, and v^*_{co} (which are the pole voltage references normalized to $V_{\text{dc}}/2$) can be expressed as

$$\begin{cases} v^*_{ao} = v^*_{an} + v^*_{no} = m\cos(\theta) + v^*_{no} \\ v^*_{bo} = v^*_{bn} + v^*_{no} = m\cos(\theta - 2\pi/3) + v^*_{no} \\ v^*_{co} = v^*_{cn} + v^*_{no} = m\cos(\theta - 4\pi/3) + v^*_{no} \end{cases} \tag{1}$$

where m is the MI and θ is the phase angle.

The main idea of conventional SC-GDPWM method is to select the optimal v^*_{no} that minimizes the switching losses every carrier cycle by using the information of sinusoidal modulation signals and measured phase currents. The block diagram to implement the SC-GDPWM method is shown in Fig. 2. Generally, the zero-sequence signal generator of most PWM methods requires only the sinusoidal modulation signals as its input. However, as shown in Fig. 2, that of the SC-GDPWM method additionally needs the measured phase currents as its input. Assuming that the three-phase currents, i_a, i_b, and i_c at steady state are ideally sinusoidal in a balanced load, they can be expressed as

$$\begin{cases} i_a = I_A\cos(\theta - \varphi) \\ i_b = I_A\cos(\theta - 2\pi/3 - \varphi) \\ i_c = I_A\cos(\theta - 4\pi/3 - \varphi) \end{cases} \tag{2}$$

where I_A is the amplitude and φ is the PF angle.

Note that the modulation signals and measured phase currents are regarded as constants during a short carrier cycle, T_c [32]. Then, the algorithm used in the zero-sequence signal generator of SC-GDPWM method is as follows. The flowchart is also shown in Fig. 3 [15]. First, v^*_{an}, v^*_{bn}, and v^*_{cn} generated in every carrier cycle are arranged in descending order and denoted as v^*_{1n}, v^*_{2n}, and v^*_{3n}. For example, if $v^*_{an} > v^*_{bn} > v^*_{cn}$, it satisfies that $v^*_{1n} = v^*_{an}$, $v^*_{2n} = v^*_{bn}$, and $v^*_{3n} = v^*_{cn}$. Second, the measured phase currents corresponding to each v^*_{1n}, v^*_{2n}, and v^*_{3n} are defined as i_1, i_2, and i_3, respectively. Note here that the definitions of i_1, i_2, and i_3 are not related with the magnitude

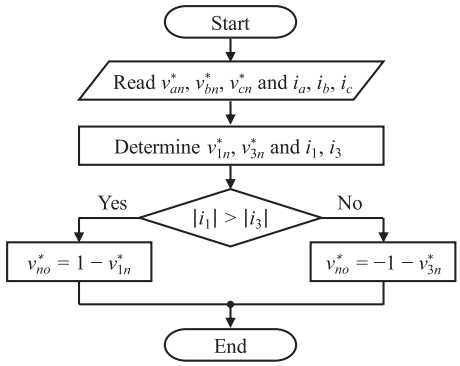

Fig. 3. Flowchart to select the zero-sequence signal of SC-GDPWM method.

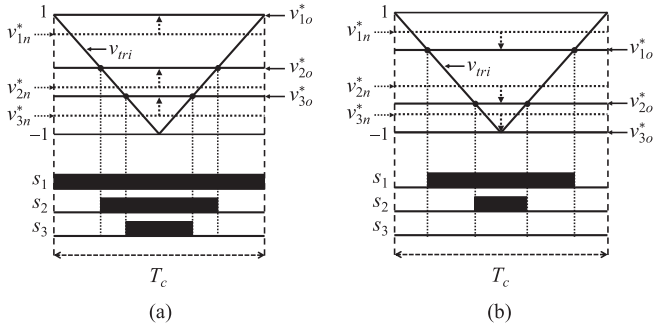

Fig. 4. Switching patterns obtained by the SC-GDPWM method. (a) $v^*_{no} = 1 - v^*_{1n}$. (b) $v^*_{no} = -1 - v^*_{3n}$.

of i_a, i_b, and i_c. For instance, if $v^*_{1n} = v^*_{an}$, $v^*_{2n} = v^*_{bn}$, and $v^*_{3n} = v^*_{cn}$, it simply satisfies that $i_1 = i_a$, $i_2 = i_b$, and $i_3 = i_c$. Last, v^*_{no} is chosen between $1 - v^*_{1n}$ and $-1 - v^*_{3n}$ depending on the absolute values of i_1 and i_3. Two possible switching patterns obtained by the SC-GDPWM method are described in Fig. 4, where v^*_{1o}, v^*_{2o}, and v^*_{3o} are the corresponding outcomes of zero-sequence signal injection, and s_1, s_2, and s_3 are the binary switching functions generated by v^*_{1o}, v^*_{2o}, and v^*_{3o}, respectively. In the first case shown in Fig. 4(a), $v^*_{no} = 1 - v^*_{1n}$ is used so that no switching event occurs at s_1. By doing this, the switching losses caused by i_1 are eliminated. In the second case shown in Fig. 4(b), on the other hand, the switching losses caused by i_3 are removed by using $v^*_{no} = -1 - v^*_{3n}$. Consequently, if $|i_1| > |i_3|$, the first case is chosen to minimize the switching losses because the switching losses are proportional to the absolute value of phase current at the switching event [33]. Otherwise, the second case is selected.

III. Analysis of DC-Link Capacitor Current

The instantaneous value of inverter input current, i_{in} is the sum of phase currents flowing through the upper switching devices, S_{a+}, S_{b+}, and S_{c+} (Fig. 1). Therefore, it can be obtained in terms of the phase currents and binary switching functions as

$$i_{\text{in}} = s_a i_a + s_b i_b + s_c i_c = s_1 i_1 + s_2 i_2 + s_3 i_3. \tag{3}$$

Two waveforms of i_{in} within a carrier cycle are shown in Fig. 5 when the SC-GDPWM method is applied. From Fig. 5,

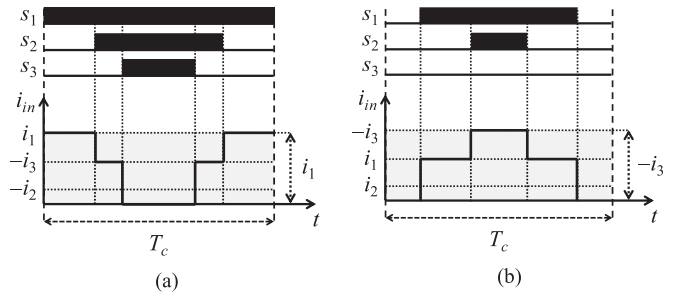

Fig. 5. Waveforms of inverter input current within one carrier cycle when the SC-GDPWM method is applied. (a) $v_{no}^* = 1 - v_{1n}^*$. (b) $v_{no}^* = -1 - v_{3n}^*$.

it is noted that the fluctuation of i_{in} is quite high as it frequently jumps between the values of phase currents and zero.

Assuming that the capacitance of dc-link capacitors is large, i_{in} can be divided into two components. The first one is the constant current, i_{bat}, flowing through the batteries. As the value of i_{bat} is equal to the per-carrier-cycle average of inverter input current, $i_{\text{in-ave}}$, it can be calculated as

$$i_{\text{bat}} = i_{\text{in-ave}} = \frac{1}{T_c}\int_0^{T_c} i_{\text{in}} dt \; i_{\text{bat}} = d_1 i_1 + d_2 i_2 + d_3 i_3$$
$$= \frac{3}{4} m I_A \cos(\varphi) \tag{4}$$

where d_1, d_2, and d_3 are the duty cycles of s_1, s_2, and s_3, respectively. It is observed from (4) that i_{bat} is the function of m, I_A, and φ (therefore, depending on the load conditions). The other component of i_{in} is the high-frequency harmonic current, i_{cap} flowing through the dc-link capacitors, which is referred to as the dc-link capacitor current. The instantaneous value of i_{cap} can be expressed by the Kirchhoff's current law as

$$i_{\text{cap}} = i_{\text{in}} - i_{\text{bat}} = i_{\text{in}} - i_{\text{in-ave}}. \tag{5}$$

According to (3)–(5), one can note that it is able to reduce the fluctuation of i_{cap} because i_{in} changes depending on the switching states of VSI. That is, if the switching patterns are properly modified, it is possible to make the peak-to-peak value of i_{cap} small. The MC-GDPWM method is proposed to adapt the switching patterns of SC-GDPWM method based on the proposed carrier selection strategy and minimize the fluctuation of i_{cap} under all operating conditions of VSI.

IV. Proposed Carrier Selection Strategy

It is shown in Fig. 5 that the waveforms of i_{in} by the SC-GDPWM method consist of i_1, $-i_3$, and 0. Also, its peak-to-peak value becomes either i_1 or $-i_3$ depending on v_{no}^*. However, this is satisfied only when the PF is high, and the waveform can vary with the PF because the state of phase currents can be changed depending on the PF. For example, the waveforms of v_{1o}^*, v_{2o}^*, v_{3o}^*, i_1, i_2, i_3, and resultant i_{in} in the range of $0° \le \theta \le 120°$ are illustrated in Fig. 6 when $\varphi = 15°$ and 60°, respectively ($m = 0.8$ and the waveforms are repeated every 120°). First, the waveform of i_{in}, shown in Fig. 6(a), corresponds well to Fig. 5 because i_1 and $-i_3$ are always positive. On the other hand, in the gray-colored areas of Fig. 6(b), the different patterns of i_{in} are

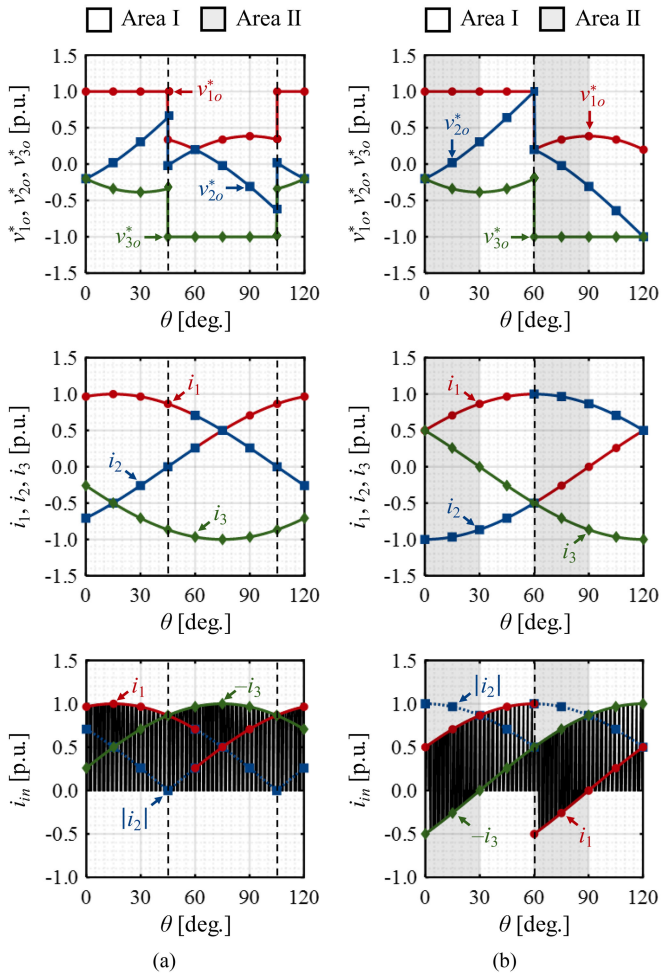

Fig. 6. Waveforms of v_{1o}^*, v_{2o}^*, v_{3o}^*, i_1, i_2, i_3, and resultant i_{in} when the SC-GDPWM method is applied at $m = 0.8$. (a) $\varphi = 15°$. (b) $\varphi = 60°$.

shown (the negative i_{in} is generated) and its peak-to-peak value becomes $|i_1 + i_3|$ as the polarities of i_1 and $-i_3$ are different.

As the waveform of i_{in} shows the different characteristics depending on the state of phase currents, it can be divided into two areas. The first one is the white-colored areas in Fig. 6, where i_1 and i_3 have the different polarity. It is defined as Area I. The second one defined as Area II is the gray-colored areas shown in Fig. 6(b), where the polarities of i_1 and i_3 are same. In Area I and II, another feature can be found in terms of i_2, which is the key factor in the proposed carrier selection strategy (details are explained behind). In Area I, $|i_2|$ is less than the larger of $|i_1|$ and $|i_3|$ (either $|i_1| > |i_2|$ or $|i_3| > |i_2|$ is satisfied). On the other hand, in Area II, it is not satisfied and $|i_2|$ is the maximum among the absolute values of three-phase currents (both $|i_2| \ge |i_1|$ and $|i_2| \ge |i_3|$ are satisfied).

The distribution chart of Areas I and II is shown in Fig. 7 according to θ and φ. As shown here, when $|\varphi| < 30°$, only Area I exists over the fundamental cycle. Area II begins to appear when $|\varphi| = 30°$ and expands as $|\varphi|$ increases from 30° to 90°. When $|\varphi| = 90°$, only Area II exists in the fundamental cycle. The proposed MC-GDPWM method takes the different carrier selection strategy in Areas I and II.

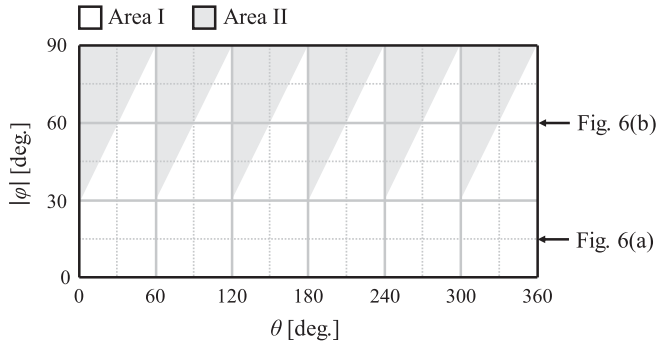

Fig. 7. Distribution chart of Areas I and II.

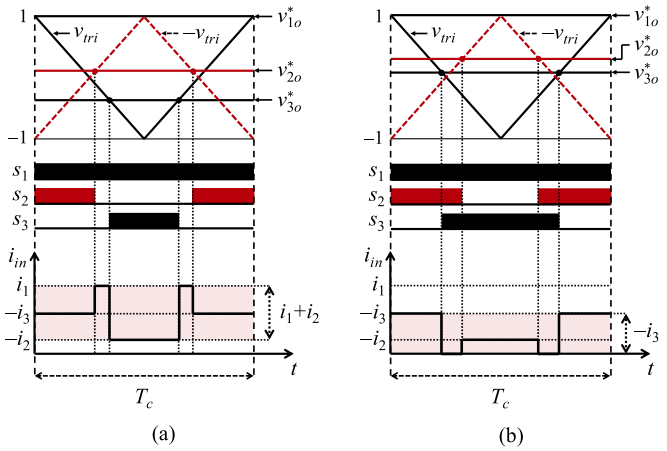

Fig. 8. Waveforms of inverter input current with the double carrier signals when $v^*_{no} = 1 - v^*_{1n}$ in Area I. (a) $d_2 + d_3 < 1$. (b) $d_2 + d_3 \geq 1$.

A. Carrier Selection Strategy in Area I

Supposing that $v^*_{no} = 1 - v^*_{1n}$ in Area I (the point where θ = 30° in Fig. 6(a) can be an example), the peak-to-peak value of i_{in} by the single carrier signal is i_1 as shown in Figs. 5(a) and 6(a). In contrast to this, two possible waveforms of i_{in} are shown in Fig. 8 when the double carrier signals are used ($-i_2$ is positive in this condition as shown in Fig. 6). Here, using the double carrier signals means that an additional carrier signal (red-dashed line) with the opposite sign to the original one (black solid line) is used, and only v^*_{2o} is compared with it. As the result, ON and OFF states of s_2 are reversed, while d_2 remains the same. Furthermore, the peak-to-peak value of i_{in} is reduced than that by the single carrier signal. However, the peak-to-peak values of i_{in} in the two cases of Fig. 8 are different from each other. In Fig. 8(a), the ON-state durations of s_2 and s_3 do not overlap ($d_2 + d_3 < 1$). In consequence, the switching state where only s_2 is 0 appears instead of the zero-voltage state (in which all switching functions simultaneously become 1) disappearing. Also, the lowest value of i_{in} increases from 0 to $-i_2$ (or $-i_3$ when it is lower than $-i_2$). On the contrary, the ON-state durations of s_2 and s_3 overlap ($d_2 + d_3 \geq 1$) in Fig. 8(b), and the highest value of i_{in} decreases from i_1 to $-i_3$ (or $-i_2$ when it is larger than $-i_3$). This is because the switching states in which only s_1 is 1 are missing and the switching state in which only s_2 is 0 occurs.

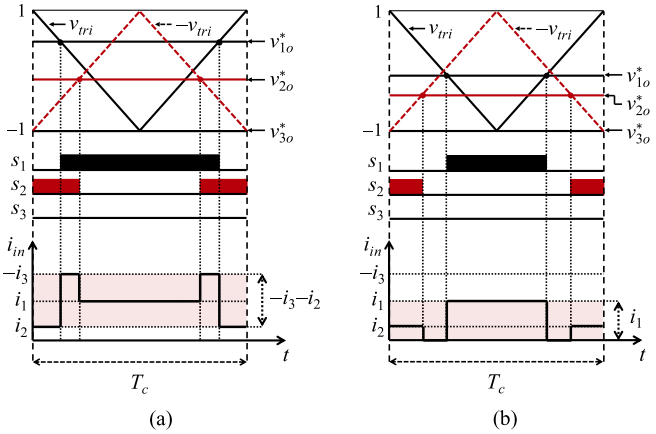

Fig. 9. Waveforms of inverter input current with the double carrier signals when $v^*_{no} = -1 - v^*_{3n}$ in Area I. (a) $d_1 + d_2 > 1$. (b) $d_1 + d_2 \leq 1$.

Two possible waveforms of i_{in} by the double carrier signals are additionally shown in Fig. 9 when $v^*_{no} = -1 - v^*_{3n}$ in Area I [the point where $\theta = 90°$ in Fig. 6(a) can be an example and i_2 is positive in this condition]. As shown here, the fluctuation of i_{in} by the double carrier signals is smaller than that by the single carrier signal according to the same principle described earlier.

Consequently, it is clearly confirmed in Area I that using the double carrier signals is more advantageous for reducing the peak-to-peak value of i_{in} than the single carrier signal, and this is because i_2 is used to form the waveform of i_{in} instead of zero or the highest peak.

It is also observed from Figs. 8 and 9 that the switching losses by the double carrier signals are theoretically same as those by the single carrier signal because the use of double carrier signals has little effect on the total number of switching events that occur during the fundamental cycle. When Area I is switched to Area II or vice versa, an additional switching event can occur (this is not problematic when $|\varphi| < 30°$). However, the number of these additional switching events is small when compared to the total number of switching events. The detailed calculation of switching loss function (SLF) by the SC-GDPWM method is given in [15], and the MC-GDPWM method has the same SLF in theory.

B. Carrier Selection Strategy in Area II

Using the double carrier signals is the typical carrier selection strategy that the NSPWM, TSPWM, DCPWM, and GTSPWM methods employ to reduce the problematic dc-link capacitor current. Nevertheless, this is not the solution to all operating conditions of VSI because the waveform of i_{in} is different in Area II from that in Area I. Supposing that $v^*_{no} = 1 - v^*_{1n}$ in Area II [the point where $\theta = 15°$ in Fig. 6(b) can be an example], the waveforms of i_{in} by the single and double carrier signals are described in Fig. 10. This time, unlike in Area I, the peak-to-peak value of i_{in} by the double carrier signals is greater than that by the single carrier signal. This is because $|i_2|$ is the maximum in Area II among the absolute values of phase currents, and it no longer guarantees the reduced fluctuation of i_{in}. It is the same

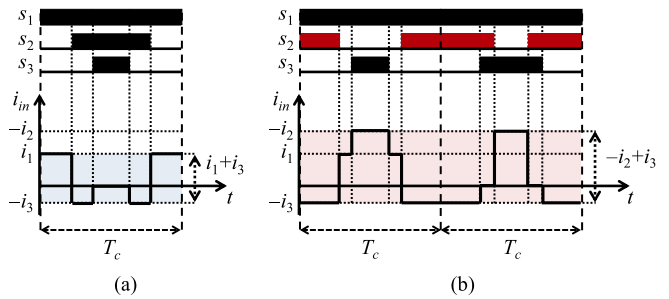

Fig. 10. Waveforms of inverter input current when $v_{no}^* = 1 - v_{1n}^*$ in Area II. (a) Case when the single carrier signal is used. (b) Case when the double carrier signals are used.

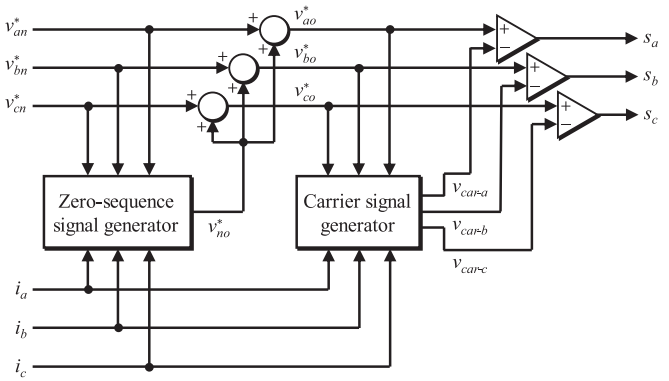

Fig. 11. Block diagram to implement the proposed MC-GDPWM method.

for the case when $v_{no}^* = -1 - v_{3n}^*$ in Area II. Thus, in Area II, using the single carrier signal is more useful for reducing the fluctuation of i_{in} than the double carrier signals.

C. Implementation of Proposed MC-GDPWM Method

The block diagram for the proposed MC-GDPWM method is shown in Fig. 11. When compared to that of conventional SC-GDPWM method shown in Fig. 2, the main difference is that the carrier signal generator individually offers the three separate multicarrier signals, $v_{\text{car}-a}$, $v_{\text{car}-b}$, and $v_{\text{car}-c}$ to the comparators of each phase. Also, the modulation signals and measured phase currents are provided as the input of carrier signal generator.

The flowcharts for the proposed carrier selection strategy of MC-GDPWM method are illustrated in Fig. 12, by which the carrier signal generator can produce the proper multicarrier signals. According to the criteria for distinguishing Area I and II, two types of flowcharts can be considered. The first one shown in Fig. 12(a) uses the product of i_1 and i_3 (which discerns whether the polarities of i_1 and i_3 are same or different), whereas the second one shown in Fig. 12(b) uses the relationship between the absolute values of three-phase currents. After Areas I and II are determined by one of those two flowcharts, the modulation signal to be compared with $-v_{\text{tri}}$ in Area I is chosen. As previously mentioned, only v_{2o}^* is compared with $-v_{\text{tri}}$ according to the proposed carrier selection strategy (Figs. 8 and 9). As an example, the waveforms of v_{ao}^*, v_{bo}^*, v_{co}^*, i_a, i_b, i_c, and resultant i_{in} in the range of $0° \le \theta \le 120°$ are described in Fig. 13 when the proposed MC-GDPWM method is applied at $\varphi = 15°$ and

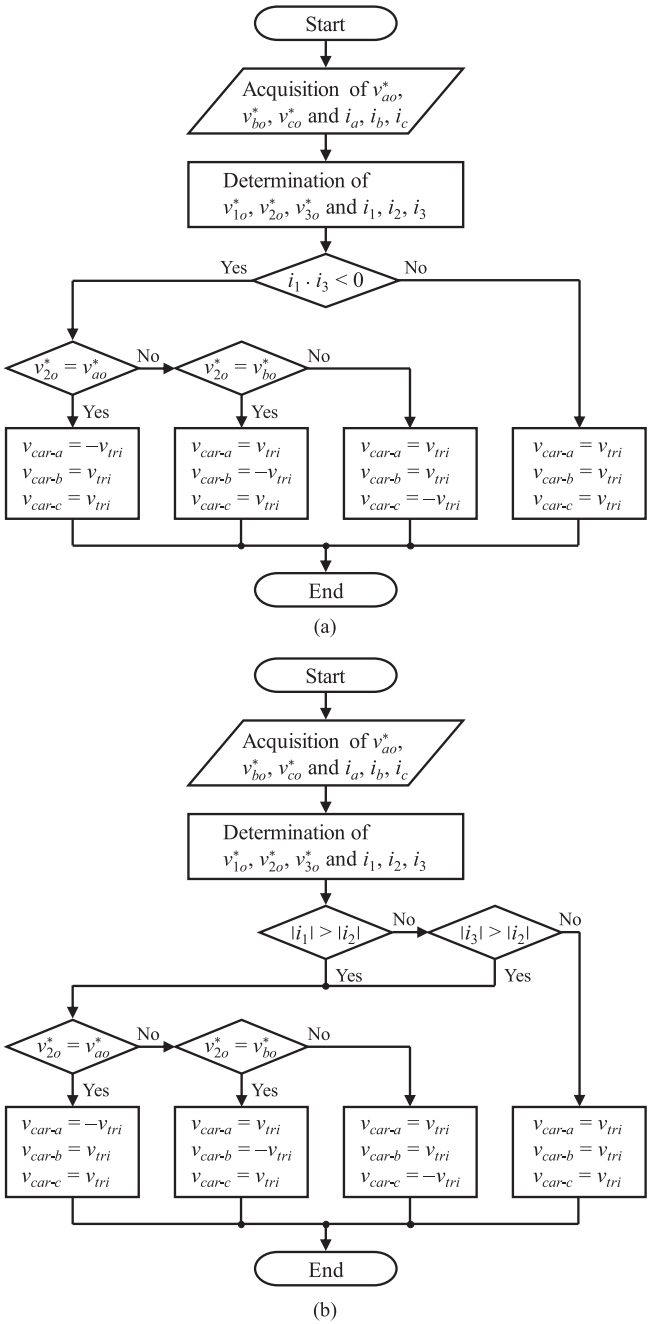

Fig. 12. Two types of flowcharts to select the multicarrier signals of proposed MC-GDPWM method. (a) First type using the product of i_1 and i_3. (b) Second type using the relationship between absolute values of phase currents.

60°, respectively ($m = 0.8$). Those waveforms can be divided into two parts. The first part is in the range of $0° < \theta < 60°$ where $v_{ao}^* > v_{bo}^* > v_{co}^*$ is satisfied ($v_{1o}^* = v_{ao}^*$, $v_{2o}^* = v_{bo}^*$, $v_{3o}^* = v_{co}^*$ and $i_1 = i_a$, $i_2 = i_b$, $i_3 = i_c$). Accordingly, $v_{\text{car}-a}$ and $v_{\text{car}-c}$ become v_{tri}, while $v_{\text{car}-b}$ becomes $-v_{\text{tri}}$ in Area I. Similarly, the second part is in the range of $60° < \theta < 120°$ where $v_{bo}^* > v_{ao}^* > v_{co}^*$ is satisfied ($v_{1o}^* = v_{bo}^*$, $v_{2o}^* = v_{ao}^*$, $v_{3o}^* = v_{co}^*$ and $i_1 = i_b$, $i_2 = i_a$, $i_3 = i_c$). Then, only $v_{\text{car}-a}$ becomes $-v_{\text{tri}}$ in Area I. As a result, it is clearly observed in Fig. 13 that the peak-to-peak value of i_{in} is minimized by the proposed MC-GDPWM method when compared to that shown in Fig. 6.

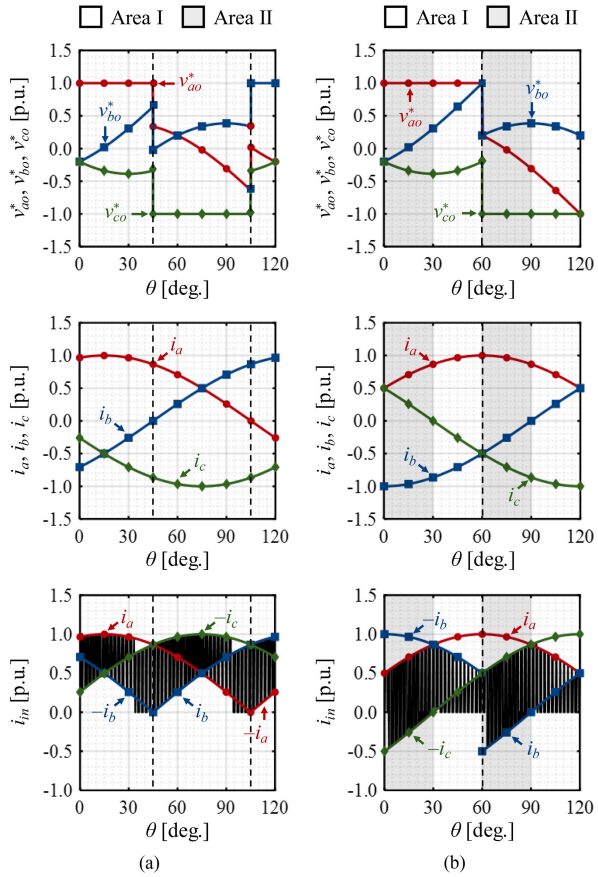

Fig. 13. Waveforms of v^*_{ao}, v^*_{bo}, v^*_{co}, i_a, i_b, i_c, and resultant i_{in} when the MC-GDPWM method is applied at $m = 0.8$. (a) $\varphi = 15°$. (b) $\varphi = 60°$.

V. Theoretical Analysis of Proposed PWM Method

A. RMS Value of DC-Link Capacitor Current

The rms calculation is commonly accepted as a criterion to quantify the dc-link capacitor current [17] because it does not contain the dc component and fluctuates around zero (its average is zero in theory). Besides, it is mathematically true that the larger the peak-to-peak value of dc-link capacitor current, the higher its rms value. Thus, reducing the peak-to-peak value and reducing the rms value are equivalent in terms of the dc-link capacitor current. To examine the dc-link capacitor current reduction effect by the proposed MC-GDPWM method, the per-carrier-cycle rms value of inverter input current, $i_{\text{in-rms}}$ and that of dc-link capacitor current, $i_{\text{cap-rms}}$ are first calculated as

$$i_{\text{in-rms}} = \sqrt{\frac{1}{T_c}\int_0^{T_c} i_{in}^2 dt} = \sqrt{\frac{1}{T_c}\int_0^{T_c} (s_1 i_1 + s_2 i_2 + s_3 i_3)^2\, dt} \quad (6)$$

$$i_{\text{cap-rms}} = \sqrt{\frac{1}{T_c}\int_0^{T_c} (i_{\text{in}} - i_{\text{in-ave}})^2\, dt} = \sqrt{i_{\text{in-rms}}^2 - i_{\text{in-ave}}^2}. \quad (7)$$

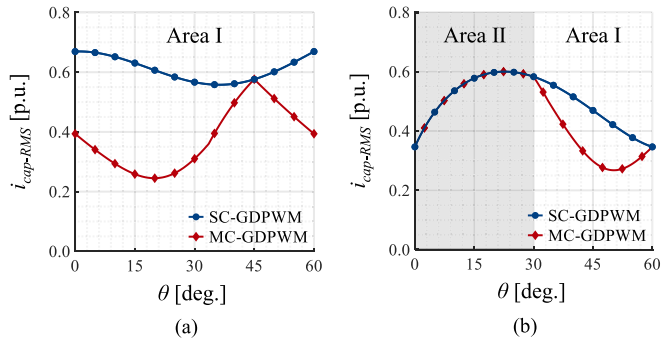

Fig. 14. Waveforms of per-carrier-cycle rms values of dc-link capacitor current at $m = 0.8$. (a) $\varphi = 15°$. (b) $\varphi = 60°$.

According to (6) and Fig. 5, when the single carrier signal is used, the value of $i_{\text{in-rms}}$ can be computed as

$$i_{\text{in-rms}} = \sqrt{i_1^2\,(d_1 - d_2) \;+\; i_3^2\,(d_2 - d_3)}. \quad (8)$$

The SC-GDPWM method always satisfies (8). In contrast, when the double carrier signals are used, it can be calculated for the four different conditions shown in Figs. 8 and 9 as

$$i_{\text{in-rms}} = \sqrt{i_1^2\,(1 - d_2 - d_3) \;+\; i_2^2 d_3 \;+\; i_3^2 d_2} \quad (\text{if } |i_1| > |i_3| \text{ and } d_2 + d_3 < 1) \quad (9)$$

$$i_{\text{in-rms}} = \sqrt{i_2^2\,(1 - d_2) \;+\; i_3^2\,(1 - d_3)} \quad (\text{if } |i_1| > |i_3| \text{ and } d_2 + d_3 \geq 1) \quad (10)$$

$$i_{\text{in-rms}} = \sqrt{i_1^2\,(1 - d_2) + i_2^2\,(1 - d_1) + i_3^2\,(d_1 + d_2 - 1)} \quad (\text{if } |i_3| > |i_1| \text{ and } d_1 + d_2 \geq 1) \quad (11)$$

$$i_{\text{in-rms}} = \sqrt{i_1^2 d_1 \;+\; i_2^2 d_2} \quad (\text{if } |i_3| \geq |i_1| \text{ and} \leq d_1 + d_2 \leq 1). \quad (12)$$

Using (4) and (7)–(12), the values of $i_{\text{cap-rms}}$ by the SC-GDPWM and MC-GDPWM methods are calculated when $m = 0.8$ and $\varphi = 15°$ and $60°$, and the results in the range of $0° \leq \theta \leq 60°$ are shown in Fig. 14 (they are repeated every 60°). The values are normalized to the rms value of phase current, $I_{A-\text{rms}}$. As the result, it is clearly observed that the proposed MC-GDPWM method produces smaller $i_{\text{cap-rms}}$ in Area I than the existing SC-GDPWM method, whereas they have the same $i_{\text{cap-rms}}$ in Area II.

The per-fundamental-cycle rms value of dc-link capacitor current, $I_{\text{cap-rms}}$ is also calculated as

$$I_{\text{cap-rms}} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} i_{\text{cap-rms}}^2\, d\theta} = \sqrt{I_{\text{in-rms}}^2 - I_{\text{in-ave}}^2} \quad (13)$$

where $I_{\text{in-rms}}$ and $I_{\text{in-ave}}$ are the per-fundamental-cycle rms value and average of inverter input current, respectively. Based on (13), the ratio of proposed MC-GDPWM method to the existing SC-GDPWM method for $I_{\text{cap-rms}}$ is obtained and shown in Fig. 15(a). It is clearly observed that the ratio is less than unity under all operating conditions of VSI, and the reduction effect is more prominent in the high PF range. The lowest ratio is 0.5664

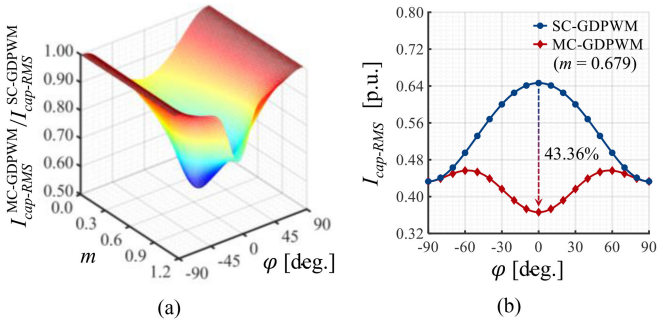

Fig. 15. Comparison of per-fundamental-cycle rms values of dc-link capacitor current. (a) Ratio of the MC-GDPWM method to the SC-GDPWM method. (b) Normalized rms values of dc-link capacitor current at $m = 0.679$.

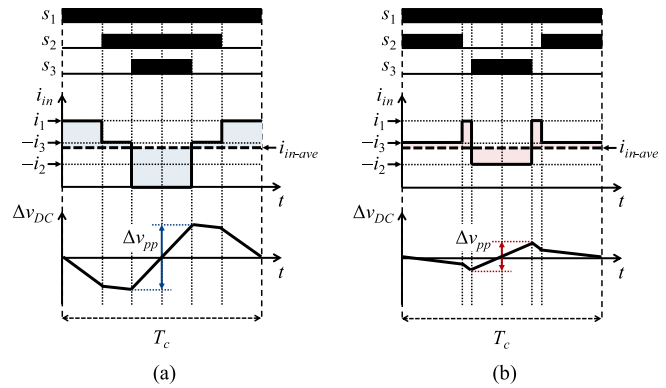

Fig. 17. Waveforms of normalized peak-to-peak dc-link voltage ripple at $m = 0.8$. (a) $\varphi = 15°$. (b) $\varphi = 60°$.

Fig. 16. Waveforms of dc-link voltage ripple within a carrier cycle. (a) Case when the single carrier signal is used. (b) Case when the double carrier signals are used.

at $m = 0.679$ and unity PF. The values of $I_{\mathrm{cap-rms}}$ at $m = 0.679$, which are normalized to $I_{A-\mathrm{rms}}$, are also shown in Fig. 15(b).

B. DC-Link Voltage Ripple

As the high-frequency fluctuating current flows through the dc-link capacitors, the voltage ripple is inevitably generated at the dc-link of VSI [34]. When Δv_{dc} is the dc-link voltage ripple within one carrier cycle, it can be obtained as

$$\Delta v_{\mathrm{dc}} = -\frac{1}{C_{\mathrm{dc}}}\int_0^{T_c} i_{\mathrm{cap}}dt = \frac{1}{C_{\mathrm{dc}}}\int_0^{T_c} i_{\mathrm{in-ave}} - i_{\mathrm{in}}\, dt \quad (14)$$

where C_{dc} is the total capacitance of dc-link capacitors.

By (14), it is known that the smaller fluctuation of i_{cap} results in the smaller fluctuation of Δv_{dc}. The waveforms of Δv_{dc} within one carrier cycle by the single and double carrier signals are described in Fig. 16 ($m = 0.8$, $\varphi = 15°$, and $\theta = 25°$). As expected, it is observed here that the peak-to-peak value of dc-link voltage ripple, Δv_{pp} becomes smaller if the double carrier signals are used when compared to the single carrier signal. In other words, the proposed MC-GDPWM method makes Δv_{pp} smaller than the conventional SC-GDPWM method in Area I.

The waveforms of Δv_{pp} by the SC-GDPWM and MC-GDPWM methods in the range of $0° \le \theta \le 60°$ are also shown in Fig. 17 when $m = 0.8$ and $\varphi = 15°$ and 60°. The value of Δv_{pp} is normalized to $I_A T_c / C_{\mathrm{dc}}$ [34]. It is observed that the proposed MC-GDPWM method has smaller Δv_{pp} in Area I than the conventional SC-GDPWM method, whereas they have the same Δv_{pp} in Area II.

C. Phase Current Quality

To evaluate the phase current quality by the proposed MC-GDPWM method, the conceptual harmonic flux vector is utilized [33]. Based on the space vector theory, the normalized harmonic flux vector, λ_{hn} within one carrier cycle can be calculated as the time integral of instantaneous voltage vector error as

$$\lambda_{\mathrm{hn}} = \frac{2}{V_{\mathrm{dc}} T_c}\int_0^t (V_k - V^*)\, d\tau (0 \le t \le T_c) \quad (15)$$

where V_k ($k = 0$–7) are the space voltage vector, and V^* is the voltage reference vector. Because the average of λ_{hn} is zero, it is also evaluated by calculating its per-fundamental-cycle rms value, $\lambda_{\mathrm{hn-rms}}$ as

$$\lambda_{\mathrm{hn-rms}} = k_f \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} \left(\frac{1}{T_c}\int_0^{T_c} {\lambda_{\mathrm{hn}}}^2 dt\right) d\theta} \quad (16)$$

where k_f is the carrier frequency coefficient [33]. The values of $\lambda_{\mathrm{hn-rms}}$ by the symmetrical SVPWM, SC-GDPWM, and MC-GDPWM methods are computed at $\varphi = 15°$ and 60° using (16) and shown in Fig. 18 (for intuitive comparison, the symmetrical SVPWM method, which is widely known to have the best harmonic performance, is involved). As a result, it is observed in Fig. 18(a) and (b) that the proposed MC-GDPWM method distorts the phase currents more than the conventional PWM methods under the same carrier frequency condition (the value of k_f for the SVPWM and both GDPWM methods is unity). This is because the use of double carrier signals causes larger voltage errors. On the other hand, under the same average switching frequency condition (the value of k_f for the SVPWM method is unity, and that for both GDPWM methods is $2/3$), the proposed MC-GDPWM method can provide relatively good quality of phase currents, particularly in the high MI range as shown Fig. 18(c) and (d).

The ratios of proposed MC-GDPWM method to the two existing PWM methods for $\lambda_{\mathrm{hn-rms}}$ are also shown in Fig. 19 under the same average switching frequency condition. It is

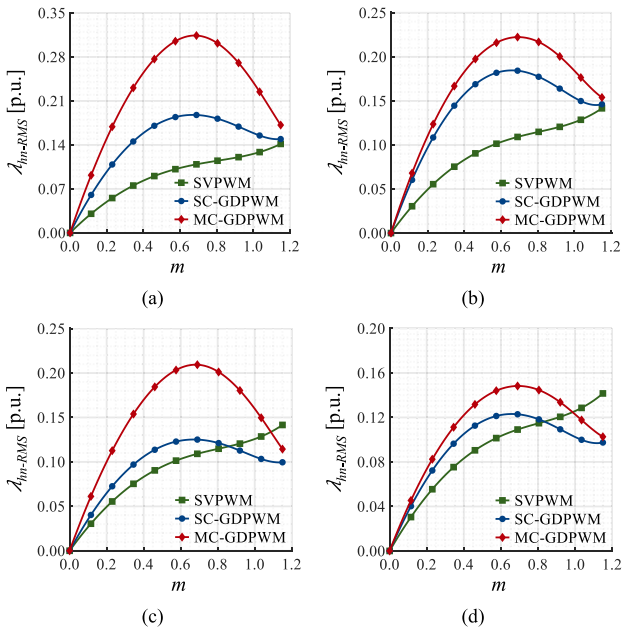

Fig. 18. Normalized per-fundamental-cycle rms values of harmonic flux vector. (a) $\varphi = 15°$ under the same carrier frequency condition. (b) $\varphi = 60°$ under the same carrier frequency condition. (c) $\varphi = 15°$ under the same average switching frequency condition. (d) $\varphi = 60°$ under the same average switching frequency condition.

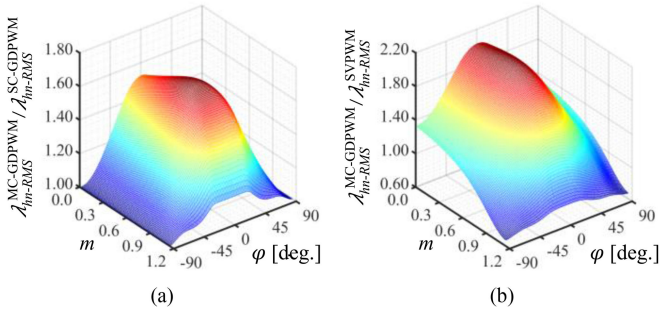

Fig. 19. Comparison of per-fundamental-cycle rms values of harmonic flux vector. (a) Ratio of the MC-GDPWM method to the SC-GDPWM method. (b) Ratio of the MC-GDPWM method to the symmetrical SVPWM method under the same average switching frequency condition.

observed in Fig. 19(a) that the ratio is greater than unity under all operating conditions. It is also shown in Fig. 19(b) that the ratio is greater than unity in the low MI range, but less than unity in the high MI range.

D. Common-Mode Voltage

The high CMV may cause the electromagnetic interference (EMI) noise and bearing failure in the motor drive system [24]. Thus, it is advantageous to reduce the CMV by modifying the switching pattern [35], [36]. The instantaneous value of CMV, $v_{\rm cm}$ is generally defined with the voltage differences, v_{aN}, v_{bN}, and v_{cN} between the output terminals of VSI and negative terminal of dc-link, and it can be expressed as

$$v_{\rm cm} = v_{nN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3}. \tag{17}$$

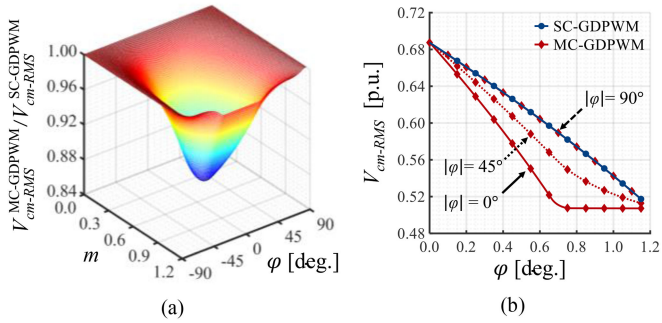

Fig. 20. Comparison of per-fundamental-cycle rms values of CMV. (a) Ratio of the MC-GDPWM method to the SC-GDPWM method. (b) Normalized rms values of CMV.

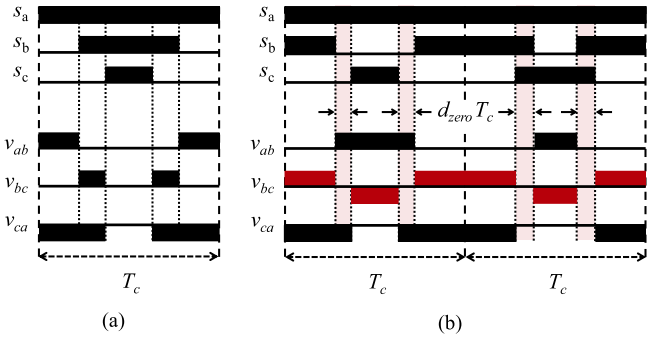

Fig. 21. Pulse patterns of three-phase line-to-line voltages. (a) Case when the single carrier signal is used. (b) Case when the double carrier signals are used.

The per-fundamental-cycle rms values of CMV, $V_{\rm cm-rms}$ by the two GDPWM methods under all operating conditions are compared in Fig. 20. The values of $V_{\rm cm-rms}$ in Fig. 20(b) are normalized to $V_{\rm dc}$. The results clearly prove that the proposed MC-GDPWM method produces lower $V_{\rm cm-rms}$ than the SC-GDPWM method (the value of $V_{\rm cm-rms}$ by the SC-GDPWM method is irrelevant to φ). This is because the use of double carrier signals effectively removes or reduces the time duration of zero-voltage states which generate the oscillation of $v_{\rm cm}$ at maximum.

E. Line-to-Line Voltage

The rapid polarity reversal of line-to-line voltages may bring about an overvoltage problem at the motor terminals that causes the destruction of motor insulation and EMI, especially in the applications using long cables between the VSI and motor [35]–[37]. Thus, the line-to-line voltage patterns need to be investigated when the switching patterns are modified. In Fig. 21, pulse patterns of the three-phase line-to-line voltages, v_{ab}, v_{bc}, and v_{ca} with the single and double carrier signals are illustrated when $v_{an}^* > v_{bn}^* > v_{cn}^*$ and $v_{no}^* = 1 - v_{1n}^*$. As shown here, one of the three-phase line-to-line voltages by the double carrier signals has bipolar patterns in Area I (v_{bc} in this example), whereas those by the single carrier signal have only unipolar patterns.

In order to avoid the problematic bipolar patterns of line-to-line voltage, the sufficient zero-voltage time intervals are required between the two voltage pulses with opposite polarity

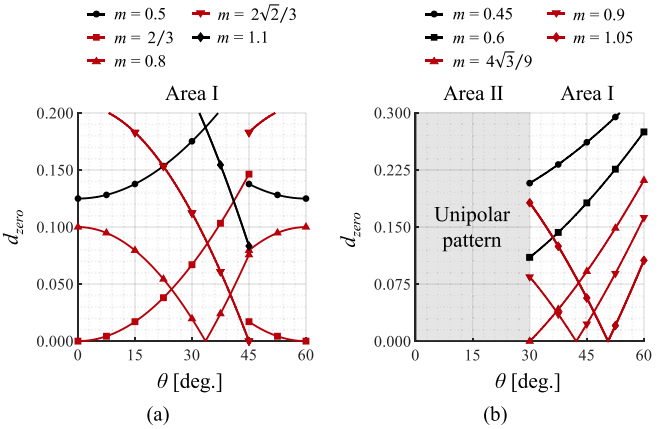

Fig. 22. Duty cycle of zero-voltage time interval of bipolar line-to-line voltage by the MC-GDPWM method. (a) $\varphi = 15°$. (b) $\varphi = 60°$.

as shown in Fig. 21. Based on the switching patterns shown in Figs. 8 and 9, the duty cycle of zero-voltage time interval, d_{zero} when the double carrier signals are used and can be obtained as

$$d_{\text{zero}} = \frac{|d_2 + d_3 - 1|}{2} (\text{if } v_{no}^* = 1 - v_{1n}^*) \tag{18}$$

$$d_{\text{zero}} = \frac{|d_1 + d_2 - 1|}{2} (\text{if } v_{no}^* = -1 - v_{3n}^*). \tag{19}$$

The values of d_{zero} in the interval of $0° \leq \theta \leq 60°$ are computed at $\varphi = 15°$ and $60°$ using (18) and (19), and they are shown in Fig. 22 (they are repeated every 60°). The results show that it is rarely possible for d_{zero} to become zero in Area I by the MC-GDPWM method (in Area II, the line-to-line voltage patterns are unipolar). In other words, the MC-GDPWM method may cause the rapid polarity reversal of line-to-line voltages at specific values of m and θ. For example, when $\varphi = 15°$, as shown in Fig. 22(a), d_{zero} is zero at the certain θ in the range of $2/3 \leq m \leq 2\sqrt{2}/3$ ($m = 2/3$, 0.8, and $2\sqrt{2}/3$ in this example). On the other hand, in the other range of m ($m = 0.5$ and 1.1 in this example), it never becomes zero. Similarly, when $\varphi = 60°$ as shown in Fig. 22(b), it becomes zero at the certain θ in the range of $m \geq 4\sqrt{3}/9$ ($m = 4\sqrt{3}/9$, 0.9, and 1.05 in this example).

VI. Experimental Verification

A. Experimental Set-Up

In this section, the practical effectiveness of proposed MC-GDPWM method is verified by the experimental tests on a motor drive system shown in Fig. 23. In this experiment, the switching devices and their gate drivers of VSI were consisted of the intelligent power module (IPM) of IKCM30F60GD made by Infineon. This IPM has been controlled by the digital signal processor (DSP) of TMS320F28377S. As the dc-link capacitor, the metallized polypropylene film capacitor of EZPE50107MTA has been used. As the test motor, the interior permanent magnet synchronous motor (IPMSM) has been utilized. The detailed specification of parameters is given in Table II.

When implementing the proposed MC-GDPWM method in practice, the multicarrier signals might be incorrectly selected

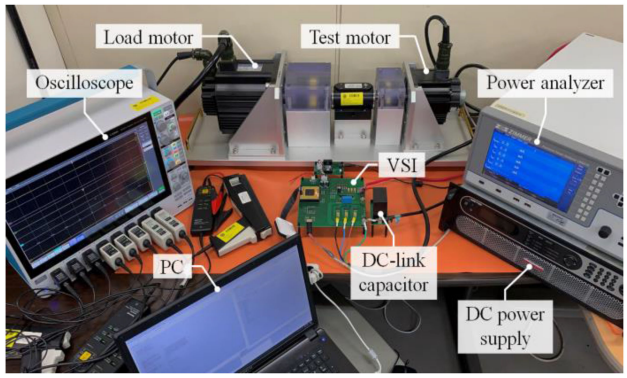

Fig. 23. Hardware set-up for the experimental test.

TABLE II
Specification of Parameters Used in the Experimental Test

Quantity	Symbol	Value
DC-link voltage	V_{DC}	200 V
Capacitance of DC-link capacitor	C_{DC}	100 μF
Carrier frequency	$f_c = 1/T_c$	10 kHz
Rated power of IPMSM	P_{rated}	2 kW
Rated speed of IPMSM	n_{rated}	2,000 RPM
Rated torque of IPMSM	T_{rated}	9.55 N·m
Rated RMS current of IPMSM	$I_{A\text{-}RMS\text{-}rated}$	9.9 A_{RMS}
d-axis inductance of IPMSM	L_d	1.867 mH
q-axis inductance of IPMSM	L_q	3.051 mH

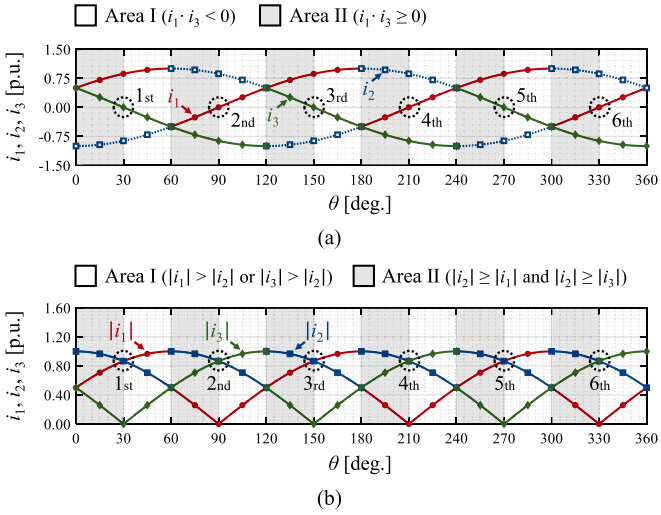

Fig. 24. Six points in which multicarrier selection errors can occur ($\varphi = 60°$). (a) Case when the first flowchart of multicarrier selection is used. (b) Case when the second flowchart of multicarrier selection is used.

near six points, where Area II is switched to Area I as shown in Fig. 24, within one fundamental cycle (this is not a problem when $|\varphi| < 30°$). This is because of the phase current measurement error. For example, the carrier selection error might occur near the zero-crossing points of i_1 and i_3 when the carrier signals are selected by the first type of flowchart shown in Fig. 12(a). Similarly, when the second type of flowchart shown in Fig. 12(b)

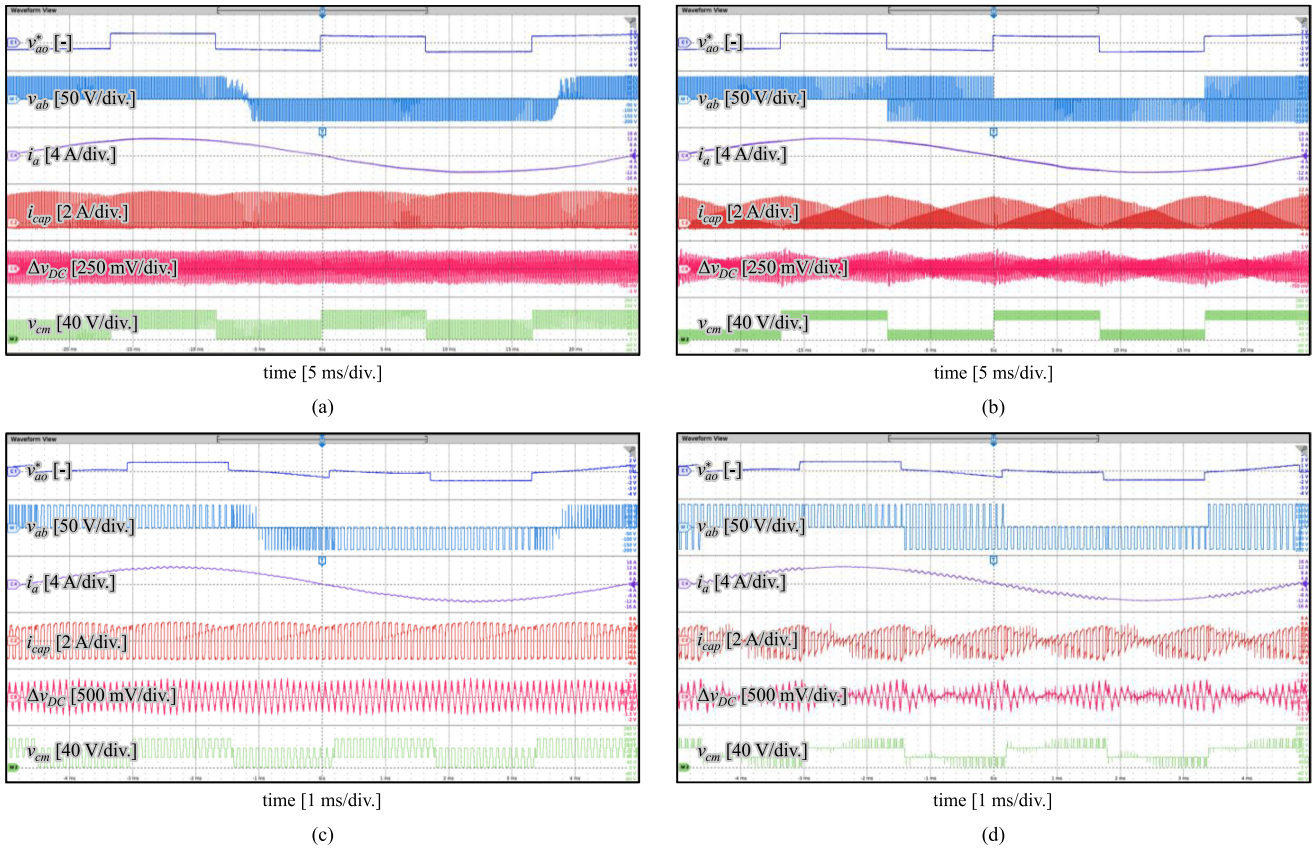

Fig. 25. Experimental waveforms of pole voltage reference, line-to-line voltage, phase current, dc-link capacitor current, dc-link voltage ripple, and CMV near $\varphi = 15°$. (a) SC-GDPWM method near $m = 0.2$. (b) MC-GDPWM method near $m = 0.2$. (c) SC-GDPWM method near $m = 0.7$. (d) MC-GDPWM method near $m = 0.7$.

is used, the error might be detected near the intersection points between $|i_1|$ and $|i_2|$ or $|i_2|$ and $|i_3|$. To minimize the carrier selection error in this experiment, the instantaneous phase currents are sampled at the center of each carrier cycle by the analog-to-digital converter in the DSP, and their fundamental component is used as far as possible. In addition, the sampled phase currents are reconstructed in the DSP by using the *d*- and *q*-axis currents filtered by the digital low-pass filter and rotor angle although delays may occur in the transient state. In this experiment, between the two types of flowcharts for the proposed carrier selection strategy, the second one has been used.

In fact, the occasional carrier selection errors are acceptable because there is no significant difference in the values of $i_{\mathrm{cap-rms}}$ at the points where Area II is switched to Area I, as shown in Fig. 14(b). Nevertheless, if it is still considered as a problem, some advanced current measurement techniques with oversampling or calculating the average over the past carrier cycle can be utilized for the accurate measurement of current [38].

B. Experimental Waveforms

The experimental waveforms of v_{ao}^*, v_{ab}, i_a, i_{cap}, Δv_{dc}, and v_{cm} by the conventional SC-GDPWM and proposed MC-GDPWM methods are shown in Fig. 25 when *m* is close to 0.2 and 0.7 and φ is close to 15°. The waveforms have been measured by the mixed signal oscilloscope of Tektronix MSO58, which has the bandwidth of 500 MHz and the dc gain accuracy of 1.0%. For the voltage measurement, the high-voltage differential probe of Tektronix THDP0200, which has the bandwidth of 200 MHz, has been used. The dc-link capacitor current has been directly measured using the ac/dc current probe of Tektronix TCP0020, which has the bandwidth of 50 MHz and high accuracy with less than 1.0% dc gain error. For the phase current measurement, the ac/dc current probe of Tektronix TCP0150, which has the bandwidth of 20 MHz, has been used. The value of I_A has been controlled to 12 A in all test conditions, and the value of φ has been set by properly controlling the *d*- and *q*-axis currents. It is observed from the results of Fig. 25 that the SC-GDPWM and MC-GDPWM methods have the different waveforms of v_{ab}, i_a, i_{cap}, Δv_{dc}, and v_{cm} due to the proposed carrier selection strategy, although they have the same v_{ao}^*. Above all, it is clearly verified that the fluctuations of i_{cap}, Δv_{dc}, and v_{cm} are significantly reduced by the proposed MC-GDPWM method. However, the MC-GDPWM method partially results in the bipolar patterns of v_{ab}, while the SC-GDPWM method only has the unipolar pattern. Because of that, the waveform of i_a by the MC-GDPWM method is more distorted than that by the SC-GDPWM method, and the rapid polarity reversal problem of line-to-line voltage can arise.

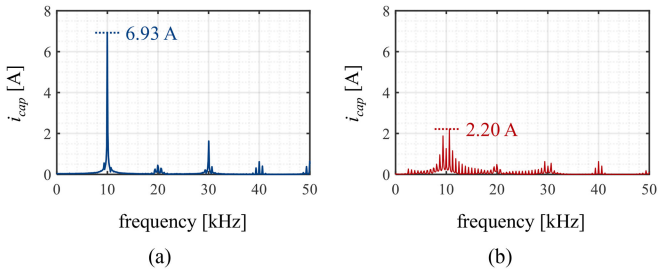

Fig. 26. Experimental frequency spectrums of dc-link capacitor current near $m = 0.7$ and $\varphi = 15°$. (a) SC-GDPWM method. (b) MC-GDPWM method.

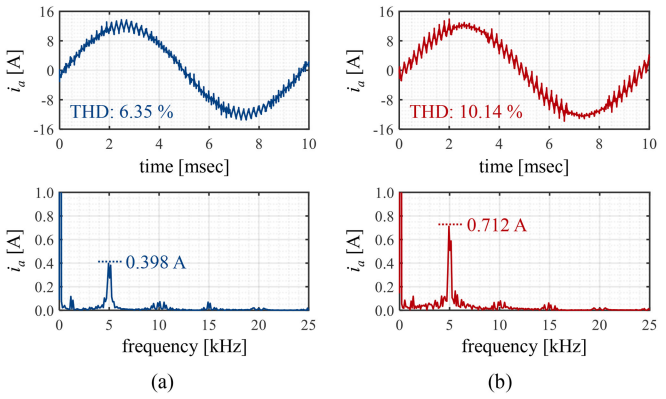

Fig. 27. Experimental waveforms and their frequency spectrums of phase current near $m = 0.7$ and $\varphi = 15°$ ($f_c = 5$ kHz). (a) SC-GDPWM method. (b) MC-GDPWM method.

The experimental frequency spectrums of i_{cap} by the SC-GDPWM and MC-GDPWM methods are shown in Fig. 26 near $m = 0.7$ and $\varphi = 15°$. It is observed here that the peak harmonic component of i_{cap} is detected near carrier frequency in both GDPWM methods. Also, it is clearly shown that not only the value of $I_{\text{cap-rms}}$ is decreased from 5.74 to 3.42 A (the reduction of 40.42%), but also its peak harmonic component near carrier frequency is dramatically reduced from 6.93 to 2.20 A (the reduction of 68.25%) by the proposed MC-GDPWM method despite the distortion of phase currents [by (3) and (5), it is known that the phase current distortion may affect the dc-link capacitor current].

The experimental waveforms and their frequency spectrums of i_a by the SC-GDPWM and MC-GDPWM methods are shown in Fig. 27 near $m = 0.7$ and $\varphi = 15°$. To exaggerate the harmonic components, both GDPWM methods have been applied with a lower carrier frequency ($f_c = 5$ kHz). As expected, the MC-GDPWM method has the worse quality of phase current than the SC-GDPWM method because the larger voltage error is generated by using the double carrier signals. The total harmonic distortion (THD) of i_a is increased from 6.35% to 10.14%, and its peak harmonic component near carrier frequency is increased from 0.398 to 0.712 A.

The bipolar pattern of v_{ab} by the MC-GDPWM method is zoomed and shown in Fig. 28 near $m = 0.7$ and $\varphi = 15°$. In this condition, there is a possibility of rapid polarity reversal of line-to-line voltage (Fig. 22). However, although the instantaneous

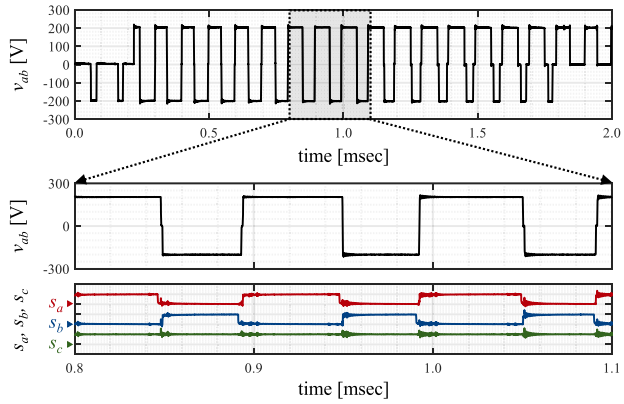

Fig. 28. Zoomed waveform of bipolar line-to-line voltage and binary switching functions by the MC-GDPWM method near $m = 0.7$ and $\varphi = 15°$.

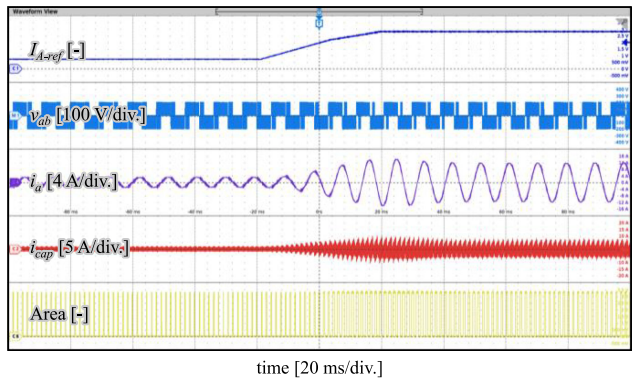

Fig. 29. Experimental waveform of line-to-line voltage, phase current, and dc-link capacitor current by the proposed MC-GDPWM method when load is changed.

voltage transition of v_{ab} between V_{dc} and $-V_{\text{dc}}$ is actually found in Fig. 28 (which is harmful to the motor windings), it rarely occurs in some narrow regions within the fundamental cycle. Also, it may not occur depending on the MI. Thus, the MC-GDPWM method does not seem to cause the serious problem in the line-to-line voltage. Nevertheless, this bipolar line-to-line voltage needs to be carefully handled case by case in practice because the minimum zero-voltage time interval for avoiding it depends on the individual motor drive system [36]. Recently, the integration of VSI and motor is being made particularly for the EV applications to place the VSI as close as possible to motor so that it can mitigate the overvoltage problem [1].

To demonstrate the dynamic transition process of Areas I and II, the experimental waveforms of v_{ab}, i_a, and i_{cap} by the proposed MC-GDPWM method are shown in Fig. 29 when the amplitude of phase current reference, $I_{A-\text{ref}}$ is increased from 3 to 12 A near $m = 0.7$ and $\varphi = 45°$. The low and high values of Area in Fig. 29 indicate Areas I and II, respectively. It is clearly observed that the transition between Area I and II is seamless without any disturbances in the motor drive system even when its load is changed. This is because the average of phase current ripple over each carrier cycle is zero although different switching patterns are applied, and this makes it possible to seamlessly change one switching pattern to another every carrier cycle [24].

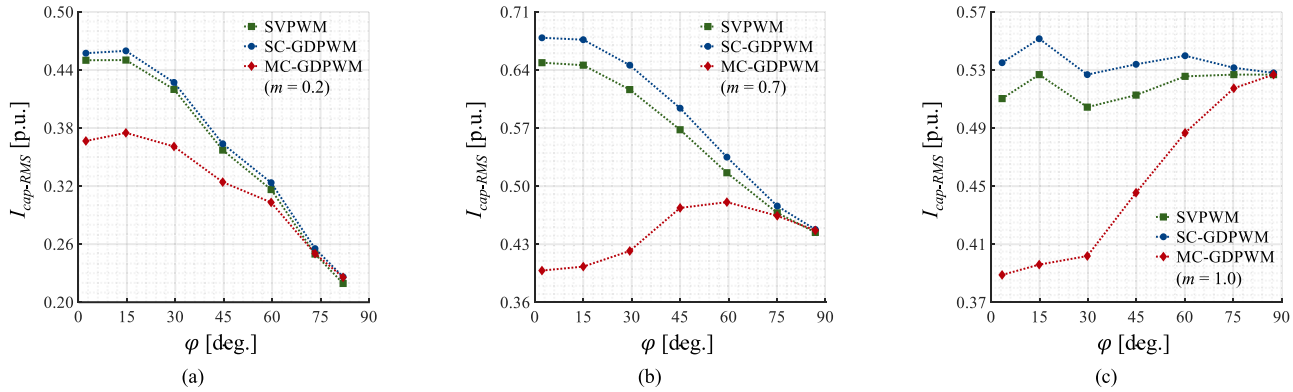

Fig. 30. Experimental results of normalized rms value of dc-link capacitor current. (a) $m = 0.2$. (b) $m = 0.7$. (c) $m = 1.0$.

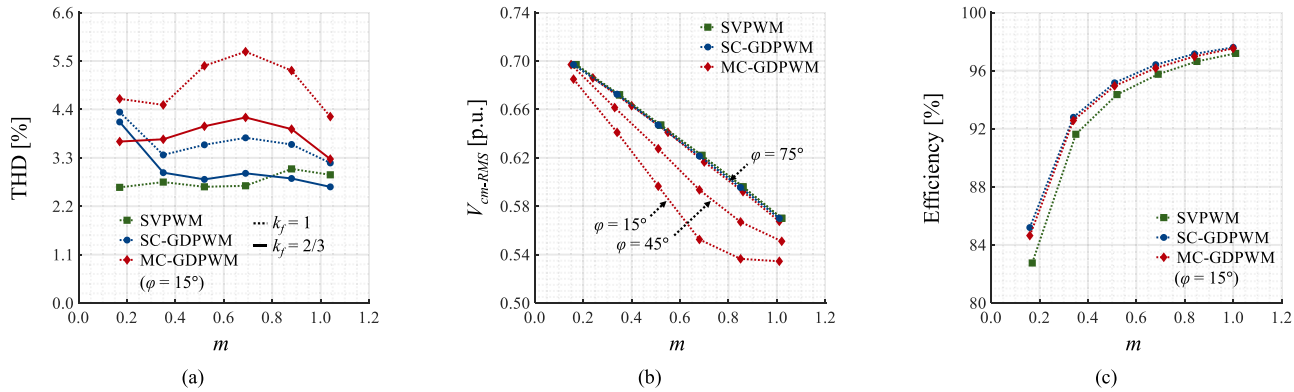

Fig. 31. Experimental results of THD of phase current, normalized rms value of CMV, and efficiency. (a) THD of phase current near $\varphi = 15°$. (b) Normalized rms value of CMV near $\varphi = 15°$, 45°, and 75°. (c) Efficiency near $\varphi = 15°$.

C. Performance Comparison

The performance by the proposed MC-GDPWM method is compared under several conditions to that by the symmetrical SVPWM and SC-GDPWM methods with respect to the rms value of dc-link capacitor current, THD of phase current, rms value of CMV, and efficiency (the experimental results by the symmetrical SVPWM method are additionally provided as a standard for intuitive comparison). In all test condition, the value of I_A has been controlled to 12 A.

First, the measured values of $I_{\mathrm{cap-rms}}$ by the symmetrical SVPWM, SC-GDPWM, and proposed MC-GDPWM methods are shown in Fig. 30 near $m = 0.2$, 0.7, and 1.0. They are directly calculated by the rms measurement algorithm of MSO58 and normalized to $I_{A-\mathrm{rms}}$. It is clearly observed here that the proposed MC-GDPWM method effectively reduces $I_{\mathrm{cap-rms}}$ when compared with the conventional SVPWM and SC-GDPWM methods under all test conditions, although it has the distorted phase currents (the degraded phase currents might increase $I_{\mathrm{in-rms}}$ and $I_{\mathrm{cap-rms}}$). In particular, the point with the largest decline is observed near $m = 0.7$ and unity PF (the reduction of 38.61% and 41.32%, when compared with that by the SVPWM and SC-GDPWM methods, respectively). This is because the dc-link capacitor current reduction effect of proposed carrier selection strategy is more dominant than its phase current distortion effect. Note that the SC-GDPWM method has higher $I_{\mathrm{in-rms}}$ than the SVPWM method due to the distorted phase currents and larger dc-link voltage ripple.

Second, the comparison for the THD of measured i_a by the three different PWM methods near $\varphi = 15°$ is shown in Fig. 31(a). The values of THD have been calculated using the fast Fourier transform algorithm. As previously analyzed with the conceptual harmonic flux vector, the proposed MC-GDPWM method has higher THD than the two conventional PWM methods under the same carrier frequency condition (1.45–2.14 times that by the SVPWM method and 1.07–1.52 times that by the SC-GDPWM method). This is a general tradeoff issue resulting from the dc-link capacitor current and CMV reduction. Nevertheless, the MC-GDPWM method provides the competitive performance of THD at the same average switching frequency condition (1.12–1.58 times that by the SVPWM method and 0.89–1.43 times that by the SC-GDPWM method). In particular, the difference between the three PWM methods becomes smaller in the high MI range, and the MC-GDPWM method even has lower THD than the SC-GDPWM method in the relatively low MI range near 0.2. Moreover, the value of $\mathrm{k_f}$ for the GDPWM methods can be reduced to a half $(1/2)$ under the same switching loss condition (this is true for $|\varphi| < 30°$, where the SLF of

GDPWM methods is 0.5 [13]). In other words, the shortcoming of increased THD by the proposed MC-GDPWM method can be overcome by using a higher carrier frequency. It is also expected that it will be possible to employ the higher carrier frequency with the advent of wide-bandgap (WBG) semiconductor devices if their high *dv*/*dt* and *di*/*dt* problems are solved by passive, active, and soft-switching techniques [39] and advanced circuit designs [40], [41].

Third, the normalized values of measured $V_{\mathrm{cm-rms}}$ by the SVPWM, SC-GDPWM, and MC-GDPWM methods near $\varphi = 15°, 45°$, and $75°$ are shown in Fig. 31(b). They also have been directly calculated by the rms measurement algorithm of MSO58. Similar to the results of $I_{\mathrm{cap-rms}}$, the proposed MC-GDPWM method provides improved common-mode features than the two conventional PWM methods. In particular, the reduction effect of CMV becomes more prominent in the high PF range.

Last, the efficiencies by the three PWM methods near $\varphi = 15°$ are compared in Fig. 31(c). They have been measured by the power analyzer of ZES ZIMMER LMG670, which has the bandwidth of 10 MHz and the accuracy of 0.015%. Due to their optimal modulation signals to minimize the switching losses, the measured efficiencies by both MC-GDPWM and SC-GDPWM methods are higher than that by the SVPWM method.

VII. Conclusion

This article proposed the carrier selection strategy of MC-GDPWM method for the two-level three-phase VSI to reduce the rms value of dc-link capacitor current while maintaining the minimum switching losses. To reduce the rms value of dc-link capacitor current, the modulation signals of existing SC-GDPWM method were selectively compared with the single and double carrier signals based on the proposed carrier selection strategy. Although it depends on the PF, the calculation of PF was avoided because the multicarrier signals were chosen based on the information of three-phase modulation signals and measured three-phase currents. The minimum switching losses were also kept by the proposed MC-GDPWM method because the modulation signals of conventional SC-GDPWM method, which were known to be optimal in terms of switching losses, were employed, and the number of switching events remained almost same even though the proposed carrier selection strategy was employed.

It was analytically validated that the proposed MC-GDPWM method effectively reduced the rms value of dc-link capacitor current under all operating conditions of VSI compared with the conventional PWM methods. The dc-link voltage ripple was also reduced as the dc-link capacitor current decreased. The high efficiency of VSI was maintained well, and the improvement of common-mode features was also made such that it is expected to help alleviate the EMI problems. However, the MC-GDPWM method distorted the phase currents more than the conventional PWM methods. This was a tradeoff issue resulting from the reduction of dc-link capacitor current and CMV. In the near future, it is expected to be overcome by increasing the switching frequency with the use of WBG semiconductor devices if their high *dv*/*dt* and *di*/*dt* problems are solved by the advanced control and design technologies. The rapid polarity reversal problem in line-to-line voltage was also observed such that it was not serious. The practical effectiveness of proposed MC-GDPWM method was verified by the experimental results on the IPMSM drive system.

References

[1] I. Husain *et al.*, "Electric drive technology trends, challenges, and opportunities for future electric vehicles," *Proc. IEEE*, vol. 109, no. 6, pp. 1039–1059, Jun. 2021.

[2] J. Reimers, L. Dorn-Gomba, C. Mak, and A. Emadi, "Automotive traction inverters: Current status and future trends," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3337–3350, Apr. 2019.

[3] S. E. Schulz, "Exploring the high-power inverter: Reviewing critical design elements for electric vehicle applications," *IEEE Electrific. Mag.*, vol. 5, no. 1, pp. 28–35, Mar. 2017.

[4] M. Dubey, S. K. Sharma, and R. Saxena, "Solar power based PMSM drive employed in refrigeration plants for isolated areas," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6299–6308, Nov./Dec. 2018.

[5] D. Anton, N. S. Kim, and Y. K. Kim, "Future drives of home appliances: Elimination of the electrolytic DC-link capacitor in electrical drives for home appliances," *IEEE Ind. Electron. Mag.*, vol. 9, no. 3, pp. 10–18, Sep. 2015.

[6] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2688–2701, May 2016.

[7] J.-G. Kim, K.-B. Lee, and J.-W. Park, "Clamping angle control PWM method to restore linear modulation range of a voltage source inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10914–10923, Dec. 2018.

[8] S.-L. An, X.-D. Sun, Q. Zhang, Y.-R. Zhong, and B.-Y. Ren, "Study on the novel generalized discontinuous SVPWM strategies for three-phase voltage source inverters," *IEEE Trans. Ind. Inform.*, vol. 9, no. 2, pp. 781–789, May 2013.

[9] J. Guo, J. Ye, and A. Emadi, "DC-link current and voltage ripple analysis considering antiparallel diode reverse recovery in voltage source inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5171–5180, Jun. 2018.

[10] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, Dec. 2013.

[11] H. W. Van Der Broeck, H.-C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Trans. Ind. Appl.*, vol. 24, no. 1, pp. 142–150, Jan./Feb. 1988.

[12] E. R. C. da Silva, E. C. dos Santos, and C. B. Jacobina, "Pulsewidth modulation strategies: Nonsinusoidal carrier-based PWM and space vector modulation techniques," *IEEE Ind. Electron. Mag.*, vol. 5, no. 2, pp. 37–45, Jun. 2011.

[13] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, Sep./Oct. 1998.

[14] L. Asiminoaei, P. Rodríguez, and F. Blaabjerg, "Application of discontinuous PWM modulation in active power filters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1692–1706, Jul. 2008.

[15] T. D. Nguyen, J. Hobraiche, N. Patin, G. Friedrich, and J.-P. Vilain, "A direct digital technique implementation of general discontinuous pulse width modulation strategy," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4445–4454, Sep. 2011.

[16] O. Oñederra, I. Kortabarria, I. M. de Alegría, J. Andreu, and J. I. Gárate, "Three-phase VSI optimal switching loss reduction using variable switching frequency," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6570–6576, Aug. 2017.

[17] B. P. McGrath and D. G. Holmes, "A general analytical method for calculating inverter DC-link current harmonics," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1851–1859, Sep./Oct. 2009.

[18] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems," *IEEE Trans. Veh. Technol.*, vol. 61, no. 7, pp. 2950–2964, Sep. 2012.

[19] R. Ramos, "Film capacitors in power applications: Choices and particular characteristics needed," *IEEE Power Electron. Mag.*, vol. 5, no. 1, pp. 45–50, Mar. 2018.

[20] M. Makdessi, A. Sari, P. Venet, P. Bevilacqua, and C. Joubert, "Accelerated ageing of metallized film capacitors under high ripple currents combined with a DC voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2435–2444, May 2015.
[21] A. Wechsler, B. C. Mecrow, D. J. Atkinson, J. W. Bennett, and M. Benarous, "Condition monitoring of DC-link capacitors in aerospace drives," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 1866–1874, Nov./Dec. 2012.
[22] M. H. Bierhoff and F. W. Fuchs, "DC-link harmonics of three-phase voltage-source converters influenced by the pulsewidth-modulation strategy—An analysis," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2085–2092, May 2008.
[23] H. Lu, W. Qu, X. Cheng, Y. Fan, and X. Zhang, "A novel PWM technique with two-phase modulation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2403–2409, Nov. 2007.
[24] E. Ün and A. M. Hava, "A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 782–793, Mar./Apr. 2009.
[25] J. Hobraiche, J.-P. Vilain, P. Macret, and N. Patin, "A new PWM strategy to reduce the inverter input current ripples," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 172–180, Jan. 2009.
[26] T. D. Nguyen, N. Patin, and G. Friedrich, "Extended double carrier PWM strategy dedicated to RMS current reduction in DC link capacitors of three-phase inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 396–406, Jan. 2014.
[27] J. Xu, J. Han, Y. Wang, M. Ali, and H. Tang, "High-frequency SiC three-phase VSIs with common-mode voltage reduction and improved performance using novel tri-state PWM method," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1809–1822, Feb. 2019.
[28] J. Xu, J. Han, Y. Wang, S. Habib, and H. Tang, "A novel scalar PWM method to reduce leakage current in three-phase two-level transformerless grid-connected VSIs," *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 3788–3797, May 2020.
[29] K. Nishizawa, J.-I. Itoh, A. Odaka, A. Toba, and H. Umida, "Current harmonic reduction based on space vector PWM for DC-link capacitors in three-phase VSIs operating over a wide range of power factor," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4853–4867, May 2019.
[30] A. M. Hava and N. O. Çetin, "A generalized scalar PWM approach with easy implementation features for three-phase, three-wire voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1385–1395, May 2011.
[31] J. Lee, H.-K. Yang, and J.-W. Park, "Scalar approach based PWM strategy for two-level three-phase VSIs to reduce switching losses and RMS current in DC-link capacitors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 3342–3348.
[32] C. B. Jacobina, A. M. N. Lima, E. R. C. da Silva, R. N. C. Alves, and P. F. Seixas, "Digital scalar pulse-width modulation: A simple approach to introduce non-sinusoidal modulating waveforms," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 351–359, May 2001.
[33] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan. 1999.
[34] M. Vujacic, O. Dordevic, and G. Grandi, "Evaluation of DC-link voltage switching ripple in multiphase PWM voltage source inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3478–3490, Apr. 2020.
[35] A. M. Hava and E. Ün, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 241–252, Jan. 2009.
[36] A. M. Hava and E. Ün, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1998–2008, Jul. 2011.
[37] S. Amarir and K. Al-Haddad, "A modeling technique to analyze the impact of inverter supply voltage and cable length on industrial motor-drives," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 753–762, Mar. 2008.
[38] S. N. Vukosavić, L. S. Perić, and E. Levi, "A three-phase digital current controller with improved performance indices," *IEEE Trans. Energy Convers.*, vol. 32, no. 1, pp. 184–193, Mar. 2017.
[39] F. Pulsinelli, M. di Benedetto, A. Lidozzi, L. Solero, and F. Crescimbini, "Power losses distribution in SiC inverter based electric motor drives," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7843–7853, Nov./Dec. 2019.
[40] S. Yin, K. J. Tseng, R. Simanjorang, Y. Liu, and J. Pou, "A 50-kW high-frequency and high-efficiency SiC voltage source inverter for more electric aircraft," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9124–9134, Nov. 2017.
[41] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and Y. Kang, "An SiC-based half-bridge module with an improved hybrid packaging method for high power density applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8980–8991, Nov. 2017.

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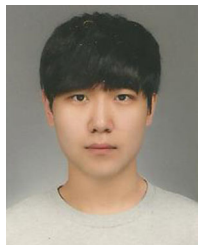

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