Analysis of Hybrid Modular Multilevel Rectifier Operated at Nonunity Power Factor for HVDC Applications

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***Abstract*—Hybrid modular multilevel rectifier (HMMR) is a type of unidirectional modular voltage source converter (VSC) that has been proposed for the high-voltage (HV) dc transmission applications. Compared to the modular multilevel converter (MMC), up to 50% of the submodules (SMs) and capacitors can be replaced by the simple HV line-frequency diode stacks at unity power factor (PF). The nonunity PF operation is also favored for the rectifier station to support the grid. Therefore, this article proposes two new current commutation methods for HMMR to reduce the SM number at nonunity PF. In addition, an average model is given to reveal the inherent power flow relationship of HMMR. It is found that part of the active power is delivered from ac to dc side through the diode directly, which reduces the energy storage requirement. The performance of HMMR is also evaluated and compared with MMC. Both methods can successfully decrease the 30% low voltage devices. Method 1 can reduce 32% capacitor and method 2 achieves 52% reduction. The feasibility of the proposed converter is verified by the simulation results from a 200-kV 200 MVA HVdc model. Finally, a scale-down 400-V HMMR prototype is developed to validate the effectiveness of the proposed control scheme.**

***Index Terms*—Current commutation, high-voltage direct current (HVdc) system, hybrid modular multilevel rectifier (HMMR), nonunity power factor (PF), power flow.**

I. Introduction

MODULAR multilevel converter (MMC) has emerged as one of the most attractive topologies for the medium-voltage (MV) and high-voltage direct current (HVdc) applications due to its flexibility, modular structure, excellent power quality, and fault-tolerant operation capability [1]–[3]. However, MMC-based HVdc (MMC-HVdc) systems still confront some limitations. First, the number of insulated-gate bipolar transistors (IGBTs) is doubled with the half-bridge (HB) submodule (SM) and quadrupled with full-bridge (FB) SM compared with the classic two-level voltage source converter (VSC). The use of low-voltage rating IGBTs in SM results in higher conduction losses. Second, the SM capacitors occupy more than 50% of the weight and size of MMC [4], hence resulting in the bulky volume and higher construction cost. This also hinders MMC for the weight or space sensitive applications, such as the offshore wind power platform.

Compared to the MMC-HVdc, the line-commutated converter based HVdc system (LCC-HVdc) reduces the cost, volume, and power conversion losses [5]. Nevertheless, LCC-HVdc also suffers from some critical drawbacks, including the large reactive power consumption, large amount of harmonic currents, and limited voltage regulation range [6], [7]. The commutation process involves interactions with the grid, leading to the commutation failure or reduced power capacity under a weak-grid condition.

Given that the power flow of MV/HV dc power delivery systems is often unidirectional, the diode rectifier based HVdc (DR-HVdc) systems have recently received notable interest [8]–[10]. By replacing the MMC rectifier station with diode rectifier (DR), the volume, weight, and cost could be decreased significantly. For example, a technical feasibility study on the use of DR for the connection of offshore wind power plants was presented in [11]. Besides, the DR-based low frequency ac transmission has been proposed in [12], which gives a competitive solution for offshore wind farm integration. Notwithstanding the advantages of smaller size and lower cost, the passive device used in DR brings some limitations as well. First, DR cannot provide reactive power, so the reactive power of the ac grid connected to DR must be compensated by other equipment. Second, DR will inject harmonic currents into the ac system, implying the need for active compensation or bulky passive filters. Third, the ac voltage magnitude has to vary in order to regulate the active power transmission. Finally, the unidirectional scheme has the drawback of the auxiliary power circuit to energize the windfarm during the start-up process.

In order to address these issues, various hybrid topologies have been proposed. In [13], a hybrid converter composed with DRs and a series connected two-level VSC was proposed. The VSC can compensate the reactive power and harmonics generated by the DR. Li *et al.* [14] proposed to connect an MMC in parallel with LCC or DR on ac sides to optimize the power distribution between two HVdc links. However, the parallel connection needs the VSC to tolerate full nominal HVdc voltage and additional full-rating ac transformer with tertiary windings.

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In [15], an HV cascaded FB branch are connected to the MMC dc side to reduce MMC SM number. But a large LC filter is required to constrain the high-frequency circulating current. In [16], a low-power FB-MMC is connected in series with DR on dc side, while their ac sides are in parallel through the transformer. The FB-MMC can control the dc voltage and regulate partial power. However, the FB-MMC may work as an inverter mode to control DR power and this circulating power will reduce the efficiency.

Different from the combination of converter level MMC and DR, another type of hybrid MMC structure is derived from device level. Various "hybrid multilevel converters" have evolved recently [17], which are created with the concept of combining the series-connected thyristors or IGBTs and chain-links (CLs). A group of converters, including alternate arm converter [18]–[20], parallel hybrid converter [21], [22], series bridge converter [23], and the hybrid MMC with mixed FB and HB SMs [24]–[26] have been proposed. They can address one or more issues of MMC. In [27]–[29], the three-level type hybrid MMC was introduced, which can save around 30% devices, 50% total capacitor, and 32% power losses compared to MMC. Based on the HMMC, a hybrid modular multilevel rectifier (HMMR) was proposed in [30], which replaces the HV IGBT stack in HMMC with a series diode. In this way, the key benefits of MMC are kept, and the SM number could be reduced similar to HMMC. Particularly at the unity power factor (PF), HMMR can reduce the SM numbers by 50%. However, the passive device of the diode does not have the current interruption capability compared to IGBT, which means more effort should be put into the current commutation design. Therefore, this article focuses on the nonunity PF operation to facilitate the practical application of HMMR. To realize the current commutation during the leading or lagging time of ac current, some additional HB or FB SMs should be added [27]. As an extension, the main contribution of this article is as follows.

1) A new current commutation method is proposed to operate HMMR at nonunity PF. This method requires only HB SM and possesses better modularity.
2) The third harmonic is injected to help reduce the FB number used in [27]. And the analysis of the two methods covers the cases of both leading and lagging PF.
3) The average model is established to reveal the inherent power flow relationship between ac and dc sides. It is found that HMMR has a lower capacitance requirement because partial active power is delivered from ac to dc side through the diode directly.
4) The performance is evaluated and compared between traditional MMC and HMMR with two methods, in terms of the device number, arm capacitance as well as semiconductor losses.

This article is organized as follows. The nonunity PF operation of HMMR with two methods is proposed in Section II. The average model is also given to understand power low in HMMR. In Section III, the performance is compared between the traditional HB MMC and HMMR at different PF. The control strategy and simulation results are assessed in Section IV, and the experimental results from a scale down prototype are provided to validate the proposed method in Section V. Finally, Section VI concludes this article.

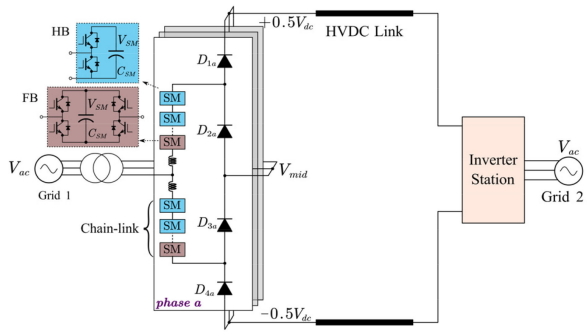

Fig. 1 Structure of HMMR.

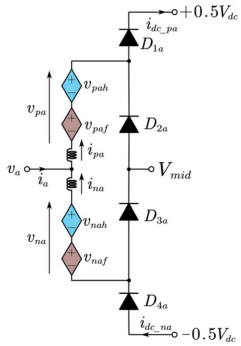

Fig. 2 Single phase simplified model of HMMR.

II. System Overview and Operation Principle

A. System Topology

Fig. 1 depicts the topology of three-phase HMMR derived from [27]. Each phase-leg consists of the upper and lower CLs, which are connected between four HV diode stacks (D_1–D_4). The midpoints of three-phase diode stacks are connected together, thereby providing a freedom to reshape the CL voltage. In this type of HMMR, each CL contains N series SMs, including $N_{\rm h}$ HB SMs and $N_{\rm f}$ FB SMs. Each of them has a floating capacitor $C_{\rm sm}$ at the rated voltage of $V_{\rm sm}$.

For the sake of simplicity, one phase (phase a) is used as an example for illustration. Fig. 2 shows the simplified model of HMMR, where the cascaded HB and FB SMs in each arm can be regarded as the controlled voltage sources. $V_{\rm dc}$ and $v_{\rm a}$ denote the rated dc-side and ac-side voltages, respectively. $V_{\rm mid}$ is the midpoint voltage, which should be controlled to be zero. $v_{\rm pah}$, $v_{\rm paf}$, $v_{\rm nah}$, and $v_{\rm naf}$ represent the voltages modulated by the HB and FB SMs in the upper and lower CLs, respectively. Their sum voltages are denoted as $v_{\rm pa}$ and $v_{\rm na}$. While $i_{\rm pa}$ and $i_{\rm na}$ are referred to the corresponding CL currents, respectively.

The ac side variables are defined as

$$v_a = V_{ac}\sin(\omega t - \varphi),\ i_a = I_{ac}\sin(\omega t) \tag{1}$$

where $V_{\rm ac}$ and $I_{\rm ac}$ represent the amplitude of ac voltage and current, respectively. The angular frequency is denoted as ω,

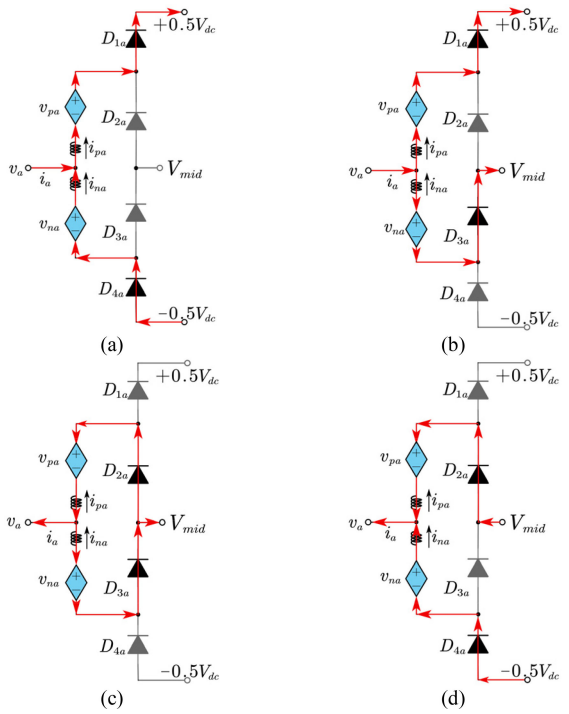

Fig. 3 Four working states of single phase HMMR, (a) *PN* state, (b) *PZ* state, (c) *ZZ* state, (d) *ZN* state.

whereas the phase angle difference between current and voltage is given by φ, which determines the PF.

Since the diode is a passive device, the polarity of $i_{\rm pa}$ directly determines whether D_{1a} or D_{2a} is turned on. Similarly, the polarity of $i_{\rm na}$ determines the conduction of D_{3a} or D_{4a}. As a result, there are four working states and connection methods for the single-phase HMMR: positive-negative (*PN*), positive-zero (*PZ*), zero-zero (*ZZ*), zero-negative (*ZN*) states as shown in Fig. 3. Accordingly, the upper and lower CL voltages could be calculated as below if neglecting the inductor voltage

$$\begin{aligned} v_{pa}^{*} &= 0.5V_{dc} - v_a,\ v_{na}^{*} = 0.5V_{dc} \\ &\quad + v_a\ (i_{pa} > 0, i_{na} > 0, PN) \\ v_{pa}^{*} &= 0.5V_{dc} - v_a,\ v_{na}^{*} = v_a - V_{mid}\ (i_{pa} > 0, i_{na} < 0, PZ) \\ v_{pa}^{*} &= V_{mid} - v_a,\ v_{na}^{*} = v_a - V_{mid}\ (i_{pa} < 0, i_{na} < 0, ZZ) \\ v_{pa}^{*} &= V_{mid} - v_a,\ v_{na}^{*} = 0.5V_{dc} + v_a\ (i_{pa} < 0, i_{na} > 0, ZN). \end{aligned} \tag{2}$$

But regardless the working state, there is always a constraint for two CL currents in the following equation:

$$i_a = i_{pa} - i_{na}. \tag{3}$$

B. Three-Phase Configuration and Current Distribution

The original unity PF operation has already been discussed in [27]. The trapezoidal current allocation method as shown in Fig. 4 can switch the CL current polarity and working state naturally at the ac voltage zero-crossing point. The formula of voltage and current of upper CL is given in the appendix.

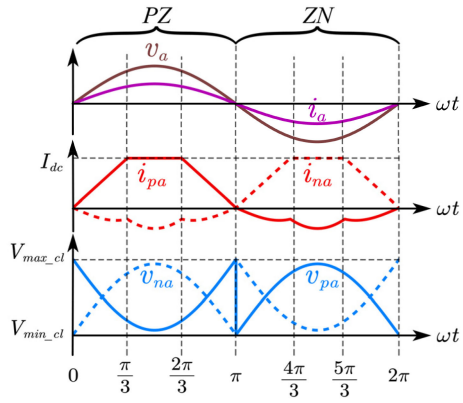

Fig. 4 Sing-phase CL current and voltage waveforms at unity PF.

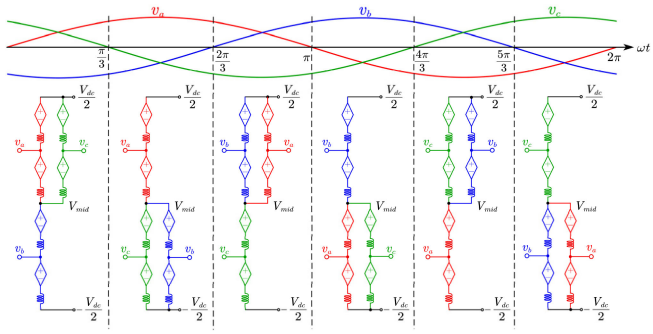

Fig. 5 Three-phase configuration of HMMR at unity PF.

Besides, the rotation between the *PZ* and *ZN* states can help achieve a minimum CL voltage stress and reduce the 50% SM number compared to the traditional HB-MMC of the same voltage rating.

Furthermore, it can be proven that this scheme is feasible at any modulation index *M*. Taking the positive half cycle $\omega t \in (0, \pi)$ as an example, $i_{\rm pa} > 0$ and $i_{\rm na} < 0$ should be met to operate in *PZ* state. Since $i_{\rm pa}$ is trapezoidal, and $i_{\rm na}$ is the subtraction of ac sinusoidal wave from $i_{\rm pa}$. As long as value of $i_{\rm na}$ at $\pi/3$ or $2\pi/3$ is negative as in (4), it will be negative during whole $(0, \pi)$

$$I_{dc} - I_{ac}\sin(\omega t) < 0, \omega t = \frac{\pi}{3}. \tag{4}$$

If *M* is defined as $M = 2V_{\rm ac}/V_{\rm dc}$, the input and output current relationship should be

$$\left.\begin{aligned} V_{dc}\, I_{dc} &= 3 \cdot \tfrac{V_{ac} I_{ac} \cos\varphi}{2} \\ I_{dc} &< \tfrac{\sqrt{3}}{2} I_{ac} \end{aligned}\right\} \Rightarrow M < \frac{2}{\sqrt{3}\cos\varphi}. \tag{5}$$

Since the maximum *M* is 1.15 with the third harmonic injection, (4) and (5) always hold at unity PF.

Considering the symmetry of the three-phase structure, the working states of the other two phases can be derived by considering the $2\pi/3$ shift of CL currents. In this way, the three-phase connection of HMMR during a one-line cycle could be divided into six segments and depicted in Fig. 5. It can be observed that during each segment, two phases are connected in parallel to the positive (or negative) terminal to share the dc bus current. And the third phase is connected to another terminal and needs to

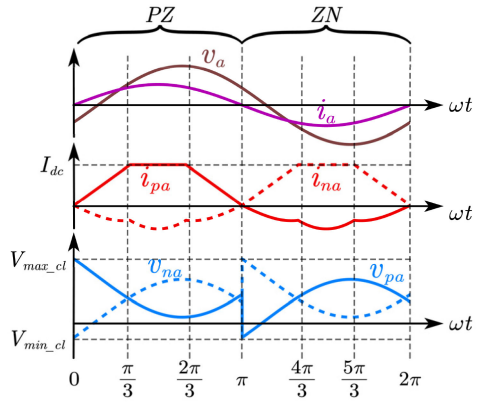

Fig. 6 Single-phase CL waveforms using previous method at leading PF.

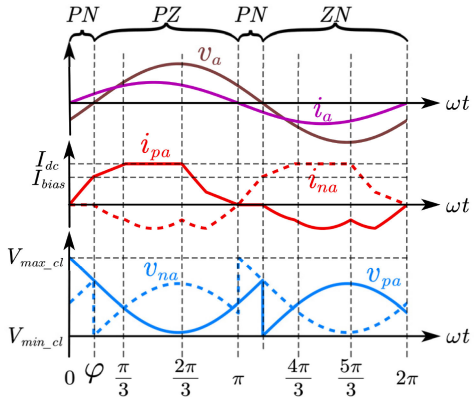

Fig. 7 Single-phase CL waveforms using method 1 at leading PF.

support the whole dc current. Therefore, the trapezoidal current allocation can keep the dc bus current constant during the overlap period of the two phases parallel connection.

Besides the unity PF operation, nonunity PF operation is also important for the rectifier in applications like HVdc to deliver some amount of reactive power and support the grid during the low-voltage transient and weak grid conditions. As shown in Fig. 6, the intuitive way is to keep the same trapezoidal current allocation aligning with the ac current, and change the CL voltages accordingly. This trapezoidal current is feasible as long as *M* and PF meet the condition of (5). As a result, the minimum and maximum CL voltage stresses will change to

$$\begin{aligned} V_{\max\_cl} &= 0.5V_{dc} + V_{ac}\sin\varphi \\ V_{min\_cl} &= -V_{ac}\sin\varphi. \end{aligned} \tag{6}$$

Obviously, extra FB SMs must be inserted to generate the negative voltage, and the total number of required SM is

$$N_{FB} = \frac{V_{ac}\sin\varphi}{V_{SM}},\ N_{HB} = \frac{0.5V_{dc}}{V_{SM}}. \tag{7}$$

However, the additional FB SMs bring higher cost, volume as well as power losses, which mitigates the benefit of HMMR. In this regard, it is desired to find other solutions to reduce the SM requirement at nonunity PF operation. In fact, besides *PZ* and *ZN* states, *PN* and *ZZ* states could also be utilized for the current commutation during the leading or lagging time of ac current. They represent two methods proposed in this article, and the detailed transient analysis and reduced CL voltage stress will be explained below.

B. Method 1 of HMMR in Nonunity PF Operation

Method 1 employs the *PN* state to reduce the CL voltage stress. The single-phase CL waveforms at leading PF are presented in Fig. 7, and the three-phase connection is shown in Fig. 8. Since six segments are symmetrical, two segments between $(0, 2\pi/3)$ are taken for illustration. When ωt is in the range of $(0, \varphi)$, the polarities of ac voltage and current are opposite. The CL currents are designed as below to make phase *a* work in *PN* state

$$i_{pa} = i_a > 0, i_{na} \approx 0, \omega t \in (0, \varphi). \tag{8}$$

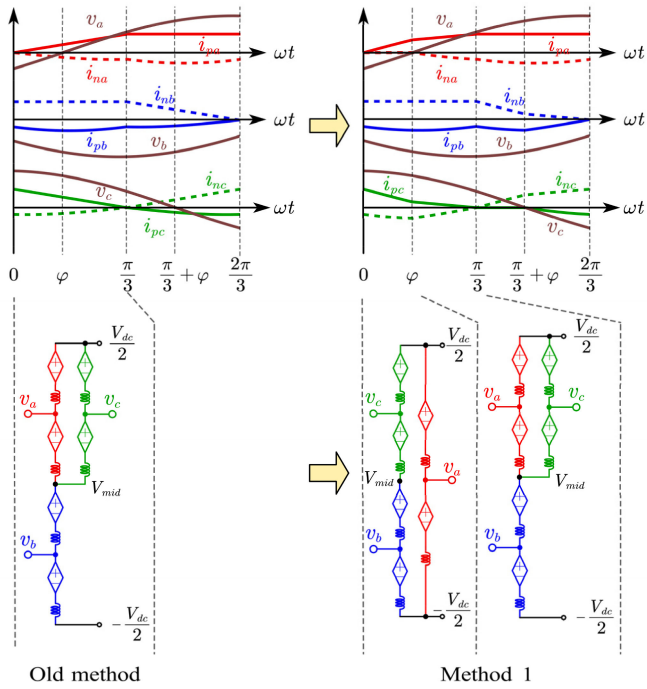

Fig. 8 Three-phase CL waveforms and transition of method 1 at leading PF.

In this way, the minimum CL voltage is reduced to 0, leading to the employment of only HB SMs. And the CL voltage stresses of method 1 become

$$V_{max\_cl1} = 0.5V_{dc} + V_{ac}\sin\varphi,\ V_{min\_cl1} = 0. \tag{9}$$

According to the three-phase connection in Fig. 8, both positive and negative dc bus currents are shared by two phases. Once phase *a* current is determined, the CL currents of phase *b* and c could be derived easily in (10) based on ac current constraint

$$\begin{cases} i_{pc} = i_{dc} - i_{pa}, & i_{nc} = i_{pc} - i_c \\ i_{nb} = i_{dc} + i_{na}, & i_{pb} = i_{nb} + i_b \end{cases}, \omega t \in (0, \varphi). \tag{10}$$

Then during (φ, π), phase *a* switches to *PZ* state as shown in Fig. 7. Similarly, $i_{\rm pa}$ is designed as a plateau of $I_{\rm dc}$ between $\pi/3$ and $2\pi/3$. Then a ramp current shape in (11) is designed for $i_{\rm pa}$ during the transition of $(\varphi, \pi/3)$. $I_{\rm bias}$ refers to the ending value

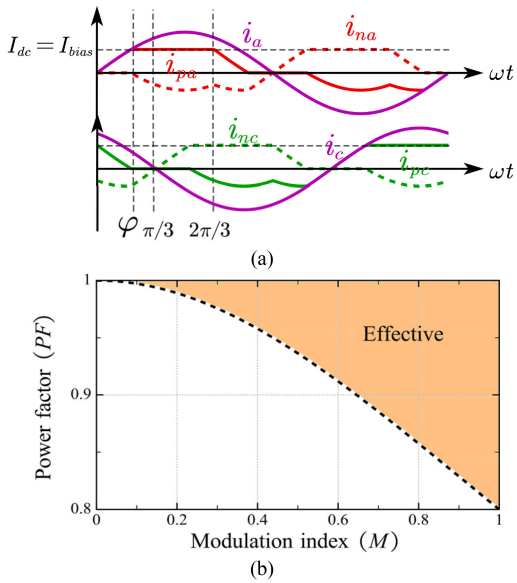

Fig. 9 (a) Boundary operation of method 1. (b) Effective region for modulation index M and PF of method 1.

of $i_{\rm pa}$ between (0, φ), and is the initial value in next stage as well

$$i_{pa}=\frac{(\omega t-\varphi)}{\pi/3-\varphi}\cdot(I_{dc}-I_{bias})+I_{bias},\ I_{bias}=I_{ac}\ \sin\varphi$$
$$i_{na}=i_{pa}\ -i_a, \omega t\in(\varphi,\pi/3)\,. \tag{11}$$

The CL currents of phase *b* and *c* could be calculated accordingly. And a similar procedure is applied during (π/3, 2π/3) as shown in Fig. 8. However, it should be noted that the designed CL current of phase *a* does not always hold to meet the requirement of *PZ* state. When PF becomes larger, $I_{\rm bias}$ becomes closer to $I_{\rm dc}$, and finally reaches the boundary as shown in Fig. 9(a). When $i_{\rm pa}$ is larger than $I_{\rm dc}$, $i_{\rm pc}$ which equals $I_{\rm dc}$-$i_{\rm pa}$, will become negative and phase *c* enters *ZZ* state. This case should be avoided and poses the limitation of (12) for method 1

$$I_{bias}=I_{ac}\sin\varphi<I_{dc}. \tag{12}$$

Substituting (5) into (12) yields

$$\frac{3M\cos\varphi}{4}-\sin\varphi>0, \varphi>\Rightarrow\frac{3M\cdot PF}{4}-\sqrt{1-PF^2}>0. \tag{13}$$

Therefore, the possible region for method 1 could be plotted in Fig. 9(b). It can be seen that the PF range is [0.8, 1], and the higher modulation index corresponds to lager PF range. As for the lagging PF, the *PN* state is also employed as shown in Fig. 10. Compared to the old method, method 1 uses only HB SM and behaves better in terms of the efficiency and modularity.

C. Method 2 of HMMR in Nonunity PF Operation

Different from method 1, method 2 utilizes the *ZZ* state to reshape the CL voltage. The single-phase CL waveforms of leading PF are presented in Fig. 11, and the three-phase connection is depicted in Fig. 12.

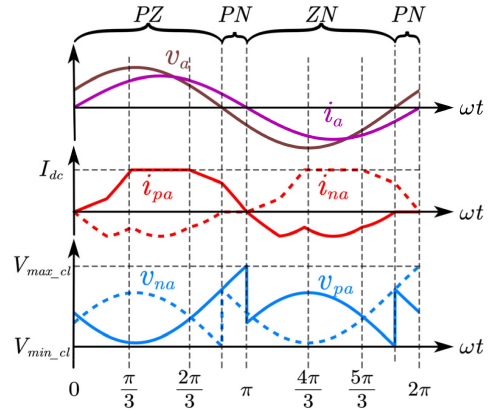

Fig. 10 Single-phase CL waveforms using method 1 at lagging PF.

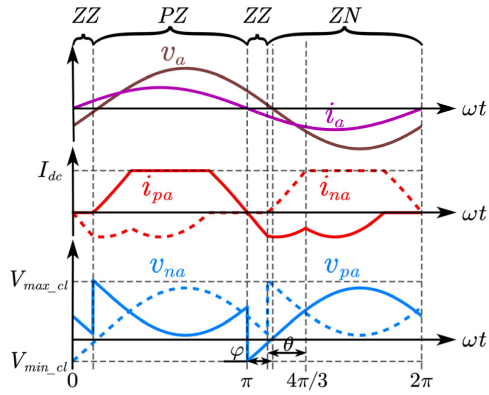

Fig. 11 Single-phase CL waveforms using method 2 at leading PF.

Similarly, two segments between (π, 5π/3) are taken as an example. When ωt is in the range of (π, π+φ), the polarities of ac voltage and current are opposite. First, it is intended for phase *a* work to *ZZ* state during the whole range of (π, π+φ) as the designed current below

$$i_{pa}=i_a\ <0, i_{na}\approx 0, \omega t\in(\pi,\pi+\varphi)\,. \tag{14}$$

According to the three-phase connection in Fig. 12, both positive and negative dc bus currents are supported by only single phase. Therefore, the CL currents of phase *b* and *c* could be derived easily in (15) based on the ac current constraint

$$\begin{cases} i_{pb}=I_{dc}\ >0,\ i_{nb}=I_{dc}\ -i_b<0 \\ i_{nc}=I_{dc}\ >0,\ i_{pc}=I_{dc}\ +i_c<0 \end{cases}. \tag{15}$$

The condition of $i_{\rm nb}<0$ is met naturally for $\omega t\in(\pi, \pi+\varphi)$, while phase *c* could yield the second constraint

$$i_{pc}=I_{dc}\ +I_{ac}\sin\left(\omega t+\frac{2\pi}{3}\right)<0$$
$$\Rightarrow\frac{\pi}{3}+\theta<\omega t<\frac{4\pi}{3}-\theta, \theta=\text{asin}\left(\frac{I_{dc}}{I_{ac}}\right). \tag{16}$$

Equation (16) gives the second constraint of ωt for negative $i_{\rm pc}$ during *ZZ* state of phase *a* to be (θ+π/3, 4π/3-θ). Once 4π/3-θ<π+φ, the *ZZ* state duration of phase *a* should be shortened to (π, 4π/3-θ) to avoid the case of positive $i_{\rm pc}$. Then during

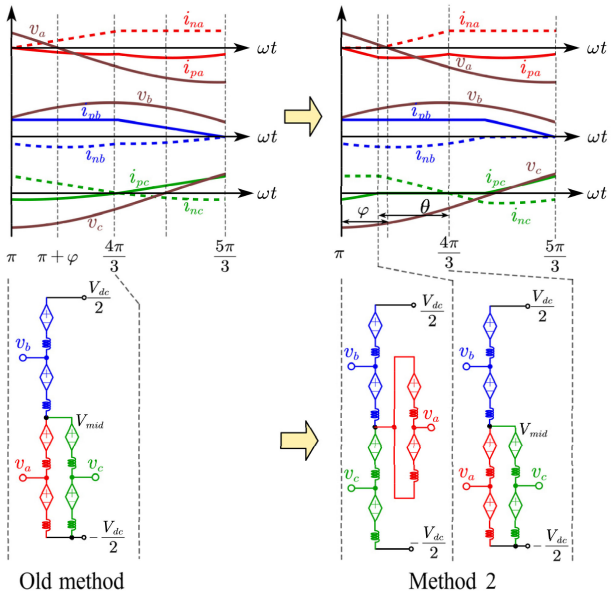

Fig. 12 Three-phase CL waveforms and transition of method 2 at leading PF.

$(4\pi/3\text{-}\theta,\ 4\pi/3)$, phase a switches to the ZN state and parallels with phase c to share the dc current. A ramp current shape in (17) is designed for this transition

$$i_{na} = \frac{\omega t - \left(\frac{4\pi}{3} - \theta\right)}{\theta} \cdot I_{dc} > 0$$
$$i_{pa} = i_{na} + i_a < 0, \omega t \in \left(\frac{4\pi}{3} - \theta, \frac{4\pi}{3}\right). \quad (17)$$

In this way, the CL voltage stress of method 2 becomes

$$V_{\max\_cl2} = 0.5V_{dc} + V_{ac}\sin(\gamma), \gamma = \theta + \varphi - \frac{\pi}{3}$$
$$V_{min\_cl2} = -V_{ac}\sin\varphi \quad (18)$$

where γ is the difference between $\theta+\varphi$ and $\pi/3$. Furthermore, this CL voltage rating can be further reduced by injecting a specific third harmonic voltage v_3. Equation (19) gives its expression, where the coefficient k_3 represents its magnitude normalized to the ac voltage

$$v_3 = k_3 \cdot V_{ac}\sin(3\omega t - 3\varphi)$$
$$v_a' = v_a - v_3. \quad (19)$$

Subtracting the third-order voltage has flattened the region of the zero crossing of the new ac voltage v_a' and accentuated the peak voltage. This is the opposite effect with the normally used third harmonic injection to flatten the peak voltage. As shown in Fig. 13, this injection has the benefits of lowering the voltage rating of the CLs, thus reducing the number of SMs required. In this way, the new maximum CL voltage stress $V_{\max\_cl2}'$ and minimum stress $V_{\min\_cl2}'$ become

$$V'_{\max\_cl2} = 0.5V_{dc} + V_{ac}\sin\gamma - k_3V_{ac}\sin(3\gamma)$$
$$V'_{min\_cl2} = -V_{ac}\sin\varphi + k_3V_{ac}\sin(3\varphi) \quad (20)$$

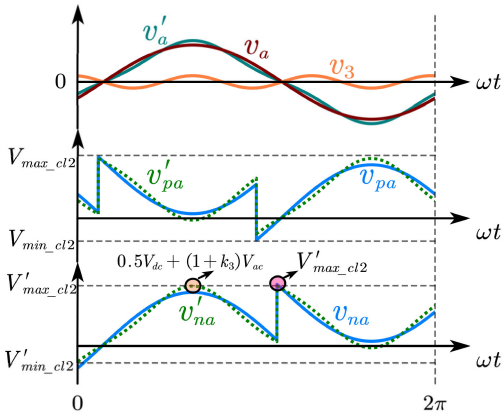

Fig. 13 Method 2 CL voltage after injecting third-order harmonic.

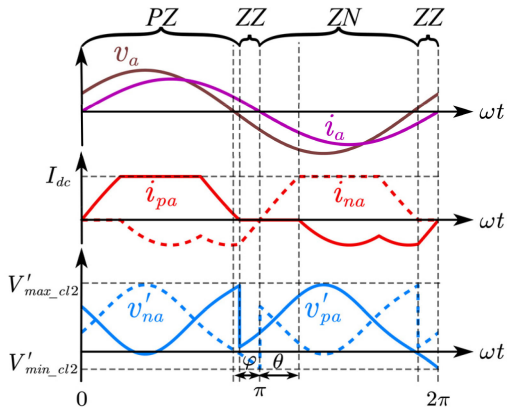

Fig. 14 Single-phase CL waveforms using method 2 at lagging PF.

TABLE I
COMPARISON OF CL VOLTAGE STRESS WITH THREE METHODS

Method	Maximum CL stress	Minimum CL stress
Original	$0.5V_{dc} + V_{ac}\sin\varphi$	$-V_{ac}\sin\varphi$
Method 1	$0.5V_{dc} + V_{ac}\sin\varphi$	0
Method 2	$0.5V_{dc} + V_{ac}\sin\gamma$ $-k_3V_{ac}\sin(3\gamma)$	$-V_{ac}\sin\varphi + k_3V_{ac}\sin(3\varphi)$

where k_3 should be designed to make sure the accentuated peak voltage does not exceed $V_{\max\_cl2}'$

$$0.5V_{dc} + (1 + k_3)V_{ac} \le V'_{max\_cl2}. \quad (21)$$

The k_3 meeting the equation of (21) has the best effect. As for the negative φ, a similar current allocation and third harmonic injection are designed as shown in Fig. 14. The summary of CL maximum and minimum voltage stresses with three methods are listed in Table I. It can be seen that method 1 reduces the minimum CL stress to 0, while method 2 reduces both values successfully.

D. Power Flow Analysis of Two Methods

The power flow analysis is important to reveal the inherent power relationship between ac, dc, and HMMR inner side, and help give the energy ripple tendency of two methods at different

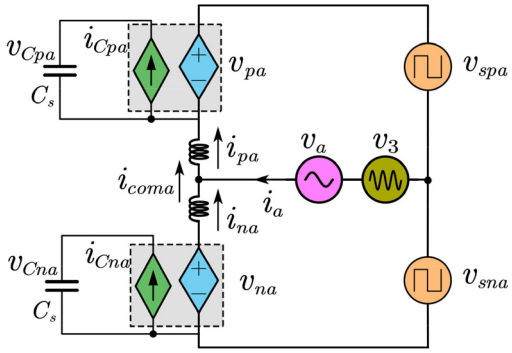

Fig. 15 Simplified average model of HMMR phase *a*.

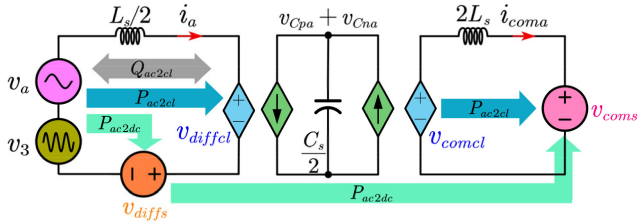

Fig. 16 Decoupling average model and power flow of HMMR phase *a*.

PFs. After neglecting the midpoint voltage and integrating the voltage source with HV diode, the average model could be derived as shown in Fig. 15. v_{spa} and v_{sna} refer to the equivalent top and bottom voltage sources in dc bus, respectively. Whereas the upper and lower CL dc-link capacitor voltages are denoted as v_{Cpa} and v_{Cna}. And the new capacitance C_{s} can be calculated as C_{sm}/N. The common-mode voltage v_3 is also given for clarification. Similar to the traditional MMC, Kirchhoff's voltage law could be applied to the upper and lower CLs as below

$$\begin{aligned} v_{spa} - v_{pa} + L_s\ (di_{pa}/dt) &= v_a\ + v_3 \\ -v_{sna} + v_{na} - L_s\,(di_{na}/dt) &= v_a\ + v_3. \end{aligned} \tag{22}$$

The addition and subtraction of two equations in (22) decompose two CL variables in the format of differential mode and common mode as in (23)

$$\begin{aligned} \frac{(v_{na}-v_{pa})}{2} + \frac{(v_{spa}-v_{sna})}{2} + \frac{L_s}{2}\frac{d\,(i_{pa}-i_{na})}{dt} &= v_a\ + v_3 \\ (v_{pa}+v_{na}) - (v_{sna}+v_{spa})\ &= L_s\,\frac{d\,(i_{pa}+i_{na})}{dt}. \end{aligned} \tag{23}$$

The differential and common mode variables are defined as

$$\begin{aligned} v_{diffs} &= \frac{(v_{sna}-v_{spa})}{2},\ v_{coms} = v_{spa}\ + v_{sna} \\ v_{diffcl} &= \frac{(v_{na}-v_{pa})}{2},\ v_{comcl} = v_{pa}\ + v_{na} \\ i_a &= i_{pa} - i_{na},\ i_{coma} = \frac{(i_{pa}+i_{na})}{2}. \end{aligned} \tag{24}$$

Then the new decoupling model could be depicted in Fig. 16. It can be observed that a new voltage source v_{diffs} is connected in series with CL voltage v_{diffcl} to follow the input ac voltage $v_{\mathrm{a}}+v_3$. While the dc side voltage source v_{coms} should be the sum of v_{pa} and v_{na}. Since the CL voltages have already been derived

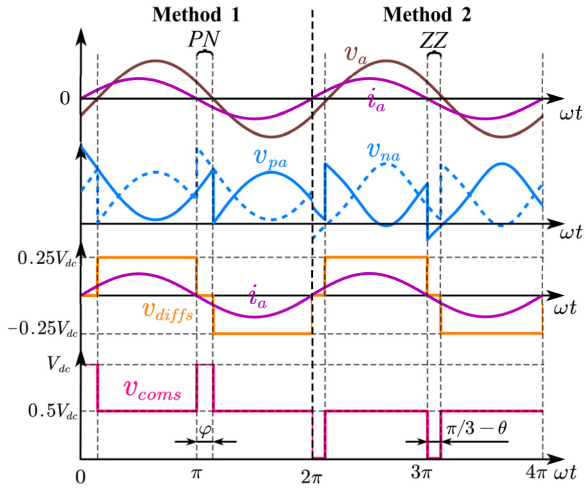

Fig. 17 Waveforms of voltage source with two different methods.

according to current allocation, the equivalent source v_{diffs} and v_{coms} could be calculated easily

$$v_{diffs} = (v_a + v_3) - v_{diffcl},\ v_{coms} = v_{comcl}. \tag{25}$$

Therefore, the source waveforms of v_{diffs} and v_{coms} with method 1 and 2 could be plotted in Fig. 17. It is interesting to find that the three-level wave of v_{diffs} aligns with the ac current i_{a}, and the duration of zero voltage in v_{diffs} equals to the lasting time of *PN* (or *ZZ*) state in method 1 (or 2). This implies that part of active power is delivered from the ac side to dc side directly, whose average value is denoted as P_{dc2ac}. And this power of method 1 could be obtained through integral in (26).

$$\begin{aligned} P_{dc2ac\_m1} &= \int_0^{2\pi} i_a v_{diffs} d\,(\omega t) = \frac{(1+\cos\varphi)\,I_{ac}V_{dc}}{4\pi} \\ &= \frac{V_{dc}I_{dc}}{3}\cdot\frac{1+\cos\varphi}{\pi M\cos\varphi}. \end{aligned} \tag{26}$$

The remaining active power is delivered via CL named P_{dc2cl}, while the reactive power Q_{ac2cl} is circulated between ac side and CL. At the unity PF and M of 1, it can be calculated that P_{ac2dc} about 63.7% (2/π) of total power. While the dc-link capacitor energy ripple of the CL E_{cl} could be calculated as

$$E_{cl} = \int v_{cl} i_{cl} dt. \tag{27}$$

The reduction of average active power indicates that the CL energy fluctuation of HMMR ΔE_{cl} could be reduced compared to MMC, which matches with the 50% reduction energy storage requirement at unity PF [27]. It is worth mentioning that the reactive power also involves and changes the CL current pattern at the nonunity PF. Therefore, the quantitative equation of ΔE_{cl} related to PF is not given here. But the results obtained from the numerical calculation will be shown in Section III. As for method 2, the power term P_{dc2ac} is

$$P_{dc2ac\_m2} = \frac{\left[1+\cos\left(\frac{\pi}{3}-\theta\right)\right]I_{ac}V_{dc}}{4\pi}. \tag{28}$$

Therefore, method 2 should have a lower energy ripple than MMC, too.

TABLE II
SPECIFICATIONS OF HMMR BASED HVDC CONVERTER

Description	Symbol	Value
Ac Line-voltage (RMS)	V_{LL_rms} (kV)	115
Ac frequency	f_{in} (Hz)	60
Output DC bus voltage	V_{dc} (kV)	200
Rated power	S (MVA)	200
PF	PF	0.9~1
SM capacitor voltage	$V_{SM}{}^*$ (kV)	2.3
SM capacitor ripple	ε	10%
SM IGBT	FZ825R33HE4D	3.3 kV / 825 A
HV diode	W0880LC720	7.2 kV / 880A

III. COMPARISON BETWEEN MMC AND HMMR

As explained earlier, the biggest advantage of HMMR is the reduced devices and capacitors. In order to perform a fair comparison between two methods at nonunity PF, designing the converters under different operating conditions is necessary. An HVdc case is performed and the electrical parameters are listed in Table II. In this case, the modulation index is fixed at 0.94, and the PF range is 0.9–1 which satisfies the effective region of method 1 in Fig. 9(b). It should be noted that lower PF operation is still possible for HMMR, but more SM should be added and mitigate the benefit of HMMR. Therefore, this article focuses on the high PF range.

A. Device Number

In this article, the Infineon 3.3 kV 825A IGBT module (FZ825R33HE4D) [31] is used for the SM. And 7.2-kV 880 A press-pack diode W0880LC720 [32] from IXYS is selected for the diode stack due to less device number. The device number used in HMMR is directly related to the CL voltage stress.

The number of SMs in each CL is selected so that the dc-link capacitor voltage $V_{\mathrm{SM}}{}^*$ does not exceed 2.3 kV, and the FB SM number should be sufficient to provide the negative voltage. Following Table I, the required SM number could be calculated as in the following equation:

$$N_{h\_MMC} = \frac{V_{dc}}{V_{SM}^*}$$
$$N_{h\_m1} = \frac{0.5 * V_{dc} + V_{ac}\sin\varphi}{V_{SM}^*}$$
$$N_{f\_m2} = \frac{\left|V'_{min\_cl2}\right|}{V_{SM}^*},\ N_{h\_m2} = \frac{V'_{max\_cl2}}{V_{SM}^*} - N_{f\_m2}. \tag{29}$$

The voltage stress for the diode stack is $0.5V_{\mathrm{dc}}$, and the required device number of traditional MMC, HMMR method 1 and 2 at different PF are given in Fig. 18. Noted that the device number is rounded up, so the curve is not smooth.

It can be seen that HMMR could achieve half IGBT reduction compared to the traditional MMC at the unity PF. Since the diode module is a passive device, the gate driver unit and sensor number are reduced as well. When the PF is 0.9, the additional device number is still lower than that of MMC. With the help of a third harmonic injection, the device number of method 2 is similar to method 1.

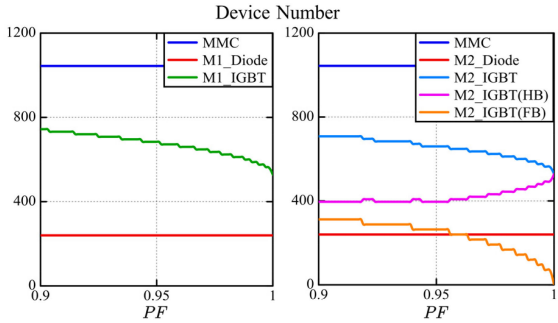

Fig. 18 Device number used in MMC and HMMR with two methods.

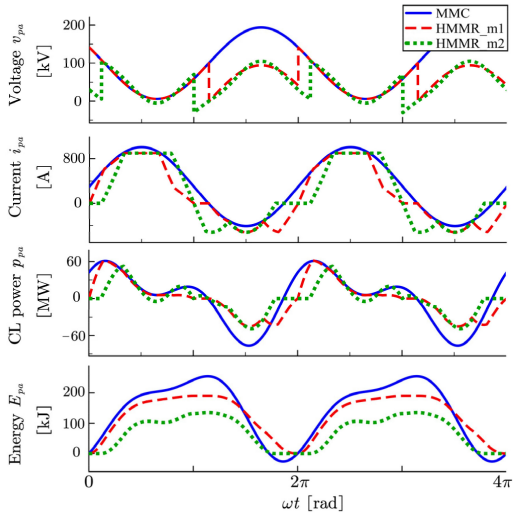

Fig. 19 CL waveforms of MMC and HMMR with two methods at 0.9 PF.

B. Capacitor Size

Capacitors in MMC are one of the most important factors affecting the power density and cost. HMMR could reduce the SM number successfully, but the capacitance value is still unknown. The capacitor energy storage requirement per unit apparent power E_{unit} is related to the energy deviation ΔE_{cl} and the capacitor voltage ripple coefficient ε [19], [27], [29]

$$E_{unit} = 6N\,\frac{C_{SM}{V_{SM}^*}^2}{2S} = \frac{3\Delta E_{cl}}{2\varepsilon S}\,. \tag{30}$$

Two HMMR methods have different instantaneous CL power, which also varies at different PFs. Due to the symmetric characteristics of the two topologies, only the upper CL waveforms of phase *a* are discussed here. According to the aforementioned equations, CL voltage, current, power, and energy variations of PF = 0.9 are plotted in Fig. 19. It can be seen that the integration of CL power during one fundamental period is zero, which proves the natural CL energy balancing.

In order to get a clearer relationship between CL variables and PF. The CL current RMS value and the required E_{unit} with $\varepsilon = 10\%$ are presented in Fig. 20. Obviously, both methods have lower CL current than the traditional MMC, which implies lower semiconductor losses. Besides, they also possess lower CL energy ripple in the PF range of 0.9–1. Especially method 2

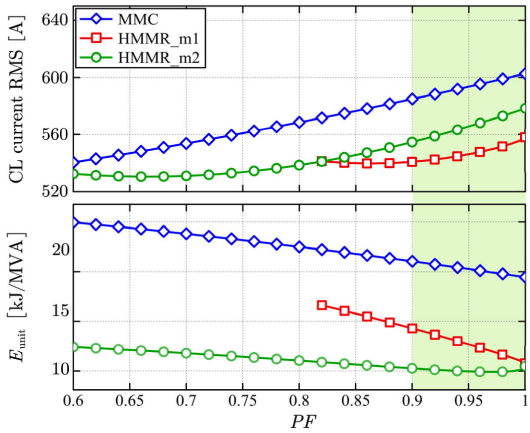

Fig. 20 CL current and energy ripple versus PF.

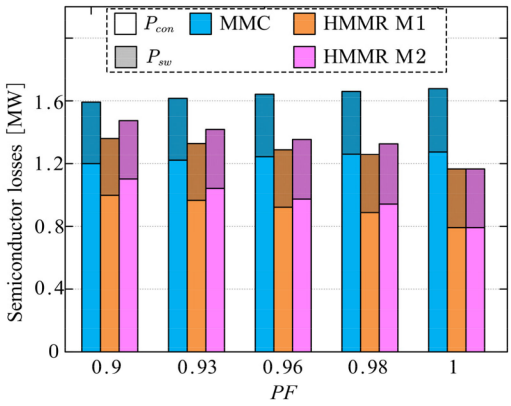

Fig. 21 Power losses in MMC and HMMR with two methods.

can achieve half reduction in the entire range. This conclusion matches the previous analysis. Therefore, the energy storage requirement will be smaller than MMC with the same ε according to (30).

C. Semiconductor Losses

In order to compare the converters from an efficiency point of view, conduction and switching losses for semiconductors are calculated here. The conduction loss is caused by the forward voltage drop of IGBTs and diode stacks, which are considered for the following calculations [33]. For simplification, the on-state voltage drop of IGBT and its antiparallel diode are assumed to be the same. Then the conduction losses for 6 CLs in MMC and HMMR can be calculated as

$$P_{con\_cl} = \frac{6}{2\pi} \int_0^{2\pi} \left(N_d \cdot v_{f\_IGBT} \cdot |i_f|\right) d\left(\omega t\right) \tag{31}$$

where N_{d} is the number of devices in the conduction path of each CL, v_{f_IGBT} refers to the on-state voltage drop of IGBT, and i_{f} denotes the current through the CL.

As for the diode stacks, $D_{1\mathrm{a}}$ and $D_{2\mathrm{a}}$ conduct the current i_{pa} alternately. Therefore, the conduction loss of two diode stacks can be combined and calculated similar to CL

$$P_{con\_diode} = \frac{6}{2\pi} \int_0^{2\pi} \left(N_{diode} \cdot v_{f\_diode} \cdot |i_f|\right) d\left(\omega t\right) \tag{32}$$

where N_{diode} is the number of devices in the conduction path of each CL, v_{f_diode} refers to the on-state voltage drop of diode.

Any SM operation state change corresponds to one-time turn-ON loss e_{on}, turn-OFF loss e_{off} of IGBT and reverse recovery loss e_{rec} of antiparallel diode. The SM capacitor ripple is neglected for to calculate the equivalent value normalized to the reference voltage $v_{\mathrm{CE,ref}}$ in datasheet. Then the switching losses are added within one fundamental output time period

$$P_{sw\_cl} = \frac{\omega}{2\pi} \sum_{\gamma=1}^{N_{sw}} \left\{ \frac{V_{SM}}{v_{CE,ref}} \cdot e_{on(off)}\left(i_f\right) + \frac{V_{SM}}{v_{F,ref}} \cdot e_{rec}\left(i_F\right) \right\}. \tag{33}$$

TABLE III
OVERALL CONVERTER COMPARISON BETWEEN HMMR AND MMC AT PF OF 0.9

Topology	MMC	HMMR (m1)	HMMR (m2)
Device number	1 p.u.	0.71 p.u. (CL) + 0.2 p.u. (diode)	0.68 p.u. (CL) + 0.2 p.u. (diode)
Capacitor	1 p.u.	0.68 p.u.	0.49 p.u.
Arm current	1 p.u.	0.93 p.u.	0.95 p.u.
Device losses	1 p.u.	0.85 p.u.	0.93 p.u.

For the HV diode stack, which is turned off naturally at zero current, the reverse recovery loss should be zero. Fig. 21 shows the total losses variation of one CL at different PF. The conduction losses are strongly related to the CL RMS current. Benefiting from the HV 7.2 kV diode, the conduction losses of HMMR are reduced a lot from MMC. Due to the larger CL current RMS value, method 2 of HMMR has larger total losses compared to method 1.

Above all, the converter parameter of two HMMR methods based on per-unit of MMC are listed in Table III. Method 1 requires only HB SM and has higher modularity, lower losses. Whereas method 2 must use FB SM and has lower capacitor, and part dc fault tolerant capability.

D. Fault Analysis and Redundant Operation

The proposed HMMR belongs to the family of VSCs despite the presence of diodes. Therefore, it does not require a strong ac grid to operate and can ride through ac faults if an appropriate control technique is utilized [34]. For the symmetrical ac fault, the active power could be reduced accordingly. There will be no current ripple in dc side due to the absence of negative sequence components.

However, the asymmetrical fault poses a control challenge owing to the shortage of control freedom [35]. Since the dc side current is synthesized by three-phase independently, the power dip of one phase will cause a large dc current ripple. If the three-phase power are controlled the same, the ac side current will not be balanced. The ac fault operation is a very complicated topic and will not be discussed comprehensively in this article.

Similar to the traditional HB-MMC, HMMR with only HB SM does not have dc fault capability. The fault current will rise quickly through the antiparallel diode of IGBT module.

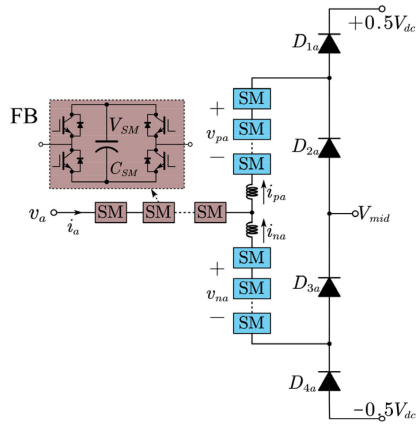

Fig. 22 HMMR with ac FB SMs for the dc fault blocking.

Therefore, the arm inductor should be designed to limit the current rise rate, and the HV dc circuit breaker is necessary to protect the system [36]. The thyristor inside each SM can protect it from the over current damage [37]. While the press-pack diode has a much higher surge current capability, which can withstand the overcurrent before the opening of the circuit breaker. In another aspect, the FB-MMC and FB-HMMR have the intrinsic dc fault tolerant capability. From this point of view, the method 2 with extra FB SM can help reduce total SM number if FB SM is employed for dc fault.

In order to have the full dc fault blocking capability (e.g., pole-pole fault), all devices in each FB SMs should be switched off. As a result, the dc-link capacitors of the FB SMs in each arm appear as the serially connected voltage sources and have the opposite polarity of the direction of the fault current flown from the ac side. Since two arms are connected in series, the FB number should be

$$N_{FB\_dc\_fault} = \frac{\sqrt{2}V_{ac}}{(2V^*_{SM})} \tag{34}$$

where V_{ac} is the line-to-line rms voltage. In fact, if HMMR is designed with full dc fault blocking capability, moving FB SMs to the ac terminal in Fig. 22 shows better performance. Because only half of the additional FB SMs will be required for each phase, but the steady-state conduction losses will be higher.

The redundant operation is also very important for this kind of modular topology. The series HV diode stack can use the press-pack diode construction, whose short circuit failure mode allows for the design of redundancy [38]. As for the CL part, the redundant SMs in hot reserve or cold reserve operation modes have been proposed [39], [40], thus not discussed here.

IV. Control Method and Simulation Results

In order to validate the functionality of the proposed methods of HMMR, an HVdc simulation model of 200 MVA is developed with the main circuit parameters listed in Table II. The structure and control block diagram are presented in Fig. 23(a). The output side of HMMR is connected to a dc source.

The key part of the HMMR control scheme in Fig. 23(b) is obtaining the six CL current references, which can be categorized into three parts: ac side component, dc side component,

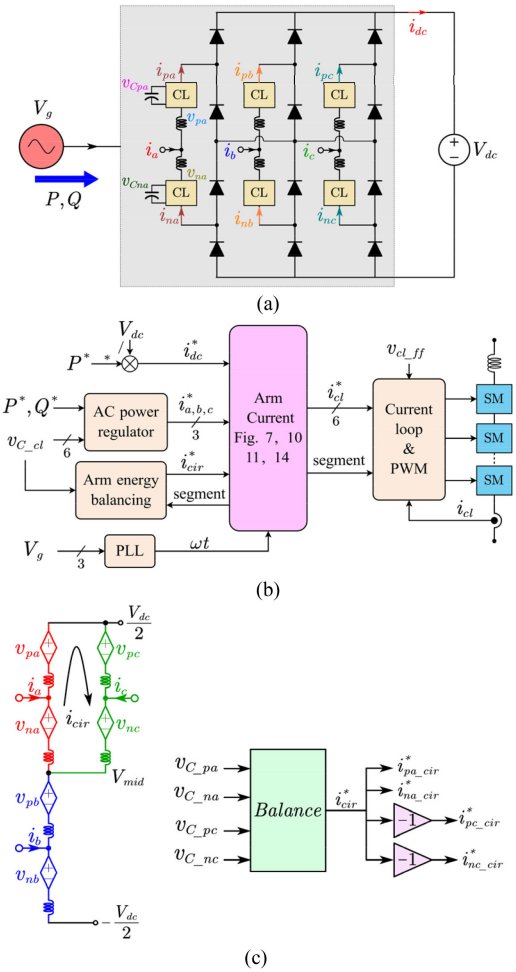

Fig. 23 (a) Simulation circuit of HMMR-HVDC system, (b) block diagram of overall control structure, (c) CL capacitor voltage balancing method.

and circulating component. The active current in the ac side component is responsible for charging the SM capacitors, hence determined by average capacitor voltage feedback control and the active power regulator. While the reactive power regulator generates the phase angle φ and combines with an active current to get full ac component. And the circulating component depends on the unbalanced distribution of CL capacitor voltage. The example of first segment is discussed here. As shown in Fig. 23(c), phase a and phase c are connected in parallel, which means a circulating current can be injected manually with arbitrary frequency and amplitude. By exchanging energy among four CLs, the CL capacitor voltage equalization can be achieved eventually [41], [42].

Fig. 24 shows the steady-state operation of HMMR at unity PF and full power. It can be seen that the ripple of dc side current $i_{\rm dc}$ in Fig. 24(c) is pretty small, which is expected after employing the trapezoidal CL current shown in Fig. 24(c) and (d). The multilevel CL voltage is presented in Fig. 24(f), which validates the half of voltage stress reduction. Fig. 24(g) is the CL capacitor voltage, which is stabled at the rated value and indicates the effectiveness of the capacitor voltage balancing scheme.

In order to validate the operation methods of HMMR at nonunity PF, method 1 is applied first with positive and negative

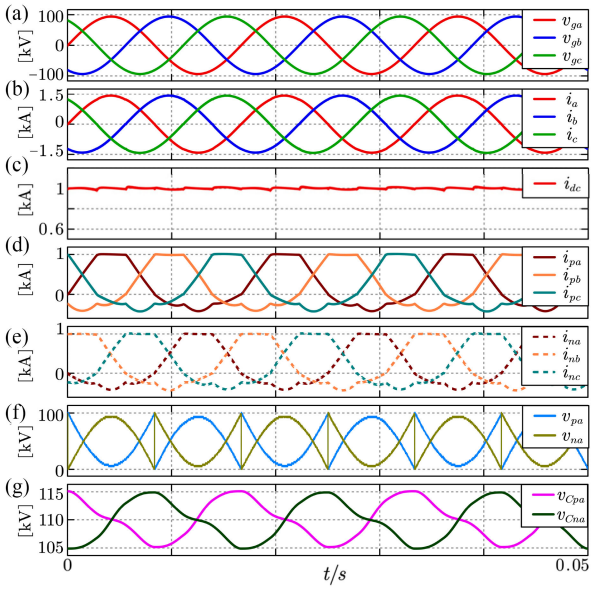

Fig. 24 Steady-state simulation waveforms of HMMR at unity PF. (a) AC grid side voltages. (b) AC side currents. (c) DC side current. (d) Three-phase upper CL currents. (e) Three-phase lower CL currents. (f) Phase a upper and lower CL output voltages. (g) Phase a upper and lower CL capacitor voltages.

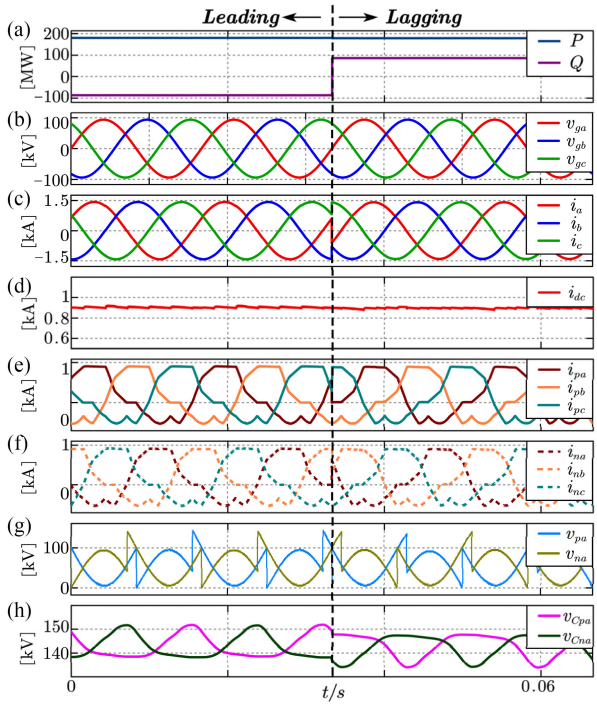

Fig. 25 Steady-state simulation waveforms of HMMR at 0.9 PF with method 1. (a) Delivered active and reactive power. (b) AC grid side voltages. (c) AC side currents. (d) DC side current. (e) Three-phase upper CL currents. (f) Three-phase lower CL currents. (g) Phase a upper and lower CL output voltages. (h) Phase a upper and lower CL capacitor voltages.

phase angle φ. The PF is set to be 0.9, so the active power is reduced to 180 MW in Fig. 25(a) and the dc side current changes to 900 A. The upper and lower CL currents as shown in Fig. 25(e) and (f) are designed to maintain the constant dc current and the sinusoidal ac current. In method 1, the *PN* state is utilized for the current commutation. As the result, the maximum CL voltage is higher than $0.5V_{\rm dc}$, and more HB SMs are connected to support higher CL voltage. And the sum of CL capacitor voltage in Fig. 25(h) is also higher than that of the unity PF case.

The same condition is also applied to HMMR with method 2. Different from method 1, method 2 utilizes *ZZ* state instead. The upper and lower CL currents in Fig. 26(e) and (f) are designed with different shape, and extra FB SMs are connected to support negative CL voltage in Fig. 26(g). And the third-order harmonic voltage in Fig. 26(h) is injected to flatten the voltage zero-crossing region so that the SM number could be reduced.

The dynamic performance of active power change with method 1 is shown in Fig. 27. When $t = 0.1$ s, the reactive power reference is changed from -87 to 87 MVAr, and the total apparent power keeps constant during the whole process. It can be seen that the CL voltage stress in Fig. 27(e) is larger when the PF is smaller, because the duration of *PN* state is shorter. The amplitude of the CL capacitor voltage ripple is also proportional to the delivered reactive power as shown in Fig. 27(f). This waveform matches the theoretical results in Fig. 20.

To test the proposed topology and control in the event of an ac grid fault, a symmetrical solid fault is applied to the ac side at $t = 0.1$ s and is cleared after 0.2 s. As shown in Fig. 28(b), the grid voltage of the drops to 0.1 p.u. after fault occurs. Then the output power of the HMMR is reduced to 0.1 p.u. accordingly and the three-phase ac current will keep the same as shown in

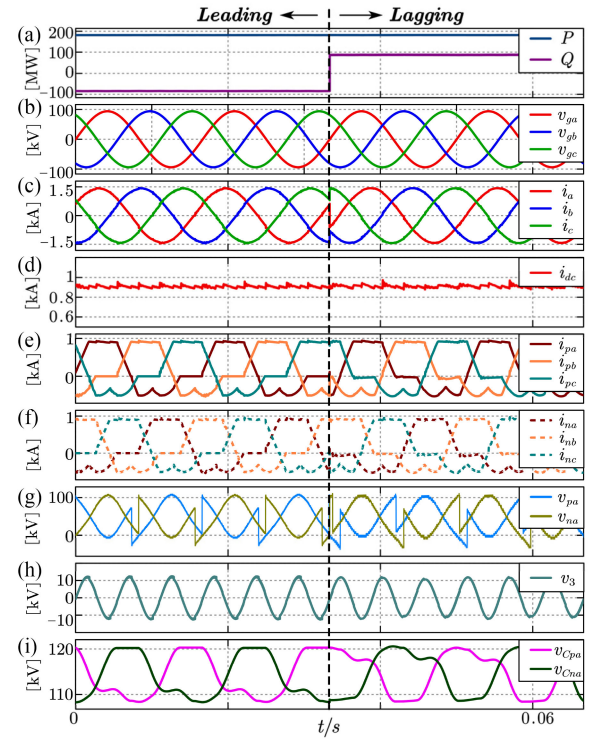

Fig. 26 Steady-state simulation waveforms of HMMR at 0.9 PF with method 2. (a) Delivered active and reactive power. (b) AC grid side voltages. (c) AC side currents. (d) DC side current. (e) Three-phase upper CL currents. (f) Three-phase lower CL currents. (g) Phase a upper and lower CL output voltages. (h) Injected third-order harmonic voltage. (i) Phase a upper and lower CL capacitor voltages.

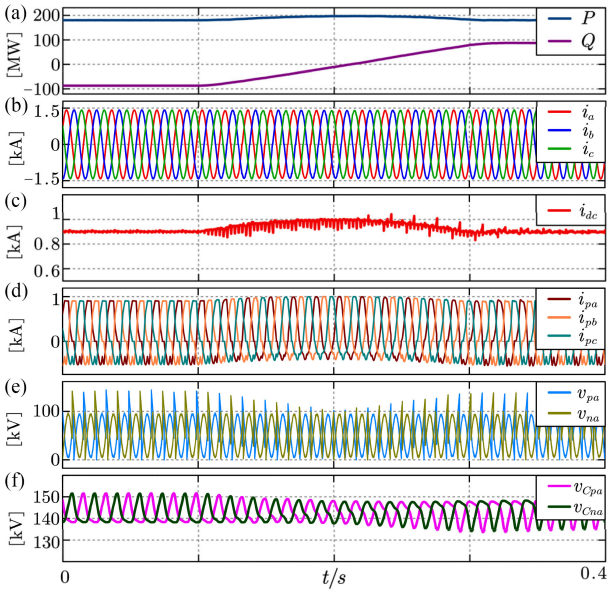

Fig. 27 Dynamic response to the change in reactive power commands with method 1. (a) Delivered active and reactive power. (b) AC side currents. (c) DC side current. (d) Three-phase upper CL currents. (e) Phase *a* upper and lower CL output voltages. (f) Phase *a* upper and lower CL capacitor voltages.

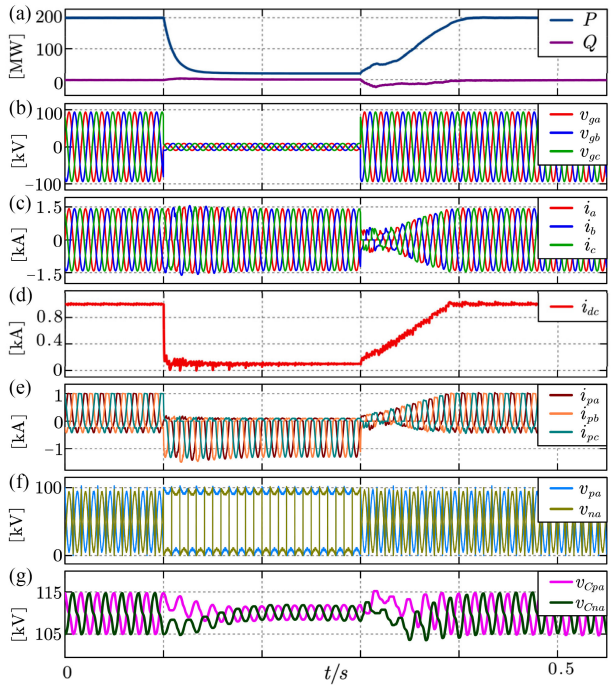

Fig. 28 Waveforms during the ac fault. (a) Delivered active and reactive power. (b) AC grid voltage. (c) AC side currents. (d) DC side current. (e) Three-phase upper CL currents. (f) Phase *a* upper and lower CL output voltages. (g) Phase *a* upper and lower CL capacitor voltages.

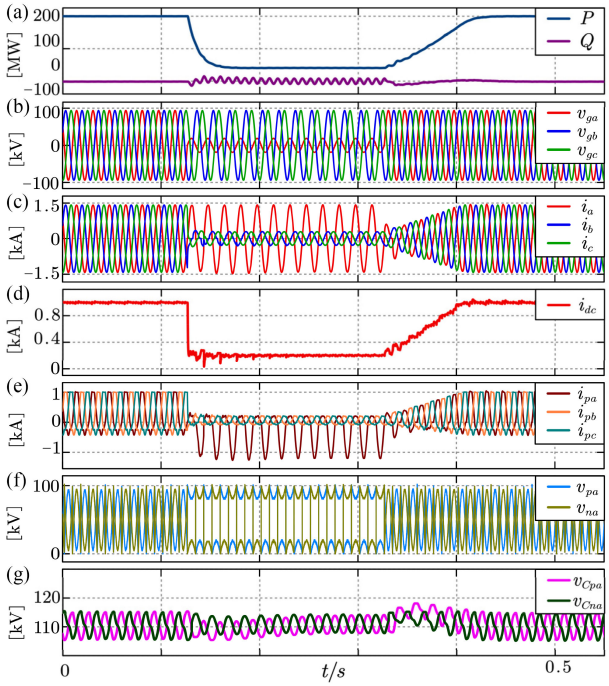

Fig. 29 Waveforms during the ac fault. (a) Delivered active and reactive power. (b) AC grid voltage. (c) AC side currents. (d) DC side current. (e) Three-phase upper CL currents. (f) Phase *a* upper and lower CL output voltages. (g) Phase *a* upper and lower CL capacitor voltages.

TABLE IV
ELECTRICAL PARAMETERS OF 3L-HMMC SYSTEM

Parameters	Symbol	Values
Ac voltage amplitude (phase)	V_o	180 V
Rated ac frequency	f_o	60 Hz
Dc bus voltage	V_{dc}	400 V
CL inductance	L_{CL}	3 mH
SM voltage	V_{CSM}	85 V
SM capacitance	C_{SM}	1.32 mF
Number of HB SM per CL	N_h	3
Number of FB SM per CL	N_f	1
Equivalent switching frequency	f_c	14.4 kHz
Power factor	PF	0.95

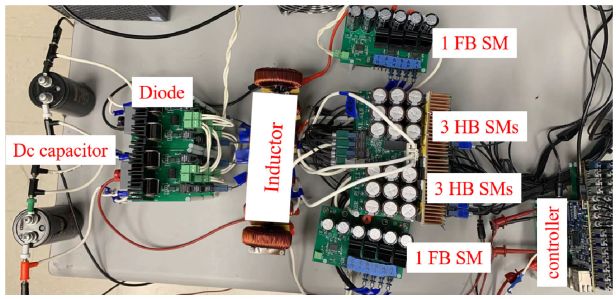

Fig. 30 Picture of laboratory HMMR prototype.

Fig. 28(c). The amplitude of dc side current in Fig. 28(d) drops to 0.1 p.u. as well. After the clearance of ac fault at $t = 0.3$ s, the power transmission resumes and the system autonomously restores normal operation with a soft start. During the whole process, the CL capacitor voltage in Fig. 28(g) is balanced pretty well.

As for the asymmetrical ac fault, HMMR can still handle it. As shown in Fig. 29, the phase *a* voltage in Fig. 29(b) drops to 0.2 p.u. at $t = 0.12$ s, while phase *b* and phase *c* voltage do not change. In order to achieve the balanced three-phase power, the ac currents of phase *b* and phase *c* reduces to 0.2 p.u. as well. It can be observed that the second-order harmonics appear in the

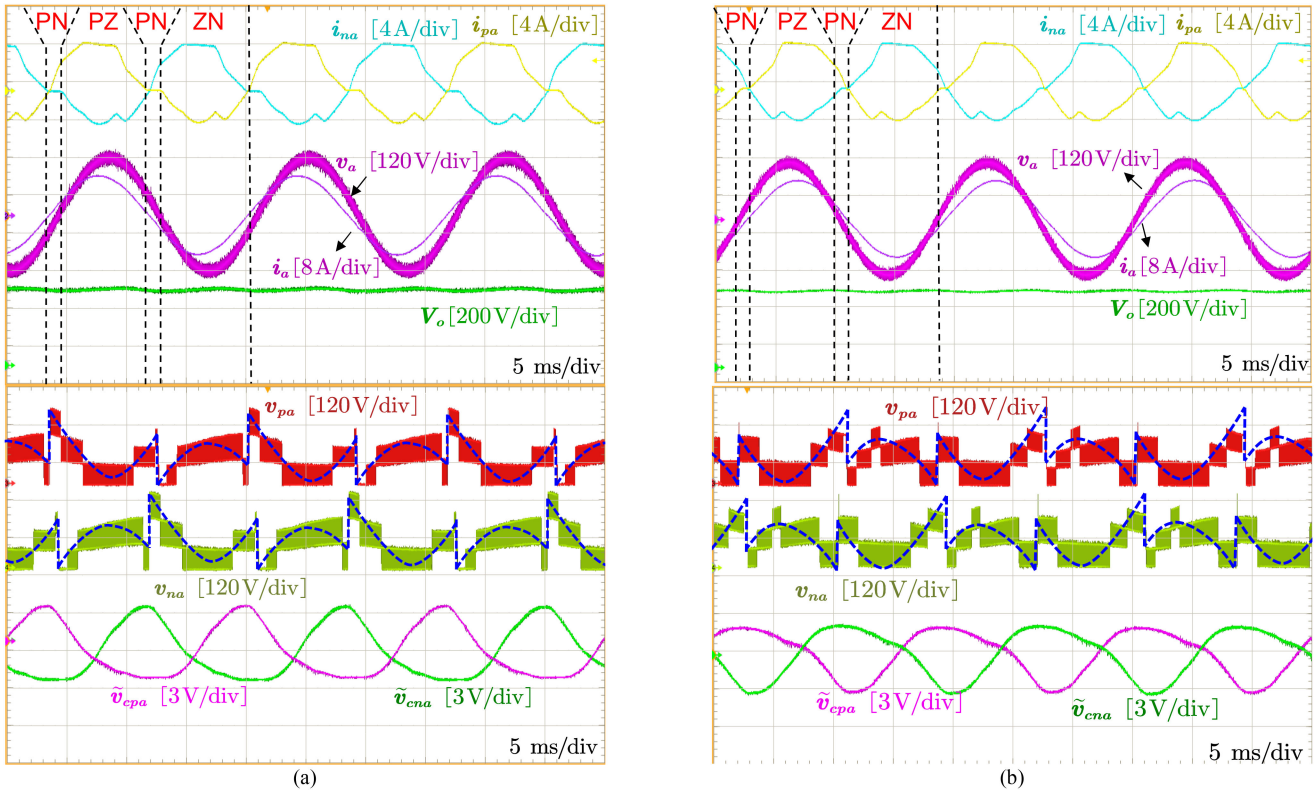

Fig. 31 Steady-state waveforms of HMMR with method 1. (a) Leading PF. (b) Lagging PF.

reactive power due to the negative sequence components. At $t = 0.32$ s, the ac fault is cleared, and the system returns back to the normal operation again.

V. Experimental Results

The working principle and performance of the proposed HMMR are also validated using a laboratory prototype with the other circuit parameters as listed in Table IV and the setup is shown in Fig. 30. The dc side uses resistor as the load, and the whole system is controlled by digital signal processor TMS320F28388. Each CL has three SMs, which are three HB SMs for method 1 and two HB SMs plus one FB SM for method 2 to verify the nonunity PF operation. The SM capacitor and CL currents sampling results are sent back to the controller through SPI communication. Results and key observations obtained using this prototype during steady state and transient conditions are provided to confirm the operating principles and control schemes of HMMR.

The steady-state results with method 1 are shown in Fig. 31 . As explained earlier, the working states of one cycle consist of *PN*, *PZ*, and *ZN* states. The four-level CL voltage is generated by the phase-shift modulation of reference voltage. Capacitor voltage of an HB SM in upper and lower CLs are shown as well, which are regulated around its nominal value and the effectiveness of the proposed control method is substantiated. The ac side current is perfectly sinusoidal as desired, which indicates the good design of the current loop parameters.

Similarly, the results obtained with method 2 are shown in Fig. 32. Since *ZZ* state is inserted between *PZ* and *ZN* states, an FB SM is connected in series to replace one HB SM. The capacitor voltage waveform of FB is different from HB, because only FB provides the negative voltage during *ZZ* state. But their voltage will be balanced during *PZ* and *ZN* state with the help of individual voltage balancing control. The converter operates as expected at both methods and provides satisfactory performance. These results obtained from the hardware prototype agree with the simulation results presented in the previous section.

In order to evaluate the performance of the control scheme during transients, the capacitor voltage reference is instantly increased from 80 to 115 V and key waveforms obtained are presented in Fig. 33. Due to the existence of capacitor average voltage control, the ac component of CL current will increase immediately. As a result, the ac side current will be higher for a short time, and the capacitor will be charged to the new reference. Since the total active power does not change, the ac and CL currents will be the same in the new steady state.

To further verify the ability of HMMR to handle sudden transients in voltage, the output dc voltage reference is suddenly altered from 360 to 420 V and the corresponding results are given in Fig. 34. Since the load resistor keeps constant, the total power will be larger if dc voltage is higher. Therefore, it can be seen the CL and ac currents amplitude increases proportionally. The amplitude of capacitor voltage fluctuation becomes higher as well due to the delivered larger power. The converter operates stably for the aforesaid transients and desired results are obtained. Hence, the feasibility of HMMR and its working

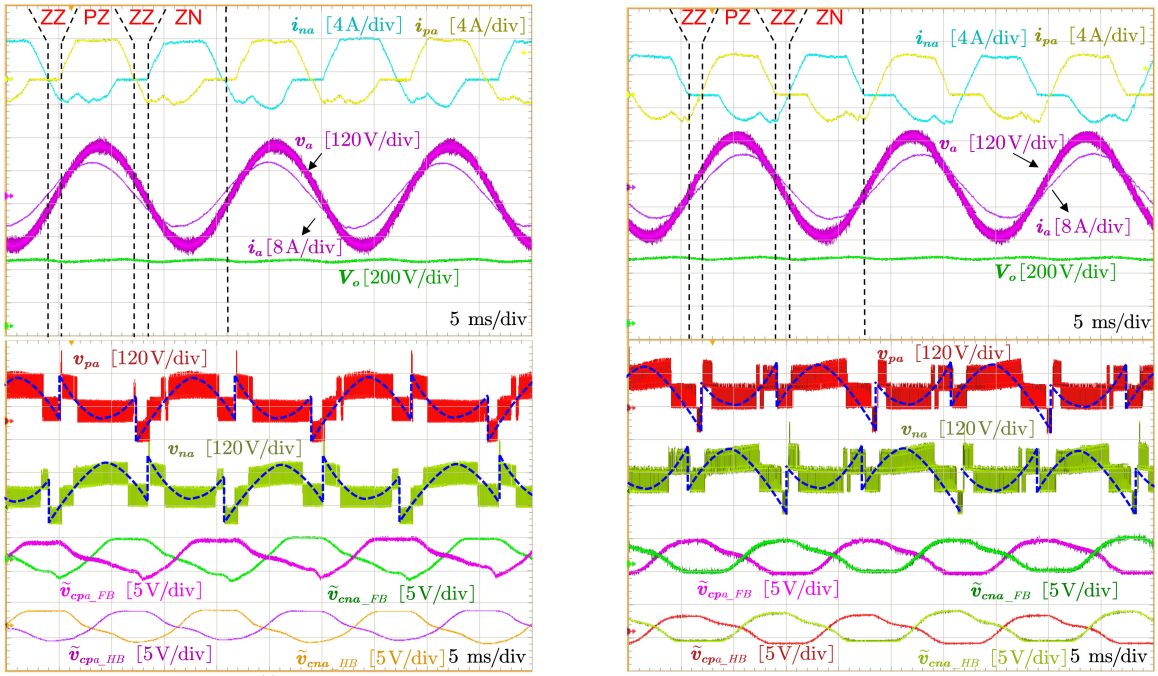

Fig. 32 Steady-state waveforms of HMMR with method 2. (a) Leading PF. (b) Lagging PF.

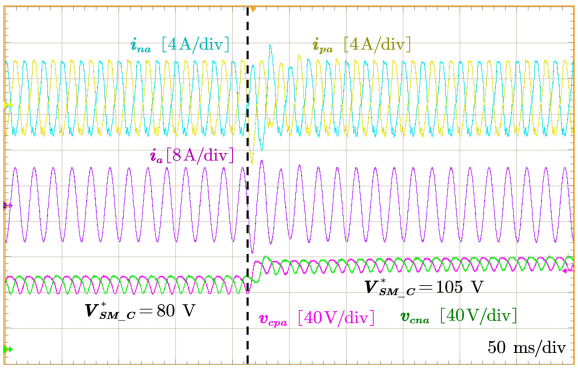

Fig. 33 Dynamic response of HMMR to the change of capacitor voltage reference with method 1.

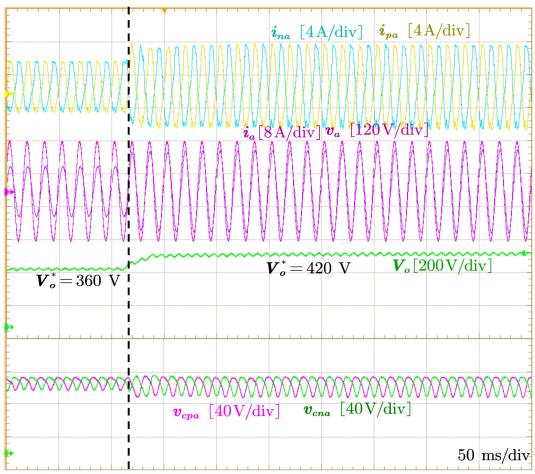

Fig. 34 Dynamic response of HMMR to the change of output dc voltage reference with method 1.

principle are verified using the experimental setup and are found to be in agreement with the above-mentioned theoretical analysis and simulation studies.

VI. Conclusion

HMMR is a unidirectional ac–dc converter intended for MV and HV ac–dc applications without reverse power flow. For HVdc or other transmission grid applications, nonunity PF operation is important for the rectifier to deliver some amount of reactive power and support the grid during the low-voltage transient and weak grid conditions. Two operational methods are presented in this article to reduce the required number of SM in the leading and lagging PF operation of HMMR. The key concept is to insert *PN* or *ZZ* state between *PN* and *NZ* state as the transition. Method 1 requires only HB SM but has the limited operation range. Whereas method 2 must use FB SM but offers part dc fault tolerant capability. Besides, the third-order harmonic is injected to further reduce the SM number of method 2. It is found that both methods can successfully reduce 0.3 p.u. LV device compared to MMC at PF of 0.9. As for the energy storage requirement, the derived average model shows that partial power is delivered from the ac to dc side through the diode directly. As a result, method 1 can reduce 32% capacitor and method 2 achieves a 52% reduction compared to the traditional MMC. Besides, benefiting from the low conduction loss of the HV diode, the efficiency of HMMR is also higher than MMC. Since HMMR is a VSC, it does not require a strong ac grid to operate and can ride through the ac faults similar to MMC. Above all, HMMR is a good candidate to replace MMC in MV/HV rectifier applications to realize higher power density and efficiency.

APPENDIX

The trapezoidal current allocation at unity PF is shown in Fig. 4, and the equation of CL current i_{pa} and voltage v_{pa} could be expressed as

$$i_{pa}=\begin{cases} I_{dc}\cdot\frac{\omega t}{\left(\frac{\pi}{3}\right)}, \omega t\in\left[0,\frac{\pi}{3}\right) \\ I_{dc}, \omega t\in\left[\frac{\pi}{3},\frac{2\pi}{3}\right) \\ I_{dc}-I_{dc}\cdot\frac{\left(\omega t-\frac{2\pi}{3}\right)}{\left(\frac{\pi}{3}\right)}, \omega t\in\left[\frac{2\pi}{3},\pi\right) \\ I_{dc}\cdot\frac{(\omega t-\pi)}{\left(\frac{\pi}{3}\right)}+i_a, \omega t\in\left[\pi,\frac{4\pi}{3}\right) \\ I_{dc}+i_a, \omega t\in\left[\frac{4\pi}{3},\frac{5\pi}{3}\right) \\ I_{dc}-I_{dc}\cdot\frac{\left(\omega t-\frac{5\pi}{3}\right)}{\left(\frac{\pi}{3}\right)}+i_a, \omega t\in\left[\frac{5\pi}{3},2\pi\right) \end{cases} \tag{35}$$

$$v_{pa}=\begin{cases} 0.5V_{dc}-v_a, \omega t\in[0,\pi) \\ -v_a, \omega t\in[\pi,2\pi) \end{cases}. \tag{36}$$

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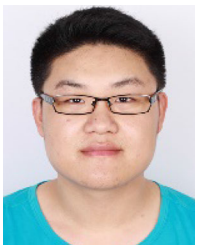

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