An Efficiency-Improved Single-Phase PFC Rectifier With Active Power Decoupling

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***Abstract*—Active power decoupling (APD) technology is an effective solution to store the double-line frequency ripple power in the single-phase system and remove the bulky aluminum electrolytic capacitors. However, APD introduces power loss because of adding extra switches operating at high frequency, which hurts the system efficiency inevitably. Addressing this issue, this article proposes an improved boost power factor correction (PFC) rectifier with a buck-type APD cell. An auxiliary circuit, composed of a resonant inductor and a diode, is added. With the developed modulation strategy, zero voltage switching of the switches both in the PFC and APD circuits is achieved, which improves the system efficiency significantly. This article first describes operating modes and then analyzes the soft-switching condition of each switch. Finally, a 300 W prototype is built and the experimental result shows that the efficiency is increased by 4%.**

***Index Terms*—Active power decoupling (APD), power factor correction (PFC), single-phase ac/dc converter, zero voltage switching (ZVS).**

I. Introduction

SINGLE phase power factor correction (PFC) rectifiers have been widely used in low- and medium-power applications [1]. Among them, the boost PFC converter is a popular choice because of the simple circuit structure and effective shaping-current ability [2]. However, to store the inherent double-line frequency ripple power, aluminum electrolytic capacitors (Al E-caps) are needed [3]. They increase the volume and degrade the reliability of the system [4], which is not expected.

Active power decoupling (APD) is confirmed to be an effective method to cope with the double-line frequency ripple power and remove the Al E-caps from the system [5], [6]. In [7], basic decoupling cells, like buck-type circuit, boost-type circuit, and buck–boost-type circuit, are introduced. They can be connected into the single-phase ac/dc converters in series or parallel. And the power density of the converters will be increased to 1.3 times the original [8]. These basic cells are easy to control because they work independently with the original circuit [9]–[11]. However, the extra power losses are inevitably introduced due to the fact that additional active and passive components are added. According to the normalized comparison results in [6], the efficiency penalty of the independent basic APD cells is 3%. This hinders the course of industrialization.

For reducing the power loss, some methods [12], [13] are proposed to decrease the conduction loss of power devices and the inductor loss in basic APD cells. They are achieved by reducing the decoupling voltage. Based on this idea, a duty ratio injection controller is proposed in [12] to generate a feed-forward to regulate the original duty ratio, then the efficiency is increased by 1%. In [13], an adaptive voltage control method is proposed to be applied for the boost-type APD cell. The minimum decoupling capacitor voltage is controlled to be constant to reduce the voltage stress. Another way to reduce power loss is to lessen the switching loss, by achieving soft switching. In [14], a variable frequency control applying for buck-type APD cell is proposed to make the current ripple of the inductor large enough to fully discharge the junction capacitance. Hence, zero voltage switching (ZVS) is achieved. The drawbacks are the complex control and filter design. To avoid this, an active-filter controller is proposed in [15]. The inductor current is controlled as a triangular shape, and the switches achieve ZVS at the peak and valley of the current. In addition to modifying the control, soft switching can be achieved by adding auxiliary circuits. In [16], the active clamp circuit is used in the parallel PFC flyback converter, to achieve ZVS of the main switch and the auxiliary switch. Due to the regulation of the output voltage by the clamp capacitor, the conduction loss will be reduced. Another method to reduce the conduction loss of the parallel PFC flyback converter is using parallel-connected flyback converters [17]. But the negative impact of double-line frequency ripple power is not considered. In [18], an APD auxiliary circuit (composed of four switches and one capacitor) is proposed to connect to a single-phase flyback converter proposed in [19]. The auxiliary capacitor is small enough to resonant with the parasitic inductor on the circuit. Each switch state of the auxiliary circuit is changed when the resonant current is zero. Therefore, zero current switching (ZCS) is achieved and the switching loss reduces. In [20], [21], the energy stored in the switch junction capacitor is transferred into the added auxiliary circuit, which is

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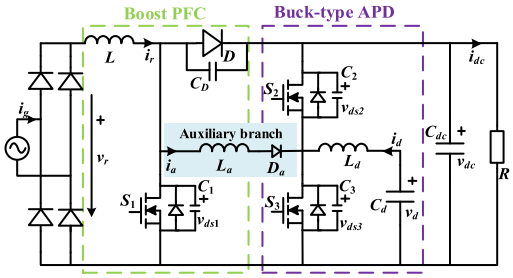

Fig. 1. Proposed single-phase PFC converter with active power decoupling and ZVS.

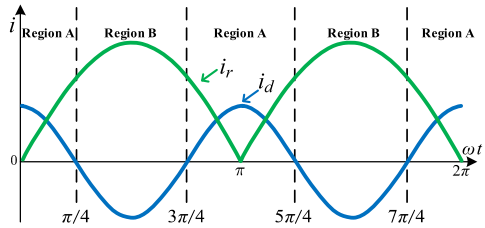

Fig. 2. Operation regions in a grid cycle.

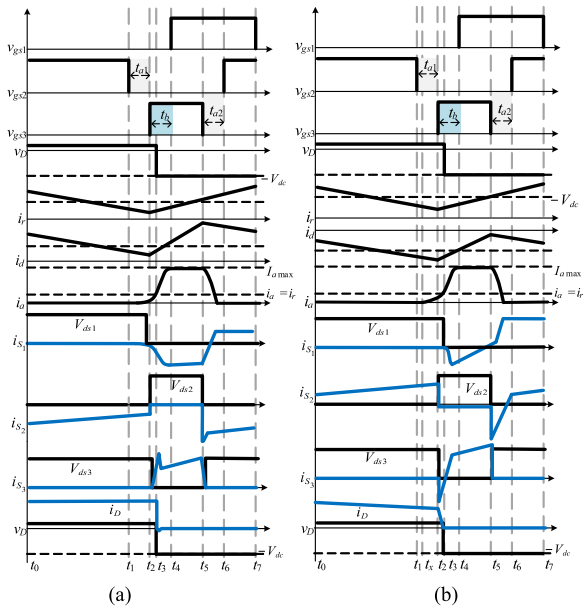

Fig. 3. Theoretical waveforms of the proposed circuit in (a) region A and (b) region B.

in series with the dc-link. Then, all switches in the inverter and buck-type APD cell realize ZVS. However, this is accomplished at the cost of increasing the voltage stresses of all switches by 10%.

This article presents a single-phase PFC rectifier with APD and ZVS (shown in Fig. 1). By adding a resonant inductor and a diode to the PFC rectifier with the buck-type APD cell, S_1 and S_2 realize ZVS operation, S_3 realizes ZVS turn-ON in half of the grid period and the diodes D and D_a realize ZCS turn-OFF. Consequently, the system efficiency is improved significantly without increasing the complexity of circuit structure and control. The remainder of this article is organized as follows: Section II introduces the proposed rectifier and describes its operation modes. Section III analyzes the ZVS conditions. Section IV introduces design considerations. Section V analyzes the power loss and provides a comparison result. Section VI depicts the controller design, and the experimental results are presented in Section VII. Finally, the conclusion is proposed in Section VIII.

II. Proposed Circuit and Operation States

In the proposed rectifier, the boost PFC circuit consists of an inductor L, a diode D, and an active switch S_1, the buck-type APD cell is composed of two active switches S_2 and S_3, an inductor L_d, and a capacitor C_d, and the auxiliary circuit includes an inductor L_a and a diode D_a. The auxiliary circuit mainly operates in the intervals before the three main switches are turned ON, resonates with the junction capacitors of the main switches, and makes the drain–source voltages equal to zero. Hence, the main switches S_1, S_2, and S_3 can achieve ZVS turn-ON, and the diodes D and D_a can achieve ZCS turn-OFF.

Assume that all components are ideal, and voltages v_r and v_d are constant during each switching period. To introduce the working process, the operating mode of the proposed circuit over one complete switching period is explained in the following. Since the ZVS conditions are related to the direction of i_d, to divide the ZVS regions easily, the positive direction of the i_d is set to be from right to left. According to the polarity of the decoupling current i_d, each grid cycle is divided into two regions, as shown in Fig. 2.

A. Operating Region A ($i_d > 0$)

In this region $i_d > 0$, S_1 and S_2 can achieve ZVS turn-ON. Fig. 3(a) shows the theoretical waveforms of the proposed circuit in region A. v_{gs1}, v_{gs2}, and v_{gs3} are the gate–source voltage of the main switches, v_D is the voltage across the diode D, t_{a1}, t_{a2}, and t_b are the key periods to achieve ZVS, and $I_{a\max}$ is the maximum value of i_a. Fig. 4 shows the equivalent circuit of each operation mode.

Interval a1 [t_0, t_1]: S_2 and D are turned ON, v_{ds1} and v_{ds3} equal to $V_{\rm dc}$, D_a is reverse biased, i_r and i_d decrease linearly, and i_d flows from the source to drain in S_2. i_r and i_d are expressed as follows:

$$i_r(t) = I_r(t_0) + \frac{v_r(t_0) - V_{dc}}{L}(t - t_0) \tag{1}$$

$$i_d(t) = I_d(t_0) + \frac{v_d(t_0) - V_{dc}}{L_d}(t - t_0). \tag{2}$$

This stage ends when S_2 is turned OFF.

Interval a2 [t_1, t_2]: S_2 is turned OFF. v_{ds1} keeps to $V_{\rm dc}$. Since $i_d > 0$, v_{ds2} is discharged to zero rapidly, and then the body diode of S_2 is turned-ON, v_{ds3} is clamped at the output voltage $V_{\rm dc}$. This stage ends when S_3 is turned ON.

Interval a3 [t_2, t_3]: S_3 is turned ON. Since $v_{ds3} = V_{\rm dc}$, S_3 is hard switching turn-ON. D_a is turned ON. i_d flows from the source to drain in S_3. Because v_{ds1} is clamped at the output voltage $V_{\rm dc}$,

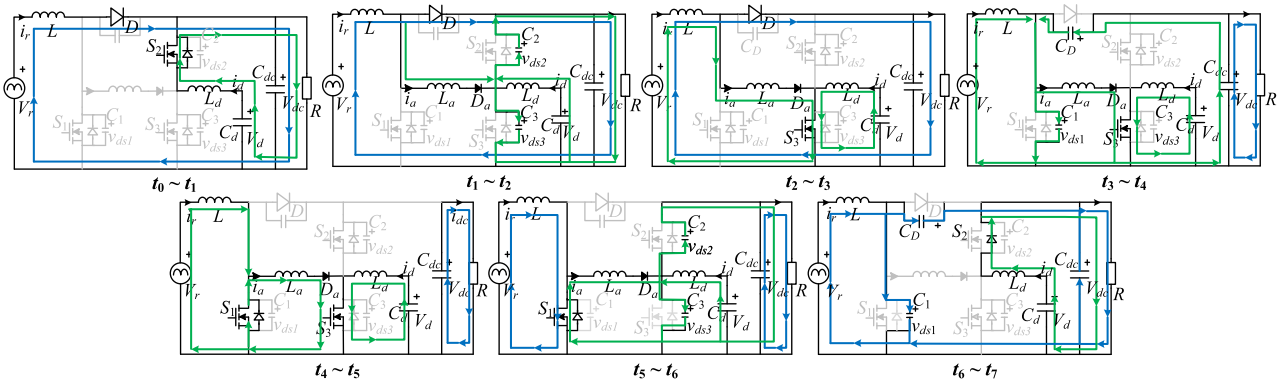

Fig. 4. Equivalent circuits of each operation mode in region A.

i_a increases linearly. i_a increases linearly as follows:

$$i_a(t) = \frac{V_{\rm dc}}{L_a}(t - t_2). \tag{3}$$

This stage ends when $i_a = i_r$.

Interval a4 [t_3, t_4]: When $i_a = i_r$, the current through D is zero, D achieves ZCS turn-OFF. C_1 is resonant with C_D and L_a. v_{ds1} decreases. v_D and i_a increase. The formulars of v_{ds1}, v_D, and i_a are as follows:

$$v_{ds1}(t) = V_{\rm dc}\cos\left[\omega_1(t - t_3)\right] \tag{4}$$

$$v_D(t) = V_{\rm dc} - V_{\rm dc}\cos\left[\omega_1(t - t_3)\right] \tag{5}$$

$$i_a(t) = I_r(t_3)\cos\left[\omega_1(t - t_3)\right] + \frac{V_{\rm dc}}{Z_1}\sin\left[\omega_1(t - t_3)\right] + I_r(t_3) \tag{6}$$

where $\omega_1 = 1/\sqrt{L_a(C_1 + C_D)}$, $Z_1 = \sqrt{L_a/(C_1 + C_D)}$.

The period that v_{ds1} drops from $V_{\rm dc}$ to zero is

$$t_{v1} = \frac{\pi}{2}\sqrt{L_a(C_1 + C_D)}. \tag{7}$$

When v_{ds1} equals zero, the body diode of S_1 is turned ON and the voltage of C_D equals $V_{\rm dc}$. At t_4, the gate signal of S_1 is applied, S_1 achieves ZVS turn-ON, and this interval ends.

Interval a5 [t_4, t_5]: S_1 and S_3 are turned ON. i_a keeps at the maximum value $I_{a\max}$. v_D and v_{ds2} equal $V_{\rm dc}$. At the end of this stage, S_3 is turned OFF.

Interval a6 [t_5, t_6]: When S_3 is turned OFF at t_5, v_{ds2} and i_a decrease, and v_{ds3} increases, which are expressed as follows:

$$v_{ds2}(t) = V_{\rm dc}\cos\left[\omega_2(t - t_5)\right] + V_{\rm dc} \tag{8}$$

$$v_{ds3}(t) = -V_{\rm dc}\cos\left[\omega_2(t - t_5)\right] \tag{9}$$

$$i_a(t) = \left[I_{a\max} + I_d(t_5)\right]\cos\left[\omega_2(t - t_5)\right] - I_d(t_5) \tag{10}$$

where $\omega_2 = 1/\sqrt{L_a(C_2 + C_3)}$.

The equivalent circuit of this interval is shown in Fig. 5(b). D_a achieves ZCS turn-OFF because it is turned OFF when i_a reduces to zero. S_1 is still turned ON and v_D equals $V_{\rm dc}$.

The period that v_{ds2} drops from $V_{\rm dc}$ to zero is as follows:

$$t_{v2} = \pi\sqrt{L_a(C_2 + C_3)}. \tag{11}$$

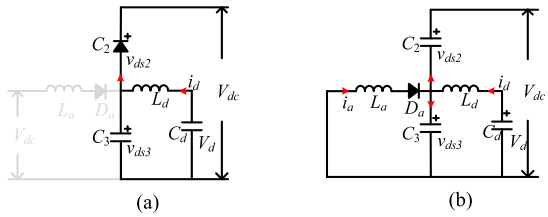

Fig. 5. Equivalent circuits of intervals a2 and a6 in region A. (a) Interval a2. (b) Interval a6.

When v_{ds2} equals zero, the body diode of S_2 is turned ON. At t_6, the gate signal of S_2 is applied, S_2 is turned ON. Meanwhile, S_1 is turned OFF. This stage ends.

Interval a7 [t_6, t_7]: S_2 is turned ON and S_1 is turned OFF, v_{ds1} increases, and v_D decreases. At t_7, v_{ds1} equals $V_{\rm dc}$, v_D equals zero, i_r flows through D. Since S_2 has already turned ON, i_d flows from the source to drain in S_2. The circuit enters operating interval a1.

B. Operating Region B ($i_d < 0$)

In this region, the operating modes are the same as those in region A. But the ZVS conditions for S_2 and S_3 are changed because of $i_d < 0$. Fig. 3(b) shows the theoretical waveforms in region B.

Interval b2 [t_1, t_2]: S_2 is turned OFF. v_{ds1} equals V_{dc}. v_{ds2} increases and v_{ds3} decreases, which are expressed as follows:

$$v_{ds3}(t) = \frac{I_d(t_1)}{C_2 + C_3}(t - t_1) + V_{\rm dc} \tag{12}$$

$$v_{ds2}(t) = -\frac{I_d(t_1)}{C_2 + C_3}(t - t_1). \tag{13}$$

The period that v_{ds3} drops from $V_{\rm dc}$ to zero is

$$t_{v3} = \frac{-V_{\rm dc}(C_2 + C_3)}{I_d(t_1)}. \tag{14}$$

At $t = t_x$, $v_{ds3} = 0$, the body diode of S_3 is turned ON, i_a rises linearly as follows:

$$i_a(t) = \frac{V_{\rm dc}}{L_a}(t - t_x). \tag{15}$$

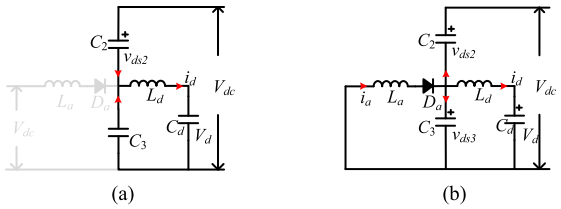

Fig. 6. Equivalent circuits of intervals b2 and b6 in region B. (a) Interval b2. (b) Interval b6.

It should be noted that when v_{ds3} equals zero, the body diode of S_3 is turned ON. The gate signal of S_3 needs to be applied before $i_a = I_d(t_1)$, otherwise the v_{ds3} will increase again then the ZVS condition will be lost. Therefore, t_{12} should be designed to avoid this situation. The period that i_a increases from 0 to $I_d(t_1)$ is as follows:

$$t_{i1} = \frac{-L_a I_d(t_1)}{V_{\rm dc}}. \tag{16}$$

When S_3 is ZVS turned ON, this stage ends.

Interval b6 [t_5, t_6]: S_3 is turned OFF. v_{ds2} and i_a decreases. Since the absolute value of i_a is greater than the absolute value of i_d, i_d will not flow through the body diode of S_3, so v_{ds3} increases. v_{ds2}, v_{ds3}, and i_a are expressed as follows:

$$v_{ds2}(t) = V_{\rm dc}\cos\left[\omega_2(t-t_5)\right] + V_{\rm dc} \tag{17}$$

$$v_{ds3}(t) = -V_{\rm dc}\cos\left[\omega_2(t-t_5)\right] \tag{18}$$

$$i_a(t) = \left[I_{a\max} - I_d(t_5)\right]\cos\left[\omega_2(t-t_5)\right] + I_d(t_5) \tag{19}$$

where $\omega_2 = 1/\sqrt{L_a(C_2+C_3)}$.

The period that v_{ds2} drops from $V_{\rm dc}$ to zero is the same as (11). When v_{ds2} equals zero, the body diode of S_2 is turned ON. At t_6, the gate signal of S_2 is applied, S_2 is ZVS turned ON. This stage ends. The equivalent circuit is shown in Fig. 6(b).

III. Analysis of ZVS Conditions

According to Section II, t_{a1}, t_{a2}, and t_b should be designed elaborately to achieve the ZVS of S_1, S_2, and S_3. In this section, the steady-state analysis is carried out first to pave the way to the analysis, then the ZVS conditions and design considerations are analyzed.

A. Steady-State Analysis

The state-space average models are expressed as follows:

$$L\frac{di_r}{dt} = v_r - (1-d_1)V_{\rm dc} \tag{20}$$

$$L_d\frac{di_d}{dt} = v_d - (1-d_3)V_{\rm dc} \tag{21}$$

$$C_d\frac{dv_d}{dt} = -i_d \tag{22}$$

$$C_{\rm dc}\frac{dv_{\rm dc}}{dt} = (1-d_1)i_r + (1-d_3)i_d - \frac{V_{\rm dc}}{R}. \tag{23}$$

The steady-state expressions of d_1 and d_3 are derived from (20) and (21) as follows:

$$d_1 = 1 - \frac{v_r}{V_{\rm dc}} \tag{24}$$

$$d_3 = 1 - \frac{v_d}{V_{\rm dc}}. \tag{25}$$

Assume v_r, i_r, and v_d are expressed as follows:

$$v_r = V_r\left|\sin(\omega t)\right| \tag{26}$$

$$i_r = I_r\left|\sin(\omega t)\right| \tag{27}$$

$$v_d = \sqrt{\frac{P_o}{\omega C_d}\left[K - \sin(2\omega t)\right]} \tag{28}$$

where V_r and I_r are the amplitudes of the v_r and i_r, P_o is the output power, and K is the energy storage margin coefficient [22].

According to the modulation method as illustrated in Fig. 3, the restrictions of d_1 and d_3 can be derived and expressed as follows:

$$d_3T_{\rm s} - t_b < d_1T_{\rm s} < T_s - t_{a1} - t_b \tag{29}$$

$$d_3T_{\rm s} > t_b. \tag{30}$$

B. ZVS Condition for S_1

For S_1, t_b is the key design parameter to achieve ZVS turn-ON. As shown in Fig. 3, t_b can be expressed as follows:

$$t_b = t_{23} + t_{34}. \tag{31}$$

According to (3), t_{23} can be expressed as follows:

$$t_{23} = \frac{I_rL_a}{V_{\rm dc}}. \tag{32}$$

As analyzed in interval a4, t_{34} needs to be greater than t_{v1} [as expressed in (7)]. Therefore, the limit of t_{34} is as follows:

$$t_{34} > t_{v1}. \tag{33}$$

Inferred from (30)–(33), the range of t_b is as follows:

$$\frac{\pi}{2}\sqrt{L_a(C_1+C_D)} + \frac{I_rL_a}{V_{\rm dc}} < t_b < d_3T_s. \tag{34}$$

To avoid damaging the PF and the effect of APD, t_b should be as small as possible. Therefore, the ZVS condition of S_1 is

$$\frac{\pi}{2}\sqrt{L_a(C_1+C_D)} + \frac{I_rL_a}{V_{\rm dc}} < t_b < d_{3\min}T_s \tag{35}$$

where $d_{3\min} = (V_{dc} - \sqrt{P_o(K+1)/\omega C_d})/V_{\rm dc}$.

C. ZVS Conditions for S_2 and S_3

For S_2, as described in interval a6 or b6, t_{a2} needs to be larger than t_{v2} [as expressed in (11)]. So, the ZVS condition of S_2 is

$$t_{a2} > t_{v2}. \tag{36}$$

For S_3, as analyzed in interval a2, S_3 cannot achieve ZVS in region A. So, the ZVS condition of S_3 is determined by region B. In interval b2, t_{a1} should be smaller than t_{i1} [as expressed in

(16)] and larger than t_{v3} [as expressed in (14)]. Hence, the range of t_{a1} is as follows:

$$\frac{-V_{\rm dc}(C_2+C_3)}{I_d(t_1)} < t_{a1} < \frac{-L_a I_d(t_1)}{V_{\rm dc}} \tag{37}$$

and $I_d\,(t_1)$ can be obtained from (2) and expressed as follows:

$$I_d(t_1) = I_d(t_0) + \frac{(v_d(t_0)-V_{\rm dc})t_{01}}{L_d} \tag{38}$$

where t_{01} is approximate as follows:

$$t_{01} = (1-d_1)T_s = \frac{V_r(t_0)T_s}{V_{\rm dc}}. \tag{39}$$

To avoid damaging the PF and the effect of APD, t_{a1} is expected to be as small as possible. Therefore, $I_d\,(t_1)$ should take the maximum. From (38), when $I_d\,(t_0)=0$, $I_d\,(t_1)$ will be the biggest. And as seen from Fig. 2, when $I_d\,(t_0)=0$, t_0 equals $\pi/4\omega$. Substitute $\pi/4\omega$ into (38) and (39), the maximum of $I_d\,(t_1)$ can be expressed as follows:

$$I_d(t_1)_{\max} = \frac{\left(\sqrt{P_o\,(K-1)/\omega C_d} - V_{\rm dc}\right)V_r T_s}{\sqrt{2}L_d V_{\rm dc}}. \tag{40}$$

Therefore, the ZVS condition of S_3 is as follows:

$$\frac{-V_{\rm dc}(C_2+C_3)}{I_d(t_1)_{\max}} < t_{a1} < \frac{-L_a I_d(t_1)_{\max}}{V_{\rm dc}}. \tag{41}$$

Selecting S_1–S_3, D, and L_d as in Table I, the ranges of t_{a1}, t_{a2}, and t_b are simplified to associate with P_o, K, C_d, and L_a.

IV. Design Considerations

Based on the above analysis in Sections II and III, the design procedure is presented. The objectives of the procedure are to ensure the ZVS conditions of main switches, the output voltage ripple meets requirements and the circuit operates stably.

A. Design Procedure

1) Determine the input voltage, output voltage, rated power, switching frequency, current ripple factor, and the maximum output voltage ripple as basic parameters.
2) According to the basic parameters and the operating characteristics analyzed in Section II, the voltage stress and current stress of each switch in the circuit can be determined as the main basis for switch selection. And the fast recovery diodes are selected to reduce the power losses.
3) As the analysis of Section III, the ranges of decoupling capacitor C_d and the auxiliary inductance L_d can be determined, and then K, t_{a1}, t_{a2}, and t_b can be determined. Therefore, the average value of v_d and the ZVS conditions of main switches can be obtained.

a) Decoupling capacitor (C_d) design

It can be inferred from (24), (25), and (29) that the steady-state voltages v_d satisfies the following:

$$V_r < v_d < V_{\rm dc}. \tag{42}$$

TABLE I
Voltage Stress and Current Stress of All Switches

Device	D_1-D_4	D	D_a	S_1	S_2	S_3
Voltage stress	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
Current stress	I_r	I_r	i_{a_max}	I_r	i_{d_max}	i_{a_max}

Note: $i_{d\max}=\sqrt{\omega C_d P_o/K}$; $i_{a\max}=I_r+V_{\rm dc}\sqrt{C_1+C_D/L_a}$.

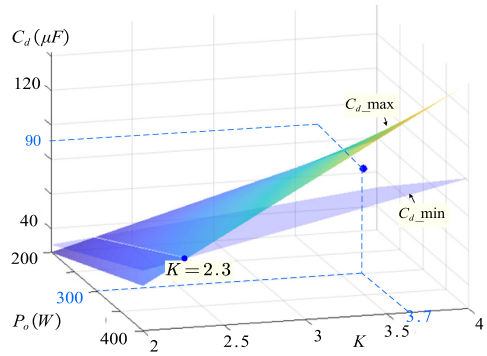

Fig. 7. Decoupling capacitor design region.

From (28) and (42), the range of C_d can be expressed as follows:

$$\frac{P_o\,(K+1)}{\omega V_{\rm dc}^2} < C_d < \frac{P_o\,(K-1)}{\omega V_r^2}. \tag{43}$$

The feasible region of C_d is shown in Fig. 7. As seen, K should be larger than 2.3 to meet the limitation of C_d.

Since the dc bias of v_d can be deduced from (28) as follows:

$$\bar{v}_d = \sqrt{\frac{P_o K}{\omega C_d}}. \tag{44}$$

When K is selected, $\bar{v}_d$ is determined.

b) Auxiliary inductor (L_a) design

Combining (35) and (41), the range of L_a is

$$\frac{\pi^2 V_{dc}^2(C_2+C_3)}{\left[-I_d(t_1)_{\max}\right]^2} < L_a < \frac{-b+\sqrt{b^2-4ac}}{2a} \tag{45}$$

where $a=I_r/V_{dc}$, $b=\pi\sqrt{C_1+C_4}/2$, and $c=-d_{3\min}T_s$. Fig. 8 shows the solution region of L_a.

4) The input inductor L, the decoupling inductor L_d, and output capacitor C_{dc} are selected by the allowable values of input current ripple, decouping current ripple and output voltage ripple to maintain good input and output characteristics.

a) Input inductor (L) and decoupling inductor (L_d) design

The ripple of i_r is

$$\Delta i_r = \frac{V_{dc}v_r - v_r^2}{V_{dc}f_s L}. \tag{46}$$

The range of L can be expressed as follows:

$$L > \frac{V_{\rm dc}v_r - v_r^2}{V_{\rm dc}f_s \Delta i_{r\max}}. \tag{47}$$

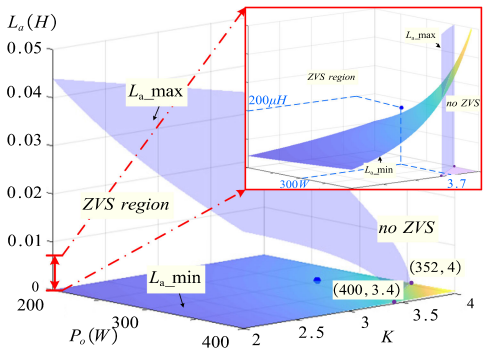

Fig. 8. Auxiliary inductor design region.

TABLE II
VOLTAGE STRESS AND CURRENT STRESS OF ALL SWITCHES

Device	D_1-D_4	D	D_a	S_1	S_2	S_3
Voltage stress	250V	250V	250V	250V	250V	250V
Current stress	4	4	4.3	4	2	4

And the decoupling inductor L_d can be similarly expressed as

$$L_d > \frac{V_{dc}v_d - v_d^2}{V_{dc}f_s\Delta i_{d\max}}. \tag{48}$$

b) Output capacitor ($C_{\rm dc}$) design

The ripple of the $v_{\rm dc}$ is as follows:

$$\Delta v_{\rm dc} = \frac{v_{\rm dc}(i_r + i_d) - 2P_o}{V_{\rm dc}f_sC_{\rm dc}}. \tag{49}$$

The range of $C_{\rm dc}$ can be expressed as follows:

$$C_{\rm dc} = \frac{v_{\rm dc}(i_r + i_d) - 2P_o}{V_{\rm dc}f_s\Delta v_{\rm dc\,max}}. \tag{50}$$

B. Parameters Selection

Following the above design guidelines, the selection of the proposed converter parameters is as follows.

1) The basic parameters are selected as follows:

Input voltage: 110 V(RMS);
Output voltage: 250 V;
Rated power: 300 W;
Switching frequency: 20 kHz;
Current ripple factor: 0.4;
Maximum output voltage ripple: 5% × $V_{\rm dc}$.

2) The theoretical voltage and current stresses are listed in Table II.

Considering that the peak value of i_r and i_d is 15 A in the initial state, the switches is chosen as S_1–S_3:FCH47N60NF; D_1–D_4:DPG60I400HA; D and Da DPG60I400HA.

3) Based on Figs. 7 and 8, when P_o equals 300 W, K is selected to be 3.7, then $\bar{v}_d$ is 200 V. The ranges of C_d and L_a are calculated from (43) and (45), and chosen as 90 μF and 200 μH. Substituting P_o, K, C_d, and L_a to (35), (36), and (41), the regions of t_{a1}, t_{a2}, and t_b are determined. Finally, t_{a1} and t_{a2} take 1 μs, and t_b takes 3 μs.

4) According to the current ripple factor and the maximum output voltage ripple, the maximum ripple of i_r, i_d, and $v_{\rm dc}$ can be carried out, substituting them into (47), (48), and (50), the ranges of L, L_d, and $C_{\rm dc}$ are calculated. To allow some margin, L is 3 mH, L_d is 1.5 mH, and $C_{\rm dc}$ is 30 μF.

The parameters of the proposed circuit are listed in Table III.

TABLE III
PARAMETERS OF THE PROPOSED CIRCUIT

Symbol	Parameter	Value
v_g	The grid voltage	110 V(RMS)
f_s	The switching frequency	20 kHz
P_o	Output power	300 W
K	Energy storage margin coefficient	3.7
$V_{\rm dc}$	Output voltage	250 V
S_1~S_3	Main switches	FCH47N60NF
$D_1 \sim D_4$	Full bridge rectifier diodes	DPG60I400HA
D *and* D_a	Boost PFC diode and Auxiliary diode	DPG60I400HA
L_a	Auxiliary inductor	200 μH
L_d	APD inductor	1.5 mH
L	PFC inductor	3 mH
C_d	APD capacitor	90 μF
C_1~C_3	Drain-source capacitor of main switches	190 pF
$C_{\rm dc}$	Output capacitor	30 μF
R	Output load	200 Ω

V. POWER LOSS AND COMPARISON

A. Power Loss

The power loss for the proposed converter mainly includes switching loss and inductor loss. According to the datasheet of semiconductor devices and the loss calculation method in [23], the power loss of switches can be estimated. As for the inductor power loss, they are composed of core loss and copper loss. They can be estimated by adopting the method in [24] and [25]. The calculation formulas of power loss are listed in Table IV. The theoretically calculated results at 300 W are shown in Fig. 9. Compared with the PFC rectifier with APD, the proposed circuit increases auxiliary branch loss by 2.6 W and reduces switching loss by 23.2 W. In contrast, the switching loss of the proposed circuit was reduced by 80%. Fig. 10 shows the power loss and efficiency of the PFC rectifier with APD and the proposed rectifier. As seen, the proposed circuit can significantly reduce the power loss of the PFC rectifier with APD. At 300 W, the power loss is reduced by 44% compared with that of the PFC rectifier with APD.

B. Comparison

To assess the pros and cons of the proposed topology, a comparison is carried out between the other four methods, which can improve the efficiency of the PFC rectifier with APD. The comparison results are shown in Table V.

TABLE IV
POWER LOSS CALCULATION FORMULAS

Power loss	PFC rectifier with APD	PFC rectifier with APD and ZVS	Note
P_{S1}	$P_{hS1}=R_{Son}I_{r1RMS}^2+(E_{on1}+E_{off1})f_s$	$P_{sS1}=R_{Son}I_{r1RMS}^2+E_{off1}f_s$	$I_{r1RMS}=\sqrt{\frac{2}{T}\int_0^{T/2}i_{S_1}^2(t)dt}$ $E_{on1}=E_{off1}+Q_{rr1}V_{dc}\quad E_{off1}=V_{dc}I_r\frac{t_{ri1}+t_{fu1}}{2}$
P_{S2}	$P_{hS2}=R_{Son}I_{d2RMS}^2+(E_{on2}+E_{off2})f_s$	$P_{sS2}=R_{Son}I_{d2RMS}^2+\frac{1}{2}E_{off2}f_s$	$I_{d2RMS}=\sqrt{\frac{2}{T}\int_0^{T/2}i_{S_2}^2(t)dt}\quad I_d=\sqrt{\omega P_oC_d/K}$ $E_{off2}=V_{dc}I_d\frac{t_{ri1}+t_{fu1}}{2}\quad E_{on2}=E_{off2}+Q_{rr1}V_{dc}$
P_{S3}	$P_{hS3}=R_{Son}I_{d3RMS}^2+(E_{on3}+E_{off3})f_s$	$P_{sS3}=R_{Son}I_{d3RMS}^2+\frac{1}{2}E_{on3}f_s\ +E_{off3}f_s$	$I_{d3RMS}=\sqrt{\frac{2}{T}\int_0^{T/2}i_{S_3}^2(t)dt}\quad I_3=I_a+I_d$ $E_{off3}=V_{dc}I_3\frac{t_{ri1}+t_{fu1}}{2}\quad E_{on3}=E_{off3}+Q_{rr1}V_{dc}$
P_D	$P_{hD}=V_{D0}I_{rDavg}+R_{Don}I_{rDRMS}^2+E_{onD}f_s$	$P_{sD}=V_{D0}I_{rDavg}+R_{Don}I_{rDRMS}^2$	$I_{rDavg}=\frac{2}{T}\int_0^{T/2}i_D(t)dt\quad E_{onD}=\frac{1}{4}Q_{rr2}V_{dc}$ $I_{rDRMS}=\sqrt{\frac{2}{T}\int_0^{T/2}i_D^2(t)dt}$
P_{Da}	–	$P_{sDa}=V_{Da0}I_{aavg}+R_{Don}I_{aRMS}^2$	$I_{aavg}=\frac{2}{T}\int_0^{T/2}i_a(t)dt\quad E_{onDa}=\frac{1}{4}Q_{rr2}V_{dc}$ $I_{aRMS}=\sqrt{\frac{2}{T}\int_0^{T/2}i_a^2(t)dt}$
P_{Dr}	$P_{Dr}=4(V_{Dr0}I_{ravg}+R_{Dr}I_{rRMS}^2+E_{onDr}f)$		$I_{ravg}=\frac{2}{T}\int_0^{T/2}i_r(t)dt\quad E_{onDr}=\frac{1}{4}Q_{rr3}V_r$ $I_{rRMS}=\sqrt{\frac{2}{T}\int_0^{T/2}i_r^2(t)dt}$
P_L	$P_L=2V_ec_mf_s^x\left(\frac{L_dI_r}{NA_e}\right)^y(c_T-c_{T1}T+c_{T2}T^2)$ $+2I_{rRMS}^2R_{dc}\Delta\left[\frac{\sinh(2\Delta)+\sin(2\Delta)}{\cosh(2\Delta)-\cos(2\Delta)}+\frac{2}{3}(p^2-1)\frac{\sinh(\Delta)-\sin(\Delta)}{\cosh(\Delta)+\cos(\Delta)}\right]$		$\delta=\frac{1}{\sqrt{\pi f\mu_0\sigma}}\qquad R_{dc}=\frac{4N\rho l_t}{\pi\delta^2}$ $\Delta=\left(\frac{\pi}{4}\right)^{0.75}\frac{d}{\delta}\sqrt{\frac{d}{l_1}}$
P_{Ld}	$P_{Ld}=V_ec_mf_s^x\left(\frac{L_dI_d}{NA_e}\right)^y(c_T-c_{T1}T+c_{T2}T^2)$ $+I_{dRMS}^2R_{dc}\Delta\left[\frac{\sinh(2\Delta)+\sin(2\Delta)}{\cosh(2\Delta)-\cos(2\Delta)}+\frac{2}{3}(p^2-1)\frac{\sinh(\Delta)-\sin(\Delta)}{\cosh(\Delta)+\cos(\Delta)}\right]$		$\delta=\frac{1}{\sqrt{\pi f\mu_0\sigma}}\qquad R_{dc}=\frac{4N\rho l_t}{\pi\delta^2}$ $\Delta=\left(\frac{\pi}{4}\right)^{0.75}\frac{d}{\delta}\sqrt{\frac{d}{l_1}}$
P_{La}	$P_{La}=V_{ea}c_mf_s^x\left(\frac{L_aI_{a\max}}{N_aA_{ea}}\right)^y(c_T-c_{T1}T+c_{T2}T^2)$ $+2I_{aRMS}^2R_{dca}\Delta_a\left[\frac{\sinh(2\Delta_a)+\sin(2\Delta_a)}{\cosh(2\Delta_a)-\cos(2\Delta_a)}+\frac{2}{3}(p_a^2-1)\frac{\sinh(\Delta_a)-\sin(\Delta_a)}{\cosh(\Delta_a)+\cos(\Delta_a)}\right]$		$\delta_a=\frac{1}{\sqrt{\pi f_s\mu_0\sigma}}\qquad R_{dca}=\frac{4N_a\rho l_{ta}}{\pi\delta_a^2}$ $\Delta_a=\left(\frac{\pi}{4}\right)^{0.75}\frac{d_a}{\delta_a}\sqrt{\frac{d_a}{l_{1a}}}$

Note: P_{S1} is the loss of S_1; P_{S2} is the loss of S_2; P_{S3} is the loss of S_3; P_D is the loss of D; P_{Dr} is the loss of D_r; P_{Da} is the loss of D_a.
P_{La} is the loss of L_a; P_L is the loss of L; P_{Ld} is the loss of L_d.
$c_m=0.25, x=1.6, y=2.5, c_T=1.26, c_{T1}=1.05\times10^{-2}, c_{T2}=0.79\times10^{-4}, T=25, \mu_0=4\pi\times10^{-7}, \sigma=59.6\times10^6, \rho=1.7\times10^{-8}$.
$V_e=28.6\ \text{cm}^3, N=62, A_e=0.19\times10^{-3}, A_{ea}=0.19\times10^{-3}, V_{ea}=16.3\ \text{cm}^3, N_a=30$.
$d=d_a=0.3\times10^{-3}, l_t=0.1, l_{ta}=0.03, l_1=0.1\times10^{-3}, l_{1a}=0.1\times10^{-3}, p=p_a=2$.

The control methods in [12] and [13] are developed to reduce the conduction loss of the APD circuit by reducing the inductor current ripple. However, the efficiency improvement is not significant in [12] (only 1%) and the method proposed in [13] fails to work at medium or heavy load. In [14], the current ripple of the APD circuit is increased on purpose to fully discharge the parasitic capacitances of switches and then the ZVS is realized. This method is a variable switching frequency control, which increases the control complexity and the inductor design difficulty. In [20], [21], and this article, the efficiency is improved by adding an auxiliary circuit. In [20], [21], the added auxiliary circuit (consisting of one active switch, one inductor, and one capacitor) is in series with the dc-link and all switches achieve ZVS turn-ON. However, it increases the voltage stresses of all switches by 10%. The added auxiliary circuit in the proposed method includes no active switch or capacitor and the cost can be smaller. Besides, the effect of the efficiency improvement is better (4% efficiency improvement). However, the lower switch

TABLE V
COMPARISON OF OTHER HIGH-EFFICIENCY METHOD

Methods	Power rating	Efficiency	Effect on the voltage stress	Added components	Kind of reduced losses	Efficiency improvement
[12]	500 W	97%	No	0	Conduction losses of APD circuit switches	1%
[13]	33.6 W	85%	No	0	Conduction losses of APD circuit switches	3% (at light load)
[14]	1000 W	94%	No	0	Switching losses of APD circuit switches	1%
[20][21]	1500 W	97%	10% increase	3(one active switch, one inductor, and one capacitor)	Switching losses for all active switches	2%
Proposed method	300 W	95%	No	2(one diode, and one inductor)	Switching losses for all switches	4%

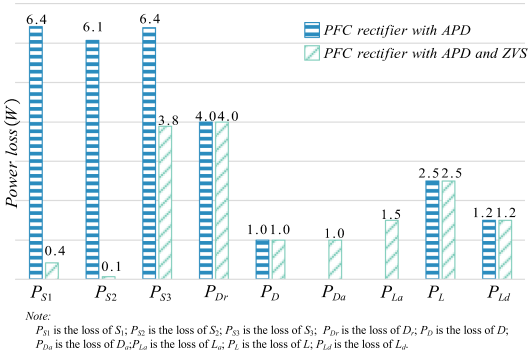

Fig. 9. Power loss comparison of PFC rectifier with APD and PFC rectifier with APD and ZVS @ $P_o = 300$ W.

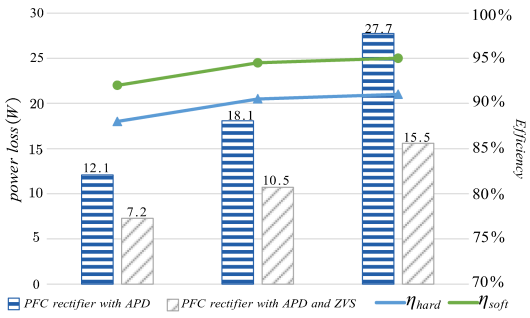

Fig. 10. Power loss and efficiency of PFC rectifier with APD and PFC rectifier with APD and ZVS at different output power.

of the APD can achieve ZVS turn-ON only in half of the grid period.

VI. CONTROLLER DESIGN

The volt-second balance-based control [26] method, also called automatic-power-decoupling control, is adopted. In this controlling idea, the bus dc voltage $v_{\rm dc}$ is regulated by the decoupling circuit and the decoupling capacitor voltage is maintained by controlling the rectifier. Its advantage is that the control loop of the dc bus voltage can be designed to be fast to regulate the

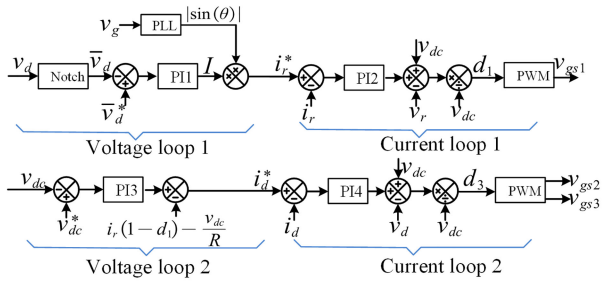

Fig. 11. Control diagram of the system.

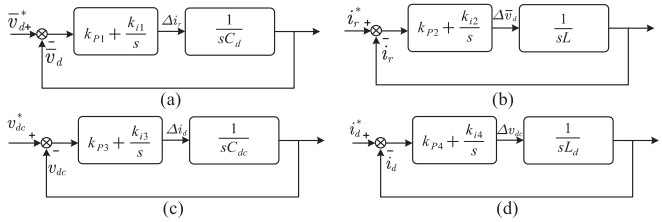

Fig. 12. Diagram of the control loops. (a) Voltage loop 1. (b) Current loop 1. (c) Voltage loop 2. (d) Current loop 2.

dc bus voltage. The control diagram is shown in Fig. 11. Two dual-loop control structures are adopted. For the first dual-loop, the average voltage of the decoupling capacitor $\bar{v}_d$ is the outer loop and the rectifier side current i_r is the inner loop. The average value of the decoupling capacitor voltage is obtained by a notch filter, and the phase information of input voltage v_g is obtained by a phase-locked loop. For the second dual-loop, the output voltage v_{dc} is the outer loop, and the decoupling current i_d is the inner loop. Proportional Integral (PI) controller is applied to achieve the control aims.

A. Controller Design and PI Parameter Selection

The state-space average models are expressed as (20)–(23). As the control diagram shown in Fig. 11 and the control diagram of four loops shown in Fig. 12, the controller of the first dual-loop

TABLE VI
THE PARAMETERS OF THE PI COMPENSATORS

Parameters	Voltage loop 1	Current loop 1	Voltage loop 2	Current loop 2
k_p	0.05	10.8	0.05	13.5
k_i	8.9	12791	26.6	47966

can be expressed as follows:

$$\left(k_{p2}+\frac{k_{i2}}{s}\right)\left(i_r^*-i_r\right)=v_r-\left(1-d_1\right)V_{\rm dc} \tag{51}$$

$$\left(k_{p1}+\frac{k_{i1}}{s}\right)\left(\bar{v}_d^*-\bar{v}_d\right)=-i_d. \tag{52}$$

And it can be deduced that

$$\frac{i_r}{i_r^*}=\frac{k_{p2}s+k_{i2}}{s^2+\frac{k_{p2}}{L}s+\frac{k_{i2}}{L}} \tag{53}$$

$$\frac{\bar{v}_d}{\bar{v}_d^*}=\frac{k_{p1}s+k_{i1}}{s^2+\frac{k_{p1}}{C_d}s+\frac{k_{i1}}{C_d}}. \tag{54}$$

Therefore, the parameters of the PI compensators are as follows:

$$k_{p1}=2\xi_1\omega_1C_d, k_{i1}=\omega_1^2C_d, k_{p2}=2\xi_2\omega_2L, k_{i2}=\omega_2^2L.$$

The controller design and parameter selection of the second dual-loop can be similarly carried out, and the parameters of the PI compensators in the second dual-loop are as follows:

$$k_{p3}=2\xi_3\omega_3C_{dc}, k_{i3}=\omega_3^2C_{dc}, k_{p4}=2\xi_4\omega_4L_d, k_{i4}=\omega_4^2L_d.$$

$\xi_1-\xi_4$ are the damping ratio of each loop, and takes 0.707. ω_1–ω_4 are the bandwidth of each loop. ω_2 is determined to be one-fifth of the switching frequency, and ω_1 is one-sixth of ω_2. To ensure faster output voltage response, ω_3 should be larger than ω_1. ω_3 is selected to be twice the ω_1, and ω_4 is six times of ω_3. The parameters of the PI compensators are shown in Table VI.

B. Stability

For the first dual-loop, d_1 is taken as the control variable and designed as follows:

$$d_1=\frac{v_{\rm dc}-v_r+L\left(k_{p2}e_2+k_{i2}z_2\right)}{v_{\rm dc}} \tag{55}$$

where k_{p2} and k_{i2} are positive gains, $e_2=i_r^*-i_r$, $\dot{z}_2=e$.

Substituting (55) into (20) leads

$$\dot{e}_2=k_{p2}e_2+k_{i2}z_2. \tag{56}$$

To verify the stability of the system, a Lyapunov function is constructed as follows:

$$V\left(e_2,z_2\right)=\frac{1}{2}k_{i2}z_2^2-\frac{1}{2}e_2^2. \tag{57}$$

Then

$$\dot{V}\left(e_2,z_2\right)=k_{i2}z_2e_2-e_2\dot{e}_2.=-k_{p2}e_2^2. \tag{58}$$

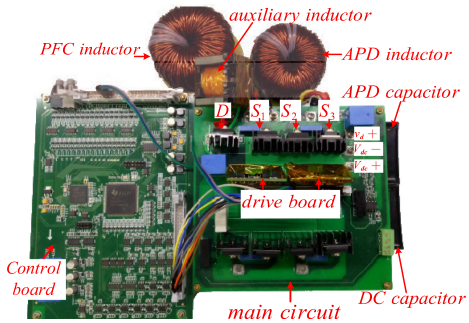

Fig. 13. Photo of the prototype.

According to the Lasalle theorem, the system is asymptotic stable.

For the second dual-loop, d_3 is taken as the control variable and designed as follows:

$$d_3=\frac{v_{dc}-v_d+L_d\left(k_{p4}e_4+k_{i4}z_4\right)}{v_{dc}}. \tag{59}$$

And the stability can be similarly proved.

VII. EXPERIMENT RESULTS

To verify the theoretical analysis, the laboratory prototype was built, which is shown in Fig. 13.

Fig. 14 exhibits the experiment results at 20 kHz of the proposed converter. Fig. 14(a)–(f) show the gate–source voltages and the currents of S_1, S_2, and S_3; the rectifier output current i_r; and the decoupling inductor current i_d. As seen, before i_{S1} and i_{S2} rise up, v_{ds1} and v_{ds2} have reached zero. As a result, S_1 and S_2 achieve ZVS turn-ON both in region A and region B. Note that, in Fig. 14(c), i_{S2} and v_{ds2} do not overlap with each other, so the turn-OFF loss of S_2 in region A equals zero. For S_3, since the voltage of the junction capacitor v_{ds3} cannot drop to zero, S_3 is hard-switching turned ON in region A, as shown in Fig. 14(e). Because of the hard-switching operation, the current oscillation of i_r and i_d occurs [27]. In region B, v_{ds3} drops to zero before i_{S3} rises, as shown in Fig. 14(f). Hence, S_3 achieves ZVS turn-ON. In short, the ZVS situations of S_1, S_2, and S_3 are consistent with the theoretical analysis in Section II.

Fig. 14(g)–(j) exhibit the voltage and current of the diode D and D_a, the gate–source voltage of S_1, and S_3 (to indicate the turn-ON and turn-OFF of the diodes). It can be seen that the currents of diodes have dropped to zero before their voltage increase and the voltage and current of the diodes do not overlap with each other, proving that D and D_a achieve ZCS turn-OFF.

Fig. 14(k) shows the waveforms of the output voltage $v_{\rm dc}$, the decoupling capacitor voltage v_d, the rectifier output voltage v_r, and the rectifier output current i_r. $v_{\rm dc}$ is regulated at 250 V with a small ripple voltage, which is lower than 5% of $v_{\rm dc}$. v_d fluctuates at the double-line frequency, the ripple voltage of v_d is 60 V, and the average value of v_d is 200 V. i_r is continuous and in phase with v_r. The PF is 0.996. Consequently, PFC and APD are effective.

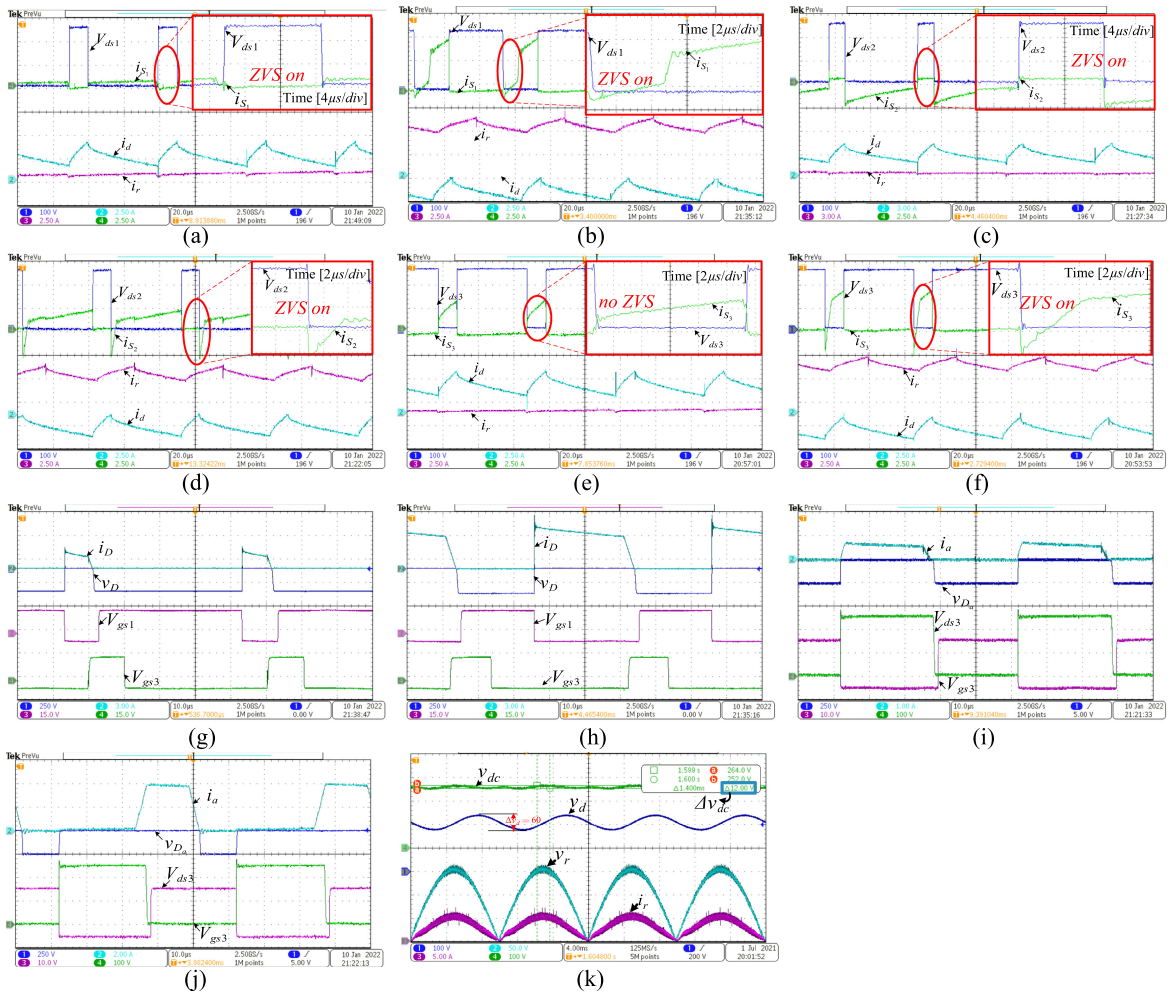

Fig. 14 The voltage and current waveforms at the switching transitions of all switches switch voltage and current. (a) ZVS situation of S_1 in region A. (b) ZVS situation of S_1 in region B. (c) ZVS situation of S_2 in region A. (d) ZVS situation of S_2 in region B. (e) ZVS situation of S_3 in region A. (f) ZVS situation of S_3 in region B. (g) ZCS situation of D in region A. (h) ZCS situation of D in region B. (i) ZCS situation of D_a in region A. (j) ZCS situation of D_a in region B. (k) Steady-state waveforms.

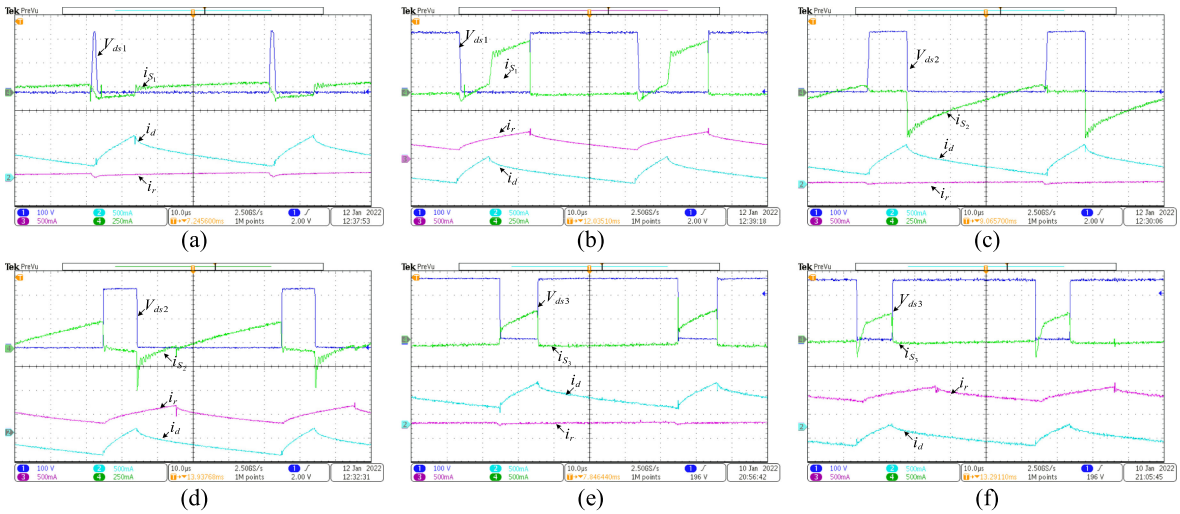

Fig. 15 Experiment results at 10% of rated output power. (a) ZVS situation of S_1 in region A. (b) ZVS situation of S_1 in region B. (c) ZVS situation of S_2 in region A. (d) ZVS situation of S_2 in region B. (e) ZVS situation of S_3 in region A. (f) ZVS situation of S_3 in region B.

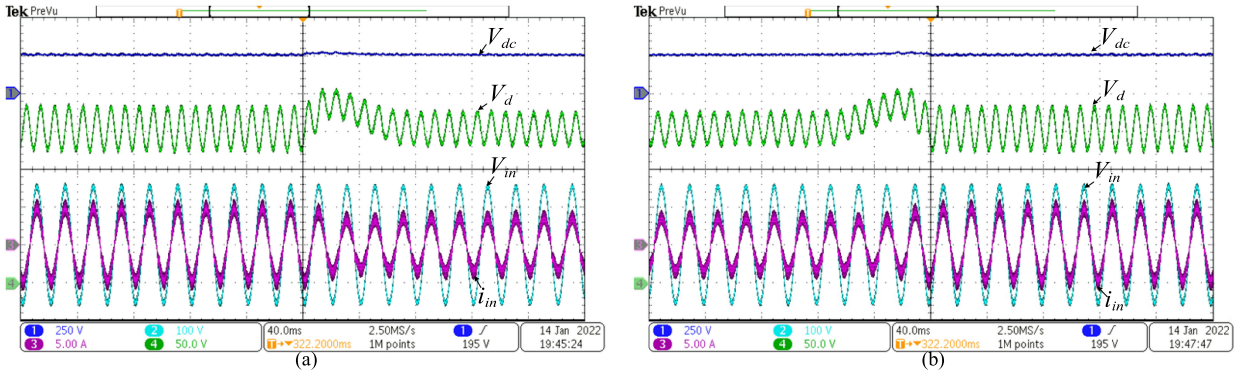

Fig. 16 Dynamic experimental waveforms. (a) Step-down output power change from 300 W to 150 W. (b) Step-up output power change from 150 W to 300 W.

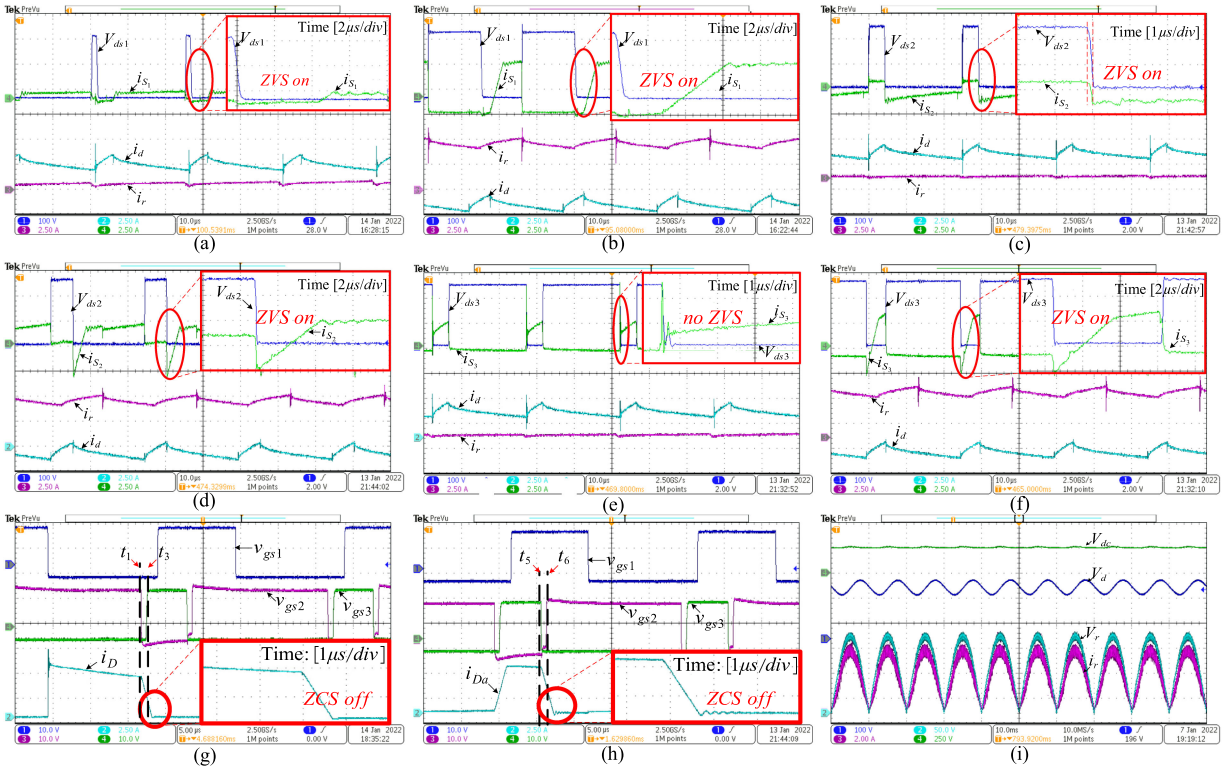

Fig. 17 Experiment results at 40 kHz. (a) ZVS situation of S_1 in region A. (b) ZVS situation of S_1 in region B. (c) ZVS situation of S_2 in region A. (d) ZVS situation of S_2 in region B. (e) ZVS situation of S_3 in region A. (f) ZVS situation of S_3 in region B. (g) ZCS turn-off of D; (h) ZCS turn-OFF of Da. (i) Steady-state result.

The experimental results at 10% load are shown in Fig. 15. As can be seen, ZVS is also achieved at light load. According to the analysis in Section III, when the circuit element parameters, the output voltage $V_{\rm dc}$ and the average value of the decoupling capacitor voltage $\bar{v}_d$ are chosen, the ZVS conditions are only related to P_o. By substituting the P_o under different loads into (35), (36), and (41), the corresponding time can be calculated to ensure the realization of ZVS.

Fig. 16 shows the dynamic experimental waveforms of the proposed circuit. In Fig. 16(a), the output power decrease from 300 to 150 W. The output voltage $V_{\rm dc}$ tracks to 250 V within 30 ms and the deviation is not obvious. The average decoupling capacitor voltage V_d tracks to 200 V within 60 ms. No current spikes occur and the transient is smooth. Fig. 16(b) shows the opposite transient process.

Fig. 17 shows the experimental results at 40 kHz. As seen, S_1 and S_2 can achieve ZVS turn-ON, S_3 can achieve ZVS turn-ON in half of the output voltage cycle (region B), D and D_a can achieve ZCS turn-OFF.

Fig. 18 shows the efficiency curves of the PFC rectifier with APD and the PFC rectifier with APD and ZVS at 10%–100% load. It can be seen that the experiment efficiencies agree with the theoretical value in Fig. 10. At 300 W, the efficiency of the

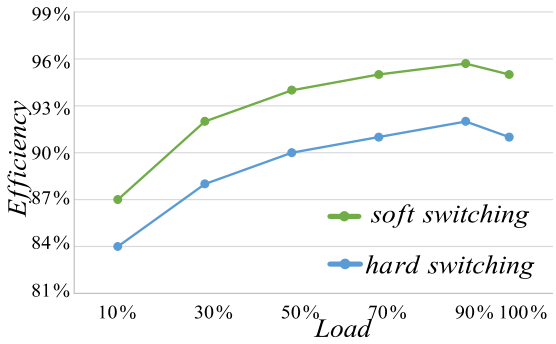

Fig. 18. Efficiency curves of the PFC rectifier with APD and PFC rectifier with APD and ZVS at 10%–100% load.

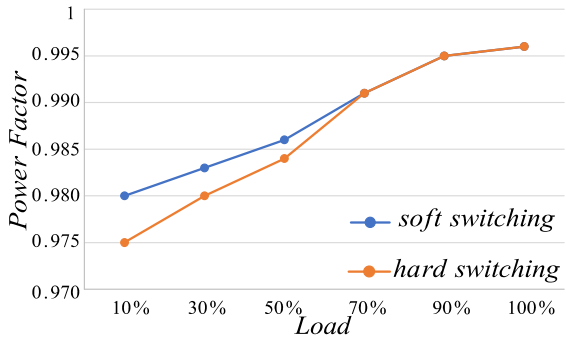

Fig. 19 Power factor of PFC rectifier with APD and PFC rectifier with APD and ZVS at 10%–100% load.

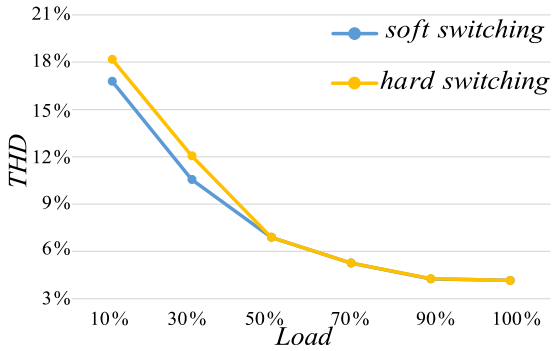

Fig. 20 THD of PFC rectifier with APD and PFC rectifier with APD and ZVS at 10%–100% load.

proposed rectifier is 95% and the PFC rectifier with APD is 91%, the auxiliary branch helps to increase the efficiency by 4%.

Figs. 19 and 20 show the power factor and THD under the condition of 10%–100% load. It can be seen that the power factor and THD of the proposed circuit are almost the same as the original circuit.

VIII. Conclusion

This article proposed a single-phase PFC rectifier with APD and ZVS. By adding an auxiliary diode-inductor branch, the main switches of the boost PFC circuit and the buck-type APD cell achieve ZVS turn-ON. Moreover, the diode of the boost PFC circuit and the auxiliary diode achieve ZCS turn-OFF. Consequently, the switching loss is reduced by 80%, and the total efficiency is improved by 4%. However, the drawback is that the lower switch of buck-type APD cell only achieves ZVS turn-ON in half of the grid period. Therefore, in future work, the method will be optimized to further improve the efficiency, and study the scalability of this method in other independent APD topologies.

References

[1] W. Lu, J. Han, S. Li, and H. H.-C. Iu, "Mitigating line frequency instability of boost PFC converter under proportional outer-voltage loop with additional third current-harmonic feedforward compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 11, pp. 4528–4541, Nov. 2019.

[2] X. Lin and F. Wang, "A novel single-phase AC–DC bridgeless boost converter for PFC application," *Int. J. Electron. Lett.*, vol. 6, no. 1, pp. 98–113, Jan. 2018.

[3] Y. Liu, H. Zhang, H. Wang, H. Dan, M. Su, and X. Pan, "Peak and valley current control for cuk PFC converter to reduce capacitance," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 313–321, Jan. 2022.

[4] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-Link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep. 2014.

[5] Y. Liu, Y. Sun, M. Su, M. Zhou, Q. Zhu, and X. Li, "A single-phase PFC rectifier with wide output voltage and low-frequency ripple power decoupling," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5076–5086, Jun. 2018.

[6] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[7] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

[8] J. Itoh, T. Sakuraba, K. Kusaka, H. Watanabe, and K. Furukawa, "Comparison of circuit topologies for active power decoupling toward high power density," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, 2016, pp. 421–428.

[9] S. Xie *et al.*, "Adaptive power decoupling control for single-phase converter with unbalanced DC-Split-Capacitor circuit," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 12127–12136, Oct. 2021.

[10] H. Li, K. Zhang, and H. Zhao, "Active DC-link power filter for single phase PWM rectifiers," in *Proc. IEEE Int. Conf. Power Electron.*, 2011, pp. 2920–2926.

[11] H. Li, K. Zhang, and H. Zhao, "DC-link active power filter for high-power single-phase PWM converters," *J. Power Electron.*, vol. 12, no. 3, pp. 458–467, May 2012.

[12] N. Deshmukh, S. Prabhakar, and S. Anand, "Power loss reduction in buck converter based active power decoupling circuit," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4316–4325, Apr. 2021.

[13] J. He, X. Ruan, and L. Zhang, "Adaptive voltage control for bidirectional converter in flicker-free electrolytic capacitor-less AC–DC LED driver," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 320–324, Jan. 2017.

[14] B. Koushki, P. Jain, and A. Bakhshai, "Minimum conduction loss ZVS control for buck-type active filter operating as decoupling circuit," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1322–1328.

[15] B. Koushki, P. Jain, and A. Bakhshai, "A bi-directional AC-DC converter for electric vehicle with no electrolytic capacitor," in *Proc. IEEE Int. Symp. Power Electron. for Distrib. Gener. Syst.*, 2016, pp. 1–8.

[16] N. Einabadi, E. Adib, and H. Farzanehfard, "New soft switching parallel PFC circuit," in *Proc. 6th Power Electron., Drive Syst. Technol. Conf.*, 2015, pp. 561–566.

[17] S. Kim and P. N. Enjeti, "A parallel-connected single phase power factor correction approach with improved efficiency," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 87–93, Jan. 2004.

[18] Z. Shan, X. Chen, S. Fan, G. Yuan, and C. K. Tse, "Resonant Switched-capacitor auxiliary circuit for active power decoupling in electrolytic Capacitor-less AC/DC LED drivers," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 866–871.

[19] Z. Shan, X. Chen, J. Jatskevich, and C. K. Tse, "An AC-DC LED driver with an additional active rectifier and a unidirectional auxiliary circuit for AC power ripple isolation," *IEEE Trans. Power Electron.*, vol. 34, no.no. 1, pp. 685–699, Jan. 2019.
[20] M. Chen, Z. Ye, Y. Chen, and D. Xu, "Zero-Voltage-switching single-phase full-bridge inverter with active power decoupling," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 571–582, Jan. 2021.
[21] Y. Chen *et al.*, "A ZVS grid-connected full-bridge inverter with a novel ZVS SPWM scheme," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3626–3638, May 2016.
[22] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 89–95.
[23] D. Graovac, M. Pürschel, and A. Kiep, *MOSFET Power Losses Calculation Using the Data-Sheet Parameters*. Neubiberg, Germany: Infineon, 2006. [Online]. Available: http://www.scribd.com/doc/34308439/MOSFET-Power-Losses-Calculation-Using-the-Data-Sheet-Parameters
[24] M. Bartoli, A. Reatti, and M. K. Kazimierczuk, "Minimum copper and core losses power inductor design," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 31st IAS Annu. Meeting*, 1996, vol. 3, pp. 1369–1376.
[25] R. P. Wojda and M. K. Kazimierczuk, "Analytical optimization of solid–round-wire windings," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 1033–1041, Mar. 2013.
[26] Y. Liu, W. Zhang, Y. Sun, M. Su, G. Xu, and H. Dan, "Review and comparison of control strategies in active power decoupling," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14436–14455, Dec. 2021.
[27] H. Watanabe and J. Itoh, "Zero voltage switching scheme for flyback converter to ensure compatibility with active power decoupling capability," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 896–903.

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