Accurate Steady-State Modeling and Design Based on State Trajectory Analysis for *LCC* Resonant Converter With Voltage Doubler Rectifier

Jimin Chen, *Student Member, IEEE*, Han Peng, *Member, IEEE*, Yong Kang, *Senior Member, IEEE*, Jinglin Wu, and Xu Chu

***Abstract*—The *LCC* series–parallel resonant converter with a voltage doubler rectifier, widely used in X-ray machines, is required to meet an extremely wide output range. However, state-of-the-art models are based on fundamental harmonic approximation and cannot maintain good accuracy over the entire output range. The state trajectory method has the potential to achieve a full range of high accuracy without high complexity, but it only applies to simple topologies, like *LCC* with a full-bridge rectifier. For *LCC* with a voltage multiplier, the capacitors in the multiplier are involved in the resonance, which can be modeled as a five-element resonant circuit. Moreover, the conduction sequence of components in the minor mode is different from that in the major mode, which is usually ignored in the steady-state model. The influence of the output capacitance of power transistors on the state trajectory is so unclear that the model accuracy decreases considerably at high frequencies. In this article, the equivalent parallel resonant capacitance is derived through the current distribution. The steady-state model of the *LCC* converter with a voltage doubler rectifier is developed for both major mode and minor mode. The deviation of the state trajectory and modeling accuracy induced by the output capacitor is investigated. Based on the proposed model and device stress analysis, the design procedure for *LCC* under a wide operation range is presented. The simulations and experiments verify the accuracy of the model and the validity of the design method. The simulation mismatches are less than 2.3% over the entire output range. The maximum experimental mismatch is 15%.**

***Index Terms*—Converter design, *LCC* resonant converter, state trajectory, steady-state model, voltage doubler rectifier, wide operation range.**

Manuscript received September 19, 2021; revised February 23, 2022; accepted March 26, 2022. Date of publication April 7, 2022; date of current version May 23, 2022. This work was supported in part by the National Natural Science Foundation of China under Grant 52007077 and in part by United Imaging Healthcare Company. Recommended for publication by Associate Editor A. Safaee. *(Corresponding author: Han Peng.)*

Jimin Chen, Han Peng, and Yong Kang are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: jm_chen@hust.edu.cn; pengh@hust.edu.cn; ykang@hust.edu.cn).

Jinglin Wu and Xu Chu are with the United Imaging Healthcare Company, Shanghai 201807, China (e-mail: jinglin.wu@united-imaging.com; xu.chu@united-imaging.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3165591.

Digital Object Identifier 10.1109/TPEL.2022.3165591

I. Introduction

X-RAY machines, like digital radiography and computed tomography, are widely used in medical diagnosis. A high-voltage generator (HVG), as the key equipment in an X-ray machine, provides direct current (dc) high-voltage pulses with width ranging from several milliseconds to seconds to the X-ray tube [1], [2]. The output range of a typical 50-kW HVG is shown in Fig. 1 [3], where the output voltage, output current, and load resistance can vary up to 150 times. The *LCC* series–parallel resonant converter (SPRC) with a voltage doubler rectifier, as shown in Fig. 2, is prevalent for HVG due to soft switching capability, high gain, and easy integration of HV transformer parasitic parameters [4]–[7]. The converter operating in above resonance region is concerned for power transistors zero-voltage switching (ZVS) [8], [9].

An appropriate frequency range and acceptable resonant component stresses under the entire output range are important for an *LCC* converter design. An accurate analytical model reduces the designers' reliance on the experience and useless trials. However, most of the state-of-the-art models of *LCC* with a voltage doubler rectifier are based on fundamental harmonic approximation [4], [10], which cannot maintain high precision under a wide output range due to the neglect of high-order harmonics [11]–[13]. The state trajectory method [14]–[18] keeps a good balance between accuracy and complexity and is promising for *LCC* converter modeling with a wide output range. However, there are still some limitations. First of all, only the converter with a full-bridge rectifier was modeled [15], [16], [19]. The parallel resonant capacitor C_{p} was bypassed by the load in the rectifier's conducting stage. The converter with a full-bridge rectifier was simplified as an L_{s}–C_{s} series resonant circuit, shown in Fig. 3(a). This model is not suitable for the *LCC* converter with a voltage doubler rectifier since C_{p} and voltage doubler capacitors all participate in the resonance process when the voltage doubler rectifier conducts. Multiple resonant elements make the conductive condition of the rectifier, the resonance process, and the state trajectory more complicated. Moreover, the minor operation mode of the *LCC* converter with a voltage double rectifier has not been discussed in prior studies [4], [10]. The operation mode of the *LCC* converter can be divided into major mode and minor mode according to the sequence of v_{AB}'s switching and rectifier's conducting. When

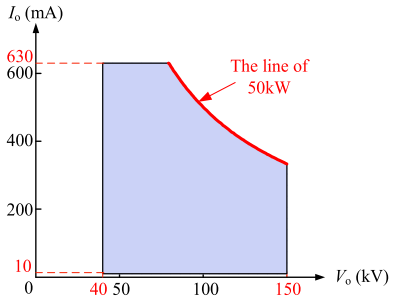

Fig. 1. Typical output range of a 50-kW HVG.

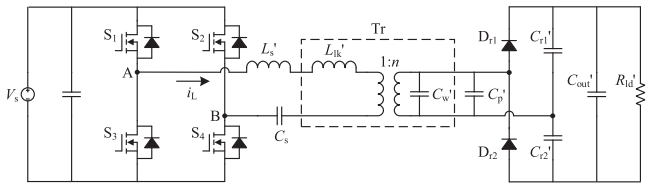

Fig. 2. Topology of *LCC* SPRC with a voltage doubler rectifier and a *C* filter.

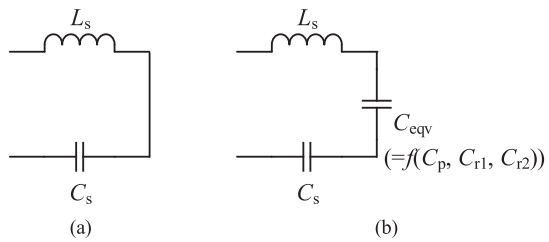

Fig. 3. Difference of resonant characteristics for *LCC* SPRC with (a) full-bridge rectifier or (b) voltage doubler rectifier.

v_{AB}'s switching at t_3 lags behind the rectifier's conducting at t_2, as shown in Fig. 4, it is considered as the major mode. When the time sequencing is opposite, it is considered as minor mode, as depicted in Fig. 5. The operating mode of the *LCC* converter changes as the converter load varies [20], [21]. The model of the minor mode is less studied [22], [23], which is important for applications with a wide output range. Second, the switching of drain–source voltage (v_{ds}) becomes a ramp trend due to the output capacitance of power transistors and the extra snubber capacitor for turn-OFF loss reduction [24]. The degradation of modeling accuracy caused by the capacitance has not been discussed in the literature. The influence of the output capacitances on the state trajectory is urgently needed to be clarified with the increasing switching frequencies. Third, preset parameters are usually required in the design of *LCC* converters, such as normalized switching frequency in [25], normalized switching frequency and parallel-to-series capacitor ratio in [24], and power factor, conduction angle, and quality factor in [10]. It is empirically driven and requires repeated attempts and iterations from initial parameters to the final result, which wastes a lot of labor costs.

A steady-state model is proposed in this article to provide precise design guidelines for the *LCC* converter with a voltage doubler rectifier under a wide operation range. The main contributions of this article can be summarized as follows.

1) For the problem of ignoring the voltage doubler rectifier in state trajectory analysis, the equivalent parallel resonant capacitance is acquired based on the current distribution between C_p and voltage doubler capacitors, which is the basis for establishing the steady-state model of the *LCC* converter with a voltage doubler rectifier. In addition, a steady-state model, including major mode and minor mode, is established for the *LCC* converter with a voltage doubler rectifier to provide extremely high accuracy over a wide operation range.
2) To solve the modeling error caused by the parasitic output capacitor of the power transistor, a state trajectory considering output capacitance is developed. The impact of output capacitance is analyzed quantitatively. Furthermore,

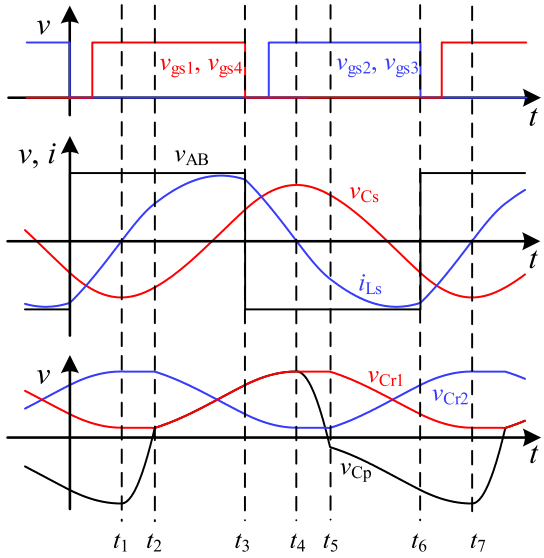

Fig. 4. Typical steady-state waveforms of the converter in the major mode.

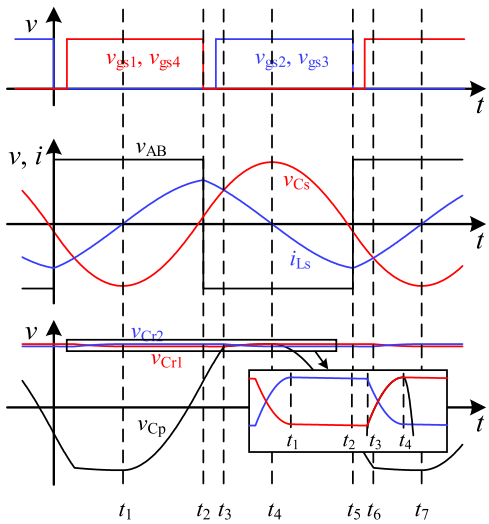

Fig. 5. Typical steady-state waveforms of the converter in the minor mode.

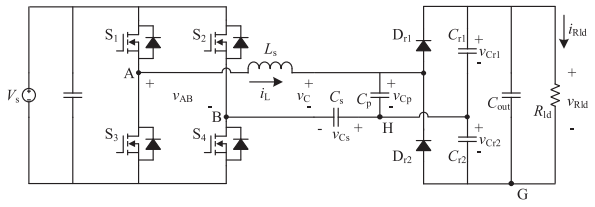

Fig. 6. Topology of *LCC* SPRC with transformer canceled.

the maximum acceptable output capacitance under a certain modeling error is revealed, which provides guidelines for power transistor selections.

3) To overcome the current limitation of *LCC* designed based on experience, a quantitative method for determining the *LCC* parameters under a wide output range is proposed. The design process can be fully automated.

The organizations of this article are as follows. The state trajectory of the converter is obtained, and the steady-state models for major mode and minor mode are proposed in Sections II–IV. The component stresses are demonstrated based on the state trajectory and steady-state model in Section V. The effect of the output capacitor on the model for the minor mode is investigated in Section VI. In Section VII, a nonempirical design process considering a wide output range is shown. To verify the proposed model, both simulation and experimental results are given in Section VIII. The proposed model is compared with the state of arts in Section IX. Finally, Section X concludes the article.

II. Assumptions and Normalization

The following basic assumptions are used in the analysis and modeling.

1) All the switches, diodes, inductors, and capacitors are considered ideal components.
2) Magnetizing inductance is neglected in transformer modeling, with its leakage inductance L_{lk}' and winding capacitance C_w' integrated into the resonant tank as part of the series inductance and parallel capacitance, respectively.
3) All the capacitors in the voltage doubler rectifier are the same.
4) The ripple of the output voltage is neglected.

As depicted in Fig. 6, components on the secondary side are transferred to the primary side as follows: $L_s = L_s' + L_{lk}'$, $C_p = n^2\,(C_p' + C_w')$, $C_{r1} = n^2\,C_{r1}'$, $C_{r2} = n^2\,C_{r2}'$, $C_{out} = n^2\,C_{out}'$, and $R_{ld} = R_{ld}' / n^2$, where n is the turn ratio of the transformer. With the assumptions, $C_{r1} = C_{r2} = C_r$.

The ratio of capacitances C_{ps} and C_{rs} is defined as $C_{ps} = C_p/C_s$ and $C_{rs} = C_r/C_s$, respectively. For an intuitive characteristics acquisition, the model is normalized with the following base quantities

$$V_{base} = V_s,\ Z_{base} = \sqrt{\frac{L_s}{C_T}},\ I_{base} = V_s\sqrt{\frac{C_T}{L_s}},$$

$$\omega_{base} = \frac{1}{\sqrt{L_s C_T}},\ f_{base} = \frac{1}{2\pi\sqrt{L_s C_T}}$$

where $C_T = C_s\frac{C_{ps}+2C_{rs}}{1+C_{ps}+2C_{rs}}$.

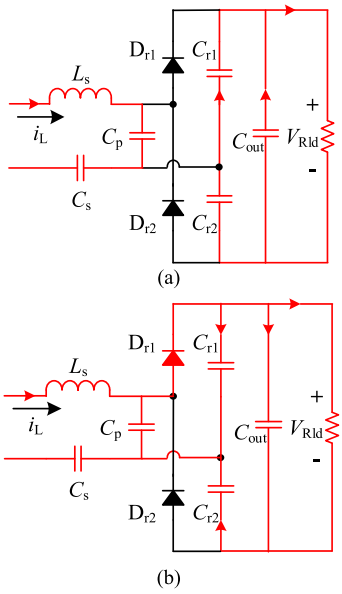

Fig. 7. Current path of resonant tank and rectifier in the intervals (a) t_1–t_2 and (b) t_2–t_4.

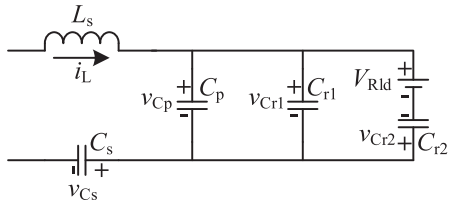

Fig. 8. Equivalent circuit of resonant tank and rectifier in the interval t_2–t_4.

Normalized quantities are denoted by adding "n" to their subscripts as follows: $i_{nL} = i_L / I_{base}$, $v_{nCs} = v_{Cs} / V_{base}$, $v_{nCp} = v_{Cp} / V_{base}$, $V_{nRld} = V_{Rld} / V_{base}$, and $I_{nRld} = I_{Rld} / I_{base}$. A new normalized variable v_{nC} is defined as $v_{nC} = v_{nCs} + v_{nCp}$.

III. Analysis and Modeling for the Major Mode

A. Derivation of Equivalent Parallel Resonant Capacitance

When the reconnection between rectifier and C_p is behind v_{AB}'s switching, the converter is defined as working under the major mode. As shown in Fig. 4, the periodic waveforms can be divided into six subintervals as t_1–t_7, where v_{gs1}–v_{gs4} are the gate driver signals of the MOSFET S_1–S_4.

t_1–t_2: The voltage doubler rectifier is blocked in this interval, as illustrated in Fig. 7(a). C_p is charged by i_L: $i_L = C_p \cdot dv_{Cp}/dt$.

t_2–t_4: As shown in Fig. 7(b), the upper diode D_{r1} of the voltage doubler rectifier conducts. C_{r1} and C_{r2} are connected to the resonant tank. C_p and C_{r1} are charged by i_L, whereas C_{r2} is discharged at the same time. The equivalent circuit in this interval is shown in Fig. 8. Following KVL and considering output voltage V_{Rld} being constant, it can be derived as follows:

$$\frac{dv_{Cp}}{dt} = \frac{dv_{Cr1}}{dt} = -\frac{dv_{Cr2}}{dt}. \tag{1}$$

And the resonant inductor current i_{L} can be expressed follows:

$$i_{\mathrm{L}} = C_{\mathrm{p}}\frac{dv_{\mathrm{Cp}}}{dt} + C_{\mathrm{r1}}\frac{dv_{\mathrm{Cr1}}}{dt} - C_{\mathrm{r2}}\frac{dv_{\mathrm{Cr2}}}{dt}. \tag{2}$$

Combining (1) and (2), $i_{\mathrm{L}} = (C_{\mathrm{p}} + C_{\mathrm{r1}} + C_{\mathrm{r2}})dv_{\mathrm{Cp}}/dt$ can be obtained.

Therefore, the equivalent parallel resonant capacitances for different resonant subintervals can be derived as follows:

$$C_{\mathrm{p\_eqv}} = \begin{cases} C_{\mathrm{p}} & t_1 \le t < t_2 \\ C_{\mathrm{p}} + C_{\mathrm{r1}} + C_{\mathrm{r2}} & t_2 \le t \le t_4 \end{cases}. \tag{3}$$

Equivalent parallel resonant capacitances in subintervals t_4–t_5 and t_5–t_7 are the same as subintervals t_1–t_2 and t_2–t_4, respectively.

B. State Trajectory Equations

From the state equation of the converter [16] and the equivalent parallel resonance capacitance mentioned above, the trajectory equations for normalized resonant current $i_{\mathrm{nL}}(t)$ and resonant capacitor voltage $v_{\mathrm{nC}}(t)$ in different subintervals can be derived. Here, the interval t_1–t_2 is taken as an example to illustrate the acquisition of the state trajectory for a better insight into the time-related and space-related angle.

t_1–t_2: The equations to describe the resonant converter in this interval are the following:

$$\begin{cases} L_{\mathrm{s}}\frac{di_{\mathrm{L}}(t)}{\mathrm{d}t} = V_{\mathrm{s}} - v_{\mathrm{Cs}}(t) - v_{\mathrm{Cp}}(t) \\ C_{\mathrm{s}}\frac{dv_{\mathrm{Cs}}(t)}{\mathrm{d}t} = i_{\mathrm{L}}(t) \\ C_{\mathrm{p\_eqv}}\frac{dv_{\mathrm{Cp}}(t)}{dt} = i_{\mathrm{L}}(t) \end{cases}. \tag{4}$$

Normalizing (4) to obtain the following:

$$\begin{cases} \frac{di_{\mathrm{nL}}(t)}{dt} = [1 - v_{\mathrm{nC}}(t)] \cdot \omega_{\mathrm{base}} \\ \frac{dv_{\mathrm{nC}}(t)}{dt} = i_{\mathrm{nL}}(t) \cdot \frac{C_{\mathrm{T}}}{C_{\mathrm{M}}} \cdot \omega_{\mathrm{base}} \end{cases}. \tag{5}$$

The solution of (5) can be expressed as follows:

$$\begin{cases} i_{\mathrm{nL}}(t) = \frac{[1-v_{\mathrm{nC}}(t_1)]}{\sqrt{C_{\mathrm{T}}/C_{\mathrm{M}}}} \sin\left[\sqrt{\frac{C_{\mathrm{T}}}{C_{\mathrm{M}}}}\omega_{\mathrm{base}}(t_2 - t_1)\right] \\ v_{\mathrm{nC}}(t) = 1 - [1 - v_{\mathrm{nC}}(t_1)]\cos\left[\sqrt{\frac{C_{\mathrm{T}}}{C_{\mathrm{M}}}}\omega_{\mathrm{base}}(t_2 - t_1)\right] \end{cases}. \tag{6}$$

Therefore, the trajectory equations for this interval can be obtained as follows:

$$\frac{(v_{\mathrm{nC}}(t) - 1)^2}{r_1^2} + \frac{i_{\mathrm{nL}}^2(t)}{\frac{r_1^2}{C_{\mathrm{T}}/C_{\mathrm{M}}}} = 1 \tag{7}$$

where $C_{\mathrm{M}} = C_{\mathrm{s}}\frac{C_{\mathrm{ps}}}{1+C_{\mathrm{ps}}}$, and $r_1 = 1 - v_{\mathrm{nC}}(t_1)$. $C_{\mathrm{T}}/C_{\mathrm{M}}$ is larger than 1, and the state trajectory for this interval is an ellipse with a center at (1, 0), as plotted with a solid line in Fig. 9. During t_1–t_2, the state of the circuit runs from $(v_{\mathrm{nC}}(t_1), 0)$ to $(v_{\mathrm{nC}}(t_2), i_{\mathrm{nL}}(t_2))$ along the elliptical arc. A space-related angle α', defined as $\alpha' = \arctan(\frac{i_{\mathrm{nL}}(t_2)}{1-v_{\mathrm{nC}}(t_2)})$, is corresponding to the elliptical arc. On the other hand, a time-related angle α is defined as $\alpha = \sqrt{\frac{C_{\mathrm{T}}}{C_{\mathrm{M}}}}\omega_{\mathrm{base}}(t_2 - t_1)$. The relationship between α and α' is acquired from (6) as $\alpha = \arctan(\sqrt{\frac{C_{\mathrm{T}}}{C_{\mathrm{M}}}}\tan\alpha')$. The time-related angle needs to be acquired from the conversion of the ellipse to the circle, in which the ellipse corresponds to the space-related angle.

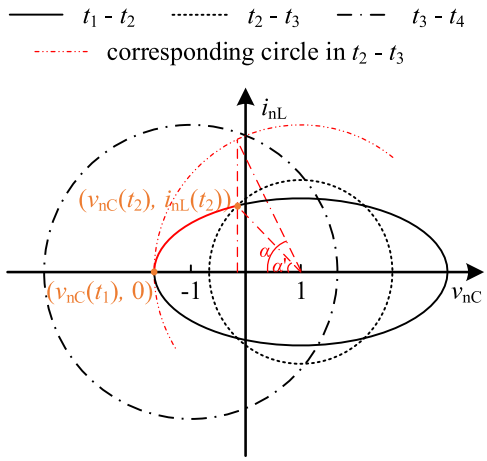

Fig. 9. State trajectories of different time intervals for the major mode in t_1–t_4.

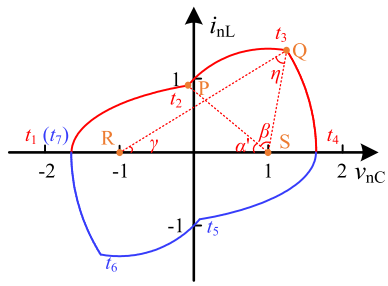

Fig. 10. Entire state trajectory for the major mode.

t_2–t_3: The trajectory equations for this interval can be obtained as follows:

$$(v_{\mathrm{nC}}(t) - 1)^2 + i_{\mathrm{nL}}^2(t) = r_2^2 \tag{8}$$

where $r_2 = \sqrt{[1 - v_{\mathrm{nC}}(t_2)]^2 + i_{\mathrm{nL}}^2(t_2)}$. It can be seen that the state trajectory in this interval is a circle shape with a center at (1, 0) and a radius of r_2, as plotted with dotted lines in Fig. 9. The space-related angle of the circular arc is the same as the time angle of this arc. Thus, only the time-related angle is marked in later figures.

t_3–t_4: The trajectory equations for this interval can be obtained as follows:

$$(v_{\mathrm{nC}}(t) + 1)^2 + i_{\mathrm{nL}}^2(t) = r_3^2 \tag{9}$$

where $r_3 = \sqrt{[v_{\mathrm{nC}}(t_4) + 1]^2 + i_{\mathrm{nL}}^2(t_4)}$. Equation (9) illustrates the state trajectory in this interval as a circle with a center at $(-1, 0)$ and a radius of r_3, as also shown with dashed lines in Fig. 9.

The state trajectories in subintervals t_4–t_7 and in subintervals t_1–t_4 are symmetric with respect to the origin of the coordinate. All segments of the trajectory in six subintervals are combined in Fig. 10.

C. Characteristics of Time-Domain Waveforms

From the time-domain waveforms, essential factors, such as the coordinates of the start and end points of each interval in the trajectory, can be represented by circuit parameters, switching frequency, and converter output.

1) State $\mathrm{v}_{nC}(\mathrm{t}_1)$*:* Applying KCL to the junction of branches where R_{ld}, C_{out}, and C_{r2} are located (node G in Fig. 6) and integrating from t_1 to t_4

$$\int_{t_1}^{t_4} i_{\mathrm{Rld}}dt + \int_{t_1}^{t_4} i_{\mathrm{Cout}}dt + \int_{t_1}^{t_4} i_{\mathrm{Cr2}}dt = 0 \tag{10}$$

i_{Rld} satisfies $\int_{t_1}^{t_4} i_{\mathrm{Rld}}dt = \frac{T_{\mathrm{s}}}{2} I_{\mathrm{Rld}}$, where I_{Rld} is the average of converter output current. With the assumption of constant output voltage, $\int_{t_1}^{t_4} i_{\mathrm{Cout}}dt = 0$ can be derived.

The correlation between the voltage and current of C_{r2} satisfies $\int_{t_1}^{t_4} i_{\mathrm{Cr2}}dt = C_r[v_{\mathrm{Cr2}}(t_4) - v_{\mathrm{Cr2}}(t_1)]$.

Consequently, the normalized state $v_{\mathrm{nCr2}}(t_1)$ can be derived from (10) as

$$v_{\mathrm{nCr2}}(t_1) = \frac{\pi \cdot C_{\mathrm{T}}}{2F_{\mathrm{n}} \cdot C_{\mathrm{r}}} I_{\mathrm{nRld}} + \frac{1}{2} V_{\mathrm{nRld}} \tag{11}$$

in which, $F_{\mathrm{n}} = f_{\mathrm{s}} / f_{\mathrm{base}}$, is the normalized switching frequency.

During t_1–t_2, the ratio of C_{p} to C_{s} complies with the expression

$$\frac{C_{\mathrm{p}}}{C_{\mathrm{s}}} = \frac{v_{\mathrm{Cs}}(t_2) - v_{\mathrm{Cs}}(t_1)}{v_{\mathrm{Cp}}(t_2) - v_{\mathrm{Cp}}(t_1)} \tag{12}$$

Equation (13) is deduced via applying KCL to the node H in Fig. 6 and integrating from t_2 to t_4

$$\int_{t_2}^{t_4} i_{\mathrm{L}}dt = \int_{t_2}^{t_4} i_{\mathrm{Cp}}dt + \int_{t_2}^{t_4} i_{\mathrm{Cr1}}dt - \int_{t_2}^{t_4} i_{\mathrm{Cr2}}dt. \tag{13}$$

The waveform of $v_{\mathrm{Cr1}}(t)$ is the same as $v_{\mathrm{Cr2}}(t)$ after a half period shift. $v_{\mathrm{Cs}}(t)$ and $v_{\mathrm{Cp}}(t)$ have the odd harmonic characteristic. Combining (12) and (13), $v_{\mathrm{nCs}}(t_1)$ can be calculated as follows:

$$v_{\mathrm{nCs}}(t_1) = V_{\mathrm{nRld}} \cdot C_{\mathrm{rs}} - v_{\mathrm{nCr2}}(t_1) \cdot (C_{\mathrm{ps}} + 2 \cdot C_{\mathrm{rs}}). \tag{14}$$

Consequently, $v_{\mathrm{nC}}(t_1)$ can be derived from (11) and (14) as follows:

$$v_{\mathrm{nC}}(t_1) = -\frac{(C_{\mathrm{ps}} + 2C_{\mathrm{rs}}) I_{\mathrm{nRld}}\pi}{2C_{\mathrm{rs}}F_{\mathrm{n}}} - \frac{1}{2}(C_{\mathrm{ps}} + 1) V_{\mathrm{nRld}}. \tag{15}$$

2) State $\mathrm{v}_{nC}(\mathrm{t}_2)$*:* From (12), $v_{\mathrm{Cs}}(t_2)$ can be deduced as follows:

$$v_{\mathrm{Cs}}(t_2) = C_{\mathrm{ps}}[v_{\mathrm{Cp}}(t_2) - v_{\mathrm{Cp}}(t_1)] + v_{\mathrm{Cs}}(t_1). \tag{16}$$

With the characteristic of $v_{\mathrm{Cp}}(t)$ and $v_{\mathrm{Cr2}}(t)$, $v_{\mathrm{Cs}}(t_2)$ is further expressed as follows:

$$v_{\mathrm{Cs}}(t_2) = C_{\mathrm{ps}}V_{\mathrm{Rld}} + v_{\mathrm{Cs}}(t_1). \tag{17}$$

Therefore, $v_{\mathrm{nC}}(t_2)$ is calculated as follows:

$$v_{\mathrm{nC}}(t_2) = \frac{1}{2}\left[(C_{\mathrm{ps}} + 1) V_{\mathrm{nRld}} - \frac{(C_{\mathrm{ps}} + 2C_{\mathrm{rs}}) I_{\mathrm{nRld}}\pi}{C_{\mathrm{rs}}F_{\mathrm{n}}}\right]. \tag{18}$$

D. Characteristics of State Trajectory

In Fig. 10, P is on the elliptic arc of t_1–t_2, so the following equation can be deduced from (7) and (15):

$$i_{\mathrm{nL}}^2(t_2) = \frac{(1 + C_{\mathrm{ps}} + 2C_{\mathrm{rs}})(2C_{\mathrm{rs}}F_{\mathrm{n}} + (C_{\mathrm{ps}} + 2C_{\mathrm{rs}}) I_{\mathrm{nRld}}\pi) C_{\mathrm{ps}}V_{\mathrm{nRld}}}{C_{\mathrm{rs}}(C_{\mathrm{ps}} + 2C_{\mathrm{rs}}) F_{\mathrm{n}}}. \tag{19}$$

P is also on the elliptic arc of t_2–t_3, and thus the following equation is obtained from (8):

$$r_2^2 = (v_{\mathrm{nC}}(t_2) - 1)^2 + i_{\mathrm{nL}}^2(t_2). \tag{20}$$

Q is on both the arc of t_2–t_3 and the arc of t_3–t_4. Equation (21) is acquired according to (8) and (9)

$$r_2^2 - (v_{\mathrm{nC}}(t_3) - 1)^2 = r_3^2 - (v_{\mathrm{nC}}(t_3) + 1)^2. \tag{21}$$

Combining (18)–(21), $v_{\mathrm{nC}}(t_4) = -v_{\mathrm{nC}}(t_1)$, and $i_{\mathrm{nL}}(t_4) = 0$, the following equation is derived:

$$v_{\mathrm{nC}}(t_3) = \left(\frac{I_{\mathrm{nRld}}\pi}{2F_{\mathrm{n}}} + \frac{C_{\mathrm{rs}}}{C_{\mathrm{ps}} + 2C_{\mathrm{rs}}}\right) V_{\mathrm{nRld}}. \tag{22}$$

E. Steady-State Model for the Major Mode

Besides α, other time-related angles are defined as follows: $\beta = \omega_{\mathrm{base}}(t_3 - t_2)$ and $\gamma = \omega_{\mathrm{base}}(t_4 - t_3)$. The normalized switching frequency F_{n} is satisfied by

$$\alpha\sqrt{\frac{C_{\mathrm{M}}}{C_{\mathrm{T}}}} + \beta + \gamma = \frac{\pi}{F_{\mathrm{n}}} \tag{23}$$

where the time-related angles can be derived according to its relationship with space-related angle

$$\alpha = \arccos\left(\frac{1 - v_{\mathrm{nC}}(t_2)}{1 - v_{\mathrm{nC}}(t_1)}\right) \tag{24}$$

$$\beta = \arcsin\left(\frac{v_{\mathrm{nC}}(t_3) - 1}{r_2}\right) - \arctan\left(\frac{v_{\mathrm{nC}}(t_2) - 1}{i_{\mathrm{nL}}(t_2)}\right) \tag{25}$$

$$\gamma = \arccos\left(\frac{1 + v_{\mathrm{nC}}(t_3)}{1 - v_{\mathrm{nC}}(t_1)}\right). \tag{26}$$

Substituting (15), (18), (20), and (22) into (23), the steady-state model among the converter normalized outputs (V_{nRld} and I_{nRld}), circuit parameters (C_{ps} and C_{rs}), and normalized switching frequency (F_{n}) is obtained by forcing $f_{\mathrm{VnRld\&InRld}}(C_{\mathrm{ps}}, C_{\mathrm{rs}}, F_{\mathrm{n}}, V_{\mathrm{nRld}}, I_{\mathrm{nRld}}) = 0$. The expression of $f_{\mathrm{VnRld\&InRld}}(\bullet)$ is expressed in (28).

IV. Analysis and Modeling for the Minor Mode

Minor mode usually occurs at light loads. As the load decreases, the interval of t_1–t_2 in Fig. 4 becomes longer, during which the rectifier is disconnected from C_{p} and the load is only powered by C_{out}. When v_{Cp} equaling to v_{Cr1} (i.e., t_3 in Fig. 5) lags behind the time point of v_{AB}'s switching from $+V_{\mathrm{s}}$ to $-V_{\mathrm{s}}$ (i.e., t_2 in Fig. 5), the converter can be recognized as in minor mode. Due to symmetrical waveforms, the analysis below mainly focuses on the subintervals t_1–t_4.

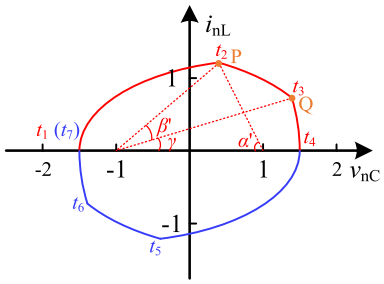

Fig. 11. Entire state trajectory for the minor mode.

A. Derivation of Equivalent Parallel Resonant Capacitance

In minor mode, the voltage doubler rectifier is blocked in t_1–t_3 and conducted in t_3–t_4, whose equivalent circuits are the same as those shown in Fig. 7(a) and (b), respectively. Consequently, the equivalent parallel resonant capacitances for different subintervals can be expressed as follows:

$$C_{\text{p\_eqv}} = \begin{cases} C_{\text{p}} & t_1 \le t < t_3 \\ C_{\text{p}} + C_{\text{r1}} + C_{\text{r2}} & t_3 \le t \le t_4 \end{cases} \tag{27}$$

B. State Trajectory Equations

Similarly, the normalized trajectory equations for minor mode in different intervals can be obtained. It shows that the trajectory equations in the intervals of t_1–t_2 and t_3–t_4 are the same as t_1–t_2 and t_3–t_4 in the major mode, respectively. The trajectory equation in t_2–t_3 is expressed as follows:

$$\frac{\left(v_{\text{nC}}\left(t\right)+1\right)^2}{r_2^2} + \frac{i_{\text{nL}}^2\left(t\right)}{\frac{r_2^2}{C_{\text{T}}/C_{\text{M}}}} = 1 \tag{29}$$

where $r_2 = \sqrt{\left[v_{\text{nC}}(t_2)+1\right]^2 + \frac{C_{\text{T}}}{C_{\text{M}}} i_{\text{nL}}^2(t_2)}$. $C_{\text{T}}/C_{\text{M}}$ is larger than 1, and the state trajectory for this interval is an ellipse with a center at $(-1, 0)$, whose ratio of ellipse's major and minor axes is the same as in t_1–t_2. The entire state trajectory for minor mode is plotted in Fig. 11.

C. Characteristics of Time-Domain Waveforms

$v_{\text{nC}}(t_1)$ and $v_{\text{nC}}(t_3)$ for the minor mode are the same as in the major mode condition as

$$v_{\text{nC}}\left(t_1\right) = -\frac{\left(C_{\text{ps}}+2C_{\text{rs}}\right) I_{\text{nRld}}\pi}{2C_{\text{rs}}F_{\text{n}}} - \frac{1}{2}\left(C_{\text{ps}}+1\right) V_{\text{nRld}} \tag{30}$$

$$v_{\text{nC}}\left(t_3\right) = \frac{1}{2}\left[\left(C_{\text{ps}}+1\right) V_{\text{nRld}} - \frac{\left(C_{\text{ps}}+2C_{\text{rs}}\right) I_{\text{nRld}}\pi}{C_{\text{rs}}F_{\text{n}}}\right]. \tag{31}$$

D. Characteristics of State Trajectory

In Fig. 11, Q is on the arc of t_3–t_4, then the following equation can be derived from (9)

$$\left(v_{\text{nC}}\left(t_3\right)+1\right)^2 + i_{\text{nL}}^2\left(t_3\right) = \left(v_{\text{nC}}\left(t_4\right)+1\right)^2 + i_{\text{nL}}^2\left(t_4\right). \tag{32}$$

Combining (30)–(32), $v_{\text{nC}}(t_4) = -v_{\text{nC}}(t_1)$, and $i_{\text{nL}}(t_4) = 0$, $i_{\text{nL}}(t_3)$ is expressed as follows:

$$i_{\text{nL}}\left(t_3\right) = \sqrt{\frac{\left(C_{\text{ps}}+2C_{\text{rs}}\right)\left(2+V_{\text{nRld}}+C_{\text{ps}}V_{\text{nRld}}\right) I_{\text{nRld}}\pi}{C_{\text{rs}}F_{\text{n}}}}. \tag{33}$$

Q is also on the elliptic arc of t_2–t_3, hence the following equation is derived from (29):

$$r_2^2 = \left(v_{\text{nC}}\left(t_3\right)+1\right)^2 + i_{\text{nL}}^2\left(t_3\right)\cdot\frac{C_{\text{T}}}{C_{\text{M}}}. \tag{34}$$

P is on both the elliptic arc of t_1–t_2 and the elliptic arc of t_2–t_3. Equation (35) is obtained from (7) and (29)

$$\frac{r_1^2 - \left(v_{\text{nC}}\left(t_2\right)-1\right)^2}{C_{\text{T}}/C_{\text{M}}} = \frac{r_2^2 - \left(v_{\text{nC}}\left(t_2\right)+1\right)^2}{C_{\text{T}}/C_{\text{M}}} \tag{35}$$

where $v_{\text{nC}}(t_2)$ and $i_{\text{nL}}(t_2)$ are derived by combining (32)–(35)

$$v_{\text{nC}}\left(t_2\right) = \frac{\left(C_{\text{ps}}+2C_{\text{rs}}\right)\left(2+\left(1+C_{\text{ps}}\right)V_{\text{nRld}}\right) I_{\text{nRld}}\pi}{2C_{\text{ps}}\left(1+C_{\text{ps}}+2C_{\text{rs}}\right)F_{\text{n}}} \tag{36}$$

$$i_{\text{nL}}\left(t_2\right) = \sqrt{\left[\left(1-v_{\text{nC}}\left(t_1\right)\right)^2 - \left(v_{\text{nC}}\left(t_2\right)-1\right)^2\right]\cdot\frac{C_{\text{M}}}{C_{\text{T}}}}. \tag{37}$$

$$\begin{aligned} f_{\text{VnRld\&InRld}}\left(C_{\text{ps}}, C_{\text{rs}}, F_{\text{n}}, V_{\text{nRld}}, I_{\text{nRld}}\right) &= \sqrt{\frac{C_{\text{ps}}\left(1+C_{\text{ps}}+2C_{\text{rs}}\right)}{\left(1+C_{\text{ps}}\right)\left(C_{\text{ps}}+2C_{\text{rs}}\right)}} \\ &\cdot \arccos\left[\frac{4F_{\text{n}}C_{\text{rs}}+2I_{\text{nRld}}\pi\left(C_{\text{ps}}+2C_{\text{rs}}\right)}{\left(C_{\text{ps}}+2C_{\text{rs}}\right)I_{\text{nRld}}\pi + F_{\text{n}}C_{\text{rs}}\left(\left(1+C_{\text{ps}}\right)V_{\text{nRld}}+2\right)} - 1\right] \\ &+ \arcsin\left[\frac{\frac{\left(2F_{\text{n}}C_{\text{rs}}+\left(C_{\text{ps}}+2C_{\text{rs}}\right)I_{\text{nRld}}\pi\right)V_{\text{nRld}}}{2F_{\text{n}}\left(C_{\text{ps}}+2C_{\text{rs}}\right)} - 1}{\sqrt{\frac{C_{\text{ps}}\left(1+C_{\text{ps}}+2C_{\text{rs}}\right)\left(2C_{\text{rs}}F_{\text{n}}+\left(C_{\text{ps}}+2C_{\text{rs}}\right)I_{\text{nRld}}\pi\right)V_{\text{nRld}}}{F_{\text{n}}C_{\text{rs}}\left(C_{\text{ps}}+2C_{\text{rs}}\right)}} + \left(\frac{1}{2}\left(1+C_{\text{ps}}\right)V_{\text{nRld}} - \frac{\left(C_{\text{ps}}+2C_{\text{rs}}\right)I_{\text{nRld}}\pi}{2C_{\text{rs}}F_{\text{n}}} - 1\right)^2}}\right] \\ &- \arctan\left[\frac{\sqrt{C_{\text{ps}}+2C_{\text{rs}}}\left(F_{\text{n}}C_{\text{rs}}\left(\left(1+C_{\text{ps}}\right)V_{\text{nRld}}-2\right) - \left(C_{\text{ps}}+2C_{\text{rs}}\right)I_{\text{nRld}}\pi\right)}{2\sqrt{\left(1+C_{\text{ps}}+2C_{\text{rs}}\right)\left(2F_{\text{n}}C_{\text{rs}}+\left(C_{\text{ps}}+2C_{\text{rs}}\right)I_{\text{nRld}}\pi\right)F_{\text{n}}C_{\text{ps}}C_{\text{rs}}V_{\text{nRld}}}}\right] \\ &+ \arccos\left[\frac{C_{\text{rs}}\left(\left(C_{\text{ps}}+2C_{\text{rs}}\right)V_{\text{nRld}}I_{\text{nRld}}\pi + 2F_{\text{n}}\left(C_{\text{ps}}+2C_{\text{rs}}+C_{\text{rs}}V_{\text{nRld}}\right)\right)}{\left(C_{\text{ps}}+2C_{\text{rs}}\right)\left(\left(C_{\text{ps}}+2C_{\text{rs}}\right)I_{\text{nRld}}\pi + F_{\text{n}}C_{\text{rs}}\left(\left(1+C_{\text{ps}}\right)V_{\text{nRld}}+2\right)\right)}\right] - \frac{\pi}{F_{\text{n}}}. \end{aligned} \tag{28}$$

E. Steady-State Model for the Minor Mode

Time-related angles of α, β, and γ for the minor mode are defined similarly to those for the major mode. The normalized switching frequency $F_{\rm n}$ is satisfied by

$$(\alpha+\beta)\sqrt{\frac{C_{\rm M}}{C_{\rm T}}}+\gamma=\frac{\pi}{F_{\rm n}} \tag{38}$$

where the time-related angles are

$$\alpha=\arccos\left(\frac{1-v_{\rm nC}\left(t_2\right)}{1-v_{\rm nC}\left(t_1\right)}\right) \tag{39}$$

$$\beta=\arcsin\left(\frac{v_{\rm nC}\left(t_3\right)+1}{r_2}\right)-\arcsin\left(\frac{v_{\rm nC}\left(t_2\right)+1}{r_2}\right) \tag{40}$$

$$\gamma=\arccos\left(\frac{1+v_{\rm nC}\left(t_3\right)}{1-v_{\rm nC}\left(t_1\right)}\right). \tag{41}$$

Therefore, the normalized steady-state model can be expressed as $f_{\rm VnRld\&InRld}(C_{\rm ps}, C_{\rm rs}, F_{\rm n}, V_{\rm nRld}, I_{\rm nRld})=0$, where $f_{\rm VnRld\&InRld}(\bullet)$ is shown in the following equation:

F. Boundary of the Major Mode and the Minor Mode

The analysis mentioned above about the minor mode is on the premise of $v_{\rm nC}(t_2)\le v_{\rm nC}(t_3)$, which can be used to conduct the boundary of the major mode and the minor mode as follows:

$$F_{\rm n}\begin{cases}\le F_{\rm n\_crit} & \text{for major mode}\\ \ge F_{\rm n\_crit} & \text{for minor mode}\end{cases} \tag{44}$$

where

$$F_{\rm n\_crit}=\frac{\left[\left(C_{\rm ps}+2C_{\rm rs}\right)+C_{\rm rs}V_{\rm nRld}\right]\left(C_{\rm ps}+2C_{\rm rs}\right)I_{\rm nRld}\pi}{\left(1+C_{\rm ps}+2C_{\rm rs}\right)C_{\rm ps}C_{\rm rs}V_{\rm nRld}}.$$

V. Component Stresses

Component stresses are critical to the design feasibility of high-voltage and high-power converters under a wide output range. From the state trajectory and the converter model mentioned above, the component rating can be derived for converter design guidance.

A. Peak Current of Resonant Inductor

As shown in Fig. 10, there are two scenarios to determine the normalized peak current of resonant inductor $I_{\rm nLpk}$ for the major mode. When $\alpha'+\beta<\pi/2$, $I_{\rm nLpk}$ is $I_{\rm nL}(t_3)$. When $\alpha'+\beta\ge\pi/2$, $I_{\rm nLpk}$ is equal to r_2. As depicted in Fig. 11 for the minor mode, $I_{\rm nLpk}$ is always equal to $I_{\rm nL}(t_2)$. Thus, the peak current $I_{\rm Lpk}$ is expressed as (43), in which the angles are obtained from (23) and (38) for major and minor modes, respectively.

B. Peak Voltage of Parallel Resonant Capacitor and Voltage Doubler Capacitor

From Figs. 4 and 5, the peak voltages in $C_{\rm r1}$ and $C_{\rm r2}$, represented by $V_{\rm Crpk}$, are the same in $C_{\rm p}$, denoted by $V_{\rm Cppk}$. $C_{\rm r2}$'s voltage peaks at t_1 for both major and minor modes. Considering (11), the peak voltage can be calculated as follows:

$$V_{\rm Cppk}=v_{\rm Cr2}\left(t_1\right)=\frac{1}{4}\left(\frac{I_{\rm Rld}}{C_{\rm r}f_{\rm s}}+2V_{\rm Rld}\right). \tag{45}$$

C. Peak Voltage of Series Resonant Capacitor

The peak voltage of the series resonant capacitor $V_{\rm Cspk}$ occurs at t_4 for both major and minor modes. Combining (11) and (14), $V_{\rm Cspk}$ can be calculated as follows:

$$V_{\rm Cspk}=\frac{C_{\rm p}+2C_{\rm r}}{4C_{\rm r}C_{\rm s}f_{\rm s}}\cdot I_{\rm Rld}+\frac{C_{\rm p}}{2C_{\rm s}}V_{\rm Rld}. \tag{46}$$

$$\begin{aligned}f_{\rm VnRld\&InRld}\left(C_{\rm ps},C_{\rm rs},F_{\rm n},V_{\rm nRld},I_{\rm nRld}\right)&=-\frac{\pi}{F_{\rm n}}+\arccos\left[\frac{2C_{\rm rs}F_{\rm n}-\left(C_{\rm ps}+2C_{\rm rs}\right)I_{\rm nRld}\pi+\left(1+C_{\rm ps}\right)C_{\rm rs}F_{\rm n}V_{\rm nRld}}{2C_{\rm rs}F_{\rm n}+\left(C_{\rm ps}+2C_{\rm rs}\right)I_{\rm nRld}\pi+\left(1+C_{\rm ps}\right)C_{\rm rs}F_{\rm n}V_{\rm nRld}}\right]\\&+\sqrt{\frac{C_{\rm ps}\left(1+C_{\rm ps}+2C_{\rm rs}\right)}{\left(1+C_{\rm ps}\right)\left(C_{\rm ps}+2C_{\rm rs}\right)}}\cdot\left\{\arccos\left[\frac{C_{\rm rs}\left(2C_{\rm ps}F_{\rm n}\left(1+C_{\rm ps}+2C_{\rm rs}\right)-\left(2+\left(1+C_{\rm ps}\right)V_{\rm nRld}\right)\left(C_{\rm ps}+2C_{\rm rs}\right)I_{\rm nRld}\pi\right)}{C_{\rm ps}\left(1+C_{\rm ps}+2C_{\rm rs}\right)\left(2C_{\rm rs}F_{\rm n}+\left(C_{\rm ps}+2C_{\rm rs}\right)I_{\rm nRld}\pi+\left(1+C_{\rm ps}\right)C_{\rm rs}F_{\rm n}V_{\rm nRld}\right)}\right]\right.\\&+\arcsin\left[\frac{1-\frac{\left(C_{\rm ps}+2C_{\rm rs}\right)I_{\rm nRld}\pi}{2C_{\rm rs}F_{\rm n}}+\frac{1}{2}\left(1+C_{\rm ps}\right)V_{\rm nRld}}{\sqrt{\frac{\left(1+C_{\rm ps}\right)\left(C_{\rm ps}+2C_{\rm rs}\right)^2\left(2+\left(1+C_{\rm ps}\right)V_{\rm nRld}\right)I_{\rm nRld}\pi}{C_{\rm ps}C_{\rm rs}F_{\rm n}\left(1+C_{\rm ps}+2C_{\rm rs}\right)}+\left(1-\frac{\left(C_{\rm ps}+2C_{\rm rs}\right)I_{\rm nRld}\pi}{2C_{\rm rs}F_{\rm n}}+\frac{1}{2}\left(1+C_{\rm ps}\right)V_{\rm nRld}\right)^2}}\right]\\&\left.-\arcsin\left[\frac{1+\frac{\left(C_{\rm ps}+2C_{\rm rs}\right)\left(2+\left(1+C_{\rm ps}\right)V_{\rm nRld}\right)I_{\rm nRld}\pi}{2C_{\rm ps}F_{\rm n}\left(1+C_{\rm ps}+2C_{\rm rs}\right)}}{\sqrt{\frac{\left(1+C_{\rm ps}\right)\left(C_{\rm ps}+2C_{\rm rs}\right)^2\left(2+\left(1+C_{\rm ps}\right)V_{\rm nRld}\right)I_{\rm nRld}\pi}{C_{\rm ps}C_{\rm rs}F_{\rm n}\left(1+C_{\rm ps}+2C_{\rm rs}\right)}+\left(1-\frac{\left(C_{\rm ps}+2C_{\rm rs}\right)I_{\rm nRld}\pi}{2C_{\rm rs}F_{\rm n}}+\frac{1}{2}\left(1+C_{\rm ps}\right)V_{\rm nRld}\right)^2}}\right]\right\}\end{aligned} \tag{42}$$

$$I_{\rm Lpk}=\begin{cases}\left[\frac{\left(C_{\rm p}+2C_{\rm r}\right)I_{\rm Rld}}{4C_{\rm r}f_{\rm s}}\sqrt{\frac{1}{L_{\rm s}C_{\rm T}}}+\frac{\left(C_{\rm p}+C_{\rm s}\right)V_{\rm Rld}}{2C_{\rm s}}\sqrt{\frac{C_{\rm T}}{L_{\rm s}}}+V_{\rm s}\sqrt{\frac{C_{\rm T}}{L_{\rm s}}}\right]\cdot\sin\gamma & \alpha'+\beta<\frac{\pi}{2},\ \text{for major mode}\\ \left[\frac{\left(C_{\rm p}+2C_{\rm r}\right)I_{\rm Rld}}{4C_{\rm r}f_{\rm s}}\sqrt{\frac{1}{L_{\rm s}C_{\rm T}}}+\frac{\left(C_{\rm p}+C_{\rm s}\right)V_{\rm Rld}}{2C_{\rm s}}\sqrt{\frac{C_{\rm T}}{L_{\rm s}}}+V_{\rm s}\sqrt{\frac{C_{\rm T}}{L_{\rm s}}}\right]\cdot\sqrt{\frac{C_{\rm M}}{C_{\rm T}}\sin^2\alpha+\cos^2\alpha} & \alpha'+\beta\ge\frac{\pi}{2},\ \text{for major mode}\\ \left[\frac{\left(C_{\rm p}+2C_{\rm r}\right)I_{\rm Rld}}{4C_{\rm r}f_{\rm s}}\sqrt{\frac{1}{L_{\rm s}C_{\rm T}}}+\frac{\left(C_{\rm p}+C_{\rm s}\right)V_{\rm Rld}}{2C_{\rm s}}\sqrt{\frac{C_{\rm T}}{L_{\rm s}}}+V_{\rm s}\sqrt{\frac{C_{\rm T}}{L_{\rm s}}}\right]\cdot\sqrt{\frac{C_{\rm M}}{C_{\rm T}}}\sin\alpha & \text{for minor mode}\end{cases}. \tag{43}$$

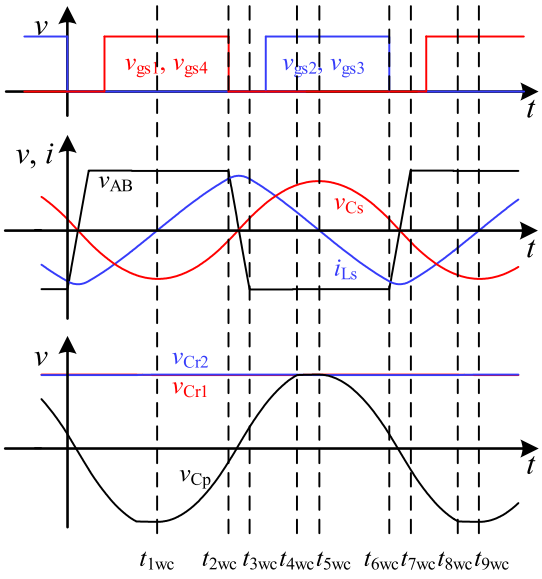

Fig. 12. Typical steady-state waveforms of the converter for the minor mode with output capacitor.

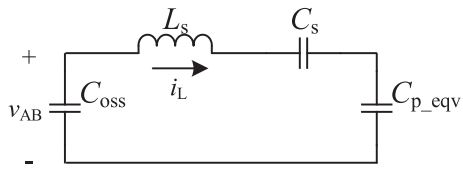

Fig. 13. Equivalent resonant circuit of the converter in t_{2wc}–t_{3wc} for the minor mode with output capacitor.

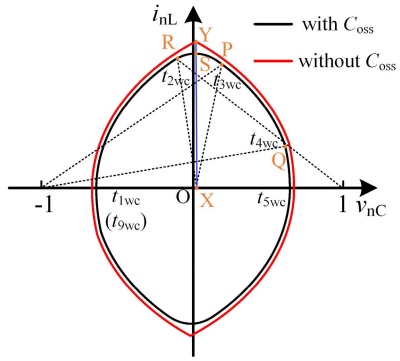

Fig. 14. State trajectory for the minor mode with and without output capacitor.

It is easy to find the relationship between V_{Cspk} and V_{Cppk} as follows:

$$V_{Cspk} = \frac{I_{Rld}}{2C_s f_s} + \frac{C_p}{C_s} V_{Cppk}. \tag{47}$$

VI. Impact of C_{oss} on the Minor Mode Model and Maximum Capacitance Selection

As the load becomes lighter, *LCC* SPRC's switching frequency increases and resonant current decreases. The switching speed of drain–source voltage v_{ds} and output voltage of full-bridge v_{AB} become slower, in which the switching duration accounts for a longer proportion in one switching period. Therefore, the output capacitor of the transistor, together with extra snubber capacitors, usually has a larger effect in the minor mode than in the major mode. In this section, the effect of output capacitors for the minor mode is analyzed, and the maximum acceptable value of the output capacitance is determined to avoid a large deviation from the proposed model mentioned above.

A. Impact of Output Capacitance

Typical waveforms for the minor mode with a significant output capacitance effect are exhibited in Fig. 12. The subscript "wc" is added to distinguish from the case not considering C_{oss}. t_{2wc}–t_{3wc} represents the duration of a slow v_{AB} ramp, whereas the processes of t_{1wc}–t_{2wc}, t_{3wc}–t_{4wc}, and t_{4wc}– t_{5wc} are the same as shown in Fig. 5. Thus, the analysis mainly focuses on the interval of t_{2wc}–t_{3wc}.

At t_{2wc} in Fig. 12, v_{ds} and v_{AB} start to switch, and the channel current of the power transistor is assumed to decrease to zero immediately [26]. Thus, the resonant current i_L is distributed between output capacitors. During t_{2wc}–t_{3wc}, the rectifier is disconnected from C_p with C_{p_eqv} equaling C_p. Assuming that the output capacitances of the four switches in the full-bridge are the same, the equivalent resonant circuit of the converter is illustrated in Fig. 13. The state trajectory equation in the interval of t_{2wc}–t_{3wc} is

$$\frac{(v_{nCwc}(t) - A_{2wc})^2}{\frac{r_{2wc}^2}{B_{2wc}}} + \frac{i_{nLwc}^2(t)}{r_{2wc}^2} = 1 \tag{48}$$

where $B_{2wc} = (1 + \frac{C_M}{C_{oss}}) \cdot \frac{C_M}{C_T}$, $A_{2wc} = [1 + \frac{C_M}{C_{oss}} \cdot v_{nCwc}(t_{2wc})]/(1 + \frac{C_M}{C_{oss}})$, and $r_{2wc} = \sqrt{B_{2wc} \cdot [v_{nCwc}(t_{2wc}) - A_{2wc}]^2 + i_{nLwc}^2(t_{2wc})}$. It can be seen that the state trajectory in this interval is an ellipse with a center at (A_{2wc}, 0), which varies as $v_{nCwc}(t_{2wc})$. Assuming $B_{2wc} > 1$, the entire state trajectory for the minor mode with output capacitor is plotted in Fig. 14. Compared with the trajectory without output capacitors, the overall trajectory shrinks, and the trajectory between t_{2wc} and t_{3wc} is smoother. The largest divergence appears in the region of t_{2wc}–t_{3wc}. As shown in Fig. 14, S is the intersection of the line YX and the elliptical arc $\overset{\frown}{\mathrm{RP}}$ corresponding to t_{2wc}–t_{3wc}. The closer SX/YX is to 1, the smaller the error induced by C_{oss}. Thus, the modeling error caused by C_{oss} can be expressed as follows:

$$\frac{SX}{YX} = \frac{r_{2wc}}{\sqrt{B_{2wc}(v_{nC}(t_2) - A_{2wc})^2 + i_{nL}^2(t_2)}}. \tag{49}$$

B. Determination of Maximum Output Capacitance

Given an acceptable C_{oss}-induced error ε, the maximum allowable C_{oss} is determined at the lightest load operating point as follows.

TABLE I
DESIGN SPECIFICATIONS AND RESTRICTIONS

Specifications	Values
Input voltage V_s	400 V
Transformer turns ratio	1 : 1
Output voltage V_{Rld}	[200 V, 666.67 V]
Output current I_{Rld}	[0.1875 A, 11.25 A]
Output power P_{Rld}	[37.5 W, 5 kW]
Switching frequency f_s	[600 kHz, 1 MHz]
I_{Lpk} limit	60 A
V_{Cspk} limit	1000 V
V_{Cppk} limit	800 V

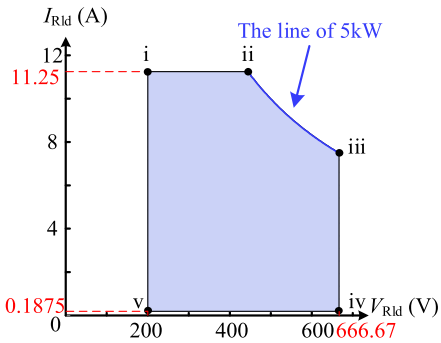

Fig. 15. Output range of the design specification.

1) Obtain the normalized output voltage V_{nRld} and the coordinates of Y ($v_{nC}(t_2)$, $i_{nL}(t_2)$) based on the minor model without output capacitance presented in Section IV.
2) Take $V_{nRldwc} = V_{nRld}$ for the case with output capacitance. Obtain the elliptic arc information (r_{2wc}, A_{2wc}, and B_{2wc}) of t_{2wc}– t_{3wc} as a function of C_{oss} based on the analysis in this section.
3) Therefore, the maximum allowable C_{oss} is solved from the following equation:

$$\frac{r_{2wc}}{\sqrt{B_{2wc}(v_{nC}(t_2) - A_{2wc})^2 + i_{nL}^2(t_2)}} \geq 1 - \varepsilon. \quad (50)$$

VII. Design Process Under a Wide Output Range

It can be seen from the model and stress expressions that the values of C_{ps}, C_r, and C_s vary with design requirements like output range and component stresses. Nevertheless, conventional methods neglect these relationships and apply predetermined values based on experience [10], [24], [25], [27]. In this section, design methodology with no experience-based predetermined value is developed for *LCC* SPRC under a wide output range.

The design procedure is demonstrated with an *LCC* converter operating in the burst mode. It operates and repeats with a 500-ms pulsewidth and a duty cycle of 2% [1], whose specifications are shown in Table I. Fig. 15 shows the output range of the designed converter, and five operation points (OPs) at the boundary are marked as i–v. First, the applicable range of C_r and C_{ps} is determined by the requirement of V_{Cppk} and V_{Cspk} limit. Possible values for C_r and C_{ps} can be selected. Second, for each combination of selected (C_r, C_{ps}), L_s and C_s can be solved from simultaneous equations about the output and current stress in one preselected OP. Third, five OPs will be evaluated comprehensively to make sure that the performance in the entire output range meets the specifications. A design example is shown below.

The range of C_r can be obtained from (45)

$$C_r \geq \frac{I_{Rld}}{f_s\,(4V_{Cppkmax} - 2V_{Rld})} \quad (51)$$

where $V_{Cppkmax} = 800$ V. The right-hand side of (51) determines its maximum at $f_s = f_{smin}$, $I_{Rld} = I_{Rld\cdot OPii}$, and $V_{Rld} = V_{Rld\cdot OPiii}$. Thereby C_r can be acquired as $C_r > 10$ nF. The range of C_{ps} is constricted by voltage stress. From (46), a sequence of inequality constraints can be derived as follows:

$$\frac{C_{ps}}{2} V_{Rld} \leq V_{Cspk} \leq V_{Cspkmax} \quad (52)$$

in which $V_{Cspkmax}$ is 1000 V. C_{ps} should be less than 3 when $V_{Rld} = 667$ V.

Based on the appropriate range of C_r and C_{ps}, C_r is chosen from 10 to 300 nF with a step increment of 10 nF. C_{ps} is selected from 1 to 3 with a step increment of 0.1.

According to [28], the maximum of I_{Lpk} usually occurs at OP ii with the minimum switching frequency, which is in the major mode usually. Consequently, the following equations should be satisfied

$$f_{VRld}(L_s, C_s, C_{ps}, C_r, R_{ld\_OPii}, f_{s\,min}, V_{Rld\_OPii}) = 0 \quad (53)$$

$$f_{ILpk}(L_s, C_s, C_{ps}, C_r, R_{ld\_OPii}, f_{s\,min}, I_{Lpkmax}) = 0 \quad (54)$$

where $R_{ld\cdot OPii}$ and $V_{Rld\cdot OPii}$ are, respectively, the load resistance and output voltage at OP ii. $f_{smin} = 600$ kHz. $I_{Lpkmax} = 60$ A. The functions $f_{VRld}(\bullet)$ are extracted by converting the normalized value in (28) to the actual value. The $f_{ILpk}(\bullet)$ can be obtained from (43).

L_s and C_s are solved by inserting different value pairs of C_{ps} and C_r into (53) and (54), and appropriate values are found to satisfy the frequency range and device stress requirements in Table I for all the five OPs.

The designed components of L_s, C_s, C_p, and C_r are 7.6 μH, 15.8 nF, 25.3 nF, and 180 nF, respectively. The switching frequency range is 600–987 kHz. The calculated component stresses are exhibited in Table III, from which $I_{Lpkmax} = 60$ A, $V_{Cspkmax} = 989$ V, and $V_{Cppkmax} = 350$ V. Among the five OPs, i, ii, and iii are in the major mode, whereas iv and v are in the minor mode. Taking an acceptable C_{oss}-induced error $\varepsilon = 5\%$, the maximum allowable C_{oss} is calculated as 1.72 nF according to (50).

VIII. Simulation and Experiment Verification

To verify the accuracy of the proposed analytical model and the validity of the design method, a prototype of *LCC* SPRC with a voltage doubler based on the above-mentioned design results is built. Open-loop simulations and experiments are carried

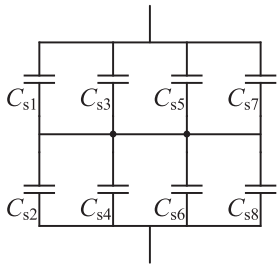

Fig. 16. Composition of series resonant capacitor C_s.

out. Converter output and component stresses are acquired and compared with the theoretical model.

A. Consideration for the Prototype Design

1) Power Devices and Gate Driver: Power transistors adopted in this design are C3M0030090K from Cree. The charge equivalent C_{oss} [29] at 400 V is 0.35 nF [30], which is much less than the maximum acceptable output capacitance of 1.72 nF. Gate drivers are configured with a digital isolator of Si8271 and a push–pull stage of IXDN609. Secondary rectifier diodes are GC2X10MPS12-247 from GeneSiC.

2) Dead Time Selection: The maximum allowable dead time should be terminated earlier than the time point of i_L from positive zero crossing to negative to ensure ZVS. The minimum allowable dead time is required for both C_{oss} to be charged above dc bus voltage V_{dc} and C_{gs} to be discharged below threshold voltage V_{th}.

Theoretically, the optimal dead time should be at its minimum value to minimize dead time loss. However, the minimum allowable dead time is hard to be accurately calculated because it is related to the printed circuit board (PCB) layout of the full-bridge and the characteristics of power devices [31]. Hence, actual dead time used in the design is obtained through experiments.

3) Transformer and Series Resonant Inductor: A high-frequency transformer with a turns ratio of 1:1 is adopted using 3C95A ferrite core. Agilent 4294A precision impedance analyzer is used to measure the transformer parameters, as magnetizing inductance $L_m = 2.2$ mH, leakage inductance $L_{lk} = 2.2$ μH, and winding capacitance $C_w = 41$ pF.

A single-layer helical air-core coil with Litz wire is used as the resonant inductor. Considering the leakage inductance of the transformer, the inductance of the air-core inductor is selected as 5.4 μH. The number of turns is calculated through [32].

4) Series Resonant Capacitor: The design of the series resonance capacitor should consider the alternating current handling capability. Metallized polypropylene film capacitors specialized for high-pulse and high-frequency applications are chosen, and combination connections of series and parallelization are adopted. As shown in Fig. 16, C_{s1}–C_{s6} are FKP1U021006B rated 2000 V_{dc}/10 nF. C_{s7} and C_{s8} are FKP1U011505B rated 2000 V_{dc}/1.5 nF.

The temperature rise is evaluated based on the derating curve of the V_{rmsmax}–f provided in datasheets [33], [34]. The maximum allowable temperature rise ΔT_{max} under continuous current is derived as follows:

$$\Delta T_{\max} = \left(\frac{V_{\text{rms max}}}{2\pi f \cdot C}\right)^2 \cdot \text{ESR} \cdot R_{\text{th}} \tag{55}$$

where C, ESR and R_{th} are the capacitance, equivalent series resistance, and thermal resistance of the capacitor, respectively. For the burst mode with a duty cycle of D, the temperature rise ΔT for the ac voltage of V_{rms} can be expressed as follows:

$$\Delta T = \left(\frac{V_{\text{rms}}}{V_{\text{rmsmax}}}\right)^2 \cdot D \cdot \Delta T_{\max}. \tag{56}$$

The temperature rise at the OP ii is considered here because the capacitor current is the largest. With $\Delta T_{max} = 15$ °C and $D = 0.02$, the temperature rises are calculated as 6.7 °C for FKP1U021006B and 1.2 °C for FKP1U011505B. Both of the temperature rises are acceptable.

5) Tolerance of Resonant Components: The maximum acceptable tolerances of components are discussed to ensure that the deviation from the target specification caused by the tolerance is as small as possible.

Series resonant inductor L_s is custom designed, whose tolerance can be well controlled and minimized to less than 3%. C_s, C_p, and C_r are all from the WIMA FKP1 series with tolerances of 5% selected. The Monte Carlo method is applied to further evaluate the tolerances, which generally follow normal distributions. Table II summarizes the obtained error for every design index. The maximum error of V_{Cspk} under a capacitance tolerance of 5% is 17.5%, whereas for capacitance tolerance of 10%, the maximum error becomes 32.3%, which is not acceptable. Therefore, the capacitors with 5% tolerance can lead to reasonable accuracies.

TABLE II
ERRORS OF OUTPUT VOLTAGE AND STRESSES

Cap. Tol.	V_{Rld}	I_{Lpk}	V_{Cspk}	V_{Cppk}
5%	13.7%	12.1%	17.5%	13.8%
10%	22.7%	19.9%	32.3%	22.8%

6) PCB Layout Considerations: With up to megahertz high switching frequency, the prototype design should fully consider the side effects brought by layout parasitics. To avoid excessive voltage overshoot of v_{ds}, the power transistors are installed on a multilayer PCB with mutual inductance cancellation technology employed to minimize the parasitic inductance of the power loop [35]. The designed prototype of *LCC* SPRC is shown in Fig. 17.

B. Simulation Verification

The Matlab/Simulink model is developed for the *LCC* converter with the designed resonant components. The model of MOSFET is without C_{oss}. The parasitic parameters of the transformer are integrated. The filter capacitance C_{out} is 3.2 μF. The critical waveform of OP ii is shown in Fig. 18. The load resistance is 39.5 Ω, and the switching frequency is 600 kHz. The current of resonant inductor i_L is lagging to the output voltage of the full-bridge v_{AB}, which proves that the *LCC* operates above resonance. The average output voltage V_{Rld} is 448.3 V. The error of output voltage between the simulation and the analytical

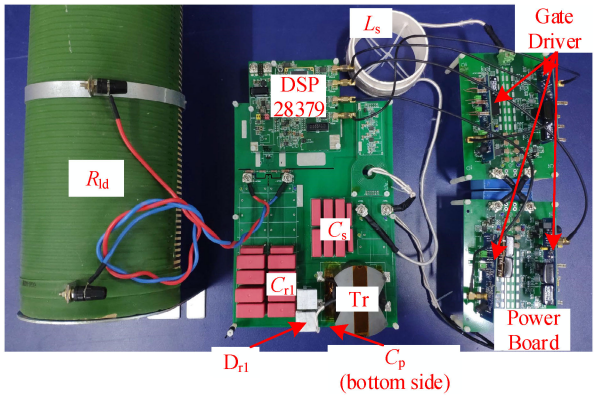

Fig. 17. Prototype of the designed 5-kW LCC SPRC.

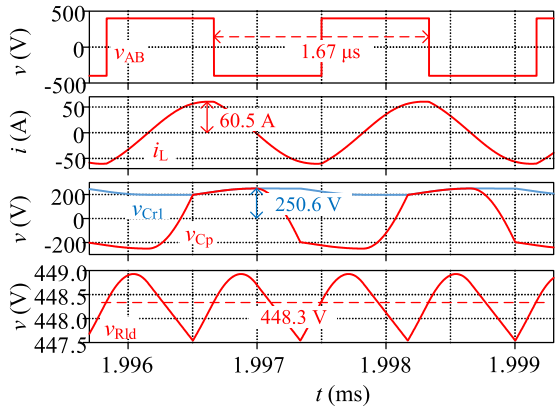

Fig. 18. Simulation waveforms for the OP ii.

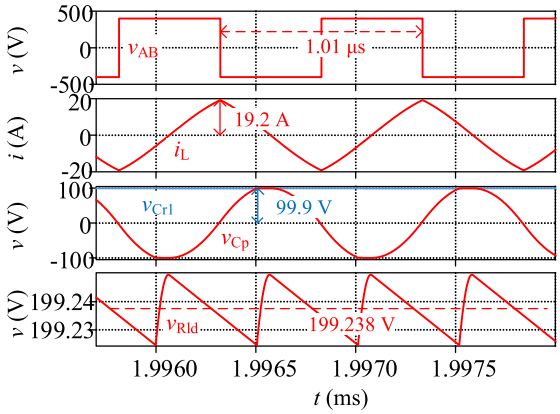

Fig. 19. Simulation waveforms for the OP v.

model is 0.9%. The peak current of resonant inductor I_{Lpk} and the peak voltages of resonant capacitor V_{Cspk} and V_{Cppk} at this OP are 60.5 A, 1000.2 V, and 250.6 V, respectively. The mismatch of the peaks between simulation and calculated model is 0.8%, 1.1%, and 0.9%, respectively.

The waveforms of OP v are shown in Fig. 19 with the resistor load of 1066.67 Ω. The switching frequency is 986 815 Hz. As the switching frequency is away from resonance, resonant current i_{L} tends to be triangular. The simulated output voltage V_{Rld} is 199.24 V with a mismatch of 0.4% to the analytical model. The peaks of i_{L}, v_{Cs}, and v_{Cp} are 19.2 A, 166.1 V, and 99.9 V, respectively. Deviations of 0, 0.1%, and 0.1% are captured between simulation and analytical calculation.

TABLE III
COMPARISONS OF OUTPUT AND STRESS AMONG ANALYTICAL MODEL, SIMULATION, AND EXPERIMENT

	OP	i	ii	iii	iv	v
V_{Rld} (V)	Prop.	200	444.44	666.67	666.67	200
	Sim.	202.2	448.3	672.7	656.2	199.24
	Error	1.1%	0.9%	0.9%	1.6%	0.4%
	Exp.	199.5	440.3	690.4	646	193.9
	Error	0.3%	0.9%	3.6%	3.1%	3.1%
I_{Lpk} (A)	Prop.	51.02	60	59.36	43	19.2
	Sim.	51.4	60.5	60.7	43	19.2
	Error	0.7%	0.8%	2.3%	0	0
	Exp.	49.76	56.7	54.2	43.1	18.7
	Error	2.5%	5.5%	8.7%	0.2%	2.6%
V_{Cspk} (V)	Prop.	785.57	989.32	935.05	534.6	166.2
	Sim.	793.3	1000.2	945.3	534.3	166.1
	Error	1.0%	1.1%	1.1%	0.1%	0.1%
	Exp.	817.3	1005	906.2	542.6	163.5
	Error	4.0%	1.6%	3.1%	1.5%	1.6%
V_{Cppk} (V)	Prop.	125.71	248.26	349.84	328.9	100
	Sim.	126.9	250.6	353.2	328.5	99.9
	Error	0.9%	0.9%	1.0%	0.1%	0.1%
	Exp.	144.6	284.5	386.4	329.7	100.8
	Error	15.0%	14.6%	10.5%	0.2%	0.8%

The simulation results of V_{Rld}, I_{Lpk}, V_{Cspk}, and V_{Cppk} at five OPs are summarized in Table III and compared with analytical results. Mismatches are well below 2.3% for V_{Rld}, I_{Lpk}, V_{Cspk}, and V_{Cppk} at all OPs. It shows the high accuracy of the proposed analytical model.

To validate the method of the maximum C_{oss} selection, the simulation at OP v is redone with extra 1.72 nF output capacitors included with power transistors. The simulation results show that the differences of V_{Rld}, I_{Lpk}, V_{Cspk}, and V_{Cppk} between with and without C_{oss} are 0.8%, 5.6%, 0.8%, and 0.8%, respectively. The maximum difference of 5.6% for I_{Lpk} is slightly larger than the given error of 5% due to a small drop of 0.8% in V_{Rld}. Furthermore, the error caused by C_{oss} can be neglected for selected C3M0030090K with only 0.35 nF C_{oss}.

C. Experiment Verification

Oscilloscope MSO56 from Tektronix is employed with low-voltage isolated probe TIVH02 to measure the gate–source voltage (v_{gs}), high-voltage differential probe THDP0200 to measure the full-bridge output voltage, C_{s} voltage, C_{p} voltage, C_{r1} voltage, converter output voltage, and dc bus voltage (v_{AB}, v_{Cs}, v_{Cp}, v_{Cr1}, v_{Rld}, and V_{dc}), and current probe TCP0030A for resonant current (i_{L}) measurement.

The experimental switching waveforms of OP v are shown in Fig. 20, which are used to determine the minimum dead time. v_{gs4} takes 41 ns to drop from a high level to V_{th}. v_{ds} spends

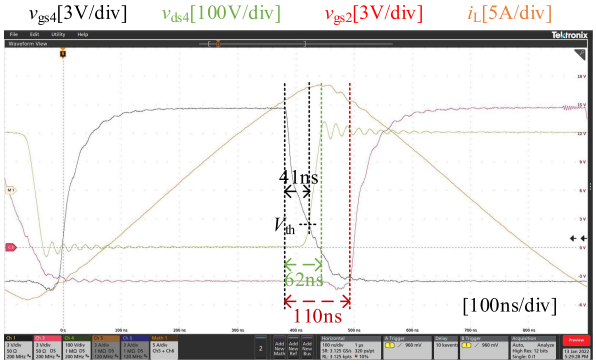

Fig. 20. Experimental waveforms of dead time determination.

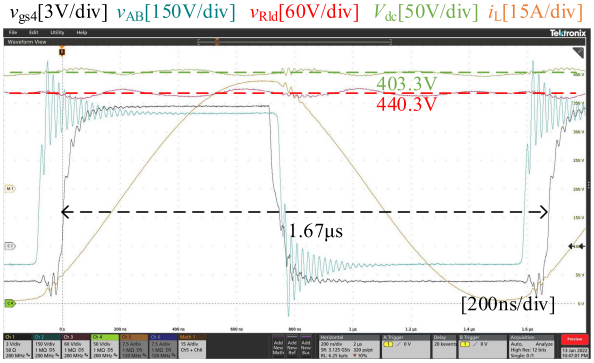

Fig. 21. Experimental waveforms of the full-bridge inverter and the converter output for OP ii.

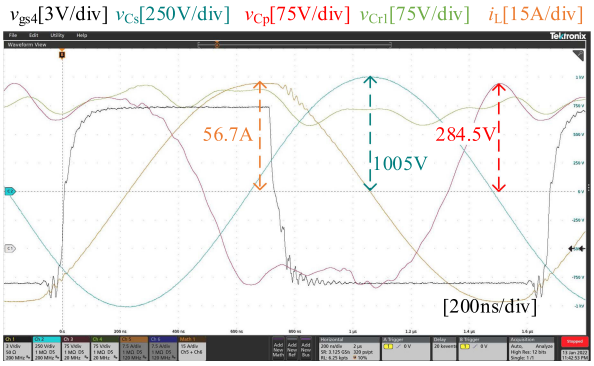

Fig. 22. Experimental waveforms of component stresses for OP ii.

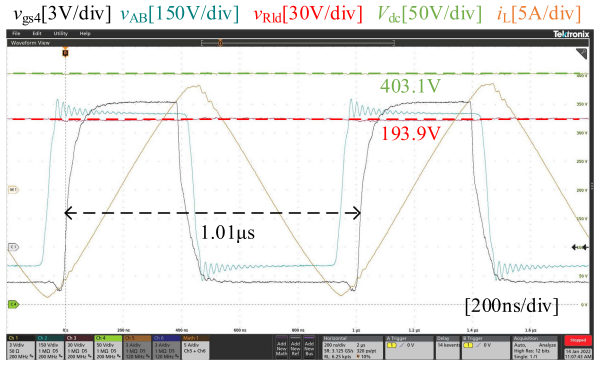

Fig. 23. Experimental waveforms of the full-bridge inverter and the converter output for OP v.

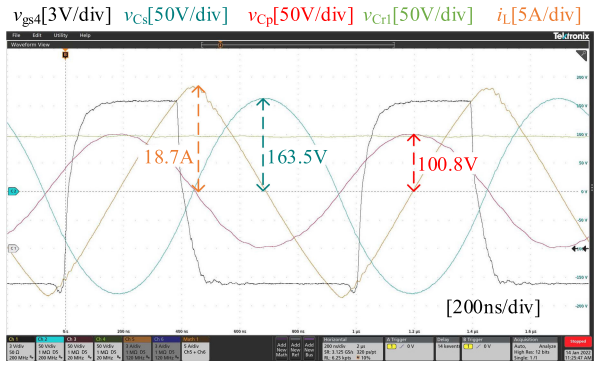

Fig. 24. Experimental waveforms of component stresses for OP v.

62 ns to reach dc bus voltage. Hence, the dead time is selected as 110 ns with large design margins.

Fig. 21 shows the key waveforms of the full-bridge inverter and the converter output for OP ii. The load resistance and switching frequency in the experiment are the same as in the simulation. The average output voltage V_{Rld} is measured as 440.3 V for OP ii. There is a 0.9% mismatch between the experiment and the calculated model. The critical waveforms of resonant components are depicted in Fig. 22. The measured peak levels of I_{Lpk}, V_{Cspk}, and V_{Cppk} are 56.7 A, 1005 V, and 284.5 V, respectively. The mismatches are 5.5%, 1.6%, and 14.6% compared to the analytical model. Low-amplitude high-frequency oscillations are observed in v_{Cp} and v_{Cr1}, which lead to an error of 14.6% for V_{Cppk}. The oscillations are caused by the resonance between the parasitic inductance of the PCB traces, C_{p}, C_{r1}, and C_{r2}.

Figs. 23 and 24 exhibit the waveform of the output voltage and stresses of OP v. The measured output voltage V_{Rld}, L_{s}'s peak current I_{Lpk}, C_{s}'s peak voltage V_{Cspk} and C_{p}'s peak voltage V_{Cppk} are 193.9 V, 18.7 A, 163.5 V, and 100.8 V, respectively. The deviations between the experimental result and the calculated model are 3.1%, 2.6%, 1.6%, and 0.8%, respectively. It should be noted that the overshoots and oscillations of v_{AB} are caused by the resonance between the parasitic inductance of the commutation loop in the bridge and the output capacitance C_{oss} of the power transistor [36], [37]. More energy is stored on the parasitic inductance with a larger resonant inductor current. When all the energy on the parasitic inductance is converted to C_{oss}, it will cause greater voltage overshoots and oscillations. The resonant inductor currents at the time of switching are nearly 60 A for OP ii and 20 A for OP v. Therefore, the overshoot of v_{AB} for OP ii is larger than for OP v, although OP ii has a lower switching frequency.

Thermal performances of the prototype are measured using the FLIR T640 thermal imaging camera, which is carried out when the converter is running at OP ii for 15 min in a burst mode with a pulsewidth of 500 ms and a duty cycle of 2%. As shown in Fig. 25, the maximum temperature is 41.7 °C for SiC MOSFETs

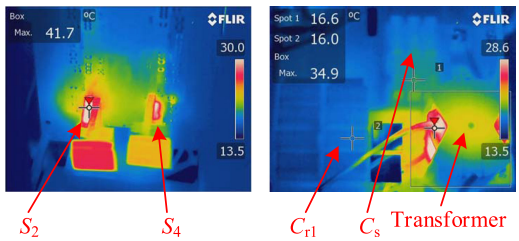

Fig. 25. Temperature measurement of the *LCC* SPRC prototype.: (a) SiC MOSFETs. (b) Passive components.

TABLE IV
RESULTS OF SIMULATION AND THREE MODELS

R_{ld}	(Ω)	5	10	50	80
V_{Rld} (V)	Sim.	169	337.6	1518.3	1985.8
	[10]	844	875.4	752.2	327.8
	Error	399.4%	159.3%	50.5%	83.5%
	[4]	111.5	221.1	1076.9	1589.3
	Error	34%	35%	29%	20%
	Prop.	168.9	337.5	1518.2	1985.7
	Error	0.06%	0.03%	0.01%	0.01%
I_{Lpk} (A)	Sim.	168.9	171.5	192	192.7
	[10]	22.6	46.14	315.9	956.6
	Error	86.6%	73.1%	64.5%	396.4%
	[4]	74.5	78.3	111	126.4
	Error	56%	54%	42%	34%
	Prop.	168.8	171.4	192	192.6
	Error	0.06%	0.06%	0	0.05%
V_{Cspk} (V)	Sim.	1335.9	1390.5	1655	1600.7
	[10]	187.1	381.5	2611.8	7909.3
	Error	86.0%	72.6%	57.8%	394.1%
	[4]	616.1	647.7	917.7	1044.8
	Error	54%	53%	45%	35%
	Prop.	1335.5	1390	1654.6	1600.4
	Error	0.03%	0.04%	0.02%	0.02%
V_{Cppk} (V)	Sim.	688.1	771.8	1301.7	1436.5
	[10]	16.9	65.1	1532.3	6015.6
	Error	97.5%	91.6%	17.7%	318.8%
	[4]	-	-	-	-
	Error	-	-	-	-
	Prop.	687.9	771.5	1301.3	1436.1
	Error	0.03%	0.04%	0.03%	0.03%

and 34.9 °C for the transformer under an ambient temperature of 14 °C. The temperature rises of other components are relatively low.

The test results of output voltages and stresses are summarized in Table III. It shows good consistency between the experiments and the design over the entire output range. The maximum mismatch of the experiment is 15%, which is greater than the simulation due to the parasitics of the PCB layout and the tolerances of inductors and capacitors. Hence, the feasibility of the proposed design method is well validated.

IX. COMPARISON OF MODELS

To show the superiority of the proposed analytical model, two analytical models of the *LCC* SPRC with a voltage doubler rectifier proposed by prior studies [4], [10] are compared with this article. A set of resonant parameters from other literature [38] are used for the comparison. They are the following: $L_s = 35\ \mu$H, $C_s = 275$ nF, $C_p = 183$ nF, and $C_r = 200$ nF. The switching frequency is selected as 70 kHz with variable load resistances from 5 to 80 Ω.

The calculation results of the proposed model and the models presented in [4] and [10] are compared with the simulation results in Table IV. As the model presented in [4] lacks the derivation of V_{Cspk}, the information about V_{Cspk} in [4] is blank. It can be seen that with the change of load resistance, the maximum error is 399.4% between simulation and [10], 56% between simulation, and [4], and only 0.06% between simulation and the proposed model. The comparison demonstrates that the proposed model has higher accuracy than the other two models in a wide range.

X. CONCLUSION

The state trajectory analysis and steady-state model for the *LCC* resonant converter with a voltage doubler rectifier are proposed in this article. The proposed model is capable to provide effective guidance for the design of HVGs in medical X-ray machines and satisfies high accuracy for a wide output range.

Different from the *LCC* converter with a full-bridge rectifier, the capacitor in the voltage doubler rectifier circuit will participate in the resonant process. The equivalent parallel capacitor is introduced to include the impact of voltage doubler capacitors on the resonance process. The relationship of edges and angles under the combining state trajectories is investigated to construct the steady-state model both for the major mode and the minor mode. The effects of devices' output capacitors are taken into account, and model errors induced by output capacitance can be limited. Accurate voltage/current stresses of the resonant components are calculated as the function of the converter output and switching frequency. The design method of the *LCC* converter under the wide output range is given, which is free of preassumed values and manual tuning.

Both simulations and experiments are used to verify the accuracy of the proposed analytical model and the feasibility of the design method. The maximum simulation error in the entire output range is 2.3%. The experimental mismatches are all lower than 15%. The designed *LCC* converter is sufficient to satisfy the target specifications.

APPENDIX

A. Derivation of (48)

The equations to describe the resonant circuit in t_{2wc}–t_{3wc} are

$$\begin{cases} L_s \frac{di_{Lwc}(t)}{dt} = v_{AB} - v_{Cswc}(t) - v_{Cpwc}(t) \\ C_{oss} \frac{dv_{AB}(t)}{dt} = -i_{Lwc}(t) \\ C_s \frac{dv_{Cswc}(t)}{dt} = i_{Lwc}(t) \\ C_{p\_eqv} \frac{dv_{Cpwc}(t)}{dt} = i_{Lwc}(t) \end{cases} \tag{57}$$

from which (58) and (59) can be acquired

$$v_{\mathrm{Cwc}}(t) - v_{\mathrm{Cwc}}(t_{2\mathrm{wc}}) = \frac{1}{C_{\mathrm{M}}}\int_{t_{2\mathrm{wc}}}^{t} i_{\mathrm{Lwc}}(t)\,dt \tag{58}$$

$$v_{\mathrm{AB}}(t) - v_{\mathrm{AB}}(t_{2\mathrm{wc}}) = -\frac{1}{C_{\mathrm{oss}}}\int_{t_{2\mathrm{wc}}}^{t} i_{\mathrm{Lwc}}(t)\,dt. \tag{59}$$

With $v_{\mathrm{AB}}(t_{2\mathrm{wc}}) = V_{\mathrm{s}}$, $v_{\mathrm{AB}}(t)$ is expressed as follows:

$$v_{\mathrm{AB}}(t) = V_{\mathrm{s}} - \frac{C_{\mathrm{M}}}{C_{\mathrm{oss}}}\left(v_{\mathrm{Cwc}}(t) - v_{\mathrm{Cwc}}(t_{2\mathrm{wc}})\right). \tag{60}$$

Equation (61) is derived from (57) and (60)

$$\begin{cases} \frac{di_{\mathrm{nLwc}}(t)}{\mathrm{d}t} \\ \quad = \left[1 + \frac{C_{\mathrm{M}}}{C_{\mathrm{oss}}}\cdot v_{\mathrm{nCwc}}(t_{2\mathrm{wc}}) - \left(1 + \frac{C_{\mathrm{M}}}{C_{\mathrm{oss}}}\right)\cdot v_{\mathrm{nCwc}}(t)\right] \cdot \\ \cdot\omega_{\mathrm{base}}\frac{dv_{\mathrm{nCwc}}(t)}{dt} = i_{\mathrm{nLwc}}(t)\cdot\frac{C_{\mathrm{T}}}{C_{\mathrm{M}}}\cdot\omega_{\mathrm{base}} \end{cases} \tag{61}$$

Hence, the trajectory equations for this interval can be obtained as (48). With $v_{\mathrm{nCwc}}(t_{3\mathrm{wc}}) - v_{\mathrm{nCwc}}(t_{2\mathrm{wc}}) = \frac{2C_{\mathrm{oss}}}{C_{\mathrm{M}}}$, $v_{\mathrm{nCwc}}(t_{2\mathrm{wc}})$ and $i_{\mathrm{nLwc}}(t_{2\mathrm{wc}})$ can be calculated as follows:

$$v_{\mathrm{nCwc}}(t_{2\mathrm{wc}}) = \frac{(C_{\mathrm{ps}} + 2C_{\mathrm{rs}})\left(2 + (1 + C_{\mathrm{ps}})V_{\mathrm{nRldwc}}\right) I_{\mathrm{nRldwc}}\pi}{2F_{\mathrm{n}}C_{\mathrm{ps}}(1 + C_{\mathrm{ps}} + 2C_{\mathrm{rs}})} - \frac{(1 + C_{\mathrm{ps}})C_{\mathrm{os}}}{C_{\mathrm{ps}}} \tag{62}$$

$$i_{\mathrm{nLwc}}(t_{2\mathrm{wc}}) = \sqrt{\left[\left(1 - v_{\mathrm{nCwc}}(t_{2\mathrm{wc}})\right)^2 - \left(v_{\mathrm{nCwc}}(t_{2\mathrm{wc}}) - 1\right)^2\right]\cdot\frac{C_{\mathrm{M}}}{C_{\mathrm{T}}}} \tag{63}$$

where $C_{\mathrm{os}} = C_{\mathrm{oss}} / C_{\mathrm{s}}$.

REFERENCES

[1] Spellman, *2020 High Voltage Reference Manual, REV.*7, Jan. 2020. [Online]. Available: https://www.spellmanhv.com/en/Technical-Resources/Downloads

[2] R. Behling, "X-ray generators," in *Handbook of X-Ray Imaging*, Boca Raton, FL, USA: CRC Press, 2017, pp. 93–104.

[3] Amrad Medical, *AmRad DR Series (CMP 200) Brochure*, 2018. [Online]. Available: https://summitindustries.net/wp-content/uploads/2020/11/AMRAD_DR_SERIES_GEN_LIT_2018_web.pdf

[4] F. D. S. Cavalcante, "High output voltage series-parallel resonant DC–DC converter for medical X-ray imaging applications," Ph.D. dissertation, ETH Zürich, Zürich, Switzerland, 2005.

[5] H. Zhang, C. Tong, and Z. Wang, "Normalized analysis and optimal design of DCM-LCC resonant converter for high voltage power supply," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 4496–4506, Jun. 2020.

[6] Z. Cao, M. Hu, N. Fröhleke, and J. Böcker, "Modeling and control design for a very low-frequency high-voltage test system," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 1068–1077, Apr. 2010.

[7] C. Lin, L. He, X. Li, M. Xie, L. Cheng, and S. Fan, "Modeling and digital control of 100kV/50kW high voltage power supply based on PPSS-LCC for X-ray generator," in *Proc. IEEE 4th Int. Elect. Energy Conf.*, Wuhan, China, 2021, pp. 1–6.

[8] A. J. Gilbert, C. M. Bingham, D. A. Stone, and M. P. Foster, "Normalized analysis and design of LCC resonant converters," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2386–2402, Nov. 2007.

[9] H. Peng, J. Chen, Z. Cheng, Y. Kang, J. Wu, and X. Chu, "Accuracy-enhanced miller capacitor modeling and switching performance prediction for efficient SiC design in high-frequency X-ray high-voltage generators," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 179–194, Mar. 2020.

[10] S. Mao, C. Li, W. Li, J. Popovic, S. Schröder, and J. A. Ferreira, "Unified equivalent steady-state circuit model and comprehensive design of the LCC resonant converter for HV generation architectures," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7531–7544, Sep. 2018.

[11] S. S. Dhillon, "Frequency domain modelling & design of an LCC resonant converter with capacitive output filter," Master's dissertation, Queen's Univ., Kingston, ON, Canada, 2020.

[12] A. J. Gilbert, "Analysis, design and control of LCC resonant power converters," Ph.D. dissertation, Univ. Sheffield, Sheffield, U.K., 2007.

[13] H. Hu, T. Cai, S. Duan, X. Zhang, J. Niu, and H. Feng, "An optimal variable frequency phase shift control strategy for ZVS operation within wide power range in IPT systems," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5517–5530, May 2020.

[14] I. Batarseh, R. Liu, C. Q. Lee, and A. K. Upadhyay, "Theoretical and experimental studies of the LCC-type parallel resonant converter," *IEEE Trans. Power Electron.*, vol. 5, no. 2, pp. 140–150, Apr. 1990.

[15] H. Chen, E. K. K. Sng, and K. J. Tseng, "Optimum trajectory switching control for series–parallel resonant converter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1555–1563, Oct. 2006.

[16] L. Wu, J. Zhao, H. Lin, X. Sun, and G. Chen, "State trajectory control of start-up for LCC resonant converters with capacitive output filter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 2317–2327, Apr. 2020.

[17] A. Nabih, M. H. Ahmed, Q. Li, and F. C. Lee, "Transient control and soft start-up for 1-MHz LLC converter with wide input voltage range using simplified optimal trajectory control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 24–37, Feb. 2021.

[18] W. Feng, "State-trajectory analysis and control of LLC resonant converters," Ph.D. dissertation, Virginia Polytechnic Inst. and State Univ., Blacksburg, VA, USA, 2013.

[19] S. Sooksatra, "Analysis of asymmetrical LCC parallel resonant converter," in *Proc. 8th Int. Elect. Eng. Congr.*, Chiang Mai, Thailand, 2020, pp. 1–4.

[20] Y. Horen, S. Bronshtein, D. Baimel, and A. Abramovitz, "On the operational modes of LCC resonant converter with a capacitive output filter," in *Proc. Int. Conf. Elect. Drives Power Electron.*, High Tatras, Slovakia, 2019, pp. 93–97.

[21] J. Zhao, L. Wu, H. Lin, X. Sun, and G. Chen, "State trajectory control of burst mode for LCC resonant converters with capacitive output filter," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 377–391, Jan. 2022.

[22] Z. Yu, J. Chen, Y. Wang, and Y. Xu, "Analytical modeling and optimization of LCC resonant converter in CCM based on state plane analysis," in *Proc. IEEE 1st China Int. Youth Conf. Elect. Eng.*, Wuhan, China, 2020, pp. 1–6.

[23] Y. Xu *et al.*, "Multimode constant power control strategy for LCC resonant capacitor charging power supply based on state plane analysis," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8399–8412, Jul. 2021.

[24] H. Jafari and M. Habibi, "High-voltage charging power supply based on an LCC-type resonant converter operating at continuous conduction mode," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5461–5478, May 2020.

[25] C. Liu, Z. Zhang, Y. Liu, Y. Si, M. Wang, and Q. Lei, "Mega-hertz high voltage EMAT pulser based on LCC resonant inverter using SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, Jul. 2021, doi: 10.1109/JESTPE.2021.3095611.

[26] X. Li *et al.*, "Achieving zero switching loss in silicon carbide MOSFET," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12193–12199, Dec. 2019.

[27] A. K. S. Bhat, "A resonant converter suitable for 650 V DC bus operation," *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 739–748, Oct. 1991.

[28] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174–182, Apr. 1988.

[29] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 985–995, Feb. 2015.

[30] Wolfspeed, *C3M0030090K Silicon Carbide Power MOSFET C3MTM MOSFET Technology, Datasheet Rev. C*, Jul. 2018. [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/1185/product/253/c3m0030090k.pdf

[31] Y. Zhang, C. Chen, Y. Xie, T. Liu, Y. Kang, and H. Peng, "A high-efficiency dynamic inverter dead-time adjustment method based on an improved GaN HEMTs switching model," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2667–2683, Mar. 2022.

[32] H. A. Wheeler, "Inductance formulas for circular and square coils," *Proc. IEEE*, vol. 70, no. 12, pp. 1449–1450, Dec. 1982.

[33] TDK Group Company, *Film Capacitors General Technical Information*, Jun. 2018. [Online]. Available: https://www.tdk-electronics.tdk.com/download/537974/480aeb04c789e45ef5bb9681513474ba/pdf-generaltechnicalinformation.pdf

[34] WIMA, *WIMA FKP 1 Capacitors, Datasheet*, Jun. 2021. [Online]. Available: https://www.wima.de/wp-content/uploads/media/e_WIMA_FKP_1.pdf
[35] R. S. K. Moorthy *et al.*, "Estimation, minimization, and validation of commutation loop inductance for a 135-kW SiC EV traction inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 286–297, Mar. 2020.
[36] T. Liu, R. Ning, T. T. Y. Wong, and Z. J. Shen, "Modeling and analysis of SiC MOSFET switching oscillations," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 747–756, Sep. 2016.
[37] L. Wang, H. Ma, H. Qiu, K. Yuan, Z. Liu, and G. Cao, "Modelling and optimization of SiC MOSFET switching voltage and current overshoots in a half-bridge configuration," *IET Power Electron.*, vol. 14, no. 9, pp. 1684–1699, May 2021.
[38] J. A. Martín-Ramos, Ó. Pardo-Vaquero, J. Díaz, F. Nuño, P. J. Villegas, and A. Martín-Pernía, "Modelling a multilevel LCC resonant AC–DC converter for wide variations in the input and the load," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5217–5228, Jun. 2019.

Jimin Chen (Student Member, IEEE) received the B.S. degree in electrical engineering from Dalian Maritime University, Dalian, China, in 2016. He is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronics Engineering, Huazhong University of Science and Technology, Wuhan, China.

His research interest includes power converters based on wide-bandgap (WBG) devices.

Han Peng (Member, IEEE) received the B.S. degree from Southeast University, Nanjing, China, in 2006, and the Ph.D. degree from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2011, both in electrical engineering.

From 2011 to 2017, she was the Lead Electrical Engineer with the Global Research Center, General Electric Company, Niskayuna, NY, USA. Since 2018, she has been a Professor with the Huazhong University of Science and Technology, Wuhan, China. She has published more than 30 articles in refereed journals and international conference proceedings. She has four U.S. patent and two Chinese patent filed. Her research interests include high-frequency, high-power density power management IC design, high-frequency supply modulators and applications of wide-bandgap power devices, energy harvesting, communication power, healthcare electronics, more electrical aircraft systems, and electric vehicles.

Dr. Peng has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2017. She was the Associate Technical Program Chair for the IEEE 11th Annual Energy Conversion Congress and Exposition 2019.

Yong Kang (Senior Member, IEEE) was born in Hubei, China, on October 16, 1965. He received the B.E. M.E, and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 1988, 1991, and 1994, respectively, all in electrical engineering.

In 1994, he joined the Huazhong University of Science and Technology as a Lecturer, where he was promoted to an Associate Professor in 1996 and a Full Professor in 1998. He has authored more than 60 technical articles. His research interests include power electronic converter, ac drivers, electromagnetic compatibility, their digital control techniques, and wide-bandgap device packaging and applications.

Jinglin Wu received the B.Sc. degree in applied physics and Ph.D. degree in engineering electronic science and technology from the University of Science and Technology of China, Hefei, China, in 2008 and 2014, respectively.

He is currently a Senior Engineer with the Department of Power Electronics Components, United Imaging Healthcare Company, Ltd., Shanghai, China. His research interests include high-voltage generators and wide-bandgap-power-semiconductor-device-based power conversion.

Xu Chu received the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2005.

He was with the GE Global Research Center, Shanghai, China, from 2006 to 2012. He is with the United Imaging Healthcare Company Ltd., Shanghai, China, where his work is focused on power conversion technology in medical equipment.