A Three-Phase Five-Level Inverter With High DC Voltage Utilization and Self-Balancing Capacity of Floating Capacitor

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***Abstract*—Multilevel inverter are popular solutions in photovoltaic power station, wind farm, and other renewable energy generation. This article presents a three-phase five-level inverter with high dc voltage utilization. A significant feature of the inverter is that its maximum dc voltage utilization is twice that of the traditional three-phase inverters such as neutral point clamped, flying capacitor (FC), cascaded H-bridge, and active NPC. What is more, the inverter can realize the self-starting and self-balancing of the FC, and the self-balancing of the dc-link capacitors, so the complex FC voltage balancing strategy and bus midpoint voltage control method are not needed anymore. The voltage and current stresses analysis and the design guidelines of components are discussed in detail. A comparison with some existing topologies has also been made to highlight its performance. Taking one phase as an example, both the simulations and experiments are carried out to verify the validity of the proposed inverter and modulation strategy.**

***Index Terms*—High dc voltage utilization, multilevel inverter, pulsewidth modulation (PWM), self-balancing capacity, three-phase system.**

I. Introduction

IN RECENT years, the development and utilization of clean and renewable energy has attracted much attention with the increasingly serious problems of environmental pollution and energy crisis. Among them, photovoltaic and wind power generation have been widely used because of their wide distribution, clean production process, safe, and reliable. In the photovoltaic and wind power generation system, power electronic inverter is the core equipment. And multilevel inverter has important application prospects because of its excellent output waveform quality, small harmonic content of output voltage, low voltage stress of switching devices, and small output filter [1], [2].

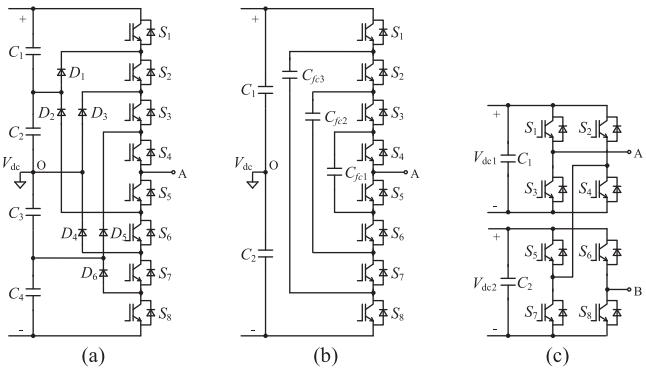

Fig. 1. Conventional 5L topologies. (a) 5L-NPC. (b) 5L-FC. (c) CHB.

Multilevel inverter has experienced decades of development since its birth. The popular multilevel topologies widely used in industrial applications mainly include the following categories: Neutral point clamped (NPC) converter [3], flying capacitor (FC) converter [4], and cascaded H-bridge (CHB) converter [5], as shown in Fig. 1. As the number of voltage level increases, the voltage stresses of the devices, the total harmonic distortion (THD) and the electromagnetic interference decrease, hence, excellent output quality and low system cost can be obtained. At the same time, the complexity regarding the structure and control technique for multilevel inverters also increases. For example, as the voltage level in NPC increases, the number of clamping diodes and capacitors also increases dramatically. Furthermore, it is difficult to realize the dc-link capacitor voltage balance in higher-level NPC topologies [6]. Likewise, a more complex control scheme is required to balance the voltage of each capacitor in the higher level FC type topologies [7]. The CHB requires a large number of isolated dc sources or phase-shifting isolation transformers, which makes the system bulkier and more expensive [8]. In addition to these general topologies, some improved topologies are proposed in the literature. The active NPC (ANPC) inverter, which combines the concept of NPC, FC, and CHB has received more attention [9], [10]. The hybrid topology, which is obtained through the combination of basic three-level cells, is one type of scheme to reduce the elements. For example, the combination of three-level FC and

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H-bridge cells [11], and the combination of three-level T-type NPC and H-bridge cells [12]. In order to reduce the number of active devices, the devices are multiplexed such as seven-switch 5L-ANPC [13] and six-switch 5L-ANPC [14]. By coupling three-phase together, a reduced components three-phase five-level topology is proposed in [15].

Multilevel inverter is the key equipment in OFF grid and grid connected occasions such as motor drive and photovoltaic power station. It is reported that an increase of inverter maximum dc-link voltage from 1000 V to 1500 V can lead to 15–85% saving in conductor mass of the cables, and the saving in the number of combiner boxes can range between 25 and 60% [16]. Similarly, increasing the ac voltage of PV system is also conducive to reducing the initial investment cost of the system and improve the system efficiency. That is because multilevel inverter requires a higher dc-link voltage, which is two times the peak of the ac output voltage. For many applications, the traditional designs may require an additional boost converter in the input or a step-up transformer in the output. However, the multistage power conversion reduces the efficiency and reliability, whilst increasing the size and cost of the system. Therefore, the inverter with the ability to improve the ac output voltage offers an interesting alternative compared to two stage approach.

There are several kinds of single-stage boost inverter such as Z-source inverter (ZSI) and switched-capacitor-based inverter. In ZSI, two inductors and two capacitors consist of an X-type structure. The X-type structure enables ZSI to realize single-stage boost capability by the shoot-through states. Therefore, ZSI does not need to add dead time, and it works more reliably and has less harmonic content of output voltage. Various improved ZSI topologies have been proposed in the academic. For example, the topologies with the purpose of reducing the voltage stress of Z-source network [17], [18], the topology aiming at reducing the number of inductors or capacitors [19], and the topologies aiming at increasing the boost ratio [20]. A five-level quasi Z-source inverter is proposed in [21]. Six passive elements are required, which increases the system volume. A three-phase five-level ANPC Z-source inverter is proposed in [22]. It also suffers from more passive elements. In summary, ZSI also has its own inherent disadvantages, such as limited boost ratio, small power volume ratio, and complex design for snubber circuit [23]. Switched-capacitor based inverter is also an effective way to achieve boost capability. A five-level inverter with a two times voltage boosting feature for grid-tied applications is proposed in [24]. A topology that can achieve four times the voltage gain is proposed in [25]. Some five- or seven-level topologies are proposed in [26]–[30]. Most of these topologies are full-bridge configurations, which means that they are not easily extended to three-phase systems. Two topologies with boost capability, named 5L-boost-ANPC and 7L-boost-ANPC, are designed for three-phase system in [31] and [32], respectively. Both of them can obtain up to twice the voltage gain, while the voltage stress of the active switch is doubled at the same time.

In this article, a three-phase five-level high dc voltage utilization inverter is proposed. It achieves a compromise between voltage gain and device stress. Two times the voltage gain is obtained, and the stresses of all devices are only half of the dc-link voltage at the same time. This article is organized as follows: Section II provides the structure and detailed operating principles of the proposed inverter; Section III gives the modulation strategy; the components design rules and a comparison table are presented in Section IV; Section V gives the simulation and experimental results; and Finally, Section VI concludes this article.

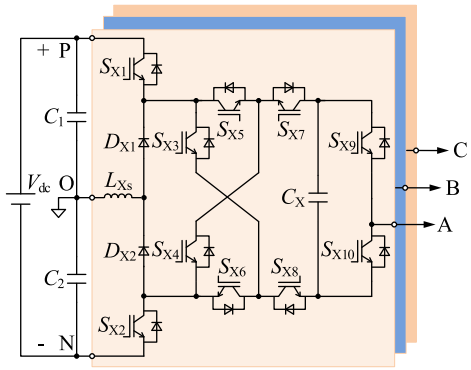

Fig. 2. Schematic of the proposed inverter.

II. Operation Principles and Modulation Strategy of the Proposed Inverter

A. Introduction of the Proposed Inverter

The schematic of the inverter is shown in Fig. 2. The dc-link voltage is defined as $V_{\rm dc}$. C_1 and C_2 are dc-link split capacitors, whose rated voltages are half the dc-link voltage. The phase leg consists of ten active switches ($S_{\rm X1}$–$S_{\rm X10}$), two diodes ($D_{\rm X1}$–$D_{\rm X2}$), one flying capacitor (FC) $C_{\rm X}$ and one current-limiting inductance $L_{\rm Xs}$ (X ∈ (A, B, C) phases). Here, the role of $L_{\rm Xs}$ is to limit the charging current of FC and it can be considered as a wire when the converter enters in the steady state at each voltage level. $C_{\rm X}$ is charged to $V_{\rm dc}/2$ through the power devices and current-limiting inductor within every switching cycle from the input supply $V_{\rm dc}$ to generate a doubled voltage level. Through the voltage combination of dc-link capacitors and the FC, five output voltage levels $+V_{\rm dc}$, $+V_{\rm dc}/2$, 0, $-V_{\rm dc}/2$, and $-V_{\rm dc}$ can be obtained, which are defined, respectively, as $+2$, $+1$, 0, -1, and -2.

Some of the prominent features of the proposed inverter are as follows.

1) The dc voltage utilization rate is doubled compared with traditional three-phase five-level NPC, ANPC, and FC inverter families, while the voltage stress on each switch is $V_{\rm dc}/2$. The dc voltage utilization is defined as the ratio of the maximum amplitude of the output ac voltage to the dc-link voltage. For conventional multilevel inverters, the dc voltage utilization is 0.5; while for the proposed inverter, the dc voltage utilization is 1. It meant that when the transmission power and the dc-link voltage is constant, the ac voltage is doubled and the ac current is reduced by half, so the cost and loss of the ac cable will be reduced.

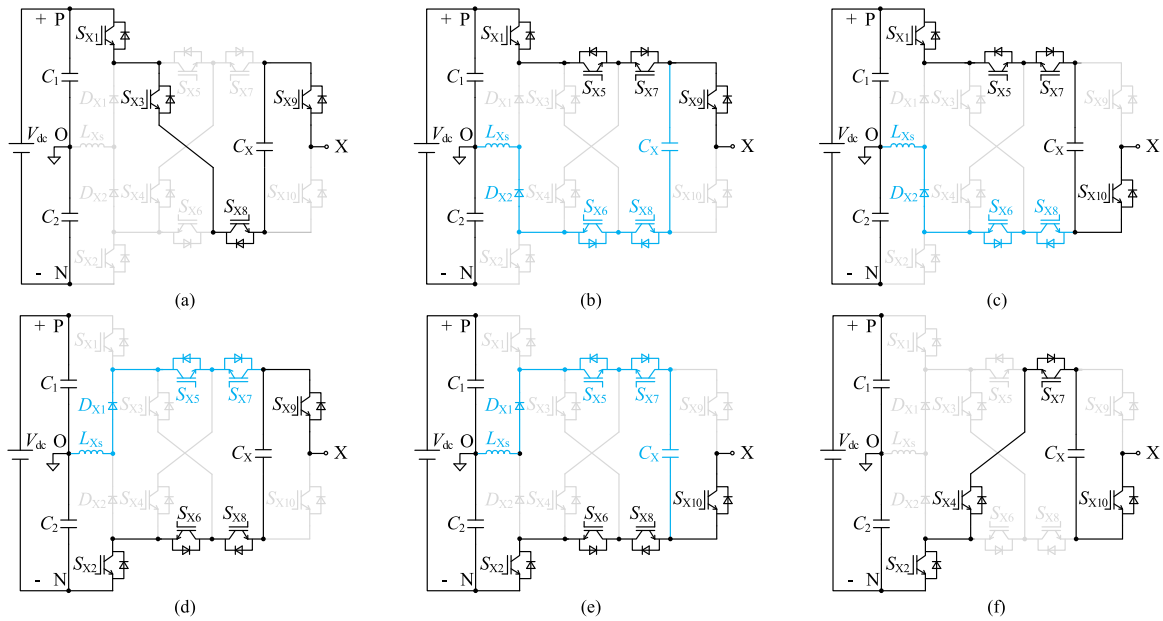

Fig. 3. Six modes for the inverter. (a) Mode A: +2. (b) Mode B: +1. (c) Mode C: 0. (d) Mode D: 0. (e) Mode E: −1. (f) Mode F: −2.

The cost of the inverter itself may not be reduced, but the total cost of the system will be reduced.

2) The FC has the capability of self-start, thus, the precharge circuits are no longer needed. And the voltage balance for dc-link capacitors and FC is achieved automatically. So, the system complexity is reduced and the system reliability is improved.
3) The inverter can operate under any power factor and the corresponding modulation strategy is easily implemented in the microcontroller.
4) The charging loop of FC and the output current loop are separated, which will help to achieve the balance of the FC more easily.

B. Operating Modes of the Proposed Inverter

The corresponding switching states in one phase are illustrated in Fig. 3. The operation of the inverter for active and reactive power conditions consists of six modes (Mode A to F). They generate the 5L voltage at the output by summing the dc link and FC voltages. Here, black line represents the load current loop, and blue line represents the FC charging loop.

Mode A: In Fig. 3(a), switches S_{X1}, S_{X3}, S_{X8}, and S_{X9} are ON and other switches become OFF state, the capacitors C_1 and C_X are series connection, the output voltage V_{XO} equals to V_{dc}. It is achieved by summing the voltages across C_1 and C_X. Since the voltage and current of the FC are in the same direction, the FC is discharged in this mode.

Mode B: In Fig. 3(b), switches S_{X1}, S_{X5}, S_{X7}, and S_{X9} are ON to carry the output current. If the voltage of C_X is lower than $V_{dc}/2$, the charging current will charge C_X through S_{X6}, S_{X8}, and D_{X2}. Due to the existing of L_{Xs}, the maximum value of the charging current will be limited within an appropriate level. Because the output current has no effect on the voltage of C_X in this mode, the voltage of C_X will be stable at $V_{dc}/2$ when it is charged to $V_{dc}/2$.

Mode C: In Fig. 3(c), switches S_{X1}, S_{X5}, S_{X7}, and S_{X10} are ON, and voltage level 0 is achieved through the difference between C_1 and C_X. When the output current is positive, C_X will be charged, and otherwise, it will be discharged.

Mode D: In Fig. 3(d), switches S_{X2}, S_{X6}, S_{X8}, and S_{X9} are ON. Modes C and D are a pair of redundant modes because the effect of the output current on the voltage of C_X is opposite.

Mode E: In Fig. 3(e), switches S_{X2}, S_{X6}, S_{X8} and S_{X10} are ON and voltage level -1 is obtained. Similar with Mode B, the output current has no influence on the voltage of C_X. The charging loop consists of S_{X5}, S_{X7}, and D_{X1}.

Mode F: In Fig. 3(f), switches S_{X2}, S_{X4}, S_{X7}, and S_{X10} are ON and other switches become OFF state. Similar, the output voltage V_{XO} equals to $-V_{dc}$, which is achieved by summing the voltages across C_2 and C_X. C_X will be discharge under the active output current.

The output voltage, corresponding switching states, and the impact of currents to C_X are listed in Table I. The current in the output power loop is defined as i_{ac} and the current in the charging loop is defined as i_{charge}. It can be seen that i_{ac} has an influence on C_X in Modes A, C, D, and F, and charging or discharging depends on the direction of i_{ac}. While, i_{charge} always charges C_X in Modes B, C, D, and E. Hence, the voltage of C_X can be maintained at a constant value by selecting the appropriate switch state combination.

III. Modulation Strategy

The modulation strategy for the proposed three-phase five-level inverter under active and reactive power conditions is discussed in this section.

TABLE I
SUMMARY OF MODES AND THEIR EFFECTS ON FC

Mode	V_{XO}	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	S_{X7}	S_{X8}	S_{X9}	S_{X10}	Impact of i_{ac} to C_X		Impact of i_{charge} to C_X
												$i_{ac}>0$	$i_{ac}<0$	
A	V_{dc}	1	0	1	0	0	0	0	1	1	0	↓	↑	-
B	$V_{dc}/2$	1	0	0	0	1	1	1	1	1	0	-	-	↑
C	0	1	0	0	0	1	1	1	1	0	1	↑	↓	↑
D	0	0	1	0	0	1	1	1	1	1	0	↓	↑	↑
E	$-V_{dc}/2$	0	1	0	0	1	1	1	1	0	1	-	-	↑
F	$-V_{dc}$	0	1	0	1	0	0	1	0	0	1	↑	↓	-

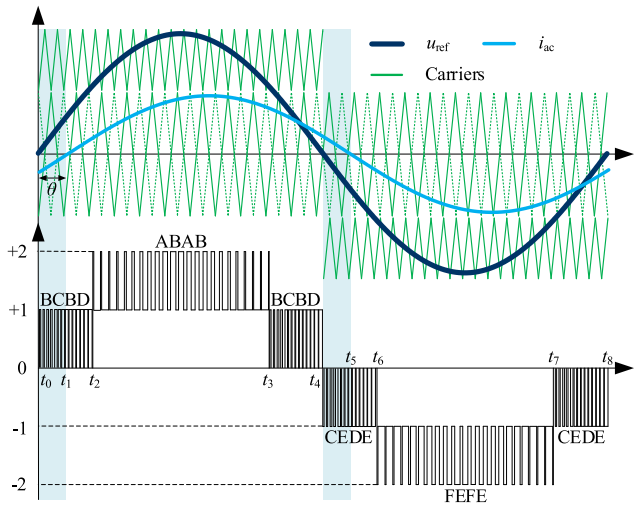

Fig. 4. Modulation strategy of the proposed inverter.

TABLE II
VOLTAGE AND CURRENT RATING OF THE PROPOSED INVERTER

Switches	Voltage stress	Current stress
S_{X1}, S_{X2}, S_{X5}–S_{X8}	$V_{dc}/2$	$I_{om}+I_{cm}$
S_{X3}, S_{X4}, S_{X9}, S_{X10}	$V_{dc}/2$	I_{om}
D_{X1}, D_{X2}	$V_{dc}/2$	I_{cm}

The diagram of the pulsewidth modulation for the proposed inverter is shown in Fig. 4. One reference signal and four carriers are required to generate the appropriate gating signals for one phase of the inverter. The dark blue line is the reference wave (u_{ref}), and the blue line is the output current (i_{ac}), which lags behind u_{ref} with a phase angle θ. The green lines represent four carriers. In order to obtain the redundant Modes C and D, the amplitudes of the middle two carriers are twice that of the other two, and their phase difference is 180°.

Based on the abovementioned analysis, switching pattern for each voltage level is discussed in detail as follows.

1) Level +1 [t_0–t_2 and t_3–t_4]: The output voltage u_{AO} is switches between +1 and 0 voltage levels; Mode B is selected to generate +1 voltage level and it always charges C_X. To keep the voltage of C_X at $V_{dc}/2$ in +1 level, the redundant Modes C and D are selected to generate 0 level. Finally, the switching sequence BCBD is obtained. When i_{ac} is negative (reactive power region t_0–t_1), Mode C will discharge C_X, and when i_{ac} is positive (active power regions t_1–t_2, t_3–t_4), Mode D will discharge C_X. By the abovementioned switching sequence, the voltage of C_X can be balanced at the switching frequency.
2) Level +2 [t_2–t_3]: The output voltage u_{AO} is switches between +2 and +1 voltage levels, thus, Modes A and B are selected to generate +2 and +1 voltage levels, respectively. Hence, the switching sequence ABAB can be obtained.
3) Level −1 [t_4–t_6 and t_7–t_8]: The output voltage u_{AO} is switches between −1 and 0 voltage levels. Similarly, Mode E is selected to generate −1 voltage level, and the redundant Modes C and D are selected to generate 0 voltage level. Then, the switching sequence CEDE is obtained. The Mode E will always charge C_X under both active and reactive power regions. While, Mode D will discharge C_X in the reactive power region (t_4–t_5), and Mode C will discharge C_X in the active power region (t_5–t_6, t_7–t_8). As a result, the voltage of C_X is balanced at $V_{dc}/2$ at the switching frequency.
4) Level −2 [t_6–t_7]: The output voltage is switches between −1 and −2 voltage levels, thus, Modes E and F are selected to generate −1 and +2 voltage levels, respectively. Hence, the switching sequence FEFE is obtained.

From the abovementioned analysis, it can be concluded that the inverter has a full reactive power capability without any special considerations, such as special modulation techniques or switch arrangements for nonunity power-factor operation.

IV. COMPARATIVE SUMMARY AND DESIGN GUIDELINES

A. Devices Stress Analysis

The voltage and current ratings of the active switches and diodes are deduced from Table II, where I_{om} is the maximum value of i_{ac}, and I_{cm} is the maximum value of the capacitor charging current. It can be seen that the voltage stresses of all the devices are $V_{dc}/2$. As for current stress, six active switches (S_{X1}, S_{X2}, S_{X5}–S_{X8}) are burdened by the capacitor charging current and the load current together; the other four active switches (S_{X3}, S_{X4}, S_{X9}, S_{X10}) and two diodes (D_{X1}, D_{X2}) are burdened by the load current and the capacitor charging current, respectively. However, by reasonably designing the current limiting inductor, the peak value of pulse current can be limited to the same level as the peak value of output current. In addition, the maximum charging current always occurs during the ±1 level, so the actual maximum current flowing switches is less than the sum of charging current and the load current. In order to ensure a

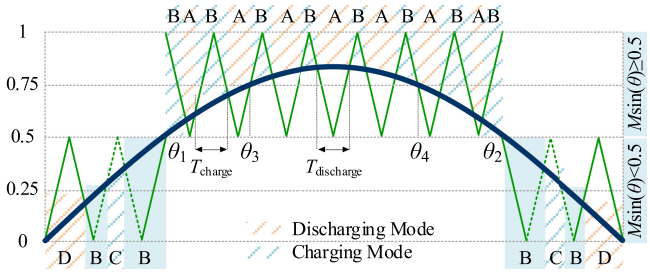

Fig. 5. Switching pattern of the modulation strategy in positive half period.

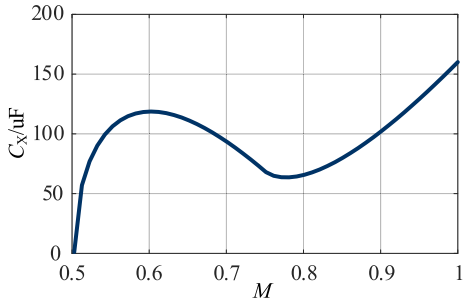

Fig. 6. Variation curve of C_X with M.

certain margin, the device is selected according to the sum of charging current and load current.

B. Self-Start of FC and Self-Balance of DC-Link Capacitors

For conventional converters, which have FC units, it is usually necessary to equip with another precharging circuit to charge the FC voltage to a given value, and then stabilize it through the corresponding modulation strategy, so the cost and complexity of the system will increase. For the proposed 5L-boost inverter, its precharging process can be realized by the topology itself. During the precharging of the dc-link capacitor, the FC exchanges energy with the two dc-link capacitors alternately. Detailly, in the positive half cycle of $u_{\rm ref}$, $C_{\rm X}$, and C_1 are connected in parallel to exchange energy (Modes B and C), so the voltage of $C_{\rm X}$ will slowly rise with the voltage of C_1; in the negative half cycle of the output voltage, $C_{\rm X}$ and C_2 are directly connected in parallel to exchange energy (Modes D and E), so the voltage of $C_{\rm X}$ will rise slowly with the voltage of C_2. The charging process will not end until the voltage of $C_{\rm X}$ and the voltages of C_1 and C_2 are equal, and finally the self-start process of $C_{\rm X}$ is achieved.

Since $C_{\rm X}$ exchanges energy with C_1 and C_2 alternately in a power frequency period, then C_1 and C_2 are equivalent to indirectly exchange energy, so the self-balance of the dc-link capacitors voltages is obtained accordingly.

C. Selection of FC

Fig. 5 shows the detailed switching pattern of the inverter and its influence on the voltage of $C_{\rm X}$ during the positive half period of $u_{\rm ref}$. $T_{\rm charge}$ and $T_{\rm discharge}$ are the time of charging and discharging modes in a switching cycle. θ_1 and θ_2 are the moments when $u_{\rm ref}$ crosses 0.5, and θ_3 and θ_4 are the moments when $u_{\rm ref}$ crosses 0.75. In combination with the modulation strategy proposed in Section III, the voltage variation of $C_{\rm X}$ under the unity power factor is analyzed in detail as follows.

When $M{\cdot}\sin\theta{\leq}0.5$, the redundant Modes C and D have an opposite effects on the $C_{\rm X}$ voltage, and the duration time and the current of these two modes is almost the same when the carrier frequency is far greater than 50/60 Hz. As a result, the voltage fluctuation of $C_{\rm X}$ will be very small.

When $M{\cdot}\sin\theta{>}0.5$, Mode A always discharges $C_{\rm X}$ and Mode B always charges $C_{\rm X}$. What is more, $T_{\rm discharge}$ is an increasing function and $T_{\rm charge}$ is a decreasing function when $u_{\rm ref}$ is increasing. In this case, the fluctuation law of $C_{\rm X}$ voltage should be discussed in the following two cases according to the modulation index M.

1) Case 1: When $0.5{<}M{<}0.75$, $T_{\rm discharge}$ is always less than $T_{\rm charge}$, so the voltage of $C_{\rm X}$ increases linearly during $[\theta_1, \theta_2]$, and the maximum FC voltage ripple $\Delta V_{\rm FC}$ is obtained by

$$\Delta V_{\rm X} = \int_{\theta_1}^{\theta_2} \delta V_{\rm X} d\theta \tag{1}$$

where θ_1 and θ_2 can be obtained with (2), $\delta V_{\rm X}$ is voltage variation during a switching cycle, which can be written as (3). $I_{\rm om}$ is the amplitude of $i_{\rm ac}$. $T_{\rm charge}$ and $T_{\rm discharge}$ can be expressed as (4) follows:

$$\begin{cases} \theta_1 = \arcsin(1/2M) \\ \theta_2 = \pi - \theta_1 \end{cases} \tag{2}$$

$$\delta V_{\rm X} = \frac{\delta Q_{\rm FC}}{C_{\rm X}} = \frac{I_{\rm om}\sin\theta \cdot (T_{\rm charge} - T_{\rm discharge})}{C_{\rm X}} \tag{3}$$

$$\begin{cases} T_{\rm discharge} = T(2M\sin\theta - 1) \\ T_{\rm charge} = T(2 - 2M\sin\theta) \end{cases}. \tag{4}$$

1) Case 2: When $0.75{<}M{<}1$, the change of $\Delta V_{\rm FC}$ with M is nonlinear during $[\theta_1, \theta_2]$. The peak and valley of $\Delta V_{\rm FC}$ appear at the moment of $T_{\rm charge} = T_{\rm discharge}$, where the moments are expressed as θ_3 and θ_4. Therefore, the maximum FC voltage ripple $\Delta V_{\rm FC}$ can be obtained by

$$\Delta V_{\rm X} = \text{Max}\left\{\int_{\theta_1}^{\theta_2} \delta V_{\rm X} d\theta, \int_{\theta_3}^{\theta_4} \delta V_{\rm X} d\theta\right\} \tag{5}$$

where θ_3 and θ_4 can be obtained by

$$\begin{cases} \theta_3 = \arcsin(3/4M) \\ \theta_4 = \pi - \theta_3 \end{cases}. \tag{6}$$

With the (1) and (5), Fig. 6 shows the curve of $C_{\rm X}$ with M, where $\Delta V_{\rm FC}$ is limited to 2% of FCs voltage [14] and the key parameters listed in Table IV. It can be seen that the maximum value of $C_{\rm X}$ is about 160 uF when $M = 1$. It is worth noting that the above calculation process is based on the assumption that the charge current and the discharge current are equal. However, in practice, it is difficult to guarantee that they are equal. Hence, a certain margin should be taken into consideration.

TABLE III
COMPARISON WITH EXISTING TOPOLOGIES

Topology	Number, voltage and current stress of devices						Number, voltage and current stress of FC							No. of dc source	Gain	Extend
	a	b	d	e	t_{vs}	t_{cs}	a	b	c	d	e	t_{vs}	t_{cs}			
5L-NPC	0	0	0	14	$3.5V_{dc}$	$14I_{om}$	0	0	0	0	0	0	0	1	0.5	Y
5L-FC	0	0	0	8	$2V_{dc}$	$8I_{om}$	0	0	1	1	1	$1.5V_{dc}$	$3I_{om}$	1	0.5	Y
5L-CHB	0	0	8	0	$4V_{dc}$	$8I_{om}$	0	0	0	0	0	0	0	2	0.5	Y
5L-ANPC	0	0	4	4	$3V_{dc}$	$8I_{o}$	0	0	0	0	1	$0.25V_{dc}$	I_{om}	1	0.5	Y
[24]	3	6	0	0	$12V_{dc}$	$8I_{om}$+$6I_{cm}$	0	2	0	0	0	$2V_{dc}$	$2I_{om}$+$2I_{cm}$	1	2	Y
[26]	5	4	0	0	$14V_{dc}$	$9I_{om}$+$4I_{cm}$	1	1	0	0	0	$3V_{dc}$	$2I_{om}$+$2I_{cm}$	1	2	Y
[27]	2	9	0	0	$13V_{dc}$	$6I_{om}$+$9I_{cm}$	0	2	0	0	0	$2V_{dc}$	$2I_{om}$+$2I_{cm}$	1	2	N
[30]	6	4	0	0	$16V_{dc}$	$8I_{om}$+$2I_{cm}$	0	1	0	0	0	V_{dc}	I_{om}+I_{cm}	1	2	N
[31]	0	4	4	0	$6V_{dc}$	$8I_{om}$+$4I_{cm}$	0	1	0	0	0	V_{dc}	I_{om}+I_{cm}	1	1	Y
Proposed	0	0	12	0	$6V_{dc}$	$10I_{om}$+$8I_{cm}$	0	0	0	1	0	$0.5V_{dc}$	I_{om}+I_{cm}	1	1	Y

gain $= V_{max}/V_{dc}$, where V_{max} represents the maximum value of the output ac voltage; $a = 2\ V_{dc}$, $b = V_{dc}$, $c = 3\ V_{dc}/4$, $d = V_{dc}/2$, e $= V_{dc}/4$, "Extend" represents that weather the inverter can be extended to three phase.

TABLE IV
PARAMETERS OF THE PROTOTYPE

Parameters	Symbols	Value
Power rating	P	1 kVA
Input voltage	V_{dc}	400 V
dc-link capacitor	C_1, C_2	940 uF, 250 V
Flying capacitor	C_X	940 uF, 250 V
Filter inductor	L_F	3 mH
Filter capacitor	C_F	2 uF
Current-Limiting Inductor	L_{Xs}	5.6 μH
Switching frequency	f_s	10 kHz
Switches	S_{X1}–S_{X10}	IKW40N60
Diodes	D_{X1}, D_{X2}	RHRG5060

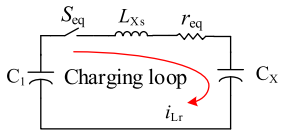

Fig. 7. Equivalent charging circuit.

D. Selection of Current-Limiting Inductor

Taking Mode B as an example, the equivalent charging circuit is shown in Fig. 7, where r_{eq} is the parasitic impedances, such as the ON-state resistances of switches, the forward voltage drops of diodes, and the equivalent series resistances of capacitors; S_{eq} denotes the switches and diodes in the charging circuit.

Turning ON S_{eq}, the charging current can be expressed as [33]

$$i_{Lr}(t) = \frac{\Delta V}{L_{Xs}\omega_d} e^{-\frac{r_{eq}}{2L_{Xs}}t} \sin \omega_d t \tag{7}$$

where ΔV is voltage difference between V_{C1} and V_{CF}, and ω_d is written as

$$\omega_d = \frac{\sqrt{4L_{Xs} - r^2{}_{eq}}}{2L_{Xs}\sqrt{C_X}}. \tag{8}$$

Thus, the maximum value of charging current be calculated as follows:

$$\begin{cases} \varphi = \arctan(2\omega_d L_{Xs}/r_{eq}) \\ i_{Lrmax} = \frac{\Delta V}{L_{Xs}\omega_d} e^{-\frac{r_{eq}\varphi}{2\omega_d L_{Xs}}} \sin\varphi \end{cases}. \tag{9}$$

It can be seen from (9) that, i_{Lrmax} is inversely proportional to L_{Xs}, which means larger charging inductor will contribute to smaller peak charging current. However, larger L_{Xs} will slow down the charging speed of C_X and increase the volume of inverter. In the experiment, $L_{Xs} = 5.6\ \mu$H, the maximum charging current is limited to 8 A.

E. Comparison With Existing Topologies

A comparative summary of the key features of the proposed inverter with some existing topologies is presented in Table III.

The parameters and numbers of components included are for a phase leg only. The total voltage stress (t_{vs}) and current stress (t_{cs}) represent the sum of the voltage stress and current stress of each device. "Extend" represents that weather the inverter can be extended to three phase.

The advantages of the conventional topologies (5L-NPC, 5L-FC, 5L-CHB, and 5L-ANPC) are that the voltage stresses of the device are small. For example, for 5L-NPC and 5L-FC, the voltage stresses are only $V_{dc}/4$; for 5L-CHB, the voltage stress is $V_{dc}/2$; and for 5L-ANPC, the voltage stress is $V_{dc}/2$ or $V_{dc}/4$. However, the dc voltage utilizations for these topologies are only 0.5.

Because multilevel converters based on switched capacitors can obtain higher dc voltage utilizations, they have become a research hotspot today. For example, the topologies in [24], [26], [27], and [30] can reach a voltage gain of 2. However, the voltage stresses of devices and FCs for these topologies are high, so does t_{vs}. In addition, most of these topologies are full bridge structures, which means that they cannot be extended to three-phase systems. The 5L-boost-ANPC [31] uses the least active switches to generate a five-level output voltage, and it also can increase dc voltage utilizations by twice. However, the voltage stresses of four switches and one FC increase to V_{dc}.

Compared with single-phase five-level Z-source inverter [21], [22], the proposed topology has advantages in the number and cost of passive components. Especially in high-power occasions, inductance and capacitance account for a large proportion in volume and cost.

The proposed inverter has lower total active devices voltage stresses compared with other topologies. As for t_{vs} of flying capacitor, it is also smaller than most topologies. Finally, the disadvantage of the proposed inverter is that the t_{cs} of active devices is the largest. All in all, the proposed topology achieves

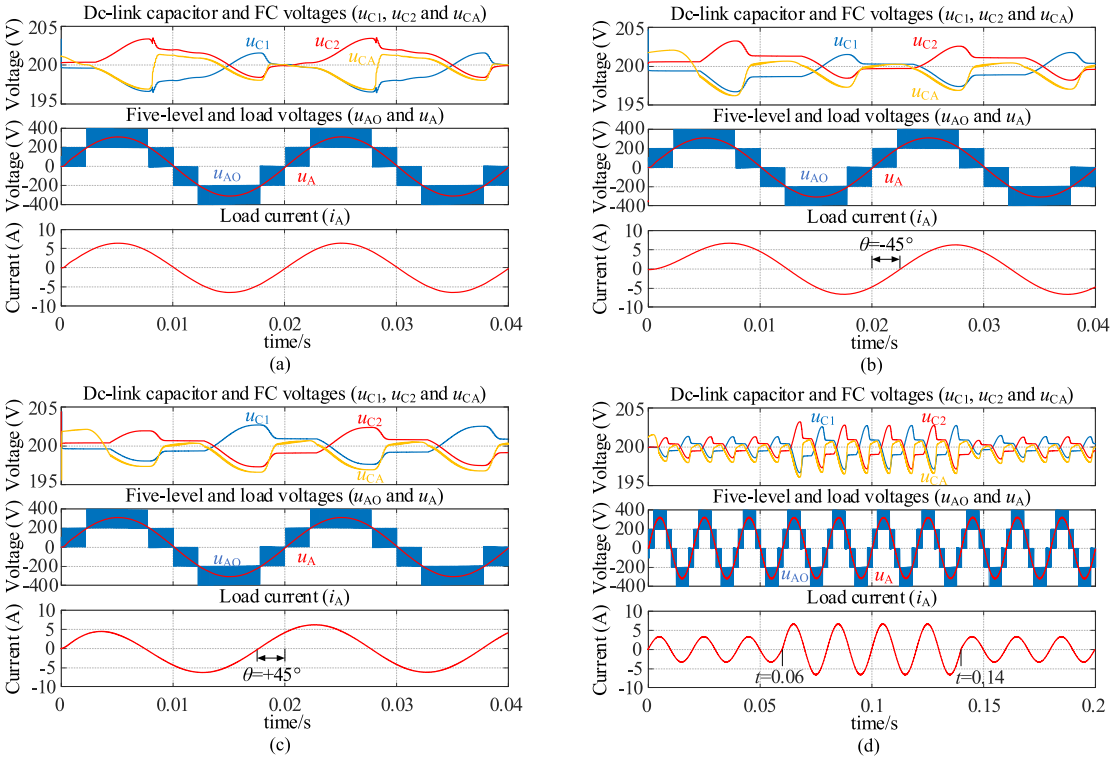

Fig. 8. Some key simulated waveforms of the inverter. (a) Waveforms under unity power factor. (b) Waveforms under lagging power factor of $\theta = -45°$. (c) Waveforms under leading power factor of $\theta = +45°$. (d) Waveforms of load mutation.

a better compromise between the dc voltage utilizations and the devices voltage stresses compared to the existing topologies.

V. Simulation and Experimental Verification

The simulations and experimental tests have been carried out to verify the effectiveness of the proposed topology. The parameters used for simulation and experimental tests are listed in Table IV.

A. Simulation Results

In order to verify the proposed topology and modulation method, the simulations have been carried out on the joint platform of MATLAB and PLECS.

Fig. 8 shows the dc-link voltages (u_{C1} and u_{C2}), FC voltage (u_{CA}), the output five-level voltage (u_{AO}), load voltage (u_A), and current (i_A) under different working conditions. Fig. 8(a) shows the simulation waveforms under unity power factor. The inverter produces an rms voltage of 220 V for a 400 V dc-link voltage. The voltages u_{C1}, u_{C2}, and u_{CA} are well stabilized at 200 V with relatively small fluctuation. It is also can be seen that the fluctuation of u_{C1}, u_{C2}, and u_{CA} is very small during the voltage levels ± 1 and 0, while the fluctuation is large during the voltage level ± 2. This is consistent with the theoretical analysis. The maximum fluctuation value of u_{CA} is about 4.16 V (4.16 V / 200 V = 2.08%).

Fig. 8(b) and (c) show the waveforms under both lagging and leading power factors, respectively. It is evident that there is a natural balance in the voltage across the dc-link capacitors around its reference value $u_{C1} = u_{C2} = V_{dc}/2 = 200$ V.

Fig. 8(d) shows the dynamic performance of the inverter. The inverter is simulated under sudden change in the load. The inverter steps from half load to full load at 0.06 s and from full load to half load at 0.14 s. It can be seen that the inverter tracks its reference very well. The fluctuations of u_{C1}, u_{C2}, and u_{CA} are different under different load currents, but they are stable at 200 V in the whole process.

Fig. 9 shows the charging current waveforms under unity power factor. Fig. 9(a) shows the dc-link and FC voltages, output voltage and current, and charging current. It can be seen from Fig. 9(a) that the maximum charging current occurs when the inverter outputs ± 1 levels. The reason can be explained as follows. During the $+2$ level, the inverter switches between Modes A and B. In Mode A, C_1, and C_X are always discharged at the same time. In Mode B, the voltage of C_1 is always less than or equal to the voltage of C_X. Therefore, the charging current is very small during Modes A and B. During $+1$ level, the inverter switches between Modes B, C, and D. Since C_2 is always charged at $+2$ level, there is a large voltage difference between C_2 and C_X in mode D, resulting in a large charging current. Fig. 9(b) shows the FFT result of output voltage u_A, where "Fund." represents the fundamental component. It can be seen that the THD of u_A is about 38.92%, the dc and low frequency harmonic components are very low as well. Therefore, the proposed inverter has good differential-mode performance.

Fig. 10 shows the charging current waveforms under reactive power condition. As shown in Fig. 10(a), the load current does

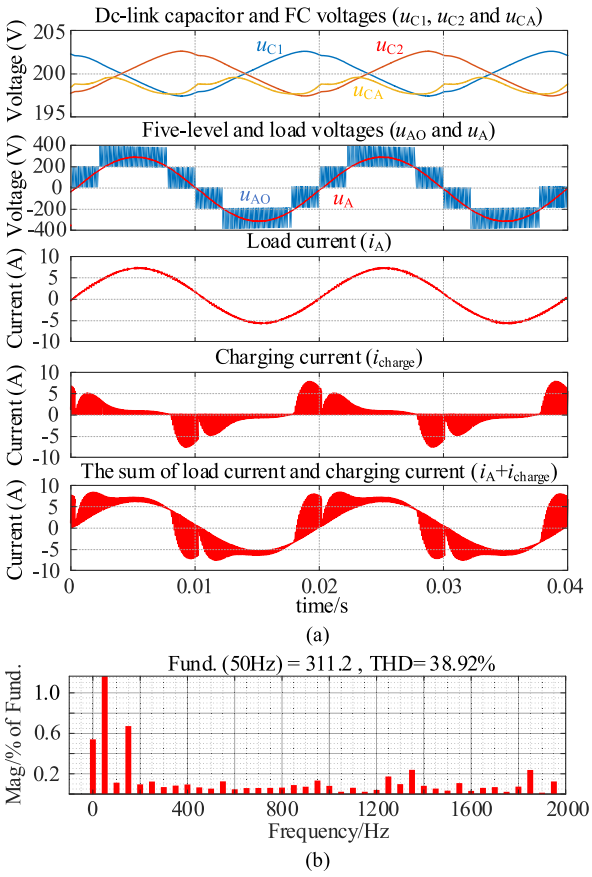

Fig. 9. Charging current waveforms under unity power factor. (a) Dc-link and FC voltages (u_{C1},u_{C2}, and u_{CA}), output voltage and current (u_{AO}, u_A, and i_A), and charging current (i_{charge} and i_A+i_{charge}). (b) FFT result of output voltage u_A.

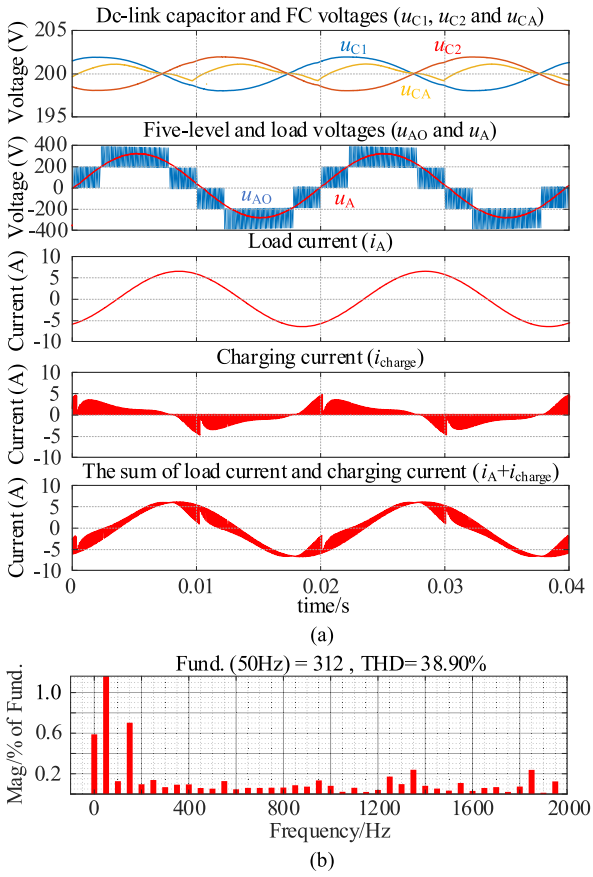

Fig. 10. Charging current waveforms under reactive power factor. (a) Dc-link and FC voltages (u_{C1} and u_{C2}), output voltage and current (u_{AO}, u_A, and i_A), and charging current (i_{charge} and i_A+i_{charge}). (b) FFT result of output voltage u_A.

not discharge C_1 at the maximum value in Mode A, so the voltage difference between C_2 and C_X in Mode D is small and the maximum charging current is also small. Fig. 10(b) shows the FFT result of output voltage u_A. It can be seen that the THD of u_A is about 38.9%. The distribution of the harmonic spectrum is the same as that under unity power factor.

It also can be seen from Figs. 9 and 10 that the maximum charging current appears at ± 1 level. In unit power factor condition, the charging current is large, but the load current at ± 1 level is small, so the sum of the charging current and the load current is small. Under reactive power factor condition, the load current at ± 1 level is large, but the charging current is small, so the sum of the charging current and the load current is still small. Therefore, the EMI and the current rating of the devices will not increase much.

B. Experimental Results

In order to verify and validate the practicality of the proposed inverter, a 1 kW prototype is built, as shown in Fig. 11, when taking one phase as an example. The system parameters are the same as those listed in Table IV.

Fig. 12 shows the experimental results under unity power factor. Detailly, Fig. 12(a) shows the voltages of u_{dc}, u_{AO}, u_A,

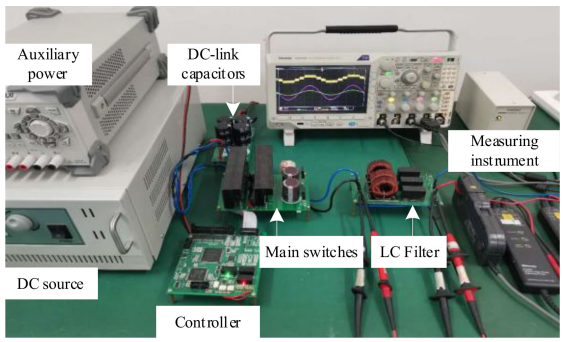

Fig. 11. Experimental prototype.

and i_A. It can be seen that a five-level output voltage is generated, and the sinusoidal phase voltage and current are also obtained. It should be noted that u_{dc} is 400 V shown in Channel 2, and the magnitude of u_A is 311 V shown in Channel 3. Hence, the high dc voltage utilization is a major achievement of the proposed inverter compared with conventional 5L topologies. Channel 4 shows the output current i_A, the rms value is about 4.6 A.

As shown in Fig. 12(b), the dc-link voltages u_{C1} and u_{C2}, the FC voltage u_{CA} and the current flowing into point O i_O

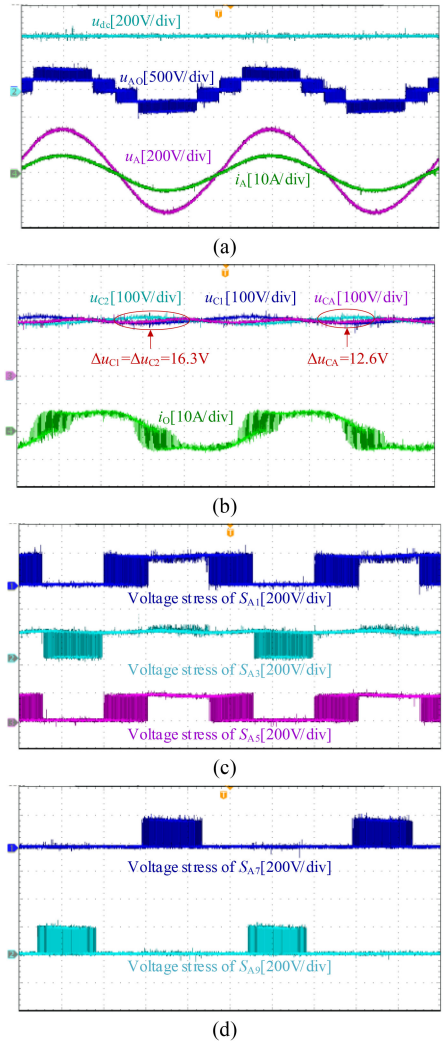

Fig. 12. Experimental results under unity power factor. (a) Input voltage, output five-level voltage, load voltage, and current. (b) Dc-link voltage, FC voltages, and current flowing into point O. (c) Voltage stresses of S_{A1}, S_{A3}, and S_{A5}. (d) Voltage stresses of S_{A7} and S_{A9}.

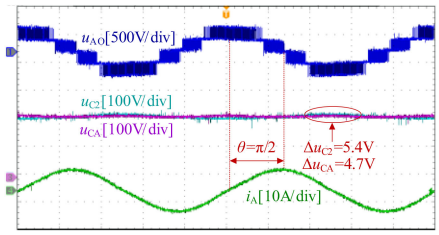

Fig. 13. Experimental results under reactive power factor $\theta = \pi/2$.

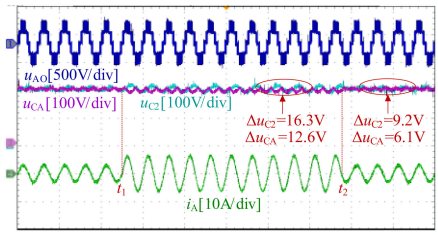

Fig. 14. Transient response of the inverter with load change.

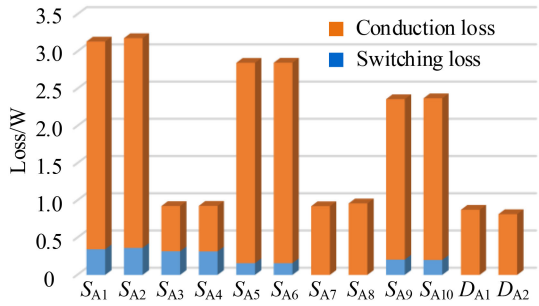

Fig. 15. Loss distribution of each device.

can be observed. The average voltages for them are all 200 V. The measured peak-to-peak dc-link capacitor voltage ripples are 16.3 V (= 16.3 V/200 V = 8.2%), and the FC voltage ripple is 12.6 V (= 12.6 V/200 V = 6.3%). The experimental results verify the advantages of the proposed topology in terms of self-balancing of dc-link and FC voltages. Channel 4 shows the current flowing into point O, which is the sum of the output current i_A and the FC charging current i_{charge}. It can be seen that the amplitude of i_{charge} is almost the same as that of i_A. In addition, i_{charge} is large during ± 1 and it is very small during ± 2. This is because FC is charge only by C_1 or C_2 during ± 2, while it is charged by both C_1 and C_2 alternately during ± 1.

When the voltages of C_1 and C_2 have a large deviation, a large charging current will appear. In this case, the current stresses of the switches do not increase much, which is beneficial to the efficient and reliable operation of the inverter.

Fig. 12(c) and (d) shows the voltage stresses of switches. The voltage stress of each switch is 200 V. For S_{A1} and S_{A9}, they are switched at the switching frequency during the voltage levels ± 1 and 0; for S_{A3}, S_{A5}, and S_{A7}, they are only switched at the switching frequency during the voltage level $+2$ or -2.

The experimental results under purely inductive load ($\theta = \pi/2$) are shown in Fig. 13. When u_{AO} is during $+2$ and -2, i_A just crosses zero, so the dc-link and FC voltages ripples are smaller than those under unity power factor. The measured peak-to-peak dc-link capacitor and FC voltage ripples are 5.4 V (= 5.4 V/ 200 V = 2.7%) and 4.7 V (= 4.7 V/200 V = 2.35%).

The transient response performance of the inverter is tested and the results are shown in Fig. 14. The load is switched from half to full load at t_1, and from full to half load at t_2. The voltage ripples of u_{C2} and u_{CA} increase with the power increases. While, they are balanced at 200 V. The output current i_A changes very smoothly. Therefore, the excellent transient response performance is obtained.

Fig. 15 shows the loss distribution of each switch based on PLECS software with the same parameters. As expected, the switches in the FC charging path have higher conduction loss then the other switches. Fig. 16 shows the loss distribution of different inverters. It can be seen that the performance of the proposed topology in loss distribution is better than 5L-NPC topology and worse than 5L-FC topology. Fig. 17 shows the experimental measured efficiency at different output power levels

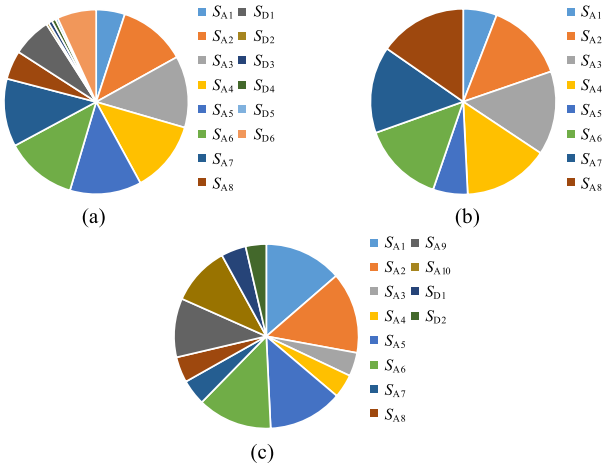

Fig. 16. Loss distribution of different inverters. (a) 5L-NPC. (b) 5L-FC. (c) Proposed inverter.

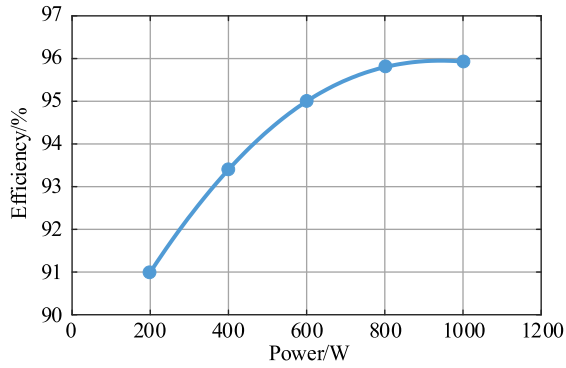

Fig. 17. Measured efficiency of the inverter.

by a power analyzer (HIOKI 3390). The maximum efficiency is about 95.96% at the 1 kW power rating.

VI. Conclusion

In this article, a three-phase five-level inverter with high dc voltage utilization is proposed. The operation principle and modulation strategy under both active and reactive power conditions are analyzed and presented. The comprehensive analysis and comparison are also given.

Compared with conventional five-level inverters, the dc voltage utilization of the proposed inverter is doubled. Compared with some existing boost inverters, the proposed inverter overcomes the shortage of high device voltage stress. What is more, the modulation strategy ensures that the FC voltage is balanced at $V_{dc}/2$ without any additional control strategy. And the dc-link capacitors voltages are also balanced automatically. All these performance have been verified by simulations and experimental tests.

The proposed inverter is suitable for grid-connected renewable energy systems such as PV and wind generation applications, and it is also suitable for OFF-grid power conversion applications such as fans, pumps, and tractions.

References

[1] A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "High-performance constant power generation in grid-connected PV systems," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1822–1825, Mar. 2016.

[2] Y. Chen, Y. Liu, S. Hung, and C. Cheng, "Multi-input inverter for grid-connected hybrid PV/Wind power system," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1070–1077, May 2007.

[3] A. Nabae, I. Takahashi, and H. Akagi, "A neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 1A-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[4] A. Stillwell and R. C. N. Pilawa-Podgurski, "A five-level flying capacitor multilevel converter with integrated auxiliary power supply and start-up," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2900–2913, Mar. 2019.

[5] M. Elias, N. Rahim, H. Ping, and M. Uddin, "Asymmetrical cascaded multilevel inverter based on transistor-clamped H-bridge power cell," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 4281–4288, Nov. 2014.

[6] Z. Shu, X. He, Z. Wang, D. Qiu, and Y. Jing, "Voltage balancing approaches for diode-clamped multilevel converters using auxiliary capacitor-based circuits," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2111–2124, May 2013.

[7] J. Rodríguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[8] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[9] W. Sheng and Q. Ge, "A novel seven-level ANPC converter topology and its commutating strategies," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7496–7509, Sep. 2018.

[10] E. Burguete, J. López, and M. Zabaleta, "New five-level active neutral-point-clamped converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 440–447, Jan. 2015.

[11] P. Roshankumar, P. Rajeevan, K. Mathew, K. Gopakumar, J. Leon, and L. Franquelo, "A five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-bridge," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3505–3512, Aug. 2012.

[12] T. Davis and A. Dey, "Investigation on extending the DC bus utilization of a single-source five-level inverter with single capacitor-fed H-bridge per phase," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2914–2922, Mar. 2019.

[13] H. Wang, L. Kou, Y. Liu, and P. C. Sen, "A seven-switch five-level active-neutral-point-clamped converter and its optimal modulation strategy," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5146–5161, Jul. 2017.

[14] H. Wang, L. Kou, Y. Liu, and P. C. Sen, "A new six-switch five-level active neutral point clamped inverter for PV applications," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6700–6715, Sep. 2017.

[15] A. Karthik and U. Loganathan, "A reduced component count five-level inverter topology for high reliability electric drives," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 725–732, Jan. 2020.

[16] E. Gkoutioudi, P. Bakas, and A. Marinopoulos, "Comparison of PV systems with maximum DC voltage 1000V and 1500V," in *Proc. IEEE 39th Photovolt. Specialists Conf.*, Jun. 2013, pp. 2873–2878.

[17] E. Babaei and E. Shokati Asl, "High-voltage gain half-bridge Z-source inverter with low-voltage stress on capacitors," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 191–197, Jan. 2017.

[18] X. Ding, Y. Hao, K. Li, H. Li, Z. Wei, and W. Wu, "Extensible Z-source inverter architecture: Modular construction and analysis," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1742–1763, Feb. 2021.

[19] A. Ho, T. Chun, and H. Kim, "Extended boost active-switched-capacitor/switched-inductor quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5681–5690, Oct. 2015.

[20] Y. Gu, Y. Chen, and B. Zhang, "Enhanced-boost quasi-Z-source inverter with an active switched Z-network," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8372–8381, Oct. 2018.

[21] C. Das, A. Kirubakaran, and V. Somasekhar, "A five-level quasi Z-source based NPC inverter for PV applications," in *Proc. IEEE Int. Conf. Environ. Elect. Eng. 2019 IEEE Ind. Commercial Power Syst. Eur.*, Jun. 2019, pp. 1–5.

[22] L. Johny and J. Mathew, "A three-phase five-level active-neutral-point-clamped Z-source inverter," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst.*, Dec. 2020, pp. 1–6.

[23] S. Dong, Q. Zhang, and S. Cheng, "Analysis and design of snubber circuit for Z-source inverter applications," *IET Power Electron.*, vol. 9, no. 5, pp. 1083–1091, Apr. 2016.

[24] R. Barzegarkhoo, Y. Siwakoti, and F. Blaabjerg, "A new switched-capacitor five-level inverter suitable for transformerless grid-connected applications," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8140–8153, Aug. 2020.
[25] K. Ito, K. Takahashi, and H. Koizumi, "A common ground five-level inverter using switched capacitor," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc.*, Lisbon, Portugal, Oct. 2019, pp. 1485–1489.
[26] S. Lee, C. Lim, and K. Lee, "Novel active-neutral-point-clamped inverters with improved voltage-boosting capability," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5978–5986, Jun. 2020.
[27] M. Saeedian, S. Hosseini, and J. Adabi, "A five-level step-up module for multilevel inverters: Topology, modulation strategy, and implementation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2215–2226, Dec. 2018.
[28] X. Zhu *et al.*, "Leakage current suppression of single-phase five-level inverter for transformer-less PV system," *IEEE Trans. Ind. Electro n.*, vol. 68, no. 11, pp. 10422–10435, Nov. 2021, doi: 10.1109/TIE.2020.3029480.
[29] X. Zhu, H. Wang, W. Zhang, H. Wang, X. Deng, and X. Yue, "A single-phase five-level transformer-less PV inverter for leakage current reduction," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3546–3555, Apr. 2022, doi: 10.1109/TIE.2021.3075874.
[30] S. Lee, C. Lim, Y. Siwakoti, and K. Lee, "Dual-T-type five-level cascaded multilevel inverter with double voltage boosting gain," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9522–9529, Sep. 2020.
[31] Y. Siwakoti, A. Palanisamy, A. Mahajan, S. Liese, T. Long, and F. Blaabjerg, "Analysis and design of a novel six-switch five-level active boost neutral point clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10485–10496, Dec. 2020.
[32] Y. Siwakoti, A. Mahajan, D. Rogers, and F. Blaabjerg, "A novel seven-level active neutral-point-clamped converter with reduced active switching devices and DC-link voltage," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10492–10508, Nov. 2019.
[33] J. Nilsson and S. Riedel, *Electric Circuits, Ninth Edition*. London, U.K.: Pearson Education, 2011.

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