






A Review of Multisampling Techniques in Power Electronics Applications

Shan He , *Student Member, IEEE*, Dao Zhou , *Senior Member, IEEE*, Xiongfei Wang , *Senior Member, IEEE*, Zhaoyang Zhao , *Member, IEEE*, and Frede Blaabjerg , *Fellow, IEEE*

Abstract—Due to the increasing performance and decreasing price of microcontrollers in recent years, applying a high sampling frequency has become more feasible in modern control that is known as multisampling technology. The first motivation to use multisampling is emulating the analog control, thereby reducing the control delay and improving the stability of power electronics controllers. On the other hand, more information can be acquired from the multisampled current/voltage, which helps to save the cost and improve the reliability. In this article, a review of the multisampling application in power electronics converters is provided. Starting from the control delay analysis in single/double-sampling control, the modeling, implementation, and related control strategies are given when using multisampling pulsewidth modulation. Then, based on the multisampled data, the applications in condition monitoring and parameter estimation are discussed. Finally, perspectives on challenges and future trends are discussed.

Index Terms—Condition monitoring, multisampling control strategies, multisampling pulsewidth modulation (PWM), parameter estimation, practical implementation.

I. INTRODUCTION

NOWADAYS, digital control is the most commonly used technology in power electronic converters due to its flexibility, adaptability, and insensitivity [1]. Nevertheless, for the regular single/double-sampling control, a control delay always exists in the control loop. Moreover, the control delay will affect the control bandwidth, dynamic performance, and stability of digital controllers, especially in high-power converters with a low switching frequency [2]. Therefore, several control delay compensation methods are proposed, which are mainly divided into two categories. The first is the digital-filter-based delay compensation, such as high-pass filter, Smith predictor, and

linear predictor, but the compensation effect in high-frequency range is limited and the high-frequency noise may even be amplified [3], [4]. The second is to shift the sampling instant or the update instant of the pulsewidth modulation (PWM), and the control delay can be reduced physically [5]–[7]. Specifically, shifting the sampling instant can minimize the computation delay but will introduce the aliased low-order harmonics. In addition, the output duty cycle is limited by the code processing time when shifting the update instant. To summarize the prior art, the control delay still cannot be reduced to one-quarter of the switching period, which is a critical stability boundary according to the passivity-based theory [8].

With the gradually decreasing cost of high-performance microprocessors, multisampling control is a potential candidate to overcome the bandwidth limits, where the state variable is sampled and the duty cycle is updated multiple times within one switching period [9], [10]. Consequently, multisampling control delay is inversely proportional to the sampling rate, which can make it close to the analog control if the sampling rate is high enough [11]. Therefore, multisampling has been widely used to improve the control bandwidth of power electronic converters, including dc–ac converters, dc–dc converters, and motor drives [12].

Besides the average value, the switching ripple is introduced in the control loop when using multisampling, which is the main difference compared with the single/double sampling [13]. Based on the voltage-second balance principle, the multisampling PWM is equivalent to a double-sampling PWM with the sampling instant and the update instant shift. Therefore, the equivalent Nyquist frequency is switching frequency, and the low-order aliased harmonics will appear in the output voltage/current [14], [15]. In order to suppress the aliasing, various repetitive filters (RFs) are proposed in dc–dc and dc–ac converters, where the introduced phase lag is the main optimization goal [13]–[16]. Another switching ripple suppression method is to change the sampling process or the carrier, but the feasibility should further be investigated [17]–[20]. For the multilevel converter, there will be no sampled switching ripple if using an optimum sampling rate. This is because the apparent switching frequency is higher than the preset switching frequency [21]–[23]. In addition, the multisampling can help to achieve a more accurate digital derivative and faster large-signal response [24], [25].

However, there are a set of nonlinearities that need to be considered when employing the multisampling PWM. The first is the multiswitching within one switching period, which will cause higher switching loss compared with the regular PWM

Manuscript received October 13, 2021; revised January 6, 2022 and March 10, 2022; accepted April 10, 2022. Date of publication April 26, 2022; date of current version May 23, 2022. This work was supported in part by the China Scholarships Council's Program and in part by the Department of AAU Energy, Aalborg University, as a part of the Villum Investigator Program funded by the Villum Foundation, through Reliable Power Electronics-Based Power System (REPEPS) Project. Recommended for publication by Associate Editor B. McGrath. (*Corresponding author: Frede Blaabjerg.*)

Shan He, Dao Zhou, Xiongfei Wang, and Frede Blaabjerg are with the AAU Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: she@energy.aau.dk; zda@energy.aau.dk; xwa@energy.aau.dk; fbl@energy.aau.dk).

Zhaoyang Zhao is with the Institute of Smart City and Intelligent Transportation, Southwest Jiaotong University, Chengdu 610031, China (e-mail: zhaoyang.zhao@swjtu.edu.cn).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2022.3169662>.

Digital Object Identifier 10.1109/TPEL.2022.3169662

[26], [27]. Second, the modulation signal may intersect with the carrier vertically, where the small-signal modulation gain is reduced and the stability margin is jeopardized [28], [29]. Third, when the modulation signal and the carrier are in-phase operations, there will be an “increased gain” zone in the modulator transcharacteristic [30]. Fourth, limit cycle oscillations may happen if the PWM clock frequency and the sampling rate are not selected properly [25], [31]. Aiming for the above issues, some related solutions are discussed in this article.

Apart from the reduced control delay and the improved stability from the multisampling control, some new state variables and parameters can be estimated based on the multisampled voltage/current data. The main principle is to utilize the sampled switching ripple instead of the suppression. First, for a three-phase two-level inverter, the current slope can be estimated during the zero/active voltage vectors. Then the estimated current slope can be used to estimate the motor speed [32], the motor inductance [33], the grid voltage [34], etc. Moreover, the estimated current slope can also be used to diagnose the converter fault [35], compensate for the dead time [36], and reduce the magnitude of the high-frequency injected voltage signal [37]. In order to improve the dc-link reliability, the dc-link parameters can be estimated by multisampling the dc-link voltage/current [38]. In addition, the grid impedance can be estimated by multisampling the voltage/current at the point of common coupling (PCC) [39], [40], [95].

The subsequent content is organized as follows. The control delay analysis of the single/double/multisampling PWM is presented in Section II. The aliasing suppression, the control of multicell converters, the multisampled digital controllers, and the practical implementation are discussed in Section III. This is followed by the condition monitoring and the parameter estimation in Section IV. The challenges and future trends are outlined in Section V. Finally, Section VI concludes this article.

II. CONTROL DELAY ANALYSIS OF SINGLE/DOUBLE-SAMPLING PWM AND MULTISAMPLING PWM

Control delay plays an important role in the digital control of power electronic converters, which affects the system stability and the control bandwidth. Considering the current control of a three-phase grid-connected inverter, as shown in Fig. 1(a), where $U_{ga}-U_{gc}$ are the grid voltages, $U_{pcca}-U_{pccc}$ are the PCC voltage, i_{inv} is the inverter-side current, L_f is the filter inductance, and L_g and C_g are the grid impedances, respectively. The dc-link voltage is controlled to generate i_{invd}^* , and the PCC voltage is measured to obtain the grid phase angle through a phase-locked loop (PLL). Fig. 1(b) illustrates the block diagram of the used dq -frame current control loop and $G_i(s)$ is the proportional–integral (PI) current controller. By substituting $s \rightarrow s+j\omega_1$, the plant model $G_p(s)$ and the control delay $G_d(s)$ (the computation delay and the PWM delay) in the dq -frame are given in (2) and (3), respectively, where ω_1 is the grid angle frequency [41].

$$G_i(s) = K_p + \frac{K_i}{s} \quad (1)$$

$$G_p(s) = \frac{1}{(s + j\omega_1)L_f} \quad (2)$$

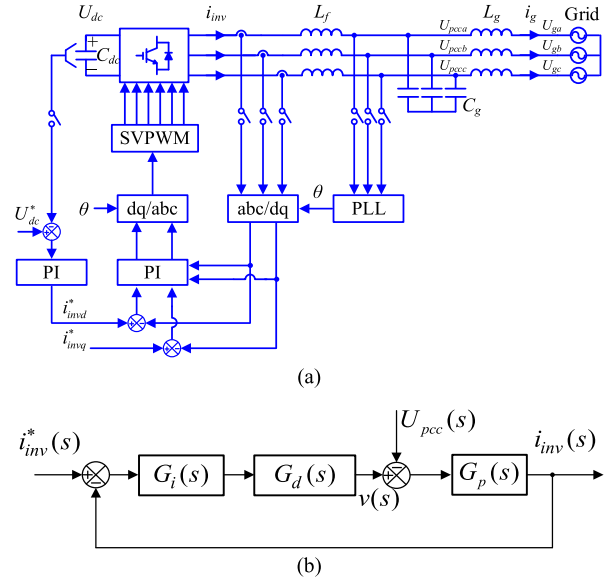


Fig. 1. Single current loop control of a three-phase grid-connected inverter. (a) System diagram. (b) Current control model.

$$G_d(s) = e^{-(s+j\omega_1)T_d} \quad (3)$$

Based on Fig. 1(b), the inverter-side current is

$$i_{inv}(s) = G_{cl}(s)i_{inv}^*(s) - Y_o(s)U_{pcc}(s) \quad (4)$$

$$G_{cl}(s) = \frac{G_i(s)G_d(s)G_p(s)}{1 + G_i(s)G_d(s)G_p(s)} \quad (5)$$

$$Y_o(s) = \frac{G_p(s)}{1 + G_i(s)G_d(s)G_p(s)} \quad (6)$$

where $G_{cl}(s)$ is the current control closed-loop transfer function and $Y_o(s)$ is the output admittance. Based on the passivity theory [8], the terminal response of a grid-connected inverter can be stabilized if the following two constraints are satisfied. First, the closed-loop transfer function $G_{cl}(s)$ should be stable. Second, the phase of $Y_o(s)$ should be within $[-90^\circ, 90^\circ]$ or the real part of $Y_o(j\omega)$ should be nonnegative [41] at all frequencies. Therefore, a positive real part of the converter admittance represents a dissipative behavior, whereas a negative resistance implies amplification of any oscillation at the respective frequency [50]. A network, consisting of resistive, inductive, and capacitive elements, results in passive $Y_{eq}(s)$. The passivity of both $Y_o(s)$ and $Y_{eq}(s)$ provides a sufficient condition for the stable operation of the closed-loop current controller [96]. Note that the pure passivity is impossible to obtain, and the upper boundary of the dissipative region is set to the Nyquist frequency [97].

In terms of the first constraint, the maximum bandwidth r_b under a given phase margin is [42].

$$r_b = \frac{\omega_c}{\omega_{sw}} = \frac{0.5\pi - \varphi_m}{T_d\omega_{sw}} = \frac{0.5\pi - \varphi_m}{2\pi h} \quad (7)$$

The control delay is expressed as $T_d = hT_{sw}$, where T_{sw} is the switching period. φ_m is the phase margin, ω_c is the crossover angle frequency, and ω_{sw} is the switching angle frequency. For

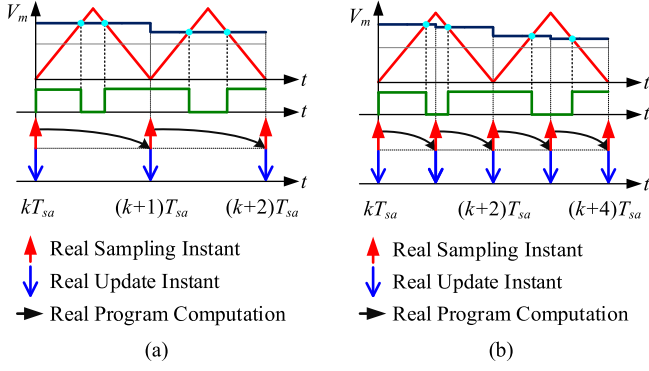


Fig. 2. Conventional digital PWM with the same sampling instant and update instant. (a) Single-update PWM with one-step computation delay. (b) Double-update PWM with one-step computation delay.

the conventional single-sampling PWM ($h = 1.5$) and double-sampling PWM ($h = 0.75$), based on (7), the bandwidth can be set to 0.08 and 0.16 when φ_m is set to 0.25π [43]. Hence, the inner stability in (5) can be easily secured.

Since the control delay mainly affects the passivity in the high-frequency range, the I current controller and the coupled term $j\omega_1 L_f$ can be neglected. By substituting “ $s = j\omega$ ” into (6), $\text{Re}\{Y_o(j\omega)\}$ can be simplified as (8). It can be seen that the sign of $\text{Re}\{Y_o(j\omega)\}$ is determined by the numerator, and the dissipative region (i.e., the frequency range when $\text{Re}\{Y_o(j\omega)\} \geq 0$ below Nyquist frequency) is given in (9) where $f_{\text{dissipative}}$ is the dissipative frequency. Hence, the dissipative region can be lifted up to the switching frequency only if the control delay T_d is $0.25T_{\text{sw}}$. To illustrate the advantage of the multisampling PWM in the control delay reduction, the regular single/double-sampling PWM and their variants are reviewed.

$$\begin{aligned} & \text{Re}\{Y_o(j\omega)\} \\ &= \text{Re}\left\{\frac{1}{j(\omega+\omega_1)L_f + K_p e^{-j(\omega+\omega_1)T_d} + \frac{K_i}{j\omega} e^{-j(\omega+\omega_1)T_d}}\right\} \\ &\approx \text{Re}\left\{\frac{1}{j\omega L_f + K_p e^{-j\omega T_d}}\right\} \\ &\approx \text{Re}\left\{\frac{K_p \cos(\omega T_d)}{(K_p \cos(\omega T_d))^2 + (\omega L_f - K_p \sin(\omega T_d))^2}\right\} \end{aligned} \quad (8)$$

$$f_{\text{dissipative}} \in \left(0, \frac{1}{4T_d}\right). \quad (9)$$

A. Control Delay Using Single/Double-Sampling PWM

1) *Without Sampling Instant and Update Instant Shift*: The timing diagram of the single-sampling single-update (SSSU) PWM is shown in Fig. 2(a); the state variables are sampled in the valley of the carrier, and the modulation signal is updated after one switching period. Since the computation delay is T_{sw} and the PWM delay is $0.5T_{\text{sw}}$, the total control delay is given in (10), where T_{sw} and T_{sa} are the switching period and the sampling period, respectively [44], [45]. Substituting (10) into (9), the dissipative region for SSSU PWM is given in (11).

$$T_{d_{\text{SSSU}}} = \underbrace{T_{\text{sw}}}_{\text{computation delay}} + \underbrace{0.5T_{\text{sw}}}_{\text{PWM delay}} = 1.5T_{\text{sw}} \quad (10)$$

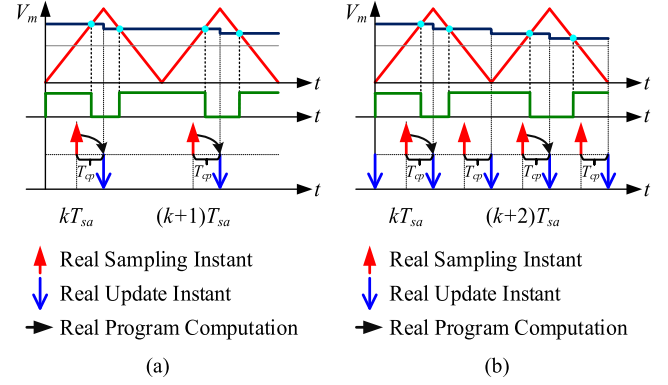


Fig. 3. Conventional digital PWM with the sampling instant shift. (a) Single-update PWM with the sampling instant shift. (b) Double-update PWM with the sampling instant shift.

$$f_{\text{dissipative_SSSU}} = \left(0, \frac{1}{6}f_{\text{sw}}\right). \quad (11)$$

Another conventional digital PWM method is double-sampling double-update (DSDU) PWM [see Fig. 2(b)], and the sampling instant and the update instant are located at the peak and the valley of the carrier, respectively. The control delay and the dissipative region are given in (12) and (13). Compared with the SSSU PWM, the DSDU PWM can effectively reduce the control delay and improve stability. In addition, both the PWM methods have the same sampling instant and the update instant, which is convenient for the practical implementation, and the switching noise is not introduced.

$$T_{d_{\text{DSDU}}} = \underbrace{0.5T_{\text{sw}}}_{\text{computation delay}} + \underbrace{0.25T_{\text{sw}}}_{\text{PWM delay}} = 0.75T_{\text{sw}} \quad (12)$$

$$f_{\text{dissipative_DSDU}} = \left(0, \frac{1}{3}f_{\text{sw}}\right). \quad (13)$$

2) *With Sampling Instant Shift*: The SSSU PWM and the DSDU PWM control delay can be smaller by shifting the sampling instant, which can be defined as SSSU_SIS and DSDU_SIS (see Fig. 3) [46]. Therein, T_{cp} is the practical code implementation time that is set to mT_{sw} , the control delay, and the dissipative region for the SSSU_SIS PWM and DSDU_SIS PWM are given as follows.

$$T_{d_{\text{SSSU_SIS}}} = \underbrace{T_{cp}}_{\text{computation delay}} + \underbrace{0.5T_{\text{sw}}}_{\text{PWM delay}} = (m + 0.5)T_{\text{sw}} \quad (14)$$

$$f_{\text{dissipative_SSSU_SIS}} = \left(0, \frac{1}{4m + 2}f_{\text{sw}}\right) \quad (15)$$

$$T_{d_{\text{DSDU_SIS}}} = \underbrace{T_{cp}}_{\text{computation delay}} + \underbrace{0.25T_{\text{sw}}}_{\text{PWM delay}} = (m + 0.25)T_{\text{sw}} \quad (16)$$

$$f_{\text{dissipative_DSDU_SIS}} = \left(0, \frac{1}{4m + 1}f_{\text{sw}}\right). \quad (17)$$

Note that the SSSU_SIS PWM and the DSDU_SIS PWM depend on the code implementation time T_{cp} . If m is small

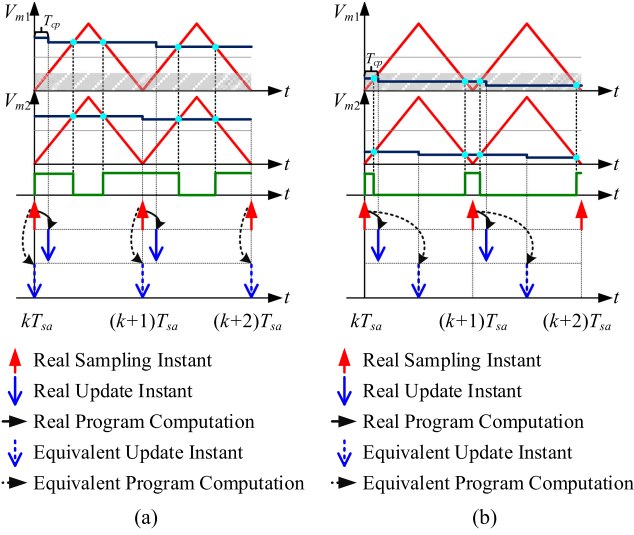


Fig. 4. Single-valley-sampling digital PWM with the update instant shift. (a) Without the duty cycle limitation. (b) With the duty cycle limitation.

enough, the critical frequency for the SSSU_SIS PWM and the DSDU_SIS PWM will be close to $0.5f_{sw}$ and f_{sw} , respectively. However, there is a tradeoff between the control delay reduction and the aliasing suppression because the nonaverage value is sampled and the low-order aliased harmonics will be introduced in the grid-side current [5], [47], [48]. When m is set to 0.25, the aliased harmonics are minimized, and the dissipative region for the DSDU_SIS is in the interval of $(0, \frac{1}{2}f_{sw})$. In addition, when m is set to 0.5 for the SSSU_SIS PWM, the computation delay is reduced from T_{sw} to $0.5T_{sw}$. As a result, the dissipative region is in the interval of $(0, \frac{1}{4}f_{sw})$ and no switching noise is introduced.

3) *With Update Instant Shift*: In addition to shifting the sampling instant, shifting the update instant is an alternative option to reduce the control delay [49]. As shown in Fig. 4(a), the sampling instant is located at the valley of the carrier, and the duty cycle is updated immediately when the calculation is finished. Based on the voltage-second balance principle, the equivalent update instant is located at the valley of the carrier. Hence, the computation delay is zero and only the PWM delay is left. However, when the duty cycle is close to zero, the updated duty cycle cannot produce an effective voltage pulse. It can be seen from Fig. 4(b) that the equivalent update instant is located at the peak of the carrier, and the computation delay changes from zero to $0.5T_{sw}$.

According to the property of the similar triangles, the critical duty cycle considering the code implementation time is given as

$$d_{cri} = \frac{2T_{cp}}{T_{sw}}. \quad (18)$$

The control delay and the dissipative region for single-valley sampling PWM with the update instant shift (SVS UIS) are given in (19) and (20). The control delay for the SVS UIS PWM is a piecewise function, which jeopardizes the system stability when the duty cycle is smaller than the critical duty cycle. The solution can be reducing the code implementation time, improving the dc-link voltage and limiting the minimum output duty cycle, which increases the overall cost and constraints the

application range.

$$\begin{cases} T_{d_SVS_UIS} = 0 & + 0.5T_{sw} = 0.5T_{sw}d \geq d_{cri} \\ \text{computation delay} & \text{PWM delay} \\ T_{d_SVS_UIS} = 0.5T_{sw} & + 0.5T_{sw} = T_{sw}d < d_{cri} \\ \text{computation delay} & \text{PWM delay} \end{cases} \quad (19)$$

$$\begin{cases} f_{dissipative_SVS_UIS} = (0, \frac{1}{2}f_{sw}) & d \geq d_{cri} \\ f_{dissipative_SVS_UIS} = (0, \frac{1}{4}f_{sw}) & d < d_{cri} \end{cases} \quad (20)$$

Similarly, when using the single-peak-sampling with the update instant, considering the code implementation time is given in (21). When the duty cycle is larger than the critical duty cycle, the control delay increases twice and the dissipative region shrinks a half, as given in (22) and (23). For both the SVS UIS PWM and the SPS UIS PWM, no switching noise is introduced.

$$d_{cri} = 1 - \frac{2T_{cp}}{T_{sw}} \quad (21)$$

$$\begin{cases} T_{d_SPS_UIS} = 0 & + 0.5T_{sw} = 0.5T_{sw}d \leq d_{cri} \\ \text{computation delay} & \text{PWM delay} \\ T_{d_SPS_UIS} = 0.5T_{sw} & + 0.5T_{sw} = T_{sw}d > d_{cri} \\ \text{computation delay} & \text{PWM delay} \end{cases} \quad (22)$$

$$\begin{cases} f_{dissipative_SPS_UIS} = (0, \frac{1}{2}f_{sw}) & d \leq d_{cri} \\ f_{dissipative_SPS_UIS} = (0, \frac{1}{4}f_{sw}) & d > d_{cri} \end{cases} \quad (23)$$

Combining the PWM methods in Figs. 4(a) and 5(a), the duty cycle limitation can be removed by switching the sampling point [50]. As shown in Fig. 6, the sampling instant is located at the valley of the carrier when the modulation signal is in the positive half cycle, while it is shifted to the peak of the carrier when the modulation signal is in the negative half cycle. Consequently, the control delay and the dissipative region for the single-sampling without the duty cycle limitation (SS_WDCL) are given in (24) and (25). Compared with the DSDU_SIS in [5], the SS_WDCL has the same control delay and no aliased low-order harmonics exist. Based on the area equivalence and single-sampling, the control delay can also be reduced to $0.5T_{sw}$ but the output duty cycle is still limited [51], [52].

$$T_{d_SS_WDRL} = 0 & + 0.5T_{sw} = 0.5T_{sw} \quad (24) \\ \text{computation delay} & \text{PWM delay}$$

$$f_{dissipative_SS_WDRL} = \left(0, \frac{1}{2}f_{sw}\right). \quad (25)$$

Shifting the update instant can be used in the DSDU PWM as well [6], [7]. As shown in Fig. 7(a), when the duty cycle is not limited, the equivalent update instant is located at the same position as the sampling point. As a result, the computation delay is zero and only the PWM delay is left. On the other hand, when the duty cycle is limited [see Fig. 7(b)], it changes back to SPS UIS in the positive half cycle and to SVS UIS in the negative half cycle. The control delay and the dissipative region for the double-sampling PWM with the update instant shift (DS UIS) are given in (26) shown at the bottom of this page, and (27).

$$\begin{cases} f_{dissipative_DS_UIS} = (0, f_{sw}) & \frac{2T_{cp}}{T_{sw}} \leq d \leq 1 - \frac{2T_{cp}}{T_{sw}} \\ f_{dissipative_DS_UIS} = (0, \frac{1}{2}f_{sw}) & \text{others} \end{cases} \quad (27)$$

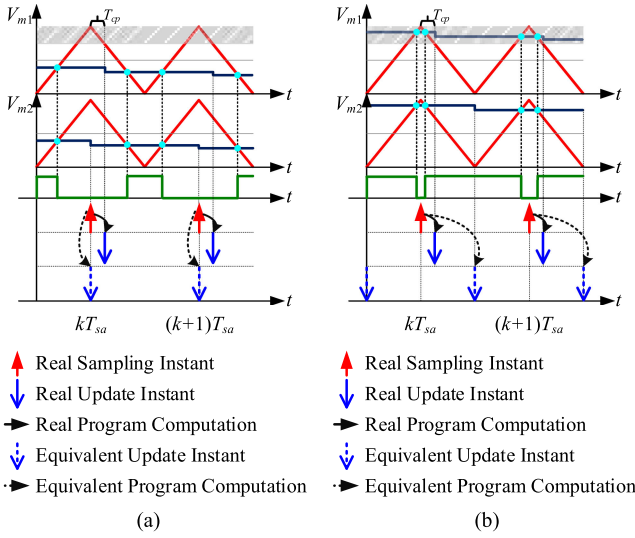


Fig. 5. Single-peak-sampling digital PWM with the update instant shift. (a) Without the duty cycle limitation. (b) With the duty cycle limitation.

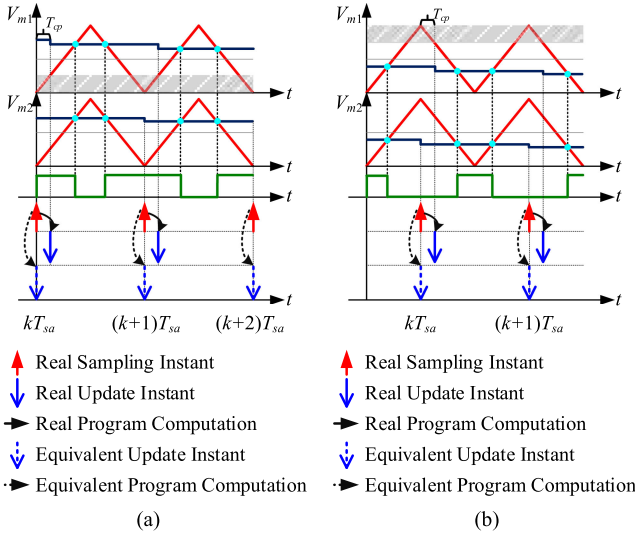


Fig. 6. Single-sampling digital PWM without duty cycle limitation. (a) Positive half cycle. (b) Negative half cycle.

In terms of the aliasing and the control delay, the DS UIS PWM is the best choice among conventional single/double-sampling methods when the computation time is short enough. Based on (26), the allowed output duty cycle can be up to 0.98 only if T_{cp} is $0.005T_{sw}$, especially if T_{cp} is equal to $0.25T_{sw}$, the DS UIS is the same as the SS WDCL.

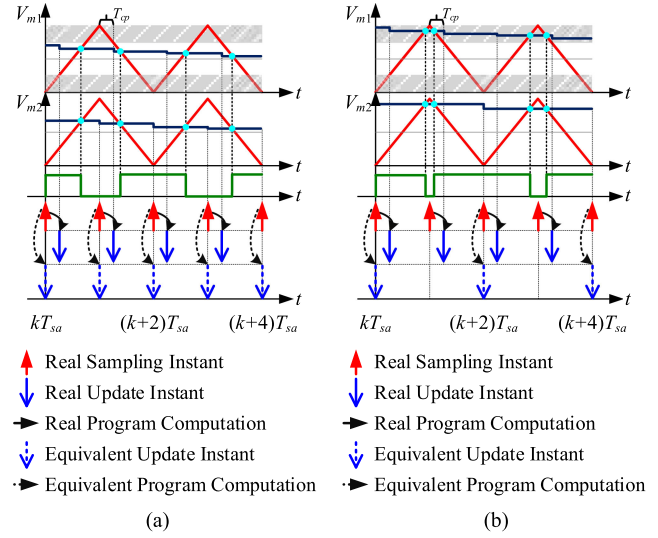


Fig. 7. Double-sampling digital PWM with the update instant shift. (a) Without the duty cycle limitation. (b) With the duty cycle limitation.

B. Control Delay Using Multisampling PWM

1) *General Multisampling PWM*: The multisampling multiupdate (MSMU) PWM is a potential candidate to reduce the control delay; and the state variable is sampled, and the duty cycle is updated multiple times within a switching period. The control delay is inversely proportional to the sampling rate N [11], [53] and it is given as

$$T_{d_MSMU} = \frac{1.5T_{sw}}{N}. \quad (28)$$

Taking four-sampling four-update PWM as an example, as shown in Fig. 8, not every duty cycle will intersect with the carrier and produce an effective pulse pattern.

In the positive half cycle [see Fig. 8(a)], D_2 and D_3 are the effective duty cycle. Based on the voltage-second balance principle, the duration time of the effective duty cycle can be extended to half of one switching period. As a result, the four-sampling PWM can be transformed into a DSDU PWM with the sampling instant shift and the update instant shift. The equivalent computation delay for D_2 is zero, and the equivalent update instant is the same as the sampling instant [14]. Besides, there is a $0.25T_{sw}$ equivalent computational delay for the duty cycle D_3 . The average computational delay in one switching period is $(0.25+0)/2 = 0.125T_{sw}$. Considering the double-sampled PWM delay of $0.25T_{sw}$, the total control delay is $0.375T_{sw}$, which is consistent with the multisampling delay $1.5T_{sw}/4$. Similarly, the effective duty cycles in the negative half cycle are D_1 and D_4 , as shown in Fig. 8(b). The equivalent computation delay for D_1 and D_4 is $0.25T_{sw}$ and zero, respectively, and the total control delay is equal to $1.5T_{sw}/4$.

$$\begin{cases} T_{d_DS_UIS} = 0 & + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = 0.25T_{sw} & \frac{2T_{cp}}{T_{sw}} \leq d \leq 1 - \frac{2T_{cp}}{T_{sw}} \\ T_{d_DS_UIS} = 0 & + 0.5T_{sw} = 0.5T_{sw} & \text{others} \end{cases} \quad (26)$$

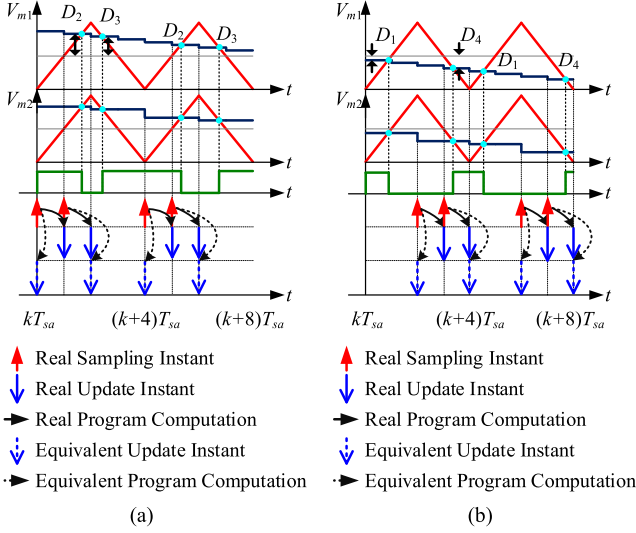


Fig. 8. General multisampling digital PWM with the same sampling instant and update instant. (a) Positive half cycle. (b) Negative half cycle.

Similarly, when the sampling rate is higher, e.g., $N = 8$, the eight-sampling PWM can be transformed into a DSDU PWM with the sampling instant shift and the update instant shift [14]. The core principle for the MSMU PWM in reducing control delay is the smaller computation delay, and the PWM delay is always equal to $0.25T_{sw}$. Therefore, a more specific control delay expression for the MSMU PWM is

$$T_{d_MSMU} = \underbrace{\frac{6-N}{4N}T_{sw}}_{\text{computation delay}} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = \frac{1.5T_{sw}}{N}. \quad (29)$$

It can be seen from (29) that when the sampling rate N is larger than six, the computation delay will be negative, which leads to a phase-leading. For example, the computation delay is $-0.0625T_{sw}$ when the sampling rate is eight and a detailed analysis can be found in [14]. Substituting (29) into (9), the dissipative region for the MSMU PWM is given in (30). Moreover, the dissipative region can be extended to switching frequency when the sampling rate N is equal to or larger than six.

$$f_{\text{dissipative_MSMU}} = \left(0, \frac{N}{6}f_{sw}\right). \quad (30)$$

In addition, the multisampling single-update (MSSU) PWM and the multisampling double-update (MSDU) PWM are also a kind of alternatives, and the multiple intersections between the modulation signal and the carrier can be avoided [54]–[56]. As a result, the control delay is the same with the SSSU_SIS and the DSDU_SIS. However, the switching noise will be introduced when using the multisampling as the average value can only be sampled at the peak/valley point of the carrier for a two-level inverter or a dc–dc converter. One typical method is to use an antialiasing filter, but the extra delay will be introduced, which will be discussed in Section III-A.

2) *Multisampling PWM for Multilevel Converters*: Multilevel converter with phase-shifted PWM modulation is a good application, and no switching noise is introduced if selecting the multisampling rate properly. For a single-phase H-bridge

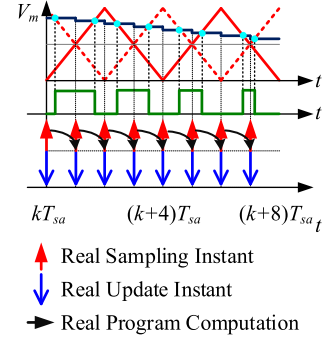


Fig. 9. Multilevel converter-based multisampling digital PWM with the same sampling instant and update instant.

inverter, the carriers are interleaved with 180° , respectively. As shown in Fig. 9, the apparent switching frequency is twice larger than the preset switching frequency. Hence, it is natural to sample four times within one switching period, including the peak/valley points and the intersection points of the carriers [21]. In particular, four-sampling four-update control for a single-phase H-bridge inverter can also be regarded as a double-sampling control with a double preset switching frequency. Hence, the control delay is given in (29), where T_{sw_ap} is the apparent switching period.

$$\begin{aligned} T_{d_4S4U} &= \frac{T_{sw}}{4} + \frac{T_{sw}}{8} = \frac{1.5T_{sw}}{4} \\ &= \frac{T_{sw_ap}}{2} + \frac{T_{sw_ap}}{4} = \frac{1.5T_{sw_ap}}{2}. \end{aligned} \quad (31)$$

More generally, for a cascaded H-bridge (CHB) inverter, the apparent switching frequency is $2Mf_{sw}$, where M is the number of cascaded cells. The optimum multisampling rate is $4M$ without introducing switching noise, and the control delay is given as follows:

$$\begin{aligned} T_{d_MSMU_CHB} &= \frac{T_{sw}}{4M} + \frac{T_{sw}}{8M} = \frac{1.5T_{sw}}{4M} \\ &= \frac{T_{sw_ap}}{2} + \frac{T_{sw_ap}}{4} = \frac{1.5T_{sw_ap}}{2}. \end{aligned} \quad (32)$$

Recalling (29), multisampling control of the CHB inverter and the HB inverter can reduce the computation delay and the PWM delay at the same time instead of reducing the computation delay only [22], [57]. Again, if seen from the apparent switching period perspective, the control delay is the same with DSDU PWM. Substituting (32) into (9), the dissipative region in terms of the cascaded cells is given in (33). The region below the switching frequency can be made dissipative when the number of cascaded cells is equal to or larger than two, but the dissipative region cannot be extended based on the apparent switching frequency f_{sw_ap} .

$$f_{\text{dissipative_MSMU_CHB}} = \left(0, \frac{2M}{3}f_{sw}\right)$$

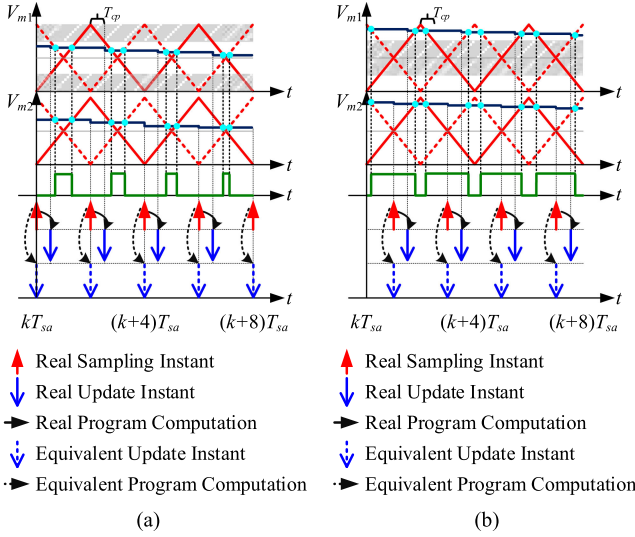


Fig. 10. Multisampling digital PWM with the update instant shift. (a) Sampling at the peak/valley points of the carriers. (b) Sampling at the intersection points of the carriers.

$$= \left(0, \frac{1}{3}f_{sw_ap}\right). \quad (33)$$

Similar to the DS UIS PWM in Fig. 7, the update instant can also be shifted for the multisampling PWM to further reduce the control delay [58]. For a single-phase HB inverter, the average current can be sampled at the peak/valley points and the intersection points of the phase-shifted carriers, and two control modes are switched based on the amplitude of the duty cycle. As shown in Fig. 10(a), when the duty cycle is in the interval of $\left[\frac{2T_{cp}}{T_{sw}}, 1 - \frac{2T_{cp}}{T_{sw}}\right]$, the sampling point is located at the peak/valley points of the carriers, and the duty cycle is updated immediately after the calculation is finished. Similarly, when the duty cycle is not in the interval, the sampling point is switched to the intersection points of the carriers [see Fig. 10(b)]. As a result, the computation delay is zero and only the PWM delay is left. The control delay for the multisampling PWM with the update instant shift (MS UIS) is $T_{sw}/4$, and no switching noise is introduced.

However, the computation time for the MS UIS should be lower than $T_{sw}/8$ according to the geometric relationship in Fig. 10, which presents a higher demand for the microprocessors compared with the four-sampling four-update control. Generally, for a CHB inverter with M cells, there will be $2M$ control modes [59]. The control delay and the dissipative region are given in (34) and (35). Similarly, seen from an apparent switching period perspective, the control delay for MS UIS for an HB inverter and MS UIS for a CHB inverter is the same with SS WDCL PWM. Hence, the sampling rate selection for multilevel converters should be further researched.

$$\begin{aligned} T_{d_MS_UIS_CHB} &= \underset{\text{computation delay}}{0} + \underset{\text{PWM delay}}{\frac{T_{sw}}{4M}} = \frac{T_{sw}}{4M} \\ &= \underset{\text{computation delay}}{0} + \underset{\text{PWM delay}}{\frac{T_{sw_ap}}{2}} = \frac{T_{sw_ap}}{2} \end{aligned} \quad (34)$$

$$\begin{aligned} f_{\text{dissipative_MS_UIS_CHB}} &= (0, Mf_{sw}) \\ &= \left(0, \frac{1}{2}f_{sw_ap}\right). \end{aligned} \quad (35)$$

C. Comparison

To evaluate the performance of the prior art, several indexes are used, i.e., control delay, dissipative region, aliasing, duty cycle limitation, and maximum allowed computation time. As given in Table I, SS WDCL PWM is the best one among single-sampling PWM methods. Specifically, by combining the update instant shift and the sampling instant shift, the control delay can be reduced to $0.5T_{sw}$. Moreover, not only the aliasing and the duty cycle limitation are removed, but also the maximum allowed computation time is acceptable ($T_{cp} = 0.25T_{sw}$).

When using double-sampling, as given in Table II, the control delay for the DSDU SIS PWM ($m = 0.25$) can also be reduced to $0.5T_{sw}$, but the extra aliasing is introduced compared with the SS WDCL PWM. By shifting the update instant for double-sampling PWM, the control delay can further be reduced to $0.25T_{sw}$, which is a big advantage compared with SS WDCL PWM. However, the duty cycle is limited; otherwise, the computation time is small enough to be ignored.

Considering the multisampling PWM in Table III, an antialiasing filter is required to remove the sampled switching harmonics, i.e., MSMU PWM with an antialiasing filter. Although an extra control delay $0.25T_{sw}$ is introduced compared with MSMU PWM, the total control delay is still lower than SS WDCL PWM when the sampling rate is larger than six. Seen from an apparent switching frequency perspective, the control delay for 4S4U for an HB inverter and MSMU for a CHB inverter is the same as the DSDU PWM. Similarly, the control delay for MS UIS for an HB inverter and MS UIS for a CHB inverter is the same with SS WDCL PWM.

To summarize, SS WDCL PWM, DS UIS PWM, and MSMU PWM with an antialiasing filter are possible candidates. Then the selection principle based on the computation time is given as follows.

- 1) If $T_{cp} \leq 0.005T_{sw}$, then choose DS UIS PWM, where $T_d = 0.25T_{sw}$ and $d \in (0.01, 0.99)$.
- 2) If $0.005T_{sw} < T_{cp} < T_{sw}/6$, then choose MSMU with an antialiasing filter, where $0.25T_{sw} < T_d < 0.5T_{sw}$ and $d \in (0, 1)$.
- 3) If $T_{sw}/6 \leq T_{cp} \leq 0.25T_{sw}$, then choose SS WDCL PWM, where $T_d = 0.5T_{sw}$ and $d \in (0, 1)$.

III. MULTISAMPLING CONTROL STRATEGIES AND PRACTICAL IMPLEMENTATION

A. Aliasing Suppression

1) *With Antialiasing Filters:* Over the past decades, linear controllers based on the PWM have been the most popular control methods due to their simpleness in the implementation, the parameter design, and the stability analysis [60]–[62]. Moreover, the multisampling PWM is an extension of the conventional PWM, and the linear controllers can be easily updated using a higher sampling frequency.

When using a multisampled linear controller with the PWM, however, the switching harmonics are introduced, which affects

TABLE I
COMPARISON AMONG VARIOUS SINGLE-SAMPLING PWM

Modulation methods Index	SSSU ^[44-45] (see Fig. 2(a))	SSSU_SIS ^[46-48] (see Fig. 3(a))			SVS UIS ^[49] (see Fig. 4)	SPS UIS ^[49] (see Fig. 5)	SS_WDCL ^[50] (see Fig. 6)
Control delay	$\frac{3}{2}T_{sw}$	$(m + \frac{1}{2})T_{sw}$	$T_{sw} (m = \frac{1}{2})$	$\frac{3}{4}T_{sw} (m = \frac{1}{4})$	$\frac{1}{2}T_{sw}$	$\frac{1}{2}T_{sw}$	$\frac{1}{2}T_{sw}$
Dissipative region	$(0, \frac{1}{6}f_{sw})$	$(0, \frac{1}{4m+2}f_{sw})$	$(0, \frac{1}{4}f_{sw})$	$(0, \frac{1}{3}f_{sw})$	$(0, \frac{1}{2}f_{sw})$	$(0, \frac{1}{2}f_{sw})$	$(0, \frac{1}{2}f_{sw})$
Aliasing	No	Large when $m \neq \frac{1}{2}$ or $\frac{1}{4}$	No	Small	No	No	No
Duty cycle limitation	No	No	No	No	Yes	Yes	No
Maximum allowed computation time	T_{sw}	mT_{sw}	$\frac{1}{2}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4}T_{sw}$

SSSU: single-sampling single-update; SSSU_SIS: single-sampling single-update with the sampling instant shift; SVS UIS: single-valley sampling with the update instant shift; SPS UIS: single-peak-sampling with the update instant shift; SS_WDCL: single-sampling without the duty cycle limitation.

TABLE II
COMPARISON AMONG VARIOUS DOUBLE-SAMPLING PWM

Modulation methods Index	DSDU ^[44-45] (see Fig. 2(b))	DSDU_SIS ^[5] (see Fig. 3(b))		DS UIS ^[6-7] (see Fig. 7)
Control delay	$\frac{3}{4}T_{sw}$	$(m + \frac{1}{4})T_{sw}$	$\frac{1}{2}T_{sw} (m = \frac{1}{4})$	$\frac{1}{4}T_{sw}$
Dissipative region	$(0, \frac{1}{3}f_{sw})$	$(0, \frac{1}{4m+1}f_{sw})$	$(0, \frac{1}{2}f_{sw})$	$(0, f_{sw})$
Aliasing	No	Large when $m \neq \frac{1}{4}$	Small	No
Duty cycle limitation	No	No	No	Yes
Maximum allowed computation time	$\frac{1}{2}T_{sw}$	mT_{sw}	$\frac{1}{4}T_{sw}$	$\frac{1}{8}T_{sw}$

DSDU: double-sampling double-update; DSDU_SIS: double-sampling double-update with the sampling instant shift; DS UIS: double-sampling with the update instant shift.

TABLE III
COMPARISON AMONG VARIOUS MULTISAMPLING PWM

Modulation methods Index	MSMU ^[11, 53] (see Fig. 8)	MSMU with an anti-aliasing filter ^[14, 34] (see Fig. 12)	MSSU ^[55] (same with Fig. 3(a))	MSDU ^[56] (same with Fig. 3(b))	4S4U for HB inverter ^[21] (see Fig. 9)	MSMU for CHB inverter ^[22] (similar with Fig. 9)	MS UIS for HB inverter ^[58] (see Fig. 10)	MS UIS for CHB inverter ^[59] (similar with Fig. 10)
Control delay	$\frac{1.5}{N}T_{sw}$	$(\frac{1.5}{N} + \frac{1}{4})T_{sw}$	$(\frac{1}{N} + \frac{1}{2})T_{sw}$	$(\frac{1}{N} + \frac{1}{4})T_{sw}$	$\frac{1.5}{4}T_{sw}$ ↓ $\frac{1.5}{2}T_{sw_eq}$	$\frac{1.5}{4M}T_{sw}$ ↓ $\frac{1.5}{2}T_{sw_eq}$	$\frac{1}{4}T_{sw}$ ↓ $\frac{1}{2}T_{sw_eq}$	$\frac{1}{4M}T_{sw}$ ↓ $\frac{1}{2}T_{sw_eq}$
Dissipative region	$(0, \frac{N}{6}f_{sw})$	$(0, \frac{N}{6+N}f_{sw})$	$(0, \frac{N}{4+2N}f_{sw})$	$(0, \frac{N}{4+N}f_{sw})$	$(0, \frac{2}{3}f_{sw})$ ↓ $(0, \frac{1}{3}f_{sw_ap})$	$(0, \frac{2M}{3}f_{sw})$ ↓ $(0, \frac{1}{3}f_{sw_ap})$	$(0, f_{sw})$ ↓ $(0, \frac{1}{2}f_{sw_ap})$	$(0, Mf_{sw})$ ↓ $(0, \frac{1}{2}f_{sw_ap})$
Aliasing	Yes	No	Yes	Yes	No	No	No	No
Duty cycle limitation	No	No	No	No	No	No	No	No
Maximum allowed computation time	$\frac{1}{N}T_{sw}$	$\frac{1}{N}T_{sw}$	$\frac{1}{N}T_{sw}$	$\frac{1}{N}T_{sw}$	$\frac{1}{4}T_{sw}$	$\frac{1}{4M}T_{sw}$	$\frac{1}{8}T_{sw}$	$\frac{1}{8M}T_{sw}$

MSMU: multisampling multiupdate; IRF: improved repetitive filter; MRF: modified repetitive filter; MSSU: multisampling single-update; MSDU: multisampling double-update; HB: H-bridge; CHB: cascaded H-bridge; MS UIS: multisampling with the update instant shift.

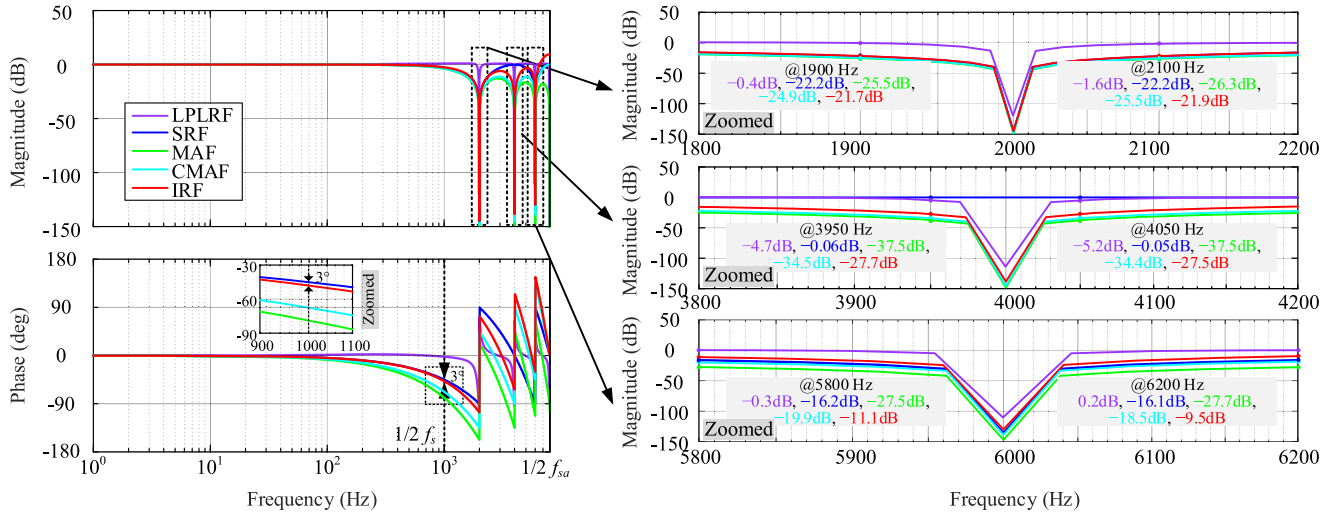


Fig. 11. Bode diagram of the RFs based on eight-sampling (LPLRF: low-phase-lag repetitive filter; SRF: simplified repetitive filter; MAF: moving average filter; CMAF: compromised moving averaging filter; IRF: improved repetitive filter).

the control performance. Specifically, the multisampling PWM is equivalent to a double-sampling PWM with the sampling instant shift and the update instant shift, and the equivalent Nyquist frequency is equal to the switching frequency. According to Fig. 8, the nonaverage value is sampled at least once within one switching period, which causes the aliased low-order harmonics. Besides the four-sampling PWM, the same conclusion can be acquired using a higher sampling rate. For example, eight-sampling PWM analysis can be found in [14], and the aliasing is still severe due to the sampled switching harmonics. The frequency-domain based aliasing analysis method in the DSDU_SIS PWM can be used directly for the MSMU PWM, where the aliased harmonics is regarded as an additional aliasing disturbing source in the control loop [48]. For example, for the current control of LCL -filtered inverters, the aliased disturbance can be added after the multisampled feedback variables, such as the inverter-side current, grid-side current, and filter capacitor voltage. Similarly, the low-order aliasing phenomenon also exists in the multisampled voltage control of dc-dc converters. Hence, using an antialiasing filter to remove the sampled switching harmonics is necessary, which can suppress the aliasing and make the analytical modeling match with the simulation results [14], [15], [63]. In order to remove the sampled high-frequency switching harmonics, various RFs are proposed based on the internal model principle. The most effective RF is the moving average filter (MAF) with a window equal to one switching period [64], as shown in (36).

But the MAF introduces a delay equal to $T_{sw}/2$, thus losing the advantage on the phase boost. Since the sampled switching harmonics for a dc-dc converter are at the integral switching frequency, a low-phase-lag RF (LPLRF) is proposed, which is given in (37) [13]. To reduce the calculation complexity, a simplified RF (SRF) is proposed, as shown in (38) [16]. For a two-level three-phase inverter, the multisampled switching harmonics are at the side switching frequency. As shown in Fig. 11, the LPLRF cannot remove the sampled even-order and odd-order switching harmonics, and the SRF cannot remove the sampled odd-order switching harmonics.

Therefore, a compromised moving average filter (CMAF) is proposed, and the size of the window reduces from one to half of the switching period, as shown in (39). However, there is still a delay from the CMAF compared with the SRF; hence, a linear delay compensation block is inserted after the CMAF, i.e., improved repetitive filter (IRF), as shown in (40) [14]. The IRF can remove the even-order and odd-order switching harmonics but also has a similar phase lag to the SRF. Moreover, when the sampling rate is higher, e.g., $N = 50$, IRF will amplify the sampled high-frequency harmonics [34]. As shown in (41), a modified repetitive filter (MRF) should be used where r is the attenuation factor.

$$\text{MAF}(z) = \frac{1}{N} \sum_{k=0}^{N-1} z^{-k} \quad (36)$$

$$\text{LPLRF}(z) = \frac{(1 + 0.25)(1 - (z^{-N} - \frac{1}{N} \sum_{n=1}^N z^{-n}))}{1 - (z^{-N} - \frac{1}{N} \sum_{n=1}^N z^{-n}) + 0.25} \approx 1 \quad (37)$$

$$\text{SRF}(z) = \frac{1}{2}(1 + z^{-N/2}) \approx z^{-N/4} \quad (38)$$

$$\text{CMAF}(z) = \frac{2}{N}(1 + z^{-2} + z^{-4} + \dots + z^{-(N-2)}) \quad (39)$$

$$\text{IRF}(z) = \frac{2}{N}(1 + z^{-2} + z^{-4} + \dots + z^{-(N-2)}) \times (3\log_2 N - 7 - (3\log_2 N - 8)z^{-1}) \quad (40)$$

$$\text{MRF}(z) = \frac{2}{N}(1 + z^{-2} + z^{-4} + \dots + z^{-(N-2)}) \times \frac{(1 - r^8)(1 - r^2 z^{-2})}{(1 - r^2)(1 - r^8 z^{-8})} \quad (41)$$

On the other hand, the IRF has a similar control delay to the SRF that is equal to one-quarter of the switching period, the total control delay, including the computation delay, PWM delay, and

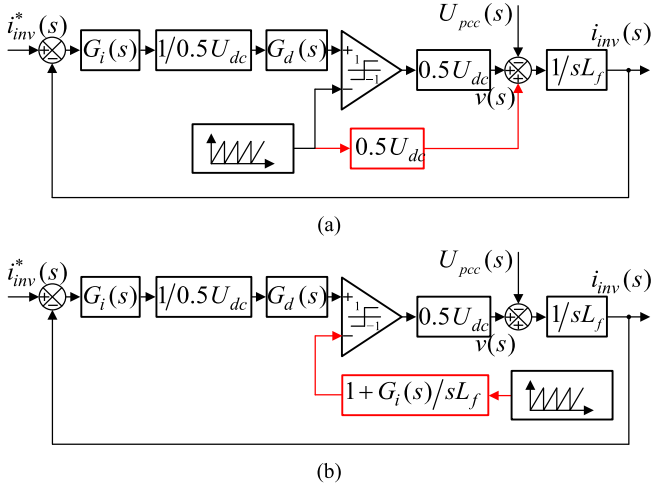


Fig. 12. Single-edge modulator with ripple compensation. (a) Carrier feedforward. (b) Equivalent transformation.

IRF delay, is

$$T_{d_MS_IRF/MRF} = \frac{6 - N}{4N} T_{sw} + \frac{0.25 T_{sw}}{\text{computation delay}} + \frac{0.25 T_{sw}}{\text{IRF/MRF delay}} = \frac{6 + N}{4N} T_{sw}. \quad (42)$$

When the sampling rate N is infinite, the control delay is close to $1/4T_{sw}$ and the dissipative region is

$$f_{\text{dissipative_MS_IRF/MRF}} = \left(0, \frac{N}{6 + N} f_{sw}\right). \quad (43)$$

Consequently, the dissipative region and the loop delay using the multisampling control strongly depend on the inserted digital filter. Therefore, in order to fully take advantage of the multisampling control, how to remove the sampled switching harmonics with less phase lag becomes an important issue.

2) *With a Changed Carrier or Sampling Process*: Based on the single-edge modulator, the multisampled SHs can be compensated through an offline predistorted carrier. As shown in Fig. 12(a), the switching harmonics are produced from the comparison process between the modulation signal and the carrier, which can be compensated through the feedforward of the carrier. Moreover, Fig. 12(a) can be equivalently transformed into Fig. 12(b), where a series combination of $G_i(s)$ and the plant model are inserted after the carrier. As a result, a new carrier can be done offline, which is stored in a lookup table [17], [18]. However, the double-edge modulator is more general, and the compensation strategy for the single-edge modulator cannot be used directly.

By replacing the zero-order hold (ZOH) with the first-order hold (FOH) in the sampling process, the modulation signal is more like a continuous signal using the MSMU PWM. The arbitrary sampling rate can be used with the improved harmonic performance, linearity, and phase delay compared with the ZOH sampler [19], [20]. The transfer functions of the FOH and the

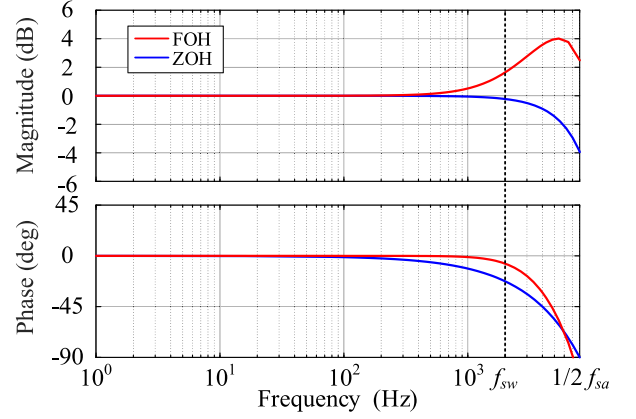


Fig. 13. Bode diagram of the ZOH and the FOH.

ZOH are

$$\text{FOH}(s) = \left(\frac{1 - e^{-sT_{sa}}}{sT_{sa}}\right)^2 (1 + sT_{sa}) \quad (44)$$

$$\text{ZOH}(s) = \frac{1 - e^{-sT_{sa}}}{sT_{sa}}. \quad (45)$$

It can be seen from Fig. 13 that the FOH has a larger amplitude response at high frequency compared with the ZOH, which may affect the small-signal stability and amplify the high-frequency noise. Hence, the analysis and controller design using FOH sampled still need to be further studied.

B. Control of Multicell Converters

In addition, noise-free sampling can be achieved for the multiparallel/series multicell converters with the phase-shifted modulation. For the CHB inverter and modular multilevel converter, the sampling rate can be four times higher than the number of cells, i.e., the sampling point is located at the intersection point and the peak/valley point of the carrier [22], [54], [57], [67]. On the other hand, for a multicell interleaved converter, the sampling rate and the update rate cannot be the same. This is because the average output voltage for every single cell is different, which leads to the circulating current among cells [23]. Taking a two-cell interleaved inverter as an example, the sampling rate can be set to four when sampling the PCC current, as shown in Fig. 14 [68].

If updating four times within one switching period, the average output voltage in the positive half cycle is

$$\begin{cases} i_{\text{inv}1}(k+4) - i_{\text{inv}1}(k) = L_{c1}(d_2 + d_3) \frac{u_{dc}}{2} \\ i_{\text{inv}2}(k+4) - i_{\text{inv}2}(k) = L_{c2}(d_1 + d_4) \frac{u_{dc}}{2} \end{cases} \quad (46)$$

where $i_{\text{inv}1}$ - $i_{\text{inv}2}$, L_{c1} - L_{c2} , d_1 - d_4 , and u_{dc} are single-phase inverter-side currents for the first- and second-cell, the inverter-side inductance for the first- and second-cell, four updated duty cycles within a switching period, and dc-link voltage, respectively. As a result, a low-frequency circulating component appears in the inverter-side currents for every single cell if the nonideal factors, such as filter-inductance variation and dead time effect, are ignored. If updating twice within one switching period, the average output voltage for every single cell is the same, as shown in (47). Hence, the four-sampling double-update

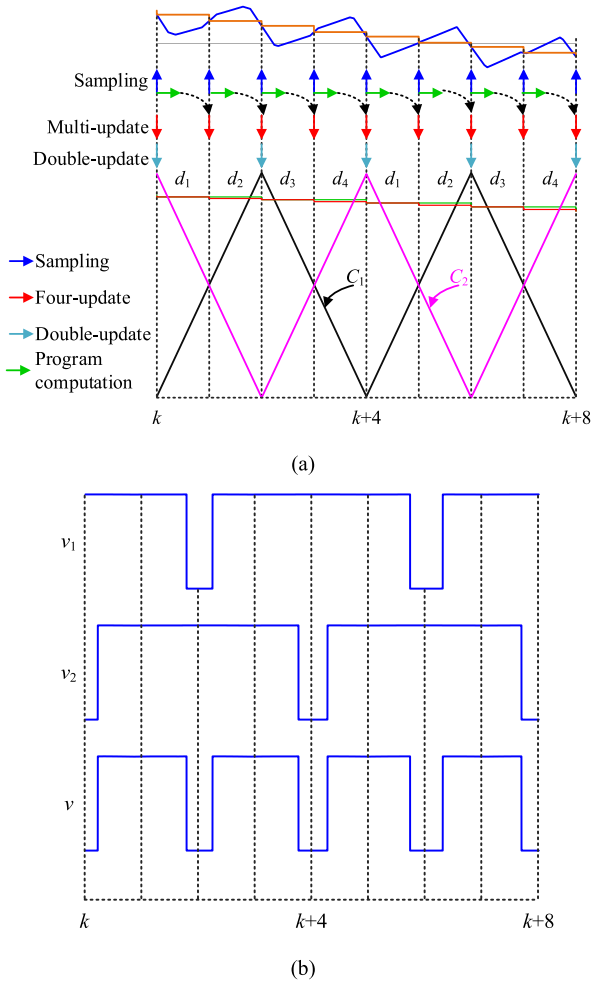


Fig. 14. Multisampling control principle of two-cell interleaved three-phase inverters. (a) Sampling process and modulation. (b) Pulse pattern.

mode is recommended.

$$\begin{cases} i_{inv1}(k+4) - i_{inv1}(k) = Lc_1(d_1 + d_3)\frac{u_{dk}}{2} \\ i_{inv2}(k+4) - i_{inv2}(k) = Lc_2(d_1 + d_3)\frac{u_{dk}}{2} \end{cases} \quad (47)$$

The control delay and dissipative region for the two-cell interleaved inverter are

$$T_{d_MS_interleaved} = \underbrace{0.25T_{sw}}_{\text{computation delay}} + \underbrace{0.25T_{sw}}_{\text{PWM delay}} = 0.5T_{sw} \quad (48)$$

$$f_{dissipative_MS_interleaved} = (0, 0.5f_{sw}). \quad (49)$$

It can be seen from (48) and (49) that the stability is weakened compared with the single-phase H-bridge inverter in (33). Moreover, when the number of interleaved cells improves, the configuration of the sampling rate and the update rate will be more complicated.

C. Multisampled Digital Controller

The digital derivative is often required in the control of power electronic converters, and the first-order and second-order forms are given in (50) and (51) [69]. The bode plot using double-sampling is given in Fig. 15(a). However, compared with the

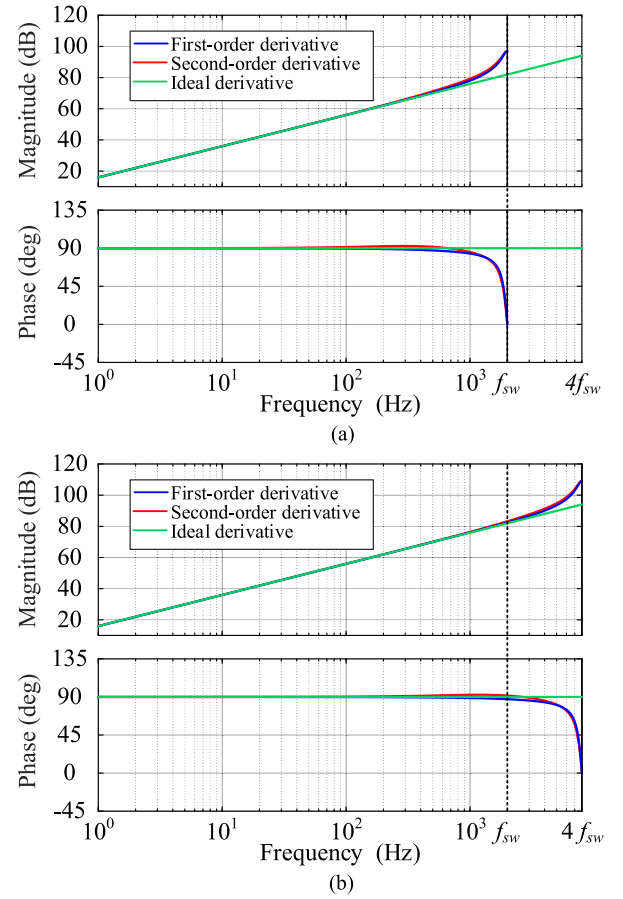


Fig. 15. Comparison between double-sampling derivative and multisampling derivative. (a) Double-sampling derivative. (b) Multisampling derivative.

ideal “ s ” function, there is a large deviation for the amplitude–frequency characteristic and the phase–frequency characteristic close to the switching frequency. Multisampling can effectively reduce the phase lag and make the digital derivative more accurate [24]. For example, when the sampling frequency is eight times higher than the switching frequency, as shown in Fig. 15(b), the multisampling derivative can emulate the characteristic of the ideal derivative accurately below the switching frequency.

$$G_{\text{first-order}}(z) = \frac{1.8}{T_{sa}} \frac{z-1}{z+0.8} \quad (50)$$

$$G_{\text{second-order}}(z) = \frac{3}{T_{sa}} \frac{(2z-1)(z-1)}{3z^2+z-1}. \quad (51)$$

For the PI controller design, there is always a tradeoff between the bandwidth and the overshoot, which weakens the advantage of multisampling PWM [65]. The pseudo-derivative-feedback (PDF) controller can be used in order to suppress the overshoot and improve the dynamic response at the same time [66], as shown in Fig. 16. Specifically, the PDF controller can be transformed into a PI controller, and a low-pass filter is inserted after the reference current. Moreover, the inserted low-pass filter will not affect the system’s stability. It can be seen from Fig. 16(b) that the delay from the low-pass filter is K_p/K_i , and increasing

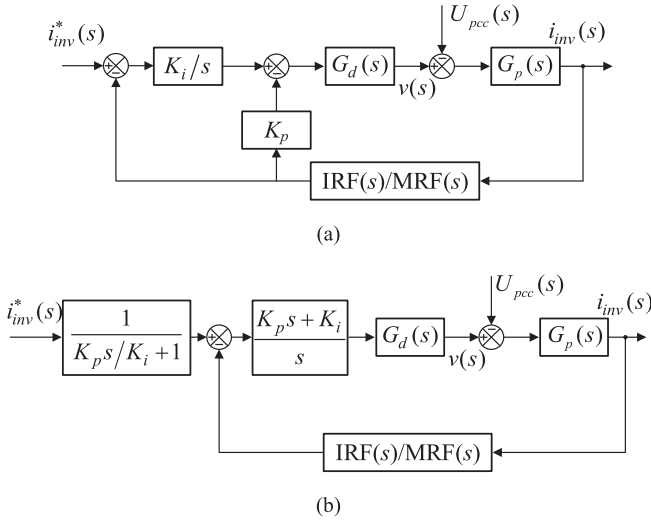


Fig. 16. Relationship between the PI and PDF controller. (a) PDF controller. (b) Equivalent transformation.

K_i can improve the response speed with the same open-loop bandwidth.

In addition, some nonlinear controllers are combined with multisampling to further improve the control performance, such as the hysteresis controller [70], [71], the sliding mode controller [72], and the model predictive controller [73], [74]. The performance comparison among the multisampled PI controller, the multisampled deadbeat controller, and the multisampled hysteresis controller is provided in [75]. When setting the same control bandwidth, the multisampled hysteresis controller has a minor control delay, where a higher sampling frequency is required. The analytical model is hard to be derived and the digital implementation is complicated instead. The model predictive controller has a similar performance to the multisampled PI controller for the current THD and step response [76]. Hence, the linear controller with a PWM modulator is still the most common controller due to its clear model in the frequency domain, which simplifies the stability analysis and parameter design. However, the nonlinear controller should inevitably earn more concerns because of the gradual development of powerful microprocessors [62], [63].

Besides the small-signal response, the multisampling can help to improve the large-signal response. When the control error derivative between the reference value and the feedback value is larger than the threshold value, the output duty cycle will be 0 or 1 within one multisampling period instead of half of the switching period [25]. Consequently, the controller saturation can be triggered faster, and the settling time under a large-signal disturbance can be shorter than the double-sampling control.

D. Practical Implementation

As aforementioned, using multisampling PWM can provide several benefits; however, the multisampling PWM also introduces a set of nonlinearities in the practical implementation. First, when the duty cycle is updated more than twice within one switching period, the switch may be triggered more than twice and the switching loss will increase compared with the

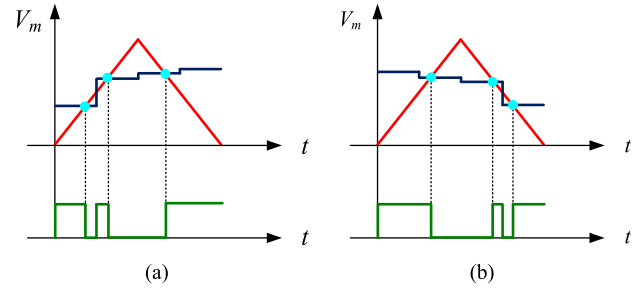


Fig. 17. Multiswitching diagram using multisampling PWM. (a) Rising edge. (b) Falling edge.

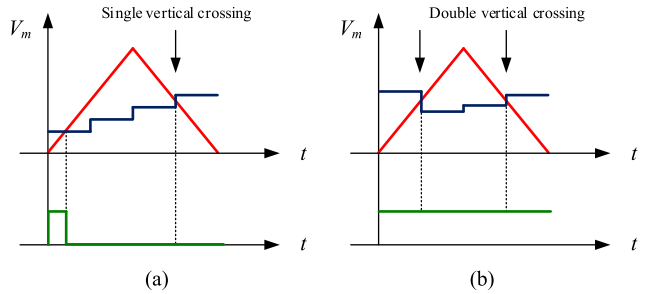


Fig. 18. Vertical crossing in multisampling PWM. (a) Single vertical crossing. (b) Double vertical crossing.

double-sampling PWM [77]. The multiswitching diagram using multisampling PWM is given in Fig. 17.

In order to avoid multiswitching, the maximum rate of change of the reference should not equal or exceed that of the carrier [26]. For the current control of a two-level inverter using the PI controller, the constraint in (52) should be satisfied. Moreover, a “self-lock” logic should be used in the microprocessors, where a single turn-OFF occurs during the first half of the switching period and a single turn-ON occurs during the second half [27].

$$K_p \frac{0.5U_{dc}}{L_f} < 2U_{dc}f_{sw}. \quad (52)$$

Moreover, the modulation signal may intersect with the carrier vertically, i.e., dead-band, where a variation in the modulating signal is no longer able to produce a change in the duty cycle [28]. This phenomenon depends on the considered modulation scheme and, more precisely, on the number of modulated edges. As shown in Fig. 18, the small-signal modulation gain will be halved or nulled under the single vertical crossing or double vertical crossing, respectively. Moreover, reduced gain regions can potentially lower the stability margins of the system, leading to oscillating behaviors.

Through the detection of vertical crossing, the dead-band can be avoided by forcing PWM to output pull-up and pull-down [29]. An alternative method is to make the modulation signal intersect with the carrier at the midpoint of two consecutive sampling events [28]. Consequently, the modulator operating point is equally distant from the two neighboring sampling instants and, thus, to the respective dead-bands. For example, in Fig. 19(a), $\varepsilon[n]$ is the error between the actual turn-OFF instant $t_{act}[n]$ and a reference turn-OFF instant $t_{ref}[n]$ in the n th

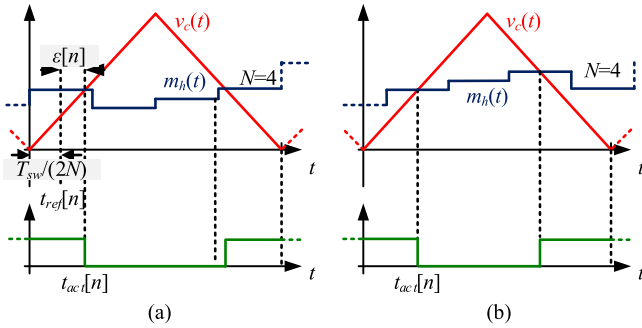


Fig. 19. Modulation diagrams (a) before and (b) after correction in multisampling PWM.

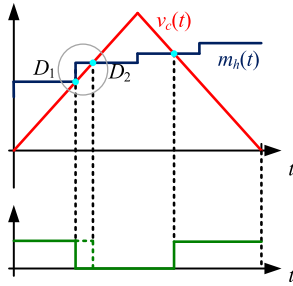


Fig. 20. Jitter amplification operating condition under four-sampling PWM.

switching cycle

$$\varepsilon[n] = t_{\text{act}}[n] - t_{\text{ref}}[n]. \quad (53)$$

The PLL correction algorithm will force $\varepsilon[n]$ to become zero by properly modulating the sampling period, as shown in Fig. 19(b), when the correction is achieved, $\varepsilon = 0$, and thus $T_{\text{sa}} = T_{\text{sw}}/N$. This property means that no provisions have to be taken to ensure stabilization of the sampling frequency.

It is worth noting that the dead-band happens when the modulation signal and the carrier are in counterphase operation. On the contrary, another nonlinear phenomenon called the jitter amplification will happen when the modulation signal and the carrier are in-phase operations [30]. As shown in Fig. 20, for a four-sampling PWM, switching action occurs near the instant at which $m_h(t)$ is updated. With a small-signal change of the controller output, such a higher duty cycle is required, and the up-count effective duty cycle changes from D_1 to D_2 . As a result, there will be an “increased gain” zone in the modulator transcharacteristic. The solution is to block the second duty cycle when the jitter is detected.

In order to prevent the limit cycle oscillations as any controller driving in a digital PWM, two conditions should be satisfied: 1) sufficient resolution of digital PWM, and 2) correct selection of the controller multisampling rate [25], [31], [60]. Assuming the digital PWM resolution is M , varying the duty cycle by $1/M$ determines an average current variation after half of the switching period, whose amplitude can be compared with the current error least significant bit value, i.e., q_{ADC} . Then the

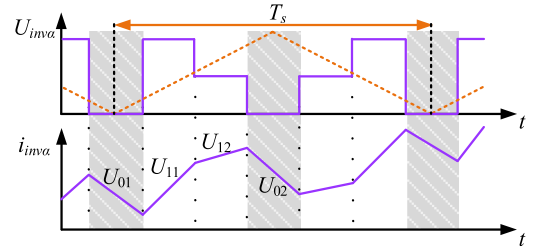


Fig. 21. Diagram of PWM voltage and current.

clock frequency constraint for an inverter is

$$f_{\text{clock}} \geq \frac{U_{\text{dc}}}{L_f} \frac{2^{n\text{bit}}}{|i_{\text{max}}|} \quad (54)$$

where $n\text{bit}$ is analog-to-digital converter (ADC) resolution and i_{max} is the full-scale range of the current sensor. In addition, the sampling process should be synchronized with the carrier, and an even number of current error samples are taken in each switching period. Only if these necessary conditions are met in the steady state, all zero crossings of the current error signal will be aligned with the average current sampling instants, and undesired transients will be avoided.

IV. CONDITION MONITORING AND PARAMETER ESTIMATION

Improving the sampling rate not only reduces the control delay and improves the stability of power electronics controllers but also provide more information from the multisampled data. The main difference with the multisampled current/voltage controllers is that the switching ripple is utilized rather than suppressed. Up till now, there are three kinds of applications, i.e., 1) current slope estimation within zero/active voltage, 2) dc-link capacitor monitoring, and 3) grid impedance estimation. The difference among these three applications only lies in the used multisampled variables and the related converters. Specifically, the current slope estimation only employs the sampled current ripple in the three-phase inverters. DC-link capacitor monitoring employs both the sampled current and the sampled voltage at the same time. Grid impedance estimation employs the sampled current and the sampled voltage for the two-level three-phase inverters, and only the sampled voltage is used in the single-phase H-bridge inverter and the interleaved two-cell three-phase inverters. Consequently, some new system state variables and parameters are estimated, which can help save the cost and improve reliability.

A. Current Slope Estimation

A three-phase PWM value can be transformed into two active vectors (U_{11} and U_{12}) and two zero vectors (U_{01} and U_{02}) within one switching period (see Fig. 21). The current slope within specific voltage vectors is widely used to estimate the position and the speed in the motor drive [32].

The current slope measurement can be achieved in two ways. One uses three low-cost current slope (di/dt) sensors to measure the current derivative directly; the other uses the motor line current samples to estimate the current slope [78]. The latter is more cost-effective in practical applications since no additional

sensors and ADC channels are required. Based on numerous current–time pairs from multisampling, the least square-based linear regression is used to calculate the current slope [79]–[82]. Assuming that the current evolves linearly during active/zero voltage vectors, a first-order function is used to fit the current data and it is given as

$$i(t) = a_1 t + a_0 \quad (55)$$

where $i(t)$, t , a_1 , and a_0 are the current, time, current slope, and intercept, respectively

$$\begin{cases} a_1 = \frac{\overline{it} - \bar{i}\bar{t}}{\bar{t}^2 - \bar{t}^2} = \frac{\frac{1}{n} \sum_{k=1}^n i(t_k)t_k - \frac{1}{n^2} \sum_{k=1}^n i(t_k) \sum_{k=1}^n t_k}{\frac{1}{n} \sum_{k=1}^n t_k^2 - \frac{1}{n^2} (\sum_{k=1}^n t_k)^2} \\ a_0 = \bar{i} - a_1 \bar{t} = \frac{1}{n} \sum_{k=1}^n i(t_k) - a_1 \frac{1}{n} \sum_{k=1}^n t_k \end{cases} \quad (56)$$

where \overline{it} , \bar{i} , \bar{t} , and \bar{t}^2 are the average product of current and time, average current, average time, and average time square during the active/zero voltage vectors. In order to mitigate the computational effort in the practical implementation, the four average values \overline{it} , \bar{i} , \bar{t} , and \bar{t}^2 can be calculated recursively and the computational effort remains the same for each sampling interval.

In addition, except for a high-performance FPGA-based platform, the current slope fitting method can also be achieved in a low-cost microprocessor-based platform. The ADC can be triggered by an internal timer block, and the direct memory access (DMA) engine is used to store the sampled currents in the software buffer after every ADC sampling is completed. The DMA engine is now common in most of the processors used in the automotive and aerospace industry [33].

During the switching transients, there will be some short-time current oscillations due to the parasitic parameters. The solution is to delay the start point of the regression window [37]. The estimation accuracy highly depends on the number of sampled data. Narrow voltage vectors should be extended to a minimum duration time, which is longer than the oscillation time of the phase current. The extension of the narrow voltage vector changes the fundamental PWM sequence, thus leading to additional current distortion and acoustic noise.

The first compensation method is shifting the double switching edge based on the voltage second balance [32], as shown in Fig. 22(a). However, modifying the standard PWM sequence can still cause additional current distortion. Another compensation method is injecting an opposite voltage pulse, as shown in Fig. 22(b), and a better current THD can be achieved [78]. Based on the artificial neural network, the minimum duration time requirement can further be relieved [83], [84]. The experimental current data are used as training data, and the target data are generated by fitting the steady-state data and propagating backward from the beginning of the sample window. Moreover, the inverter nonlinearity is also included in the training process.

Besides estimating the motor position and speed, the fitted current slope can also be used to detect the open-circuit fault of three-phase two-level inverters [35]. The current slope difference during two consecutive zero voltage vectors is approximately the same in normal conditions; however, in a fault

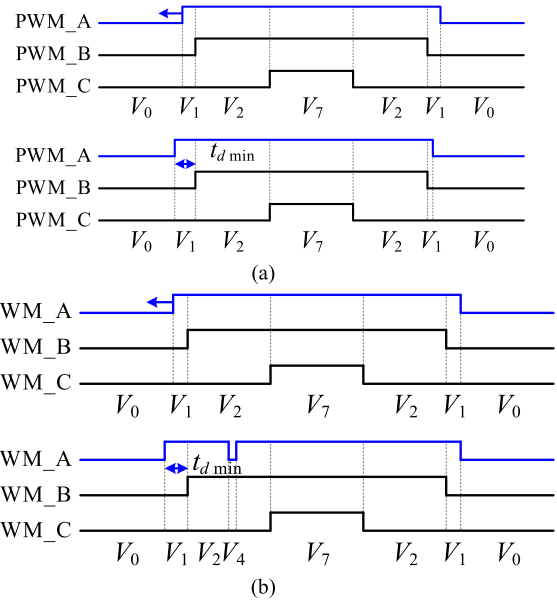


Fig. 22. Narrow voltage vector extension and compensation. (a) Shifting the double switching edge. (b) Opposite voltage pulse injection.

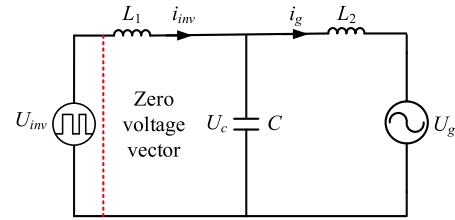


Fig. 23. Single-phase equivalent circuit of LCL-filtered inverter.

condition, the fault index is

$$\begin{cases} \varepsilon_{a01} - \varepsilon_{a02} \approx -2(\varepsilon_{b01} - \varepsilon_{b02}) \approx -2(\varepsilon_{c01} - \varepsilon_{c02}) \text{Fault}a \\ \varepsilon_{b01} - \varepsilon_{b02} \approx -2(\varepsilon_{a01} - \varepsilon_{a02}) \approx -2(\varepsilon_{c01} - \varepsilon_{c02}) \text{Fault}b \\ \varepsilon_{c01} - \varepsilon_{c02} \approx -2(\varepsilon_{a01} - \varepsilon_{a02}) \approx -2(\varepsilon_{b01} - \varepsilon_{b02}) \text{Fault}c \end{cases} \quad (57)$$

where ε_{a01} , ε_{a02} , ε_{b01} , ε_{b02} , ε_{c01} , and ε_{c02} are the current slope difference of phase a , phase b , and phase c during two consecutive zero voltage vectors, respectively. In the condition of high-frequency voltage signal injection, the current slope during other active voltage vectors can be estimated using two slopes in the zero voltage vectors. Consequently, the injection magnitude can be reduced by a factor of 7–10 compared with a standard single-sampling PWM [37]. Common approaches to the dead time compensation rely on the polarity of the sampled current with the single sampling. Due to the measurement noise, this method may cause a false compensation in the case of small currents. Based on the multisampling and the current slope measurement, the phase current at the beginning of dead time can be predicted in an FPGA and the computing process is fast due to the parallel data processing [36]. Using the voltage vector and the current slope, the motor inductance can be estimated in real time and the effect of inductor saturation is removed [33], [85]. Similarly, for an LCL-filtered inverter (see Fig. 23), the filter capacitor voltage can be estimated using the current slope

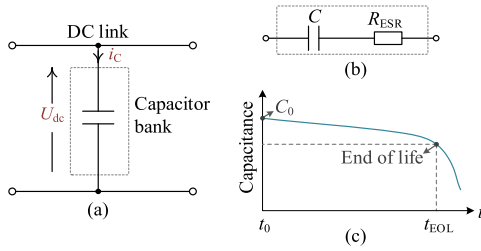


Fig. 24. Typical structure, equivalent circuit, and degradation characteristics of dc-link capacitors. (a) Typical structure. (b) Equivalent circuit. (c) Capacitance degradation characteristic.

TABLE IV
TYPICAL END-OF-LIFE CRITERIA OF CAPACITORS

	Al-Caps	MPPF-Caps	MLC-Caps
End-of-life criteria	$C/C_0 < 80\%$ $R_{ESR}/R_{ESR0} > 2$	$C/C_0 < 95\%$	$C/C_0 < 90\%$

C : capacitance; R_{ESR} : equivalent series resistance; C_0 : initial capacitance; R_{ESR0} : initial equivalent series resistance.

within zero voltage vectors [34], and it is given as

$$U_c = -L_1 \frac{di_{inv}}{dt}. \quad (58)$$

B. DC-Link Capacitor Monitoring

In dc-link applications, multisampling is used to estimate the dc-link capacitor, which aims to identify the degradation status and improves the reliability of systems [38], [86], [87]. Fig. 24(a) shows the typical structure of dc-link capacitors. Generally, three types of capacitors are used in dc-link capacitor banks, i.e., electrolytic capacitors (E-Caps), film capacitors (F-Caps), and multilayer ceramic capacitors (MLC-Caps). The equivalent circuit of dc-link capacitors is shown in Fig. 24(b), where C denotes the capacitance of capacitors, R_{ESR} represents the equivalent series resistance (ESR). According to Fig. 24(a) and (b), we have

$$\Delta U_{dc}(t) = \frac{1}{C} \int_0^t i_c(t) dt + R_{ESR} \cdot \Delta i_C(t) \quad (59)$$

where ΔU_{dc} and Δi_C represent the capacitor voltage ripple and capacitor current ripple, respectively. With the degradation of capacitors, a series of physical and chemical changes occur inside capacitors, which will cause the change of capacitor parameters (e.g., R_{ESR} and C). Taking capacitance change as an example, Fig. 24(c) gives the degradation curve of capacitors. Usually, dc-link capacitors are defined as fault states when the parameters reach the end-of-life criteria, as summarized in Table IV [88]. Fig. 25(a) shows the implementation of the multisampling in buck converters, which aims to estimate R_{ESR} and C of dc-link capacitors. The difference between the capacitor voltages sampled at points a and b is due to R_{ESR} and C . Based on (59), the estimation model is calculated as (60), where D represents the duty cycle. Here, to sample the voltage at points a and b , a PWM signal is needed [89], [90]. Similarly, the two-point sampling-based method can be used to estimate capacitor parameters in PV H5 inverter, as shown in

Fig. 25(b), the capacitance is calculated during the zero vector state, i.e., the power switch S_5 is turned OFF, and C is calculated as (61) [91].

$$\begin{cases} R_{ESR} = \frac{2L_1 f_{sw} [\Delta U_{dc}(0) + 2 \frac{2(D-1)}{(2-D)} \times \Delta U_{dc}(\frac{DT_{sw}}{2})]}{U_{dc}(D-1)} \\ C = \frac{V_o(2-D)(D-1)}{24L_1 f_{sw}^2 \Delta U_{dc}(\frac{DT_{sw}}{2})} \end{cases} \quad (60)$$

$$C = \frac{i_{pv-1} \times \Delta t}{U_{dc-2} - U_{dc-2}}. \quad (61)$$

Fig. 25(c) shows the circuit structure and key waveforms of a flyback converter with continuous conduction mode. According to the relationship between R_{ESR} , C , and capacitor voltage in (59), capacitor parameters can be calculated as (62) and (63) shown at the bottom of the next page, where f_{sw} and U_{dc} represent the switching frequency and capacitor voltage, respectively. Here, the capacitor voltage at sampling points c , d , and e is employed [92], [93].

Similarly, the multisampling can be used in a PV boost converter. Referring to Fig. 25(d), the difference between the capacitor voltages sampled at points f and h is due to R_{ESR} . The voltage difference at points g and f is only due to C . Using (59), R_{ESR} and C are calculated in (64) [93], [94].

$$C = \frac{U_{dc}(1-D)^3}{24L_s^2 f_s^2 \left\{ (1-D) \Delta U_{dc} \left(\frac{1+D}{2f_s} \right) + D \Delta U_{dc} \left(\frac{D}{2Df_s} \right) \right\}} \quad (62)$$

$$\begin{cases} R_{ESR} = [U_{dc}(0) - U_{dc}(DT_s)] L_2 / (U_{dc} DT_s) \\ C = \frac{U_{dc} DT_s^2}{8L_2 \{ U_{dc}(DT_s/2) - U_{dc}[(1+D)T_s/2] \}} \end{cases} \quad (64)$$

C. Grid Impedance Estimation

The stability of grid-connected inverters is mainly affected by the grid impedance. One method is to make the inverter output impedance dissipative by reducing control delay and adding extra state feedback [8]. The other one is to estimate the grid impedance, and the real grid voltage instead of the PCC voltage is feedforwarded [40]. By four-sampling the inverter-side currents, as shown in Fig. 26, the grid impedance can be estimated using two consecutive examples. Due to the sensitivity to sampling noise, the estimation method in [40] is not effective in identifying the grid impedance resistance. For a single-phase H-bridge inverter or an interleaved three-phase inverter, the apparent switching frequency is twice larger than the preset switching frequency. The grid impedance can also be estimated by sampling the PCC voltage four times within one switching period [39], [95]. As shown in Fig. 9, the inverter output voltage is equal to zero at the peak/valley of the carrier and equal to the dc-link voltage at the intersection point of the carrier, respectively. Then the grid impedance can be estimated through the bias between the PCC grid voltage at the peak/valley and the intersection points, as shown in (65). Both of the grid impedance estimation methods are based on multisampling, but the resistance cannot be acquired. Moreover, the more complex grid impedance including capacitance cannot be estimated because only the filter inductance is considered in [39], [40], and [95].

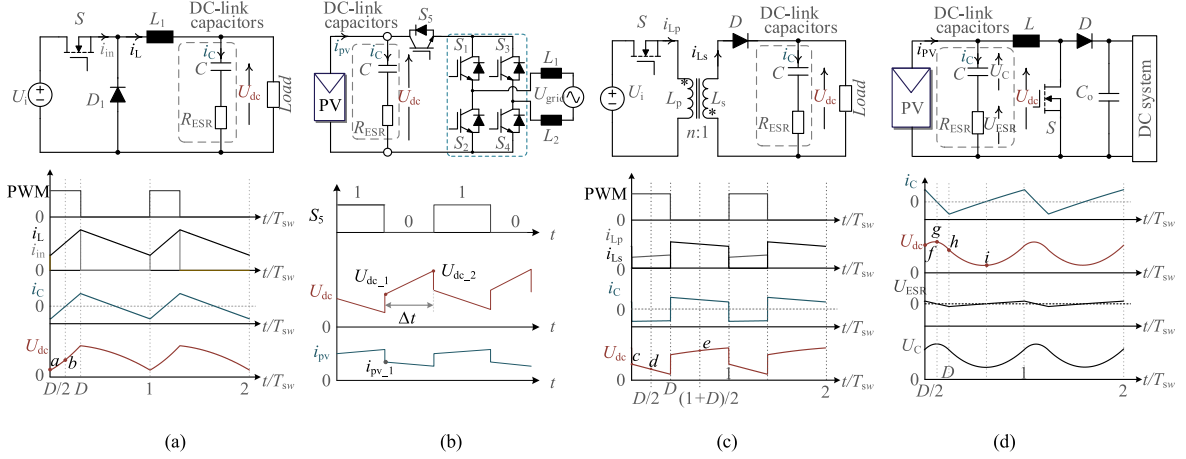


Fig. 25. Multisampling techniques used for capacitor parameters identification. (a) Buck converter. (b) Single-phase grid-connected PV H5 inverter. (c) Flyback converter. (d) PV boost converter.

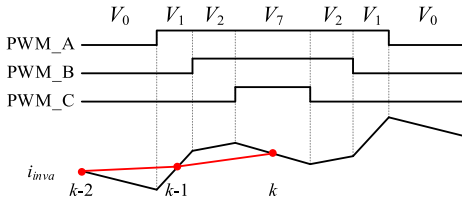


Fig. 26. Measurement instants within one switching period for a three-phase inverter.

$$L_g = L_f \frac{U_{pccinter} - U_{pccpeak/valley}}{U_{inverter} - (U_{pccinter} - U_{pccpeak/valley})} - L_f \frac{U_{ginter} - U_{gpeak/valley}}{U_{inverter} - (U_{pccinter} - U_{pccpeak/valley})} \approx L_f \frac{U_{pccinter} - U_{pccpeak/valley}}{U_{inverter} - (U_{pccinter} - U_{pccpeak/valley})}. \quad (65)$$

V. CHALLENGES AND FUTURE TRENDS

A. Sampled Switching Ripple Suppression

For the multisampling control of power electronic converters, a digital filter should be inserted in the control loop in order to remove the sampled switching harmonics. The LPLRF is mainly used in the dc-dc converter, where the introduced phase lag below switching frequency is small and the advantage of multisampling phase boost is fully exploited. However, for a two-level three-phase inverter, the sampled switching harmonics are at side switching frequencies, and the IRF/MRF still introduces a large delay that is equal to a one-fourth switching period. Consequently, the total loop control delay will be close

to one-fourth switching period with the increase in sampling rate. In order to further reduce the control delay, a more effective digital filter with a low phase-lag should be proposed. Similarly, for the multilevel inverter, the maximum allowable sampling rate is related to the apparent switching frequency. For example, the sampling rate is only four for a single-phase HB inverter, where no switching harmonics are introduced. Hence, the same challenge exists and the feasibility of using a higher sampling rate is not available. Until now, the multisampling control is only applied in a few power electronic converters, and the potentiality of multisampling on other effective converters needs to be further researched in the future. Besides the digital filter, a single-edge modulator with a predistorted carrier or the FOH sampler can also help to remove the switching ripple from a physical point of view. Actually, how to remove the multisampled switching ripple is still an open topic.

B. Stability Analysis

In the practical implementation, there are a set of nonlinearities, including multiswitching, dead-band, and jitter. Although some solutions are provided to linearize the modulation behavior, the focus is on the gain margin, and the phase margin is not considered. In addition, the control system is discretized with the multisampling period when designing the switching ripple filter and analyzing the stability. As a result, the Nyquist frequency is equal to half of the sampling frequency instead of the switching frequency, and the stability above the switching frequency is still not considered. Hence, a more accurate small-signal multisampling model should be proposed considering discretization and the related nonlinearities. In terms of large-signal stability, only the effect of reference change is investigated. How multisampling affects transient stability should further be investigated.

$$R_{ESR} = \frac{12L_s D f_s \left[2(1-D) \Delta U_{dc} \left(\frac{1+D}{2f_s} \right) + (1+2D) \Delta U_{dc} \left(\frac{D}{2f_s} \right) \right] \left[(1-D) \Delta U_{dc} \left(\frac{1+D}{2f_s} \right) + D \Delta U_{dc} \left(\frac{D}{2f_s} \right) \right]}{U_{dc} (1-D)^3 \left[\Delta U_{dc}(0) - \Delta U_{dc} \left(\frac{D}{2f_s} \right) \right]}. \quad (63)$$

C. Estimating More States and Parameters

The multisampled switching ripple is used to estimate the current slope, dc-link parameters, and grid impedance. It is worth noting that all these three applications mainly focus on a few power electronic converters, and their feasibility in more converters should further be researched. In addition, all these three applications are model-based methods, and it is hard to estimate more states and parameters. Artificial intelligence is already widely used in practice, and a large dataset is the prerequisite. Fortunately, the multisampling can provide enough data within one switching period. Therefore, it is possible to combine artificial intelligence and multisampling to improve the stability and reliability of power converters, such as fault diagnosis, sensorless control, and complex grid impedance estimation.

VI. CONCLUSION

With the gradually decreasing cost of high-performance digital processors, multisampling has become a promising technology in power electronics. In this article, the application of multisampling in power electronic converters is discussed and reviewed. Compared with the variants of regular single/double-sampling PWM, the multisampling PWM cannot only reduce the control delay but also will not introduce the aliasing and the duty cycle limitation. In addition, solutions to the issues in practical implementation are provided. With respect to the condition monitoring and parameter estimation, three kinds of applications are surveyed, including current slope estimation, dc-link parameter estimation, and grid impedance estimation. In particular, more multisampled-data-based applications in power electronics systems will be seen in the future since they provide new important information and better performance.

REFERENCES

- [1] M. Naouar, E. Monmasson, A. Naassani, I. Belkhdja, and N. Patin, "FPGA-based current controllers for AC machine drives—A review," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1907–1925, Aug. 2007.
- [2] Y. Tu, J. Liu, Z. Liu, D. Xue, and L. Cheng, "Impedance-based analysis of digital control delay in grid-tied voltage source inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11666–11681, Nov. 2020.
- [3] M. Lu, X. Wang, P. C. Loh, F. Blaabjerg, and T. Dragicevic, "Graphical evaluation of time-delay compensation techniques for digitally controlled converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2601–2614, Mar. 2018.
- [4] G. Elhassan, S. Zulkifli, E. Pathan, M. H. Khan, and R. Jackson, "A comprehensive review on time-delay compensation techniques for grid-connected inverters," *IET Renew. Power Gener.*, vol. 15, no. 2, pp. 251–266, Feb. 2021.
- [5] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of LCL-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3414–3427, Jul. 2014.
- [6] M. Hu *et al.*, "Fast current control without computational delay by minimizing update latency," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12207–12212, Nov. 2021.
- [7] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Switching harmonics suppression of single-loop multi-sampling control of grid-connected inverter," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2020, pp. 3259–3264.
- [8] L. Harnefors, X. Wang, A. Yepes, and F. Blaabjerg, "Passivity-based stability assessment of grid-connected VSCs—An overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 116–125, Mar. 2016.
- [9] G. Oriti and A. L. Julian, "Three-phase VSI with FPGA-based multisampled space vector modulation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1813–1820, May 2011.
- [10] Q. Wei, B. Wu, D. Xu, and N. Zargari, "A natural-sampling-based SVM scheme for current source converter with superior low-order harmonics performance," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6144–6154, Sep. 2016.
- [11] X. Zhang, P. Chen, C. Yu, F. Li, H. Do, and R. Cao, "Study of a current control strategy based on multisampling for high-power grid-connected inverters with an LCL filter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5023–5034, Jul. 2017.
- [12] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Overview of multisampling techniques in power electronics converters," in *Proc. IEEE 45th Annu. Conf. Ind. Electron. Soc.*, Oct. 2019, vol. 1, pp. 1922–1927.
- [13] L. Corradini, P. Mattavelli, E. Tedeschi, and D. Trevisan, "High-bandwidth multisampled digitally controlled DC–DC converters using ripple compensation," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1501–1508, Apr. 2008.
- [14] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Aliasing suppression of multi-sampled current controlled LCL-filtered inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 2411–2423, Apr. 2022.
- [15] I. Petric, S. Member, P. Mattavelli, and S. Buso, "Feedback noise propagation in multisampled DC-DC power electronic converters," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 150–161, Jan. 2021.
- [16] L. Corradini, W. Stefanutti, and P. Mattavelli, "Analysis of multisampled current control for active filters," *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1785–1794, Dec. 2008.
- [17] T. Mouton, A. Beer, B. Putzeys, and B. McGrath, "Modelling and design of single-edge oversampled pwm current regulators using z-domain methods," in *Proc. IEEE ECCE Asia*, Jun. 2013, pp. 31–37.
- [18] T. Mouton and B. Putzeys, "Digital control of a PWM switching amplifier with global feedback," in *Proc. 37th Int. Conf. Class D Audio Amplification*, Aug. 2009, pp. 1–10.
- [19] M. Broadmeadow, E. Burstinghaus, G. Walker, and G. Ledwich, "FPGA implementation of an arbitrary resample rate, FOH, pulse width modulator," *J. Eng.*, vol. 2019, no. 17, pp. 3730–3735, Jun. 2019.
- [20] E. Burstinghaus, G. Ledwich, G. Walker, H. Pezeshki, and M. Broadmeadow, "Advanced resampling techniques for PWM amplifiers in real-time applications," in *Proc. IEEE Southern Power Electron. Conf.*, Dec. 2016, pp. 1–6.
- [21] H. Fujita, "A single-phase active filter using an H-bridge PWM converter with a sampling frequency quadruple of the switching frequency," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 934–941, Apr. 2009.
- [22] J. Ma, X. Wang, F. Blaabjerg, W. Song, S. Wang, and T. Liu, "Multi-sampling method for single-phase grid-connected cascaded H-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8322–8334, Oct. 2020.
- [23] T. Correa, O. Konig, and R. Greul, "Multisampling in interleaved converters and modular multilevel converters," in *Proc. IEEE 42nd Annu. Conf. Ind. Electron. Soc.*, Oct. 2016, pp. 3500–3505.
- [24] J. Samanes, A. Urtasun, E. Gubia, and A. Petri, "Robust multisampled capacitor voltage active damping for grid-connected power converters," *Int. J. Electr. Power Energy Syst.*, vol. 105, pp. 741–752, Feb. 2019.
- [25] S. Buso, T. Caldognetto, and D. Brandao, "Dead-beat current controller for voltage source converters with improved large-signal response," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1588–1596, Mar./Apr. 2015.
- [26] J. Bocker and O. Buchholz, "Can oversampling improve the dynamics of PWM controls?," in *Proc. IEEE Int. Conf. Ind. Technol.*, Apr. 2013, pp. 1818–1824.
- [27] J. Yang *et al.*, "Carrier-based digital PWM and multirate technique of a cascaded H-bridge converter for power electronic traction transformers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1207–1223, Jun. 2019.
- [28] L. Corradini, P. Mattavelli, and S. Saggini, "Elimination of sampling-induced dead bands in multiple-sampled pulsewidth modulators for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2661–2665, Jul. 2009.
- [29] C. Yu, C. Liu, Q. Wang, W. Zhang, S. Li, and X. Zhang, "Implementation of multi-sampling current control for grid-connected inverters using TI TMS320F28377x," in *Proc. IEEE 32nd Youth Acad. Annu. Conf. Chin. Assoc. Autom.*, May 2017, pp. 1228–1233.
- [30] I. Petric, P. Mattavelli, and S. Buso, "A jitter amplification phenomenon in multisampled digital control of power converters," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8685–8695, Aug. 2021.

- [31] M. Bradley, E. Alarcon, and O. Feely, "Design-oriented analysis of quantization-induced limit cycles in a multiple-sampled digitally controlled buck converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 4, pp. 1192–1205, Apr. 2014.
- [32] Q. Gao, G. M. Asher, M. Sumner, and P. Makys, "Position estimation of AC machines over a wide frequency range based on space vector PWM excitation," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1001–1011, Aug. 2007.
- [33] R. Raja, T. Sebastian, and M. Wang, "Online stator inductance estimation for permanent magnet motors using PWM excitation," *IEEE Trans. Transp. Electrification*, vol. 5, no. 1, pp. 107–117, Mar. 2019.
- [34] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Line voltage sensorless control of grid-connected inverters using multisampling," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4792–4803, Apr. 2022.
- [35] F. Oelkers, B. Weber, and A. Mertens, "Oversampling based approach for open circuit fault detection in PMSM drive systems," in *Proc. IEEE 18th Eur. Conf. Power Electron. Appl.*, Oct. 2016, pp. 1–10.
- [36] B. Weber, T. Brandt, and A. Mertens, "Compensation of switching dead-time effects in voltage-fed PWM inverters using FPGA-based current oversampling," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, May 2016, pp. 3172–3179.
- [37] P. Landsmann, J. Jung, M. Kramkowski, P. Stolze, D. Paulus, and R. Kennel, "Lowering injection amplitude in sensorless control by means of current oversampling," in *Proc. IEEE 3rd Int. Symp. Sensorless Control Elect. Drives*, 2013, pp. 1–6.
- [38] Z. Zhao, P. Davari, W. Lu, H. Wang, and F. Blaabjerg, "An overview of condition monitoring techniques for capacitors in dc-link applications," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3692–3716, Apr. 2021.
- [39] X. Wang, K. Qin, X. Ruan, D. Pan, Y. He, and F. Liu, "A robust grid-voltage feedforward scheme to improve adaptability of grid-connected inverter to weak grid condition," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2384–2395, Jul. 2020.
- [40] A. Ghanem, M. Rashed, M. Sumner, M. Elsayes, and I. Mansy, "Grid impedance estimation for islanding detection and adaptive control of converters," *IET Power Electron.*, vol. 10, no. 11, pp. 1279–1288, Aug. 2017.
- [41] L. Harnefors, A. Yepes, A. Vidal, and J. Gandoy, "Passivity-based controller design of grid-connected VSCs for prevention of electrical resonance instability," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 702–710, Feb. 2015.
- [42] D. Holmes, T. Lipo, B. McGrath, and W. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, Nov. 2009.
- [43] D. Zhou and F. Blaabjerg, "Bandwidth oriented proportional-integral controller design for back-to-back power converters in DFIG wind turbine system," *IET Renewable Power Gener.*, vol. 11, no. 7, pp. 941–951, Jun. 2017.
- [44] D. Sype, K. Gusseme, A. Bossche, and J. Melkebeek, "Small-signal Laplace-domain analysis of uniformly-sampled pulse-width modulators," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, 2004, pp. 4292–4298.
- [45] D. Sype, K. Gusseme, F. Belie, A. Bossche, and J. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 470–478, Mar. 2006.
- [46] D. Pan, X. Ruan, X. Wang, F. Blaabjerg, X. Wang, and Q. Zhou, "A highly robust single-loop current control scheme for grid-connected inverter with an improved LCCL filter configuration," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8474–8487, Oct. 2018.
- [47] J. Ma, X. Wang, F. Blaabjerg, L. Harnefors, and W. Song, "Accuracy analysis of the zero-order hold model for digital pulse width modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10826–10834, Dec. 2018.
- [48] B. Zhang, J. Xu, and S. Xie, "Analysis and suppression of the aliasing in real-time sampling for grid-connected LCL-filtered inverters," in *Proc. IEEE 11th Conf. Ind. Electron. Appl.*, 2016, pp. 304–309.
- [49] G. Bonanno and L. Corradini, "Digital predictive current-mode control of three-level flying capacitor buck converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4697–4710, Apr. 2021.
- [50] L. Harnefors, R. Finger, X. Wang, H. Bai, and F. Blaabjerg, "VSC input-admittance modeling and analysis above the Nyquist frequency for passivity-based stability assessment," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6362–6370, Aug. 2017.
- [51] H. Deng, R. Oruganti, and D. Srinivasan, "PWM methods to handle time delay in digital control of a UPS inverter," *IEEE Power Electron. Lett.*, vol. 3, no. 1, pp. 1–6, Mar. 2005.
- [52] K. Zhu, P. Sun, L. Wang, L. Zhou, and X. Du, "Control delay compensation scheme based on non-instantaneous loading and pulse-width equivalence for active damping of LCL-type inverters," *IET Power Electron.*, vol. 12, no. 9, pp. 2389–2399, Jul. 2019.
- [53] L. Corradini and P. Mattavelli, "Modeling of multisampled pulse width modulators for digitally controlled DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1839–1847, Jul. 2008.
- [54] J. Ota, Y. Shibano, N. Niimura, and H. Akagi, "A phase-shifted-PWM D-STATCOM using a modular multilevel cascade converter (SSBC)—Part I: Modeling, analysis, and design of current control," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 279–288, Feb. 2015.
- [55] H. Tian, Y. W. Li, and P. Wang, "Hybrid AC/DC system harmonics control through grid interfacing converters with low switching frequency," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2256–2267, Mar. 2018.
- [56] H. Tian, Y. W. Li, and Q. Zhao, "Multirate harmonic compensation control for low switching frequency converters: Scheme, modeling, and analysis," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4143–4156, Apr. 2020.
- [57] X. Zhang and J. W. Spencer, "Study of multisampled multilevel inverters to improve control performance," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4409–4416, Nov. 2012.
- [58] D. Yang, X. Ruan, and H. Wu, "A real-time computation method with dual sampling mode to improve the current control performance of the LCL-type grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4563–4572, Jul. 2015.
- [59] J. Ma, X. Wang, F. Blaabjerg, W. Song, S. Wang, and T. Liu, "Real-time calculation method for single-phase cascaded H-bridge inverters based on phase-shifted carrier pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 977–987, Jan. 2020.
- [60] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, 2nd ed. San Rafael, CA, USA: Morgan & Claypool, 2015.
- [61] W. Wu, Y. Liu, Y. He, H. S. H. Chung, M. Liserre, and F. Blaabjerg, "Damping methods for resonances caused by LCL-filter-based current-controlled grid-tied power inverters: An overview," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7402–7413, Sep. 2017.
- [62] Q. Liu, T. Caldognetto, and S. Buso, "Review and comparison of grid-tied inverter controllers in microgrids," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7624–7639, Jul. 2020.
- [63] S. He, Y. Pan, D. Zhou, X. Wang, and F. Blaabjerg, "Current harmonic analysis of multisampled LCL-type grid-connected inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2020, pp. 4329–4335.
- [64] S. Vukosavić, L. Perić, and E. Levi, "AC current controller with error-free feedback acquisition system," *IEEE Trans. Energy Convers.*, vol. 31, no. 1, pp. 381–391, Mar. 2016.
- [65] A. Yepes, A. Vidal, J. Malvar, O. Lopez, and J. Gandoy, "Tuning method aimed at optimized settling time and overshoot for synchronous proportional-integral current control in electric machines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3041–3054, Jun. 2014.
- [66] J. Wang, J. D. Yan, and L. Jiang, "Pseudo-derivative-feedback current control for three-phase grid-connected inverters with LCL filters," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3898–3912, May 2016.
- [67] S. Huang, L. Mathe, and R. Teodorescu, "A new method to implement resampled uniform PWM suitable for distributed control of modular multilevel converters," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2013, pp. 228–233.
- [68] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Multisampling control of two-cell interleaved three-phase grid-connected converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Jul. 2021, pp. 1432–1437.
- [69] D. Pan, X. Ruan, and X. Wang, "Direct realization of digital differentiators in discrete domain for active damping of LCL-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8461–8473, Oct. 2018.
- [70] G. Liu and P. Mattavelli, "Hysteresis droop controller with one sample delay for DC–DC converters in DC microgrids," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2019, pp. 2078–2084.
- [71] S. Buso and T. Caldognetto, "A nonlinear wide-bandwidth digital current controller for DC–DC and DC–AC converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7687–7695, Dec. 2015.
- [72] R. Gupta, A. Ghosh, and A. Joshi, "Characteristic analysis for multi-sampled digital implementation of fixed-switching-frequency closed-loop modulation of voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2382–2392, Jul. 2009.
- [73] C. Fischer, S. Mariétoz, and M. Morari, "Multisampled hybrid model predictive control for pulse-width modulated systems," in *Proc. IEEE 50th Conf. Decis. Control Eur. Control Conf.*, Mar. 2012, pp. 3074–3079.

- [74] S. Mariethoz and M. Morari, "Multisampled model predictive control of inverter systems: A solution to obtain high dynamic performance and low distortion," in *Proc. IEEE Energy Convers. Congr. Expo.*, Nov. 2012, pp. 1692–1697.
- [75] S. Buso, T. Caldognetto, and D. Brandao, "Comparison of oversampled current controllers for microgrid utility interface converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2015, pp. 6888–6895.
- [76] M. Tomlinson, T. Mouton, and R. Kennel, "Finite-control-set model predictive control with a fixed switching frequency vs. linear control for current control of a single-leg inverter," in *Proc. IEEE Int. Symp. Predictive Control Elect. Drives Power Electron.*, Feb. 2016, pp. 109–114.
- [77] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-step controller design for LCL-type grid-connected inverter with capacitor-current-feedback active-damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239–1253, Mar. 2014.
- [78] Y. Hua, M. Sumner, G. Asher, Q. Gao, and K. Saleh, "Improved sensorless control of a permanent magnet machine using fundamental pulse width modulation excitation," *IET Electr. Power Appl.*, vol. 5, no. 4, pp. 359–370, Apr. 2011.
- [79] Y. Duan and M. Sumner, "A novel current derivative measurement using recursive least square algorithms for sensorless control of permanent magnet synchronous machine," in *Proc. ECCE Asia*, Aug. 2012, vol. 2, pp. 1193–1200.
- [80] X. Luo, Q. Tang, A. Shen, H. Shen, and J. Xu, "A combining FPE and additional test vectors hybrid strategy for IPMSM sensorless control," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6104–6113, Jul. 2018.
- [81] M. Bui, D. Guan, D. Xiao, and M. Rahman, "A modified sensorless control scheme for interior permanent magnet synchronous motor over zero to rated speed range using current derivative measurements," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 102–113, Jan. 2019.
- [82] J. Fox, *Applied Regression Analysis and Generalized Linear Models*. Thousand Oaks, CA, USA: Sage, 2015.
- [83] D. Hind, M. Sumner, and C. Gerada, "Use of an artificial neural network for current derivative estimation," in *Proc. IEEE 15th Eur. Conf. Power Electron. Appl.*, Feb. 2013, pp. 1–10.
- [84] D. Hind, M. Sumner, and C. Gerada, "Estimating current derivatives for sensorless motor drive applications," in *Proc. IEEE 17th Eur. Conf. Power Electron. Appl.*, Oct. 2015, pp. 1–10.
- [85] M. Bui, M. Rahman, D. Guan, and D. Xiao, "A new and fast method for on-line estimation of d and q axes inductances of interior permanent magnet synchronous machines using measurements of current derivatives and inverter dc-bus voltage," *IEEE Trans. Ind. Electron.*, vol. 66, no. 10, pp. 7488–7497, Oct. 2019.
- [86] Z. Zhao, W. Lu, P. Davari, X. Du, H. Iu, and F. Blaabjerg, "An on-line parameters monitoring method for output capacitor of buck converter based on large-signal load transient trajectory analysis," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4004–4015, Aug. 2021.
- [87] Z. Zhao, P. Davari, Y. Wang, and F. Blaabjerg, "Online capacitance monitoring for dc/dc boost converters based on low-sampling-rate approach," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi: [10.1109/JESTPE.2021.3108420](https://doi.org/10.1109/JESTPE.2021.3108420), 2021.
- [88] K. Yao, W. Tang, W. Hu, and J. Lyu, "A current-sensorless online ESR and C identification method for output capacitor of buck converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6993–7005, Dec. 2015.
- [89] J. Gao, D. Huang, and J. Lu, "Online output capacitor monitor for buck dc-dc converter," in *Proc. IEEE Prognostics Syst. Health Manage. Conf.*, 2018, pp. 802–806.
- [90] N. Agarwal, M. Ahmad, and S. Anand, "Condition monitoring of dc-link capacitor utilizing zero state of solar PV H5 inverter," in *Proc. IEEE 10th Int. Conf. Compat., Power Electron. Power Eng.*, Aug. 2016, pp. 174–179.
- [91] K. Yao, C. Cao, and S. Yang, "Noninvasive online condition monitoring of output capacitor's ESR and C for a flyback converter," *IEEE Trans. Instrum. Meas.*, vol. 66, no. 12, pp. 3190–3199, Dec. 2017.
- [92] K. Yao *et al.*, "A noninvasive online monitoring method of output capacitor's C and ESR for DCM flyback converter," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5748–5763, Jun. 2019.
- [93] M. Ahmad, A. Arya, and S. Anand, "An online technique for condition monitoring of capacitor in PV system," in *Proc. IEEE Int. Conf. Ind. Technol.*, Mar. 2015, pp. 920–925.
- [94] M. Ahmad, N. Agarwal, and S. Anand, "Online monitoring technique for aluminum electrolytic capacitor in solar PV-based DC system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7059–7066, Nov. 2016.
- [95] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Multisampling based grid impedance estimation for two-cell interleaved three-phase inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Nov. 2021, pp. 590–594.
- [96] L. Harnefors, L. Zhang, and M. Bongiorno, "Frequency-domain passivity-based current controller design," *IET Power Electron.*, vol. 1, no. 4, pp. 455–465, Dec. 2008.
- [97] F. Hans, W. Schumacher, S. Chou, and X. Wang, "Passivation of current-controlled grid-connected VSCs using passivity indices," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8971–8980, Nov. 2019.



Shan He (Student Member, IEEE) received the B.S. degree from Northeast Electric Power University, Jilin, China, in 2015 and the M.S. degree from Zhejiang University, Hangzhou, China, in 2018, both in electrical engineering. He is currently working toward the Ph.D. degree in power electronics with Aalborg University, Aalborg, Denmark.

He was a visiting researcher with RWTH Aachen University, Aachen, Germany, from October to December 2021. His current research interests include modeling and control of grid-connected converters.



Dao Zhou (Senior Member, IEEE) received the B.S. degree from Beijing Jiaotong University, Beijing, China, in 2007, the M.S. degree from Zhejiang University, Hangzhou, China, in 2010, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2014, all in electrical engineering.

Since 2014, he has been with the Department of Energy Technology, Aalborg University, where he is currently an Assistant Professor. His research interests include modeling, control, and reliability of power electronics in renewable energy applications.

Dr. Zhou was a recipient of the Renewable and Sustainable Energy Conversion Systems of the IEEE Industry Applications Society First Prize Paper Award in 2015 and the Best Session Paper at the Annual Conference of the IEEE Industrial Electronics Society in Austria in 2013.



Xiongfei Wang (Senior Member, IEEE) received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree from the Harbin Institute of Technology, Harbin, China, in 2008, both in electrical engineering, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013.

Since 2009, he has been with the Department of Energy Technology, Aalborg University, where he became an Assistant Professor in 2014, an Associate Professor in 2016, a Professor, and the Leader of the Electronic Power Grid (eGrid) Research Group in 2018. He has also been a part-time Professor with the KTH Royal Institute of Technology, Stockholm, Sweden, since 2020. His current research interests include modeling and control of power electronic converters and systems, stability and power quality of power-electronics-dominated power systems, and high-power converters.

Dr. Wang serves as a Co-Editor-in-Chief for the IEEE TRANSACTIONS ON POWER ELECTRONICS and as an Associate Editor for the *IEEE Journal of Emerging and Selected Topics in Power Electronics*. He was a recipient of eight prize paper awards in the IEEE transactions and conferences, the 2016 AAU Talent for Future Research Leaders, the 2018 Richard M. Bass Outstanding Young Power Electronics Engineer Award, the 2019 IEEE PELS Sustainable Energy Systems Technical Achievement Award, the 2020 IEEE PES Prize Paper Award, the 2020 JESTPE Star Associate Editor Award, and the Highly Cited Researcher in the Web of Science from 2019.



Zhaoyang Zhao (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Northeast Agricultural University, Harbin, China, in 2014 and 2017, respectively, and the Ph.D. degree in electrical engineering from Chongqing University, Chongqing, China, in 2020.

From 2019 to 2020, he was a Visiting Ph.D. Student with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. From 2021 to 2022, he was with Zhengzhou University as an Assistant Professor. In 2022, he joined Southwest Jiaotong University, Chengdu, China, as an Assistant Professor. He is an Associate Editor for *Circuit World*. His research interests include condition monitoring, reliability assessment, and control of power electronic converters.



Frede Blaabjerg (Fellow, IEEE) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He received the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1995.

He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. In 2017, he became a Villum Investigator. He has authored or coauthored more than 600 journal papers in the fields of power electronics and its applications. He is the coauthor of four monographs and Editor of ten books

on power electronics and their applications. His current research interests include power electronics and its applications, such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives.

Dr. Blaabjerg was a recipient of 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019, and the 2020 IEEE Edison Medal. He was the Editor-in-Chief for the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He was a Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 and from 2017 to 2018. During 2019–2020, he was the President of the IEEE Power Electronics Society. He was the Vice-President of the Danish Academy of Technical Sciences too. He was nominated during 2014–2019 by Thomson Reuters to be among the 250 most cited researchers in engineering in the world.