A MHz *LCLCL* Resonant Converter Based Single-Stage Soft-Switching Isolated Inverter With Variable Frequency Modulation

Hao Wen, *Member, IEEE*, Dong Jiao, Jih-Sheng Lai, *Life Fellow, IEEE*, Johan Strydom, *Senior Member, IEEE*, and Bing Lu

***Abstract*—Compared to the typical two-stage isolated inverter, which includes an isolated dc–dc and a pulsewidth modulated dc–ac, the single-stage approach features lower component counts, less control complexity, better efficiency, and power density with an isolated dc-rectified sine stage and a line frequency unfolder. In the literature, SRC and *LLC* are mostly utilized for the isolated dc-rectified sine stage, which is the key part of an efficient single-stage inverter design. This article introduces a novel MHz *LCLCL* converter based single-stage, soft-switching isolated inverter with variable frequency modulation. The paralleled *LC* within the *LCLCL* resonant tank can naturally create a zero voltage gain at their resonant frequency, which shows superior characteristics for rectified sine wave generation. With the proposed *LCLCL* resonant tank design method, simpler control and better output ac voltage waveform quality for different load conditions can be obtained. To verify the proposed resonant tank design method and the *LCLCL* converter based single-stage isolated inverter topology, a GaN based 380 V_{dc}–600 V_{ac}, 1.2 kW prototype is built and tested. Under different load conditions, the measured total harmonic distortion of the output voltage can always keep around 2% with 97.0% peak efficiency for the overall inverter.**

***Index Terms*—GaN based MHz inverter, LCLCL, multi-element resonant converter, single stage inverter, soft switching inverter, variable frequency modulation (VFM).**

I. Introduction

GALVANIC isolation is needed for the inverter design in some practical systems with safety regulations [1]. Conventionally, the two-stage approach is widely adopted, as shown in Fig. 1, with an isolated dc–dc stage and a sinusoidal pulsewidth modulation (SPWM) dc–ac stage [2]. However, this two-stage configuration suffers from more component counts, more control complexity and potentially lower power density and lower efficiency. Meanwhile, a large dc bus capacitor is also necessary to attenuate the double line frequency ripple from SPWM [3]. Therefore, the single-stage approach including an isolated dc-rectified sine stage and a line frequency unfolder, as shown in Fig. 2, becomes preferable. With the almost lossless unfolder due to line frequency switching, this approach is normally referred as a single-stage solution [4] and the isolated dc-rectified sine stage design becomes critical.

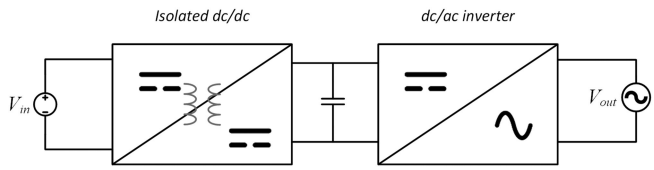

Fig. 1. Conventional two-stage inverter configuration.

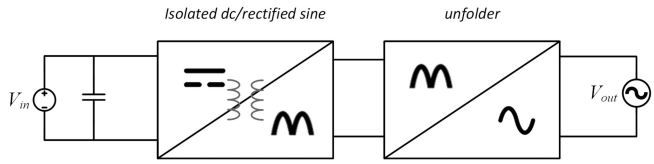

Fig. 2. Single-stage isolated inverter configuration.

Both PWM-based converter and resonant converter can be selected as the isolated dc-rectified sine stage. For PWM-based converter, which is widely used in the literature, duty cycle can be adjusted to generate a rectified sine wave. Flyback converter and Cuk converter have also been adopted in [5] and [6]. However, the hard switching will hurt the efficiency of the overall inverter. For efficiency concerns, a resonant converter with wide soft switching range is a better option but the relevant research is scarce.

There are mainly two types of approaches for the rectified or half sine generation in the literature. The first type is to apply different modulation methods on SRC/*LLC*. In [7], variable frequency modulation (VFM), which adjusts the switching frequency to control the output voltage, is applied to the SRC. COMFET was used as the main switch in [7] so ZCS was preferred and the circuit works in switching frequency lower than the resonant frequency region. VFM is beneficial for its low resonant current rms value but impractical infinite switching

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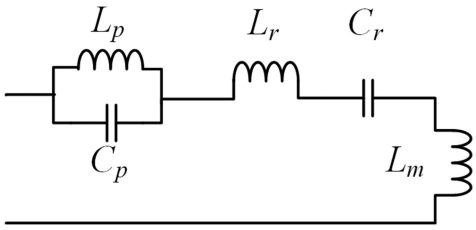

Fig. 3. *LCLCL* resonant tank.

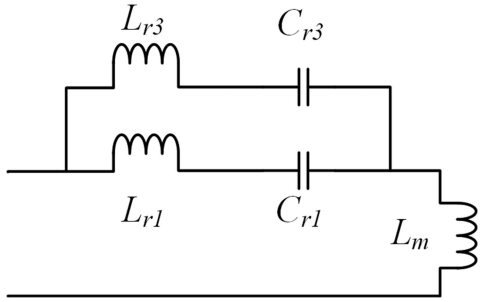

Fig. 4. *LLC* resonant tank with one more *LC* branch.

frequency is needed to achieve zero voltage gain. To solve this issue, Yeh *et al.* [8] used VFM for output high line region and proposes short pulse density modulation (SPDM) for output low line region. SPDM is similar to pulse density modulation and the difference is that SPDM works at the maximum frequency, which is much higher than the resonant frequency. However, SPDM suffers from very high resonant current rms value due to its short conduction time. Wen *et al.* [9] proposed to have full bridge (FB) VFM for output high line region and half bridge (HB) VFM for output low line region. By changing from full bridge to half bridge, the voltage gain is reduced to half while still maintaining the advantage of VFM to have low resonant current rms value. However, the control strategy is complex and the boundary between FB VFM and HB VFM needs to be determined based on the load condition. With lighter load, the boundary will be higher due to higher voltage gain at the maximum switching frequency. Therefore, the total harmonic distortion (THD) of the output voltage will be poor for light load conditions. In the meantime, Yeh *et al.* [8] and Wen *et al.* [9] needed a maximum switching frequency to be 3x or 4x of the minimum switching frequency. This wide switching frequency range makes it difficult for ferrite core material selection. In [29], phase shift modulation (PSM), which adjusts the output voltage by changing the phase shift between two switching legs, is applied to *LLC* as the isolated dc-rectified sine stage. It is a full range modulation method, but ZVS is difficult under output low line region and light load condition. Compared to VFM, PSM has higher resonant current rms value since the two upper/lower switches can be turned ON at the same time.

The second type of method is to add additional component in the SRC/*LLC* to achieve wide voltage gain range with different operation modes. In [10], an additional switch is added in the *LLC* converter. When it is turned ON, the resonant inductor will be charged and act as a boost inductor so higher voltage gain can be achieved. In [11], additional capacitors and diodes are added in the original voltage doubler rectifier of *LLC* converter. By controlling the circuit properly, it can work either as a voltage doubler or as a voltage quadrupler. For the method in [10] and [11], an extended voltage gain range can be obtained with different operation modes, but additional components are needed in the circuit.

This article proposed to utilize the characteristics of multielement resonant converter for the isolated dc-rectified sine stage. The paralleled L_p, C_p within *LCLCL* resonant tank, as shown in Fig. 3, can naturally create zero voltage gain, which is favorable for rectified sine wave generation. At the same time, VFM can be applied for the whole range without any other additional control modes.

The relevant research for multielement resonant converter was limited, and they were mostly adopted in dc–dc conversions for better performance. It has not been used for dc–ac inverters. In [12]–[15], different two, three and four-element resonant tank topologies are presented, and their benefits are discussed. Huang *et al.* [16] provided a systematic approach to group three and four-element resonant tanks based on their common characteristics. In [21] and [22], another series *LC* is added in parallel with the original *LLC* converter, as shown in Fig. 4, and the added branch is for the conduction of third harmonic current to reduce the total resonant current rms value. The *LCLCL* resonant converter is designed in [17] for dc–dc conversion and claims that the third harmonic current can go through the *LCLCL* resonant tank, which can help power delivery with less circulating energy compared to *LLC* converter. Meanwhile, the zero voltage gain point of *LCLCL* resonant tank can provide current protection during startup or short. Koscelnik *et al.* [18] and Zhang *et al.*[19] also mentioned that the *LCLCL* can help inject higher order of harmonics current to decrease the resonant current rms value. In [20], the paralleled L_p, C_p of *LCLCL* is placed on the secondary side of the transformer to further improve efficiency since they have lower current on the secondary side.

For this paper, the *LCLCL* resonant tank characteristics and design methodology will be provided in detail for dc–ac application in Section II. Section III will discuss the circuit design and considerations. For the dc–ac implementation with consideration of parasitic components, the $C_{\rm oss}$ of the synchronous rectification (SR) stage will impact the switching frequency range for different load conditions. This issue will be analyzed thoroughly in Section IV. Finally, Section V presents the experimental test results and the loss analysis.

II. *LCLCL* Resonant Tank Characteristics and Design Methodology

A. LCLCL *Resonant Tank Location*

The *LCLCL* resonant tank can be placed on either primary side or secondary side of the transformer. For the *LLC* converter based isolated inverter in [9], the *LLC* resonant tank is placed on primary side since with the resonant tank on the secondary side, it will result in higher voltage gain at the maximum switching frequency for light load conditions. However, for *LCLCL* resonant tank, zero voltage gain can always be obtained for different load conditions at the resonant frequency of L_p and C_p with the tank on either side of the transformer. Therefore, for better

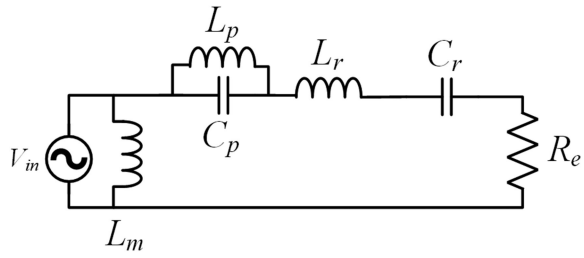

Fig. 5. *LCLCL* resonant converter equivalent circuit.

efficiency, the tank should be on the side with lower current and, thus, in this article with step-up transformer, the *LCLCL* resonant tank is placed on the secondary side.

B. LCLCL *Resonant Tank Voltage Gain Curve*

The equivalent circuit of *LCLCL* resonant converter is shown in Fig. 5. With the first harmonic analysis (FHA) method, the voltage gain equation can be derived in (1) where $k = L_m/L_r$, $h = L_m/L_p$, $g = C_r/C_p$ and the equation for f_r and f_p are shown in (2) and (3) as follows:

$$\text{Gain} = \frac{1}{\sqrt{A_1^2 + B_1^2}} \tag{1}$$

$$A_1 = 1$$

$$B_1 = \frac{1}{\frac{f_s^2}{f_p^2} - 1}\left[Q\frac{f_s}{f_r}\left(\frac{f_s^2}{f_p^2} - \left(1 + \frac{k}{hg} + \frac{k}{h}\right)\right) + Q\frac{f_r}{f_s}\right]$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

$$f_p = \frac{1}{2\pi\sqrt{L_p C_p}}. \tag{3}$$

Since the term B_1 in (1) is related to the load condition, the load independent points can be calculated by making term B_1 equal to zero. There are three load independent points for *LCLCL* resonant tank, and they are f_p, f_1, and f_2. The results of f_1 and f_2 are shown in (4) and (5). An example of *LCLCL* voltage gain curve for different load conditions are shown in Fig. 6

$$f_1 = \sqrt{\frac{\frac{L_r+L_p}{L_r} f_p^2 + f_r^2 - \sqrt{\left(\frac{L_r+L_p}{L_r}\right)^2 f_p^4 + \frac{2(L_p-L_r)}{L_r} f_r^2 f_p^2 + f_r^4}}{2}} \tag{4}$$

$$f_2 = \sqrt{\frac{\frac{L_r+L_p}{L_r} f_p^2 + f_r^2 + \sqrt{\left(\frac{L_r+L_p}{L_r}\right)^2 f_p^4 + \frac{2(L_p-L_r)}{L_r} f_r^2 f_p^2 + f_r^4}}{2}}. \tag{5}$$

Since the resonant converter will operate under ZVS when the voltage gain curve slop is negative [30], for *LCLCL* converter working as dc-rectified sine stage with ZVS, the switching frequency range should be from f_1 to f_p. f_1 is for the peak of ac output and f_p is for the zero crossing of the ac output. Thanks to f_1 and f_p being load independent points, different load condition should have the same switching frequency range. With L_m voltage clamped at the input voltage, fully ZVS can be achieved for primary side GaN devices even with low output voltage.

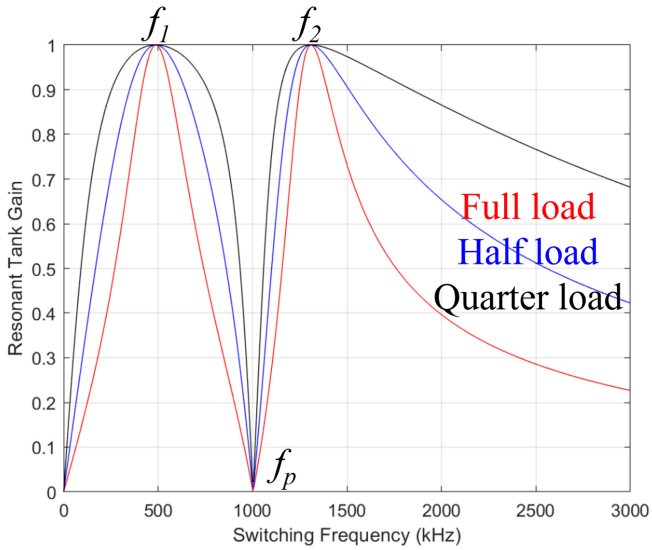

Fig. 6. Example of *LCLCL* voltage gain curve for different load conditions.

C. Monotonic Voltage Gain

Since the third harmonic of the resonant current can also go through the *LCLCL* resonant tank, the voltage gain at the third harmonic frequency needs to be taken into consideration as well. Meanwhile, for proper dc-rectified sine operation, the voltage gain curve should be monotonic in the desired switching frequency range. Therefore, considering the third harmonic gain, (6) should be satisfied to ensure voltage gain to be monotonic. By combining (4)–(6), a wider range solution of (6) can obtained in (7), which means the ratio between L_p and L_r should be at least smaller than 1.78 to make a monotonic voltage gain curve possible. The exact range of L_p/L_r is related to the circuit parameters.

$$f_2 < 3f_1 \tag{6}$$

$$\frac{L_p}{L_r} < 1.78 \tag{7}$$

D. Switching Frequency Range

As discussed previously, both f_1 and f_p are load independent points so the switching frequency range from f_1 to f_p will be an appropriate option for dc-rectified sine operation. Now the critical item is the location of f_p. In [17], it is suggested that f_p should be placed at twice f_1 since the square wave only consists of odd harmonics and it can help avoid trapping energy of the fundamental and the third harmonic.

For this design, the same rule is followed, as shown in (8), which can be further simplified and solved, as shown in (9). Compared to SRC/*LLC* solutions, the switching frequency range becomes much narrower.

$$f_p = 2f_1 \tag{8}$$

$$12\, f_r^2 = \left(3 + 4\frac{L_p}{L_r}\right) f_p^2 \tag{9}$$

E. LCLCL *Resonant Tank Design Methodology*

From Fig. 5, it can be seen that the magnetizing inductance L_m is not related to the voltage gain, and it is always clamped by the input voltage. Therefore, L_m can be designed separately based on ZVS performance of the primary side GaN devices. To ensure fully ZVS for the whole range, the worst case needs to be identified and L_m needs to be designed under the worst case. In this design, the worst case is at the maximum switching frequency with the lowest magnetizing current and the output voltage is close to zero. Hence, the primary side current will be the magnetizing current, which is utilized to charge/discharge $C_{\rm oss}$ during the deadtime for fully ZVS. Meanwhile, with the output voltage close to zero at the maximum switching frequency, the charge on the secondary side $C_{\rm oss}$ is small and can be ignored. Therefore, when considering ZVS performance, only the $C_{\rm oss}$ on the primary side needs to be focused and the ZVS condition in [23] can be simplified and shown in

$$L_m \le \frac{DT}{8 f_{\rm smax} C_{\rm oss}}. \tag{10}$$

DT is the deadtime and $C_{\rm oss}$ in (10) is the charge equivalent value for the primary side GaN device.

For other components in *LCLCL* resonant tank, which are L_p, C_p, L_r, and C_r, if L_p/L_r and C_p are designed, all the four parameters can be solved with (2), (3), (9). Therefore, only two parameters, L_p/L_r and C_p, needs be determined.

The first step is to determine the exact range of L_p/L_r. From (5) and (9), it can be seen that if L_p/L_r and f_p are determined, the location of f_2 will be fixed. As discussed previously, f_1 and f_p are predetermined parameters in the circuit specification with f_p to be twice of f_1, which means the location of f_2 is only related to L_p/L_r so the accurate range of L_p/L_r can be obtained.

The second step is to determine the range of C_p. With switching frequency close to f_p, large energy will circulate inside L_p and C_p. If C_p is too small, the voltage across C_p will be high and its voltage rating may not be enough. Meanwhile, too small C_p will lead to large L_p, which will hurt the efficiency and power density. On the other hand, if C_p is too large, the gain curve will be sharp around f_p, which is not preferred for the control. One example of gain curves with different C_p is shown in Fig. 7.

With L_p/L_r and C_p are determined, the final step is to calculate L_p, L_r, and C_r based on (2), (3), (9). The *LCLCL* resonant tank design process is summarized in the flow chart in Fig. 8. Section III will also show the details of this proposed design process for real circuit.

III. Circuit Design and Considerations

The circuit diagram discussed in this article is shown in Fig. 9 and the *LCLCL* resonant tank is on the secondary side of the transformer, which is better for ZVS performance and circuit efficiency. The input/output voltage is 380 $V_{\rm dc}$/600 $V_{\rm ac}$ with 500 kHz–1 MHz switching frequency range. 650 V GaN HEMTs are selected for both primary side devices Q_1–Q_4 and secondary side SR devices Q_5–Q_8. For the unfolder, 1200 V SiC MOSFET are utilized. It should be noted that the rectifier configuration with flying capacitor is for the use of 650 V GaN HEMTs.

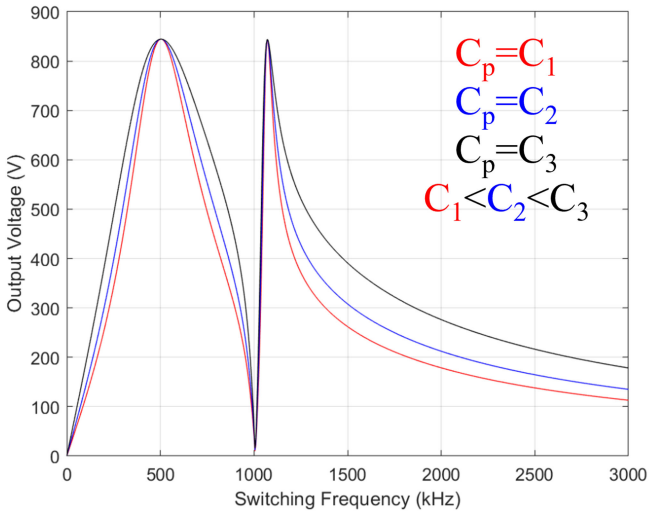

Fig. 7. Example of *LCLCL* voltage gain curve for different C_p.

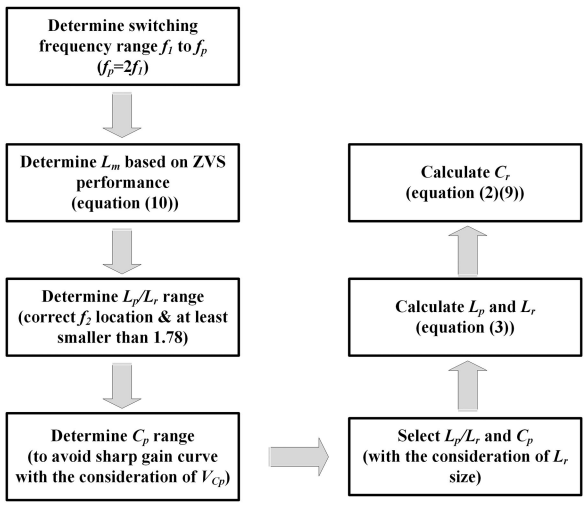

Fig. 8. Flow chart of proposed *LCLCL* resonant tank design methodology.

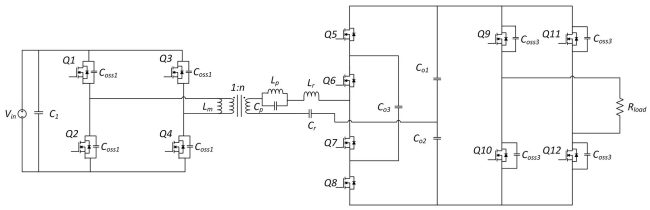

Fig. 9. *LCLCL* resonant converter based isolated inverter circuit diagram.

A. LCLCL *Resonant Tank Design*

As mentioned in Section II, L_m is designed based on fully ZVS condition at the maximum switching frequency. With the deadtime to be 70 ns at 1 MHz, L_m is calculated to be 19.6 μH from (10).

The f_2 locations for different L_p/L_r are provided in Table I based on (5) and (9). Since f_1 is 500 kHz, f_2 should be lower than 1.5 MHz. Considering some margin, L_p/L_r needs to be between

TABLE I
f_2 LOCATIONS FOR DIFFERENT L_p/L_r

L_p/L_r	0.1	0.2	0.4	0.6	0.8	1	1.2
f_2(MHz)	1.07	1.13	1.25	1.35	1.45	1.54	1.62

TABLE II
DIFFERENT COMBINATION OF C_p, L_p, L_r, AND C_r

C_p	L_p	L_r	C_r
1 nF	25 uH	41.7 – 250 uH	1.3 – 0.4 nF
2 nF	12.5 uH	20.8 – 125 uH	2.7 – 0.7 nF
3 nF	8.4 uH	14 – 84 uH	4 – 1.1 nF
4 nF	6.3 uH	10.4 – 63 uH	5.3 – 1.4 nF
5 nF	5 uH	8.3 – 50 uH	6.7 – 1.8 nF

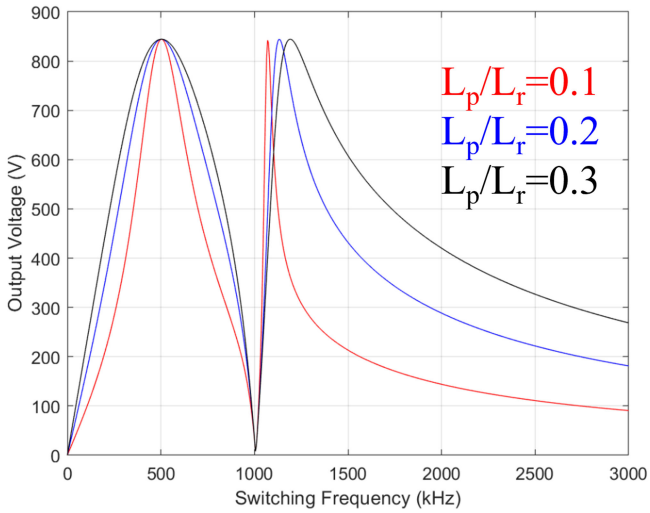

Fig. 10. *LCLCL* voltage gain curve for different L_p/L_r ($C_p = 4$ nF).

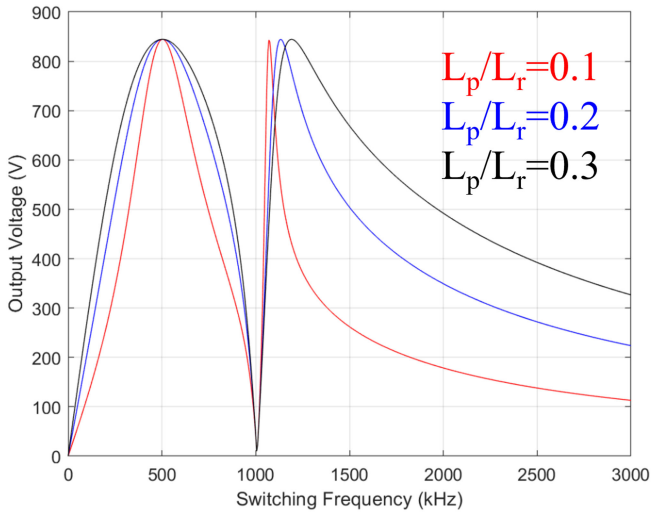

Fig. 11. *LCLCL* voltage gain curve for different L_p/L_r ($C_p = 5$ nF).

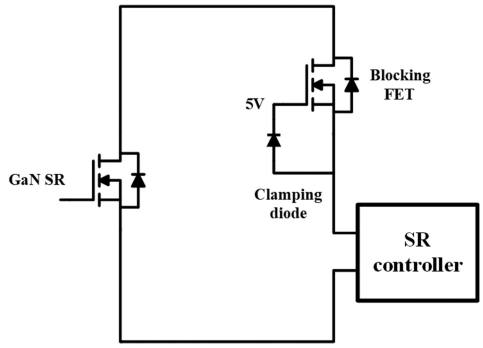

Fig. 12. High voltage SR control scheme.

0.1 and 0.6. Besides, C_p should be selected in the range of 1 nF – 5 nF. If C_p is smaller than 1 nF, its voltage will be too high. If C_p is even larger than 5 nF, the voltage gain curve will be too sharp for the region around 1 MHz. Therefore, different combinations of C_p, L_p, L_r, and C_r with L_p/L_r between 0.1 and 0.6, C_p between 1 nF and 5 nF are shown in Table II.

From Table II, C_p needs to be larger than 3 nF otherwise L_r is too large, which will hurt the efficiency and power density. The voltage gain curve $C_p = 4$ nF and 5 nF with different L_p/L_r is presented in Figs. 10 and 11. For $C_p = 4$ nF and 5 nF, L_p/L_r can only be 0.1 to avoid the voltage gain curve to be sharp. However, with L_p/L_r to be 0.1, the inductance of L_r is too large. Therefore, C_p and L_p are designed to be 3 nF and 8.4 μH, respectively. In order to have smaller L_r, L_r and C_r are designed to be 15.6 μH and 4 nF.

For higher overall circuit efficiency, polypropylene capacitor needs to be selected for C_p and C_r due to its low dissipation factor [26]. For the ferrite core material, Hitachi ML91S has shown the lowest core loss density in an early study [27]. Meanwhile, the Litz wire with AWG 48 gauge for each strand should be selected due to its small R_{ac}/R_{dc} value [27].

B. SR Control Design

Generally, there are two types of SR control methods. The first method is that the SR driving signal is generated directly from DSP as an open-loop scheme [24]. However, it is only suitable for certain switching frequency and load conditions. The other approach is to use the SR controller IC to sense V_{ds} to determine the turn-ON and turn-OFF moments [25] with tens of nanosecond delay. For the inverter with variable frequency modulation, the SR turn-ON and turn-OFF timing will vary widely for different conditions. Therefore, SR controller with V_{ds} sensing is used to generate PWM signals for SR devices.

Commercial SR controllers limit the maximum sensed voltage below 200 V. In this article, the maximum voltage across Q_5–Q_8 is over 400 V. Therefore, a high voltage blocking FET needs to be inserted between the drain of SR devices and the SR controller, as shown in Fig. 12. When SR device is ON, the blocking FET is also turned ON and SR controller can be directly connected to the drain and source of the SR device. When SR device is OFF, the C_{oss} of the blocking FET and the equivalent capacitance of SR

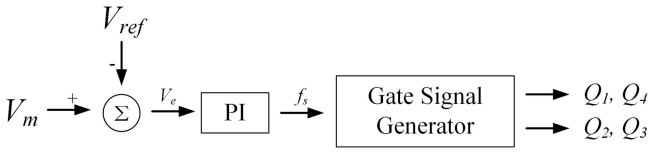

Fig. 13. Control block diagram of VFM method for *LCLCL* converter.

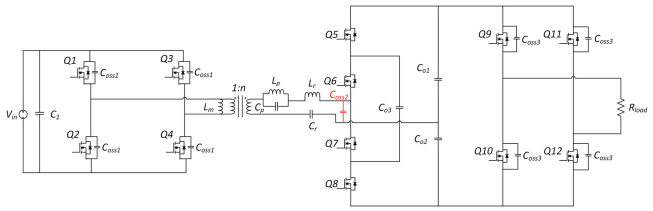

Fig. 14. Equivalent *LCLCL* converter based isolated inverter circuit diagram.

controller will form a capacitive voltage divider. Since C_{oss} is much smaller, most voltage will be blocked by the blocking FET, and the SR controller can be protected. Moreover, a clamping diode is added to further clamp the voltage across SR controller to be 5 V.

C. Control Strategy

For resonant converter with VFM, the duty cycle for Q_1–Q_4 in Fig. 9 is constant at 50% with deadtime and the switching frequency is adjusted to generate a rectified sine wave at the output of the *LCLCL* converter. The output voltage of the dc-rectified sine stage V_m is the control object and an isolated voltage sensor is added. Thanks to the zero voltage gain at the resonant frequency of L_p and C_p for different load conditions, variable frequency modulation can be applied for the whole line cycle. There is no need to have any additional control modes, which is simpler compared to other control methods for this dc-rectified sine stage in the literature. The control block diagram is shown in Fig. 13. The sensed voltage V_m will track the reference voltage V_{ref} generated inside the DSP with the help of a PI controller and the switching frequency will be adjusted accordingly for Q_1–Q_4.

IV. SR C_{OSS} Impact on Switching Frequency Range

All the abovementioned analysis is based on ideal switches. However, from the real test results, the C_{oss} of the SR devices can impact the switching frequency range for different load conditions. Therefore, the SR C_{oss} needs to be included in the voltage gain equations. The basic idea applied here is to use the equivalent *LCLCL* circuit shown in Fig. 14 to replace the original *LCLCL* converter in Fig. 9 and these two converters will have the same output voltage. The reason here is that according to [23], the equivalent capacitance for the four SR switches in Fig. 9 is $C_{\text{oss}\,2}$ with ΔV to be V_o during deadtime for charging/discharging. Therefore, this $C_{\text{oss}\,2}$ can be placed at the location in Fig. 14 where the ΔV is V_o as well and the $C_{\text{oss}\,2}$ for Q_5–Q_8 can be eliminated. Since $C_{\text{oss}\,2}$ only has effects during the deadtime, these two *LCLCL* converters can be expected to have the same voltage gain. The simulation results for both *LCLCL* converters at 800 kHz is shown in Fig. 15. The top two curves are the output voltage and the bottom two curves are the primary side resonant current. The red curves are for the original *LCLCL* converter while the blue curves are for the equivalent *LCLCL* converter. It can be seen that the output voltage and the resonant current are exactly the same for these two converters.

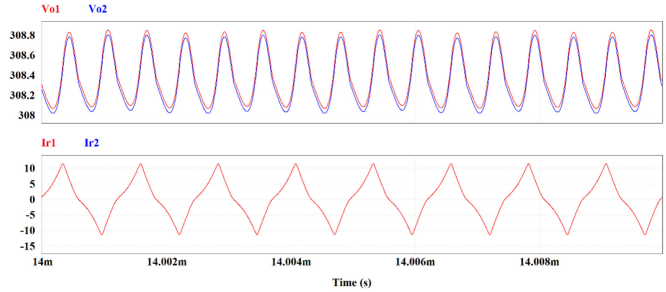

Fig. 15. Simulation results for two *LCLCL* converters at 800 kHz.

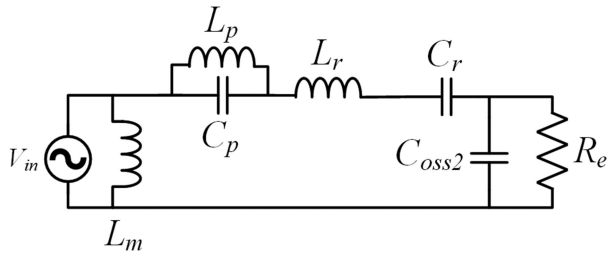

Fig. 16. Equivalent resonant tank circuit with $C_{\text{oss}\,2}$.

Now the equivalent *LCLCL* converter in Fig. 14 can be utilized to calculate the voltage gain curve with the consideration of $C_{\text{oss}\,2}$. FHA is applied for the calculation and the equivalent circuit for the new resonant tank is shown in Fig. 16. The result is provided in (11), where the additional $p = C_r/C_{\text{oss}\,2}$ is added, and all the other parameters are the same as Section II

$$\begin{aligned}
\text{Gain} &= \frac{1}{\sqrt{A_2^2 + B_2^2}} \\
A_2 &= \frac{1}{\frac{f_s^2}{f_p^2} - 1}\left[\left(1 + \frac{hg}{kp} + \frac{1+g}{p}\right)\frac{f_s^2}{f_p^2} - \frac{1}{p}\frac{f_s^2}{f_r^2}\frac{f_s^2}{f_p^2} - 1 - \frac{1}{p}\right] \\
B_2 &= \frac{1}{\frac{f_s^2}{f_p^2} - 1}\left[Q\frac{f_s}{f_r}\left(\frac{f_s^2}{f_p^2} - \left(1 + \frac{k}{hg} + \frac{k}{h}\right)\right) + Q\frac{f_r}{f_s}\right].
\end{aligned} \tag{11}$$

For (1) and (11), parameter Q, which is related to the load condition, only appears in the equations for term B. Therefore, term A is more related to resonance while term B is the load factor. By adding $C_{\text{oss}\,2}$ in the resonant tank, term B is unchanged and term A is different to show $C_{\text{oss}\,2}$ modifies the original resonant tank. By using (1) and (11), the voltage gain curves for both *LCLCL* converters with different load conditions are shown in Figs. 17 and 18.

In Fig. 17 without $C_{\text{oss}\,2}$, all the curves have the same peak voltage gain point so for different load conditions, they have the same switching frequency range. However, in Fig. 18 with $C_{\text{oss}\,2}$

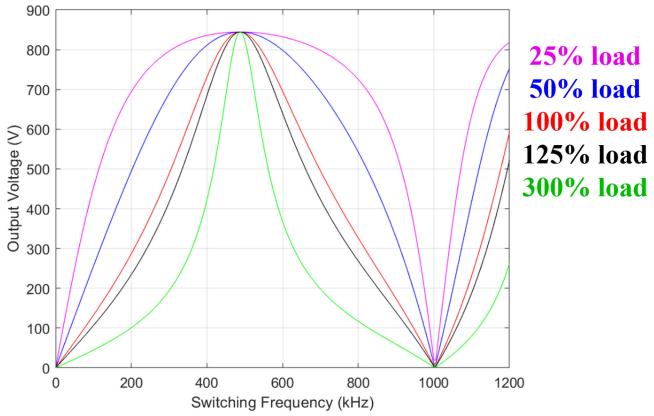

Fig. 17. Original *LCLCL* converter voltage gain curves for different load conditions.

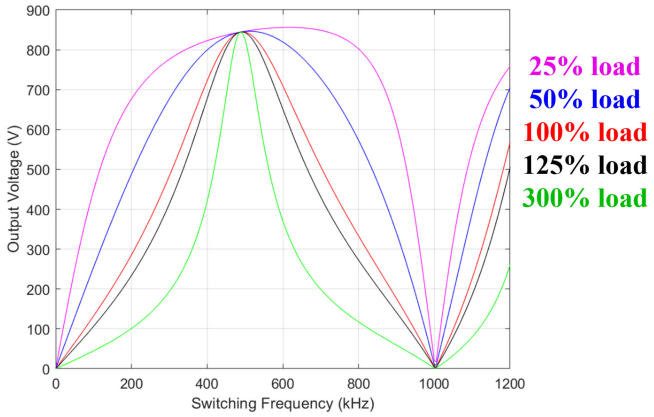

Fig. 18. *LCLCL* converter voltage gain curves considering $C_{oss\,2}$ for different load conditions.

added in the voltage gain curve calculation, narrower switching frequency range can be expected with lighter load condition. For 25% load condition, the starting switching frequency is changed to around 750 kHz. One practical issue with this narrow switching frequency range is the resolution of controller DSP. There will be only a limited number of frequency points within a narrow range for DSP and the output ac voltage waveform will be impacted. Therefore, if very light load condition is the concern, the gain curve needs to be designed properly with the consideration of $C_{oss\,2}$ at first. One solution is to design the new 100% load voltage gain curve to have similar shape as the 300% load gain curve in Fig. 18. In this way, even with very light load conditions, the switching frequency range will not be narrow. One possible new voltage gain curve is shown in Fig. 19. With 15% load condition, the switching frequency range is almost the same as that of 100% load condition.

V. Experimental Verifications

A GaN based 380 V_{dc}–600 V_{ac}, 1.2 kW single-stage *LCLCL* converter based isolated inverter prototype is built and tested for verification. The circuit diagram is shown in Fig. 9 and the circuit parameters are designed and summarized in Table III based on the analysis in Sections II and III.

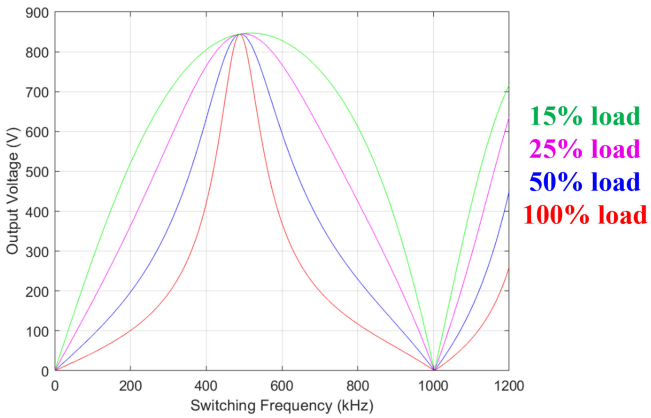

Fig. 19. One possible voltage gain curve considering very light load conditions.

TABLE III
LCLCL Converter Based Isolated Inverter Circuit Parameters

Parameter	Value
Primary side device, $Q_1 - Q_4$	GS66516T
SR device, $Q_5 - Q_8$	LMG3410R050
Unfolder device, $Q_9 - Q_{12}$	C3M0075120K
Transformer turns ratio, $1{:}n$	9:10
Switching frequency range	500 kHz – 1 MHz
SR controller	NCP4306

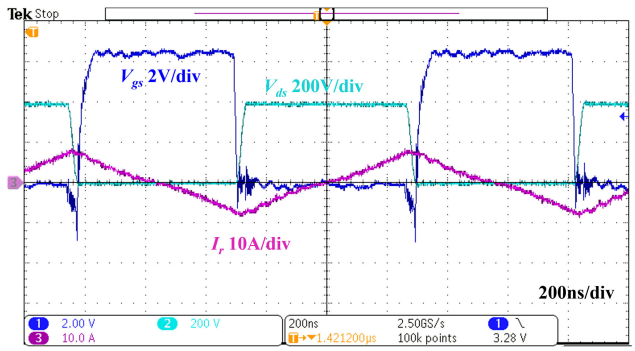

Fig. 20. Dc–dc test waveform at the maximum switching frequency.

As discussed in Section II, if fully ZVS for primary side devices can be achieved at the maximum switching frequency, the whole frequency range will have fully ZVS. Therefore, the dc–dc test at the maximum switching frequency is performed first to verify the ZVS performance. The waveform is presented in Fig. 20. The blue and cyan blue curves are the V_{gs} and V_{ds} of the primary side device, respectively. The purple curve is the resonant current. From the waveform, fully ZVS has been achieved, which ensures the soft switching performance for the whole range.

The inverter test waveforms for 100%, 75%, 50%, and 25% load conditions are shown in Figs. 21–24. The green and yellow curves are the output voltage and flying capacitor voltage, respectively. As shown in the figures, the flying capacitor voltage is always half of the rectified output voltage. The red curve is the resonant current on the primary side. For 100% load condition, the THD of output voltage is 1.81% with 97.0% efficiency. For 75% load condition, the THD of output voltage is 1.99% with

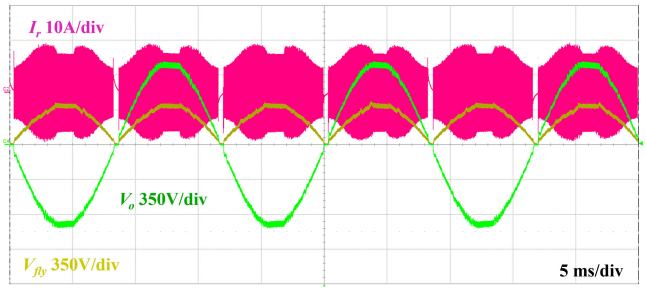

Fig. 21. Test waveform with 100% load condition.

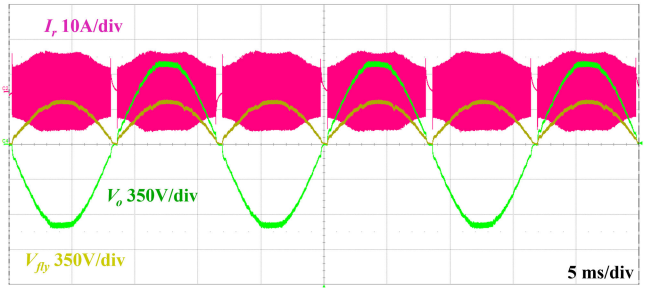

Fig. 22. Test waveform with 75% load condition.

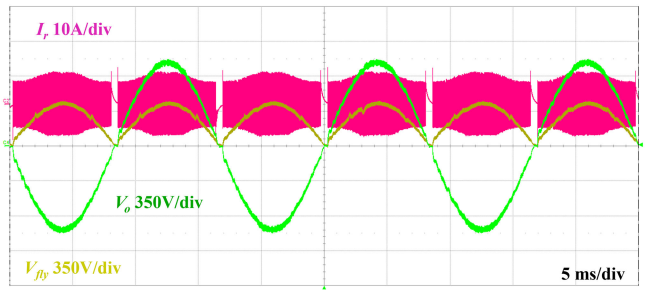

Fig. 23. Test waveform with 50% load condition.

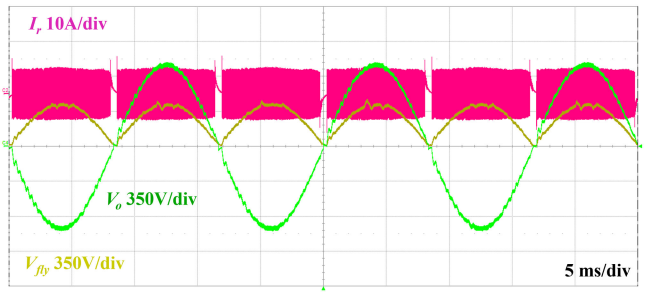

Fig. 24. Test waveform with 25% load condition.

96.3% efficiency. For 50% load condition, the THD of output voltage is 1.81% with 95.4% efficiency. For 25% load condition, the THD of output voltage is 2.19% with 91.3% efficiency. Hence, for different load conditions, the THD of the output voltage can always keep around 2%, which is better compared to *LLC*-based isolated inverter in [8] and [9]. Especially for light load conditions, the zero voltage gain point from *LCLCL* ensures low THD performance.

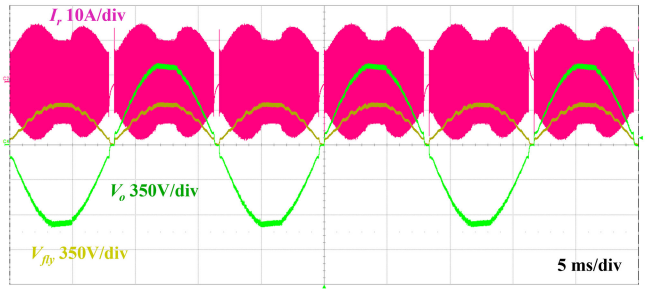

Fig. 25. Test waveform with 125% load condition.

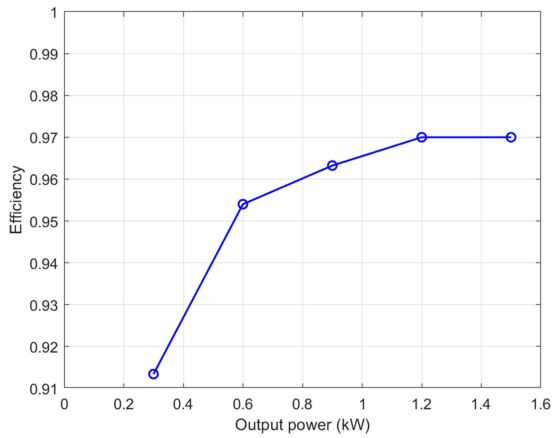

Fig. 26. Efficiency curve of experimental test results.

In Fig. 24, it can be seen that the output voltage waveform is not as smooth as the heavier load conditions in Figs. 21–23. It is due to the DSP resolution issue discussed in Section IV and there are only limited number of switching frequency points for the whole range. Thanks to the proposed *LCLCL* topology, the output voltage THD can still be kept very low even with limited DSP resolution.

To further verify the proposed circuit performance, 125% load is tested to push the limit and the test waveform is shown in Fig. 25. The THD of output voltage is 2.00% with 97.0% efficiency. The same efficiency compared to 100% load condition also indicates the circuit is optimized for efficiency at around full load condition as originally designed and expected.

The efficiency curve is provided in Fig. 26 and the peak efficiency reaches 97.0% at full load condition. The formulas for different loss are summarized in Table IV. Based on these formulas, the loss breakdown results for full load condition are presented in Table V. The temperature coefficient on $R_{ds(\text{ON})}$ has been included in conduction loss of the primary side, SR, and unfolder power devices. Meanwhile, although fully ZVS is achieved for the primary side GaN devices, there is still channel turn-OFF energy, which is the difference between hard turn-OFF energy and C_{oss} stored energy [28].

From Table V, the major loss comes from primary side GaN loss, SR loss and transformer loss. For the loss from primary side GaN devices, since the resonant tank is placed on the secondary side, the transformer primary side winding is always clamped by the input voltage 380 V, which leads to higher magnetizing

TABLE IV
FORMULAS FOR DIFFERENT LOSS

Loss type	Formula
Primary side conduction loss	$2I_{pri}^2 R_{ds(on)1}(T_j)$
Primary side channel turn-off loss	$\int \alpha I_{off1}^{\beta} f_s(\theta) d\theta$
SR conduction loss	$I_{sec}^2 R_{ds(on)2}(T_j)$
SR turn-on delay loss	$\int I_{2avg} V_F T_d f_s(\theta) d\theta$
SR early turn-off loss	$\int I_{off2} V_F T_{early} f_s(\theta) d\theta$
Unfolder conduction loss	$2I_{orms}^2 R_{ds(on)3}(T_j)$
Transformer loss	$I_{pri}^2 R_{ac1} + I_{sec}^2 R_{ac2} + \int k V_{tr} B_m^a f_s^b(\theta) d\theta$
Inductor L_r loss	$I_{pri}^2 R_{acLr} + \int k V_{Lr} B_m^a f_s^b(\theta) d\theta$
Inductor L_p loss	$I_{Lp}^2 R_{acLp} + \int k V_{Lp} B_m^a f_s^b(\theta) d\theta$
Capacitors ESR loss (C_r, C_p & voltage doubler capacitors)	$I_{pri}^2 R_{Cr} + I_{Cp}^2 R_{Cp} + 2I_{doubler}^2 R_{doubler}$

I_{pri}, I_{sec}, $I_{OFF\,1}$, $I_{OFF\,2}$, I_{2avg}, $R_{ds(ON)1}$, $R_{ds(ON)2}$, $R_{ds(ON)3}$, $R_{ac\,1}$, $R_{ac\,2}$, V_{tr}, V_{Lp}, V_{Lr}, B_m are transformer primary side current, transformer secondary side current, primary side device turn-OFF current, SR device turn-OFF current, SR device average current, primary side device ON-resistance, SR device ON-resistance, unfolder device ON-resistance, transformer primary side winding ac resistance, transformer secondary side winding ac resistance, transformer volume, L_p volume, L_r volume, and maximum flux density, respectively.

TABLE V
LOSS BREAKDOWN FOR FULL LOAD CONDITION

	Value
Primary side conduction loss	4.30 W
Primary side channel turn-off loss	1.63 W
SR conduction loss	2.41 W
SR turn-on delay loss	4.91 W
SR early turn-off loss	4.00 W
Unfolder conduction loss	0.58 W
Transformer loss	9.51 W
Inductor L_r loss	1.72 W
Inductor L_p loss	3.54 W
Capacitors ESR loss (C_r, C_p & voltage doubler capacitors)	1.50 W
Total loss (calculated)	34.10 W
Total loss (measured)	36.17 W

current. This is good for ZVS performance, but higher turn-OFF current can be expected, which increases the channel turn-OFF loss. With the same reason, the transformer will have higher core loss due to higher $B_{\max}$. For the SR loss, the turn-ON delay is caused by the SR controller IC, which is the issue with V_{ds} sensing technique. If a better SR controller with lower turn-ON delay is implemented, this part of loss can be reduced. The SR early turn OFF is also common due to the parasitic inductance in the V_{ds} sensing loop and higher *di/dt* results in even earlier turn OFF. After SR early turn OFF, the high forward voltage drop of GaN "body diode" will generate nontrivial loss. With properly designed V_{ds} sensing loop in PCB layout, *di/dt* can be reduced by increasing L_r and L_p. However, large L_r and L_p will lead to lower power density and more loss, which becomes the tradeoff for this *LCLCL* converter based isolated inverter design. Table VI summarizes the comparison between the proposed solution in this article and previous works.

TABLE VI
SUMMARIZED COMPARISON TABLE

Solution	Control Method	THD (100%/50% /25% load)	Soft Switching Performance
[5]	Flyback converter with PWM control at 40 kHz	2.5%/NA/NA	Hard Switching
[6]	Cuk converter with PWM control at 40 kHz	2%/2.5%/3%	Hard Switching
[29]	LLC converter with PSM at 100 kHz	4.2%/4.07%/NA	ZVS is hard for low line and light load regions. Different ZVS performance for two phase legs.
[8]	SRC with VFM+SPDM, 80 kHz – 250 kHz	1.8%/3.0%/3.9%	ZVS is hard for low line and light load regions. Lose ZVS during SPDM.
[9]	LLC converter with FB VFM +HB VFM, 356 kHz – 1.2 MHz	2.7%/4.7%/NA	ZVS is hard for low line and light load regions.
This work	LCLCL converter with VFM only, 500 kHz – 1 MHz	1.8%/1.8%/2.2%	Fully ZVS for the whole region.

VI. CONCLUSION

A MHz *LCLCL* resonant converter based single-stage soft-switching isolated inverter with variable frequency modulation is introduced in this article. The L_p and C_p within the *LCLCL* resonant tank can naturally create a zero voltage gain point at f_p, which shows superior characteristics for rectified sine wave generation. Compared to the SRC/*LLC*-based isolated inverter, the key advantages are summarized as follows.

1) Better THD. The zero voltage gain point ensures better output voltage THD for different load conditions.
2) Easier control. Variable frequency modulation can be used for the whole range and there is no need to have different control modes.
3) Better ZVS performance. The resonant tank can be placed on the secondary side to have better ZVS performance.
4) Narrower switching frequency range. For *LCLCL*, the switching frequency range is from f_1 to 2x f_1 while for SRC/*LLC*, switching frequency range is from f_1 to 3x f_1 or 4x f_1. Narrower switching frequency range is also better for ferrite core material selection.

Meanwhile, the *LCLCL* resonant tank design methodology for isolated inverter application is proposed and the impact of SR C_{oss} on the switching frequency range for different load condition is analyzed thoroughly. Lighter load condition leads to

narrower switching frequency range. A GaN based 380 V_{dc}–600 V_{ac}, 1.2 kW single-stage isolated inverter prototype is built and tested. The THD of the output voltage can always keep around 2% for different load conditions with peak efficiency at 97.0%. Loss analysis indicates that the transformer loss is relatively high due to the peak sine wave current related high flux density. The secondary side device losses including conduction, SR turn-ON delay and SR early turn-OFF are nontrivial, which could be reduced with a better SR control. Nearly 50% losses come from these two components together. It is possible to significantly improve the efficiency by taking into these factors into account.

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